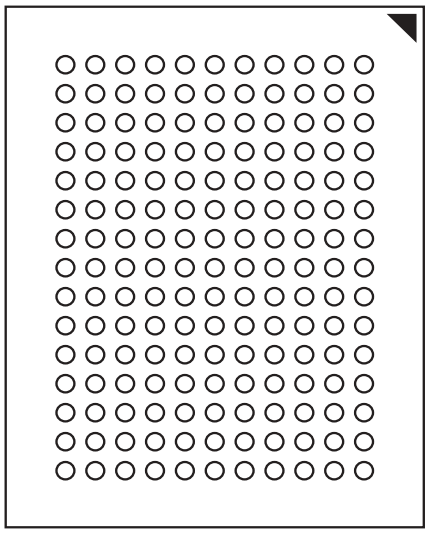
ADVANCE INFORMATION
DECEMBER 2002

ΣQUAD 18Mb Σ2x1B2 SDR SEPERATE I/O SRAM

FEATURES

- Simultaneous Read and Write SigmaQuad™ Interface
- Dual Single Data Rate interface
- Echo Clock outputs track data output drivers
- Byte Write controls sampled at data in time
- Burst of 2 Read and Write
- Single 1.8 V +150/–100 mV core power supply
- Dedicated output supply voltage (V_{DDQ}): 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 165 pin (11x15), 1mm pitch, 13mm x 15mm Ball Grid Array (BGA) package
- Pin compatible with future 36M, 72M and 144M devices

Speed	-333	-300	-250	-200	
tKHKH	3.0	3.3	4	5	ns
tKHQV	1.6	1.8	2.1	2.3	ns



Bottom View
165-Bump, 13 mm x 15mm BGA
1 mm Bump Pitch, 11 x 15 Bump Array

SIGMARAM FAMILY OVERVIEW

These Separate I/O SigmaQuads are built in compliance with the SigmaRAM pinout standard for Separate I/O synchronous SRAMs. The first implementations are 18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems. Separate I/O SigmaQuads are offered in a number of configurations. Some emulate and enhance other synchronous separate I/O SRAMs. This data sheet covers a higher performance SDR (Single Data Rate) Burst of 2 version. The logical defference between the protocols employed by these RAMs hinge mainly on various combinations of address bursting, output data registering, and write cueing. Like the Common I/O family of SigmaRAMs, SigmaQuad allow a user to implement the interface protocol best suited to the task at hand.

CLOCKING AND ADDRESSING SCHEMES

A Σ2x1B2 SigmaQuad is a synchronous device. It employs a single input register clock input K.

The device also allows the user to manipulate the output register clock inputs quasi independently with the C clock inputs. If the C clock is tied high, the K clock is routed internally to fire the output registers instead. Each Σ2x1B2 SigmaQuad also supplies Echo Clock outputs, CQ that is synchronized with read data output. When used in a source synchronous clocking scheme these Echo Clock outputs can be used to fire input registers at the data's destination.

Because Separate I/O Σ2x1B2 RAMs always transfer data in two packets, A0 is internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfer. Since the LSB is tied off internally, the address field of a Σ2x1B2 RAM is always one address pin less than the advertised index depth (e.g., the 1M x 18 has a 512K addressable index).

1M x 18 SIGMAQUAD SRAM—TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	MCL/SA (144Mb)	NC/SA (36Mb)	$\overline{W}$	$\overline{BW1}$	MCH	NC	$\overline{R}$	SA	MCL/SA (72Mb)	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	NC	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	MCH	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm2 Body—1 mm Bump Pitch

Notes:
1. Expansion addresses: A3 for 36Mb, A10 for 72Mb, A2 for 144Mb
2. $\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.
3. DNU = Do Not Use, MCH = Must Connect High, MCL = Must Connect Low.
4. It is recommended that H1 be tied low for compatibility with future devices.

512 x 36 SIGMAQUAD SRAM — TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	MCL/SA (288Mb)	NC/SA (72Mb)	$\overline{W}$	$\overline{BW2}$	MCH	$\overline{BW1}$	$\overline{R}$	NC/SA (36Mb)	MCL/SA (144Mb)	CQ
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	NC	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	Vss	Vss	V_{SS}	Vss	Vss	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	MCH	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm2 Body —1 mm Bump Pitch

Notes:
1. Expansion addresses: A3 for 36Mb, A10 for 72Mb, A2 for 144Mb
2. $\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.
3. $\overline{BW2}$ controls writes to D18:D26. $\overline{BW3}$controls writes to D27:D35.
4. DNU = Do Not Use, MCH = Must Connect High, MCL = Must Connect Low.
5. It is recommended that H1 be tied low for compatibility with future devices.

PIN DESCRIPTION TABLE

Symbol	Pin Location	Description	Type	Comments
SA	B4, B8, C5, C6, C7, N5, N6, N7, P4, P5, P7, P8, R3, R4, R5, R7, R8, R9	Address	Input	—
SA	A9	Address	Input	x18 Version
NC	A9	No Connect	—	x36 Version
$\overline{R}$	A8	Read	Input	Active Low
$\overline{W}$	A4	Writes	Input	Active Low
$\overline{BW0}$ - $\overline{BW1}$	B7, A5	Byte Writes	Input	Active Low x18 Version
NC	A7, B5	No Connect	—	x18 Version
$\overline{BW0}$ - $\overline{BW3}$	B7, A7, A5, B5	Byte Writes	Input	Active Low x36 Version
K	B6	Input Clock	Input	Active High
MCH	A6	Much Connect High	Input	DC mode pin
C	P6	Output Clock	Input	Active High
MCH	R6	Much Connect High	Input	DC mode pin
TMS	R10	Test mode Select	Input	—
TDI	R11	Test data Input	Input	—
TCK	R2	Test Clock Input	Input	—
TDO	R1	Test Data Output	Output	—
V_{REF}	H2, H10	HSTK InputReference Voltage	Input	—
ZQ	H11	Output Impedance matching Input	Input	—
MCL	A2, A10	Must Connect Low	—	—
CQ	A11	Echo Clock Output	Output	Echoes C or K Clock
DNU	A1	Do Not Use	—	—
D0 - D35	B3, B9, C1, C3, C9, C11, D1 D2, D10, D11, E2, E10, F3, F9, G1, G2, G10 G11, J1, J3, J9, J11, K2, K10, L3, L9, M1, M3, M9, M11, N1 N2, N10, N11, P2, P10	Data Inputs	Input	x36 Version
Q0 - Q35	B1, B2, B10, B11, C2, C10, D3, D9, E1, E3, E9, E11, F1, F2 F10, F11, G3, G9, J2, J10, K1, K3, K9, K11, L1, L2, L10, L11, M2, M10, N3 N9, P1, P3, P9, P11	Data Outputs	Output	x36 Version
D0 - D17	B3, C3, C11, D2, D11, E10 F3, G2, G11, J3, J11, K10, L3 M3, M11, N2, N11, P10	Data Inputs	Input	x18 Version

PIN DESCRIPTION TABLE

Symbol	Pin Location	Description	Type	Comments
Q0 - Q17	B2, B11, C10, D3, E3, E11, F2 F11, G3, J10, K3, K11, L2, L11 M10, N3, P3, P11	Data Output	Output	x18 Version
NC	B1, B9, B10, C1, C2, C9, D1 D9, D10, E1, E2, E9, F1, F9 F10, G1, G9, G10, J1, J2 J9, K1, K2, K9, L1, L9, L10, M1 M2, M9, N1, N9, N10, P1, P2, P9	No Connect	—	x18 Version
NC	A3, H1	No Connect	—	—
V_{DD}	F5, F7, G5, G7, H5, H7, J5, J7, K5, K7	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	E4, E8, F4, F8, G4, G8, H3, H4, H8, H9, J4, J8, K4, K8, L4, L8	Output Buffer Supply	Supply	1.5 V Nominal
V_{SS}	C4, C8, D4, D5, D6, D7, D8, E5 E6, E7, F6, G6, H6, J6, K6, L5, L6 L7, M4, M5, M6, M7, M8, N4, N8	Ground	Supply	—

Note: NC = Not Connected to die or any other pin

BACKGROUND

Separate I/O SigmaRAMs have been designed to be closely related to Common I/O SigmaRAMs in pinout and overall architecture. The similarities give Separate I/O SigmaRAMs a cost advantage by allowing users and vendors to reuse supporting infrastructure and design elements. Separate I/O SigmaRAMs come in Single and two Double Data Rate configurations. Because they are designed to operate with both the input data pins and the output data pins operating at full speed all the time, Separate I/O SigmaRAMs produce twice the bandwidth of Common I/O SRAMs of the same speed and output bus width. But because the bandwidth of a memory device is set by the architecture and performance of the core array, the bandwidth available from each port of a Separate I/O SRAM is half the bandwidth available from the single port of an otherwise equivalent Common I/O SRAM.

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaRAM Separate I/O interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs cut the RAM's bandwidth in half.

A Separate I/O SigmaRAM can begin an alternating sequence of reads and writes with either a read or a write. In order for any separate I/O SRAM that shares a common address between it's two ports to keep both ports running all the time, the RAM must implement some sort of burst transfer protocol. The burst must be at least long enough to cover the time the opposite port is receiving instructions on what to do next. The rate at which a RAM can accept a new random address is the most fundamental performance metric for the RAM. Each of the three Separate I/O SigmaRAMs support the same address rate because random address rate is determined by the internal performance of the RAM and they are all based on the same internal circuits. Differences between the truth tables of the different Separate I/O SigmaRAMs, or any other Separate I/O SRAMs, follow from differences in how the RAM's interface is contrived to interact with the rest of the system. Each mode of operation has it's own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

Although the Separate I/O SigmaRAM family of pinouts has been designed to support Single and Double Data Rate options, not allSigmaRAM implementations will support both protocols. The following timing diagrams provide a quick comparison between the SDR and DDR protocol options available in the context of the Separate SigmaRAM standard. This particular data sheet covers the Single Data Rate Burst of 2 (Σ2x1B2) Separate I/O SigmaRAM.

The character of the applications for fast synchronous SRAMs in networking systems are extremely diverse. SigmaRAMs ha been developed to address the diverse needs of the networking market in a manner that can be supported with a unifie development and manufacturing infrastructure. SigmaRAMs address each of the bus protocol options commonly found in networking systems.

ALTERNATING READ-WRITE OPERATIONS

Separate I/O SigmaRAMs follow a few simple rules of operation.

- Read or Write commands issued on one port are never allowed to interrupt a operation in progress on the other port.
- Read or Write data transfers in progress may not be interrupted and re-started.
- A Read of a given address location immediately after the location has just been written produces the just-written data. (i.e. SigmaRAMs are “coherent”.)
- $\overline{R}$ and $\overline{W}$ high always deselects the RAM but does not disable the CQ or $\overline{CQ}$ output pins.
- All address, data, and control inputs are sampled on clock edges.

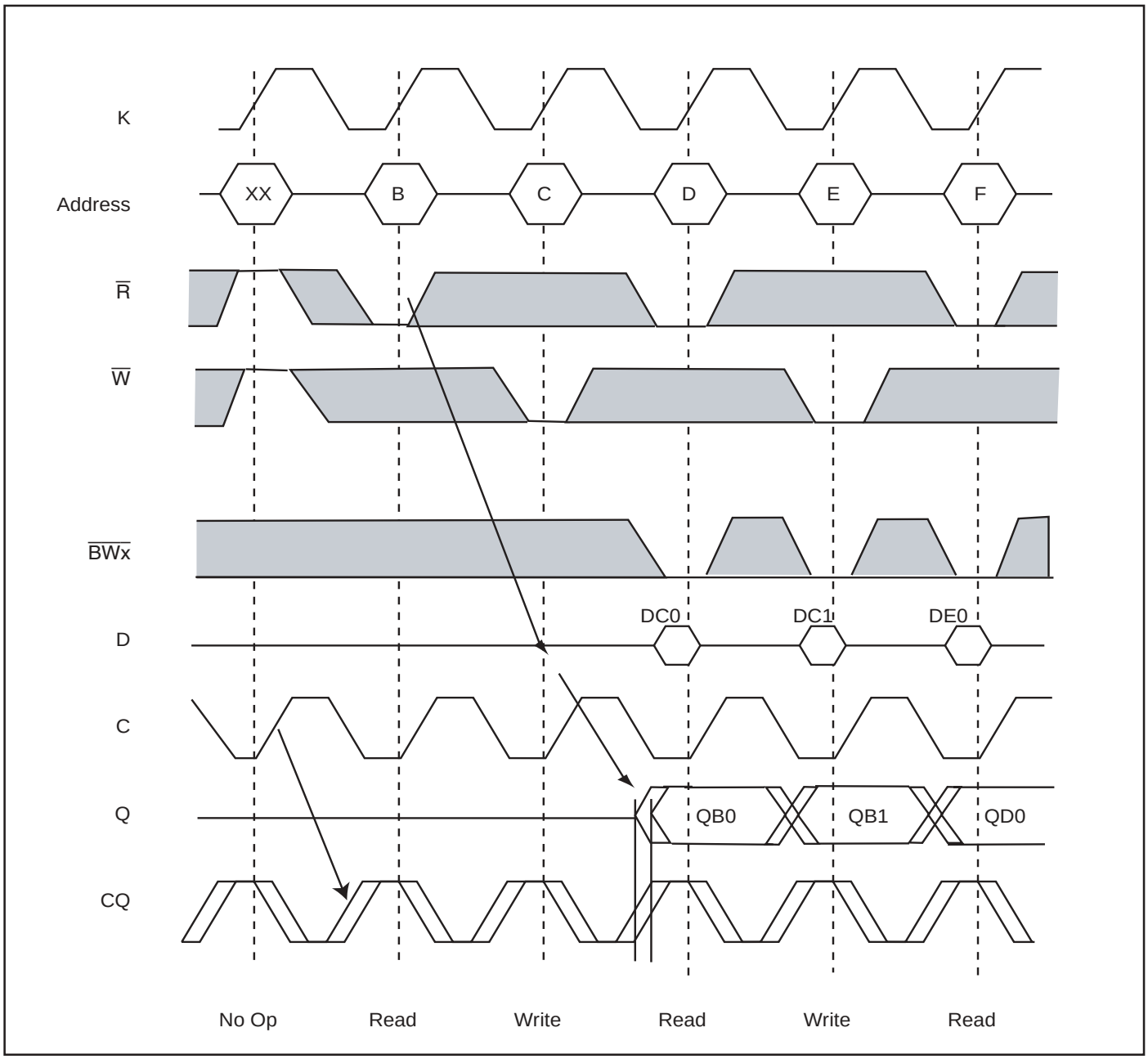
In order to enforce these rules, each RAM combines present state information with command inputs. See the Truth Table for details.

Σ2x1B2 SIGMAQUAD SRAM SDR READ

The status of the Address Input, $\overline{W}$, and $\overline{R}$ pins are sampled at each rising edge of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Read enable-bar pin, $\overline{R}$, begins a read cycle. $\overline{R}$ is always ignorned if the previous command loaded was a read command.

The two resulting data output transfers begin after the next rising edge of the K clock. Data is clocked out by the next rising edge of the C and by the rising edge of the C that follows.

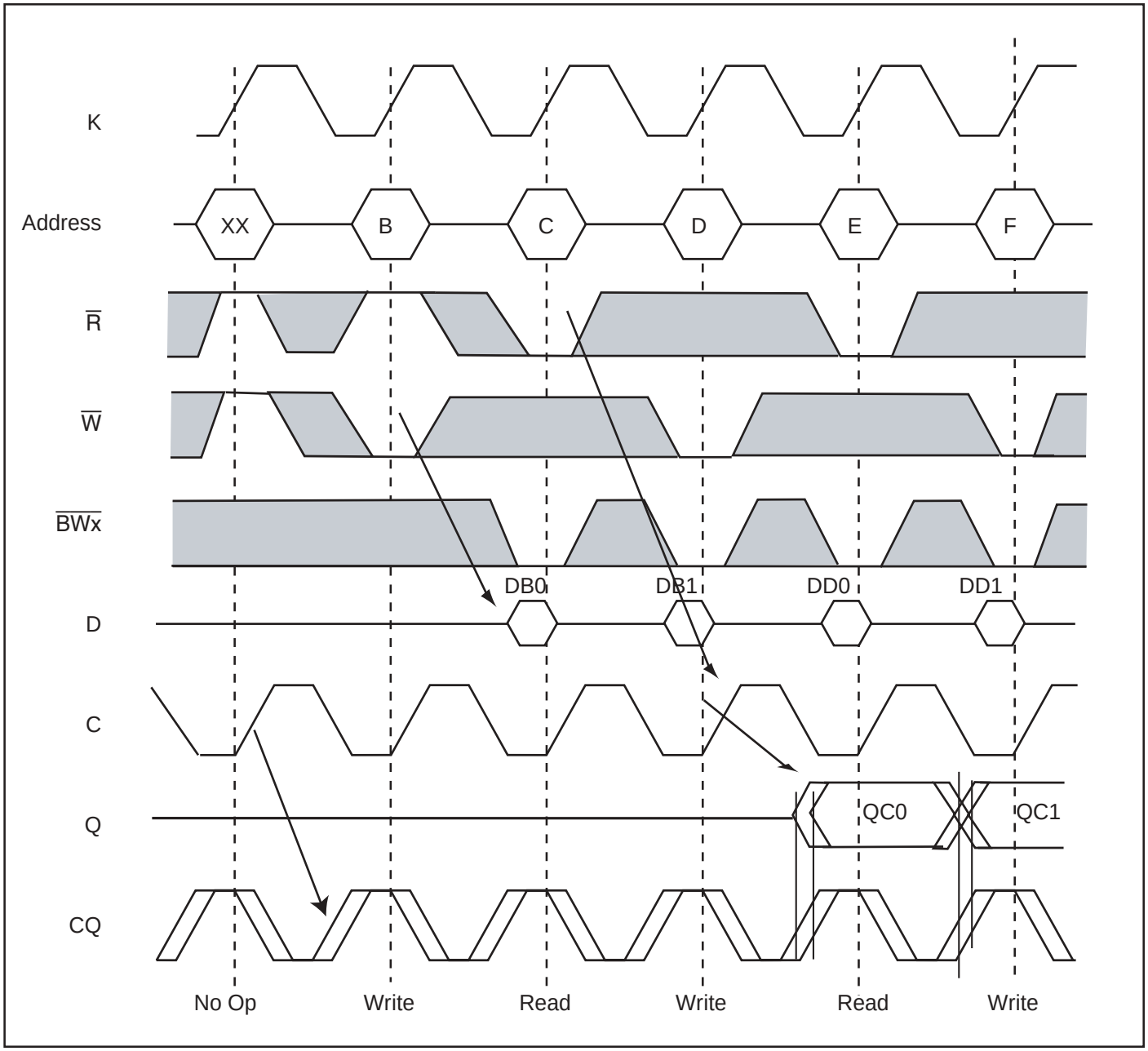
Σ2x1B2 - SINGLE DATA RATE SEPARATE I/O SIGMARAM READ FIRST



Σ2x1B2 SIGMAQUAD SRAM SDR WRITE

The status of the Adress Input, $\overline{W}$, and $\overline{R}$ pins are sampled at each rising of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Write Enable-bar pin, $\overline{W}$, and a high on the Read Enable-bar pin, $\overline{R}$, begins a write cycle. $\overline{W}$ is always ignored if the previous command was a write command. Data is clocked in by the next rising edge of K and by the rising edge of the K that follows.

Σ2x1B2 DOUBLE DATA RATE SEPARATE I/O SIGMARAM WRITE FIRST



SPECIAL FUNCTIONS

Byte Write Control
Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g. $\overline{BW0}$ controls D0- D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence. Each write enable command and write address loaded into the RAM provides the base address for a 4 beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9 bit byte may be masked in any write sequence.

RAM WRITE SEQUENCE USING BYTE WRITE ENABLES (x18)

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0-D8	D9-D17
Beat 1	0	1	Data In	Don't care
Beat 2	1	0	Don't Care	Data In

RESULTING WRITE OPERATION

Byte1	Byte 2	Byte 3	Byte 4
D0-D8	D9-D17	D0-D8	D9-D17
Written	Unchanged	Unchanged	Written

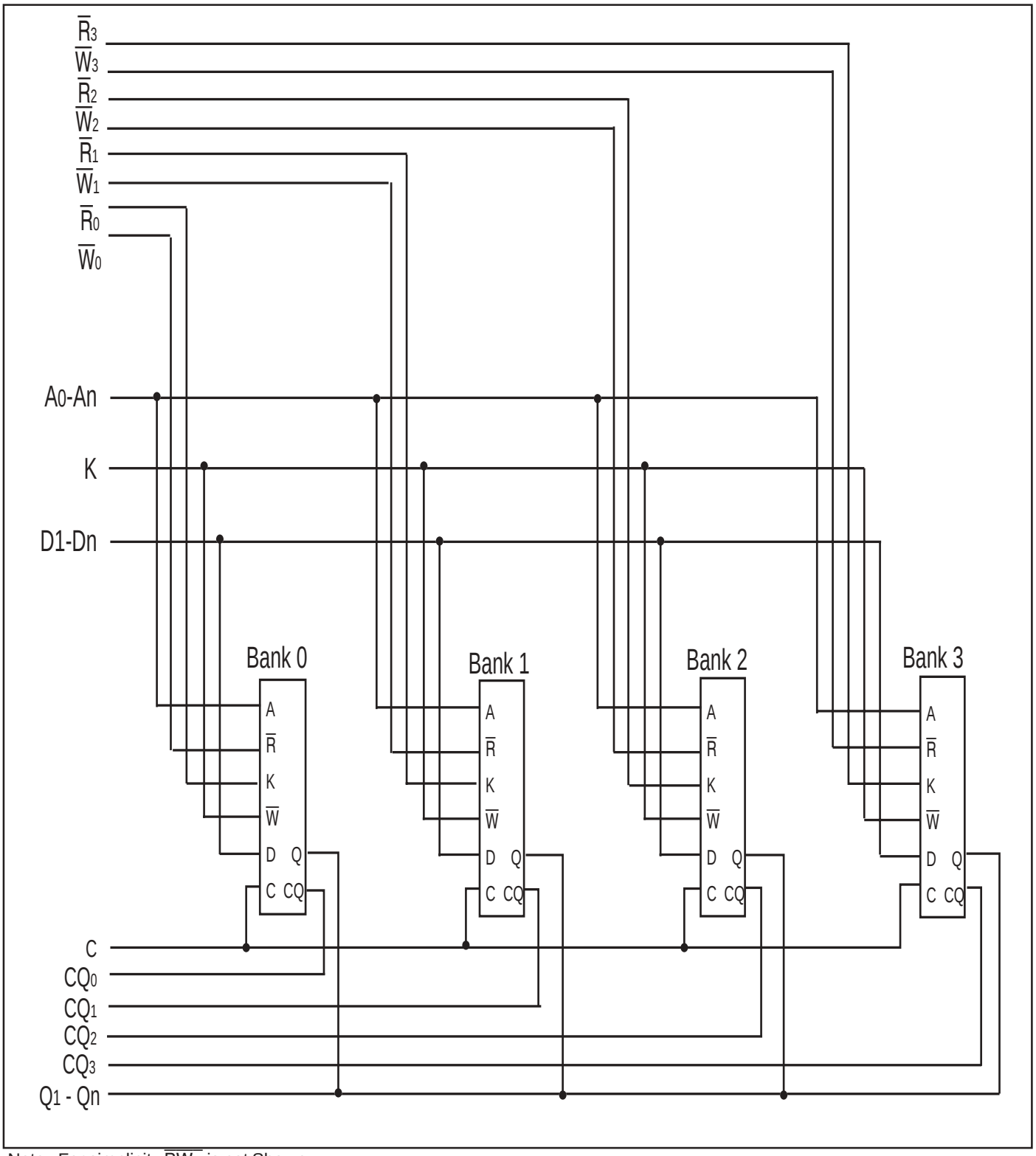
Output Register Control

Separate I/O SigmaRAMs offer two mechanisms for controlling the output data registers. Typically control is handled by the Output Register Clock input C. The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K clock. If the C clock input is tied high, the RAM reverts to K control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

Echo Clock

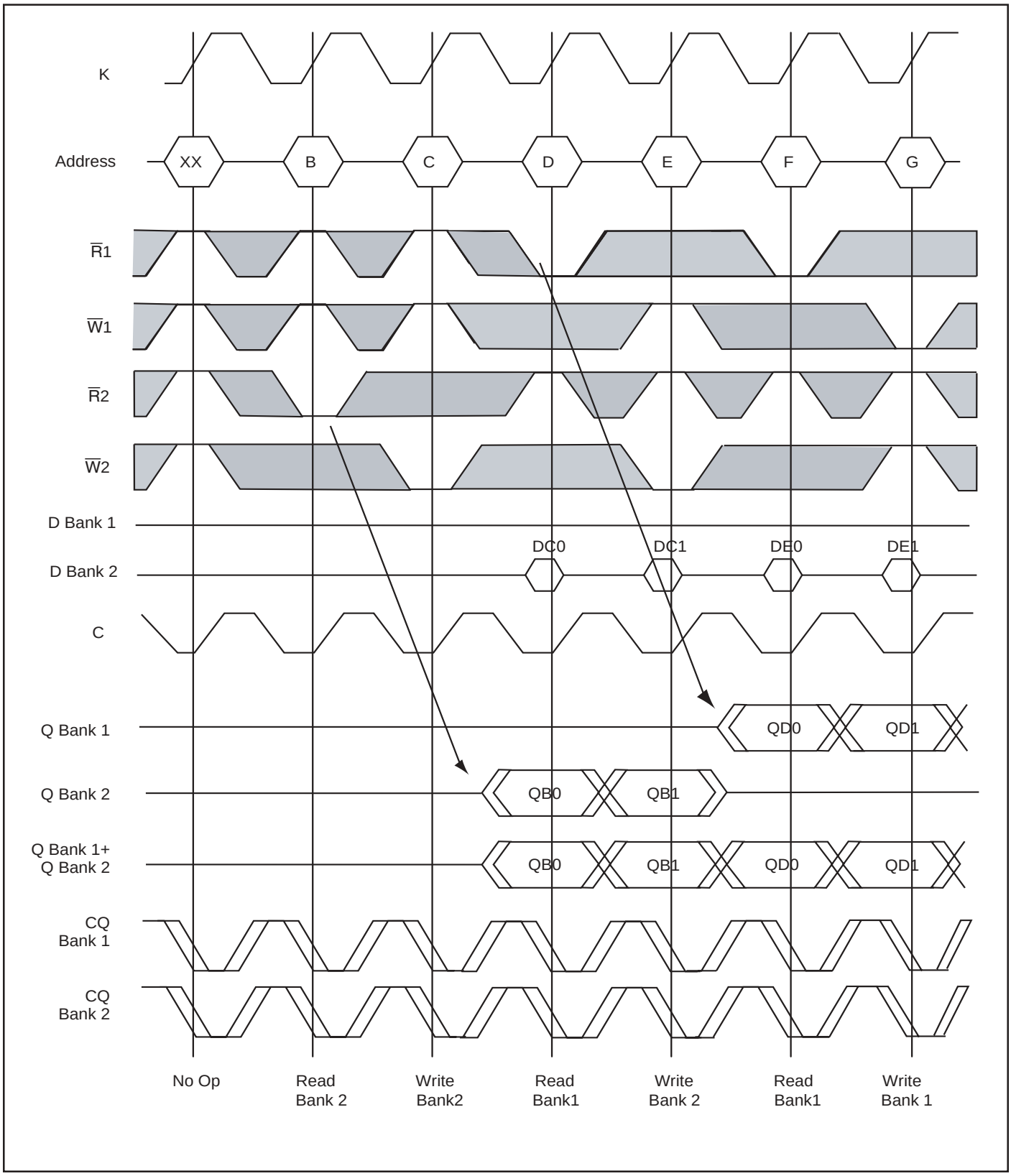
SigmaRAMs feature Echo Clocks, $\overline{CQ}$ and CQ, that track the performance of the output drivers. The Echo Clocks are delayed copies of the Output Register clock, C. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. SigmaRAMs provide both in-phase, or true, Echo Clock outputs (CQ) and inverted Echo Clock outputs ($\overline{CQ}$). Echo Clocks are always active neither inhibiting reads via holding $\overline{R}$ high, nor deselection of the RAM via holding $\overline{R}$ and $\overline{W}$ high will deactivate the Echo Clocks.

FOUR BANK DEPTH EXPANSION SCHEMATIC



Note: For simplicity $\overline{BW}n$ is not Shown

SIGMARAM DEPTH EXPANSION



SEPARATE I/O Σ2x1B2 SIGMAQUAD SRAM TRUTH TABLE

A	$\overline{R}$	$\overline{W}$	Previous Operation	Current Operation	D	D	Q	Q
K↑ (t_n)	K↑ (t_n)	K↑ (t_n)	K↑ (t_{n-1})	K↑ (t_n)	K↑ (t_{n+1})	K↑ (t_{n+2})	K↑ (t_{n+1})	K↑ (t_{n+2})
X	1	1	Deselect	Deselect	X	—	Hi-Z	—
X	1	X	Write	Deselect	D1	—	Hi-Z	—
X	X	1	Read	Deselect	X	—	Q2	—
V	1	0	Deselect	Write	D0	D1	Hi-Z	—
V	0	X	Deselect	Read	X	—	Q0	Q1
V	X	0	Read	Write	D0	D1	Q1	—
V	0	X	Write	Read	D1	—	Q0	Q1

Note:
1. "1" = input "high"; "0" = input "low"; "V" = input "vaild"; "X" = input "don't care"
2. "—" indicates that the input requirement or output state is determined by the next operation.
3. Q0 and Q1 indicate the first, second, third, and fourth pieces of output data transferred during Read operations.
4. D0 and D1 indicate the first, second, third, and fourth pieces of input data transferred during Write operations.
5. Qs are tri-stated for one cycle in respones to Deselect and Write commands, one cycle after the command is sampled, except when preceded by a Read command.
6. CQs are never tri-stated.
7. Users should not clock in metastable addresses.

x18 BTYE WRITE CLOCK TRUTH TABLE

$\overline{BW}$	$\overline{BW}$	Current operation	D	D
K↑ (t_{n+1})	K↑ (t_{n+2})	K↑ (t_n)	K↑ (t_{n+1})	K↑ (t_{n+2})
T	T	Write Dx stored if $\overline{BWn}$ = 0 in all four data transfers	D1	D2
T	F	Write Dx stored uf $\overline{BWn}$ = 0 in 1st data transfer only	D1	X
F	F	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	X
F	F	Write Abort No Dx stored in any of the four data transfers	X	X

Note:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0 then $\overline{BW}$ = "T" else $\overline{BW}$ = "F"

OUTPUT DRIVER IMPEDANCE CONTROL

HSTL I/O SigmaRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to Vss via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a vendor specified tolerance is between 150Ω and 300Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. Impedance updates for "0s" occur whenever the SRAM is driving "1s" for the same DO's (and vice-versa for "1s") or the SRAM is in Hi-Z. The SRAM requires 32K start-up cycles, selected or deselected, after V_{DD} reaches its operating range to reach its programmed output driver impedance.

x36 BYTE WRITE ENABLE TRUTH TABLE

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0-D8	D9-D17	D18-D26	D27-D35
1	1	1	1	Don't Care	Don't Care	Don't Care	Don't Care
0	1	1	1	Data In	Don't Care	Don't Care	Don't Care
1	0	1	1	Don't Care	Data In	Don't Care	Don't Care
0	0	1	1	Data In	Data In	Don't Care	Don't Care
1	1	0	1	Don't Care	Don't Care	Data In	Don't Care
0	1	0	1	Data In	Don't Care	Data In	Don't Care
1	0	0	1	Don't Care	Data In	Data In	Don't Care
0	0	0	1	Data In	Data In	Data In	Don't Care
1	1	1	0	Don't Care	Don't Care	Don't Care	Data In
0	1	1	0	Data In	Don't Care	Don't Care	Data In
1	0	1	0	Don't Care	Data In	Don't Care	Data In
0	0	1	0	Date In	Data In	Don't Care	Data In
1	1	0	0	Don't Care	Don't Care	Data In	Data In
1	1	0	0	Dont' Care	Don't Care	Data In	Data In
0	1	0	0	Data In	Don't Care	Data In	Data In
1	0	0	0	Don't Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 BYTE WRITE ENABLE ($\overline{BWn}$) TRUTH TABLE

$\overline{BW0}$	$\overline{BW1}$	D0-D8	D9-D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

ABSOLUTE MAXIMUM RATINGS

(All voltages reference to GND)

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.5	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 2.3	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.3 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.3 V max.)	V
I_{IN}	Input Current on Any Pin	±100	mA dc
I_{OUT}	Output Current on Any Pin	±100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	-55 to 125	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Operation should be limited to Recommended Operating Conditions. Exposure to conditions exceeding Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

POWER SUPPLY CHARACTERISTICS (T_A = 0 min., 25 typ, 70 max °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}[1]	1.8 V I/O Supply Voltage	1.7	1.8	V_{DD}	V
	1.5 V I/O Supply Voltage	1.4	1.5	1.6 V	V

Note:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 1.4 V ≤ V_{DDQ} ≤ 1.6V (i.e., 1.5 V I/O) and 1.7 V ≤ V_{DDQ} ≤ 1.9 V (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
2. The power supplies need to be powered up in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.

HSTL I/O DC INPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	V_{REF} + 200	—	—	mV
V_{IL}	Input Low Voltage	—	—	V_{REF} + 200	mV
V_{DIF}	Clock Input Differential Voltage	400	—	—	mV
V_{REF}	V_{REF} DC Voltage	V_{DD}(min)/2	—	V_{DDQ}(max)/2	mV

Note:
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics, V_{IH}, V_{IL}, Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

I/O CAPACITANCE (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter		Test conditions	Min.	Max.	Unit
C_A	Address	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_B	Control	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_{CK}	Clock	Input Capacitance	V_{IN} = 0 V	—	3.5	pF
C_{DQ}	Data	Output Capacitance	V_{OUT} = 0 V	—	4.5	pF
C_{CQ}	CQ Clock	Output Capacitance	V_{OUT} = 0 V	—	4.5	pF

Note: These parameters are sampled and not 100% tested.

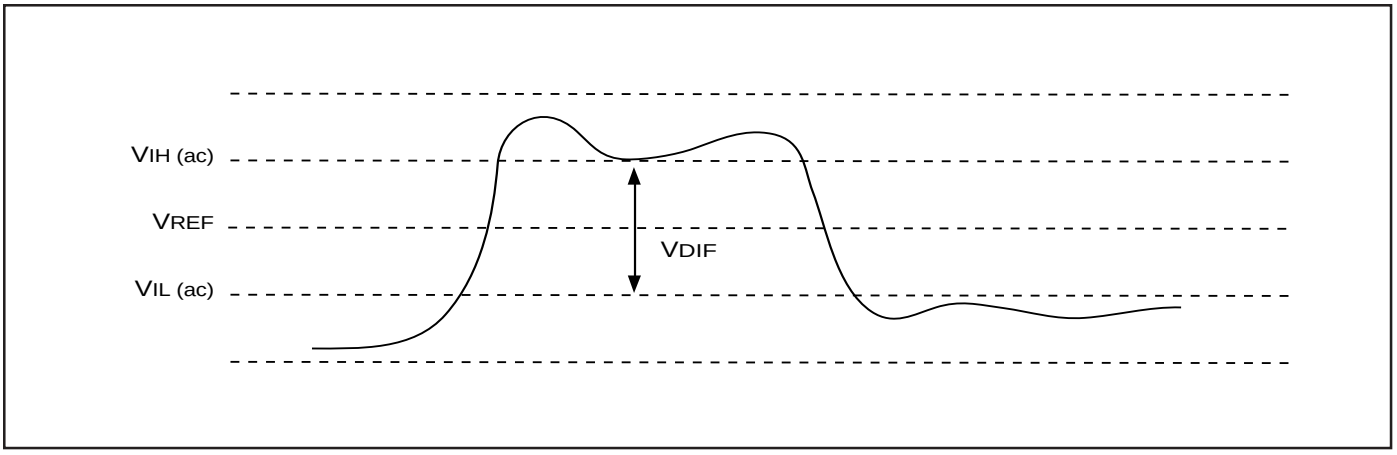
AC TEST CONDITIONS

(V_{DD} = 1.8V ± 0.1V, T_A = 0 to 85°C)

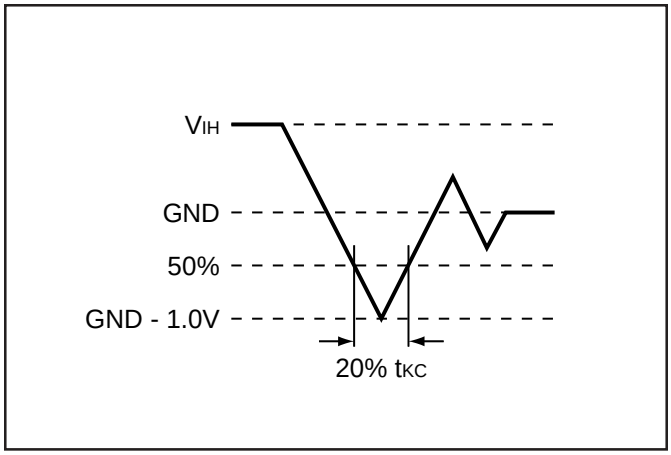
Parameter	Symbol	Conditions		Units
V_{DDQ}		1.5V±0.1	1.8 ±0.1	V
V_{REF} Peak to Peak AC Votlage(1)		5% V_{REF} (DC)	5% V_{REF} (DC)	mV
Input High Level(2,3)	V_{IH}	1.25	1.4	V
Input Low Level(2,3)	V_{IH}	0.25	0.4	V
Input Rise & Fall Time		2.0	2.0	V/ns
Clock Input Differential Voltage(2,3)		800	800	mV
Input Reference Level		0.75	0.9	V
Clock Input High Voltage	V_{KIH}	1.25	1.4	V
Clock Input Low Voltage	V_{KIL}	0.25	0.4	V
Clock Input Rise & Fall Time		2.0	2.0	V/ns
Clock Input Reference Level		0.75	0.9	V
Output Reference Level		0.75	0.9	V
Output Load Conditions ZQ = V_{IH}		see below	see below	

Notes:
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
2. SRAM performance is a function of clock input differential voltage (V_{REF}). The RAM can be operated with a single ended clocking with either K or $\overline{K}$ tied to V_{REF} .
3. To guarantee AC characteristics, V_{IH} ,V_{IH} ,Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

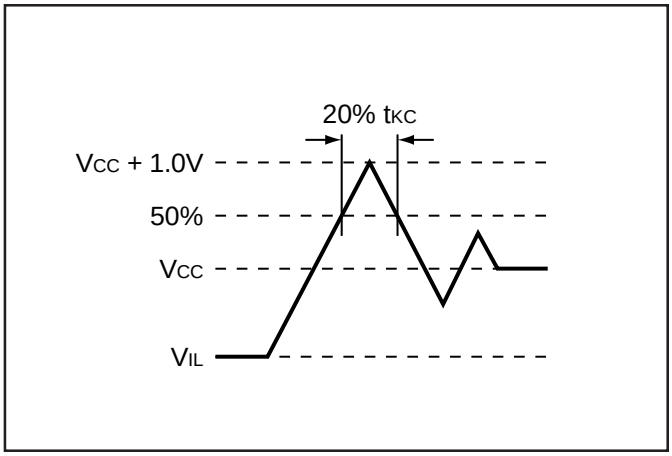
HSTL I/O AC INPUT DEFINITIONS



UNDERSHOOT MEASUREMENT AND TIMING



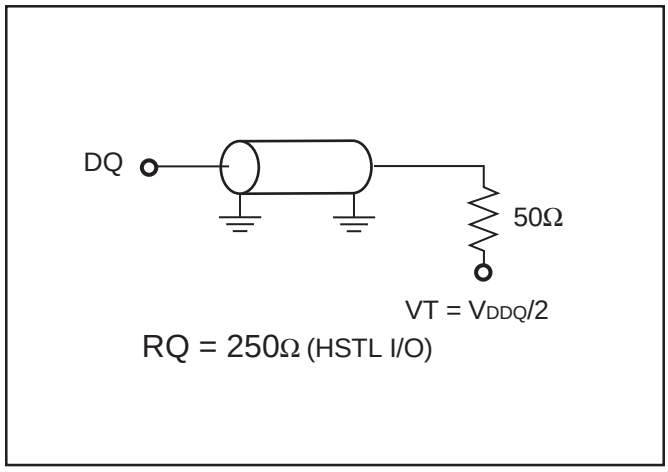
OVERSHOOT MEASUREMENT AND TIMING



AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	V_{DDQ}
Input Low level	0V
Max. Input slew rate	2V/ns
Input and Output Timing and Reference Level	$V_{DDQ}/2$

AC TEST LOADS



INPUT AND OUTPUT LEAKAGE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{IL}	Input Leakage Current (except mode pins)	V_{IN} = 0 to V_{DD}	–2	2	µA
I_{INM}	Mode Pin Input Current	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0V \leq V_{IN} \leq V_{IL}$	–100 –2	2 2	µA
I_{OL}	Output Leakage Current	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2	2	µA

SELECTABLE IMPEDANCE OUTPUT DRIVER DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
V_{OH}	Output High Voltage[1,3]	$V_{DDQ}/2$	V_{DDQ}	V
V_{OL}	Output Low Voltage [2,3]	V_{SS}	$V_{DDQ}/2$	V

Notes:
1. $I_{OH} = (V_{DDQ}/2) / (RQ / 5)$ +/- 15% @ $V_{OH} = V_{DDQ}/2$ (for: 150Ω £ RQ £ 300Ω).
2. $I_{OL} = (V_{DDQ}/2) / (RQ / 5)$ +/- 15% @ $V_{OL} = V_{DDQ}/2$ (for: 150Ω £ RQ £ 300Ω).
3. Parameter tested with RQ=250Ω and V_{DDQ} = 1.5 V or 1.8V

OPERATING CURRENTS

(T_A = 0° to 70°C Commerical, T_A = -40° to 85°C Industrial)

Symbol	Parameter	Test Conditions	-333 Com.	-333 Ind.	-300 Com.	-300 Ind.	-250 Com.	-250 Ind.	-200 Com	-200 Ind	Units
I_{DD}	Operating Current	CE1 ≤ V_{IL} Max. $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} = V_{IN} \geq V_{IH}$			tbd						mA
I_{SB1} & I_{SB2}	Bank Deselect Current & Chip Disable Current	CE1 ≤ V_{IH} Min. or CE2 or CE3 False $t_{KHKH} \geq t_{KHKH}$ Min. All other inputs $V_{IL} \geq V_{IN} \geq V_{IH}$			tbd tbd						mA
I_{DD3}	CMOS Deselect Current	Device Deselected All inputs Vss+0.10V ≥ V_{IN} ≥ V_{DD}–0.10V			tbd tbd						mA
I_{DD}	Average Power Supply Operating Current	I_{OUT} = 0mA $V_{IN} = V_{IH}$ or V_{IL}			tbd tbd						mA
I_{DD2}	Power Supply Deselect Operating Current	I_{OUT} = 0mA $V_{IN} = V_{IH}$ or V_{IL}			tbd						mA

Power measured with output pins floating.

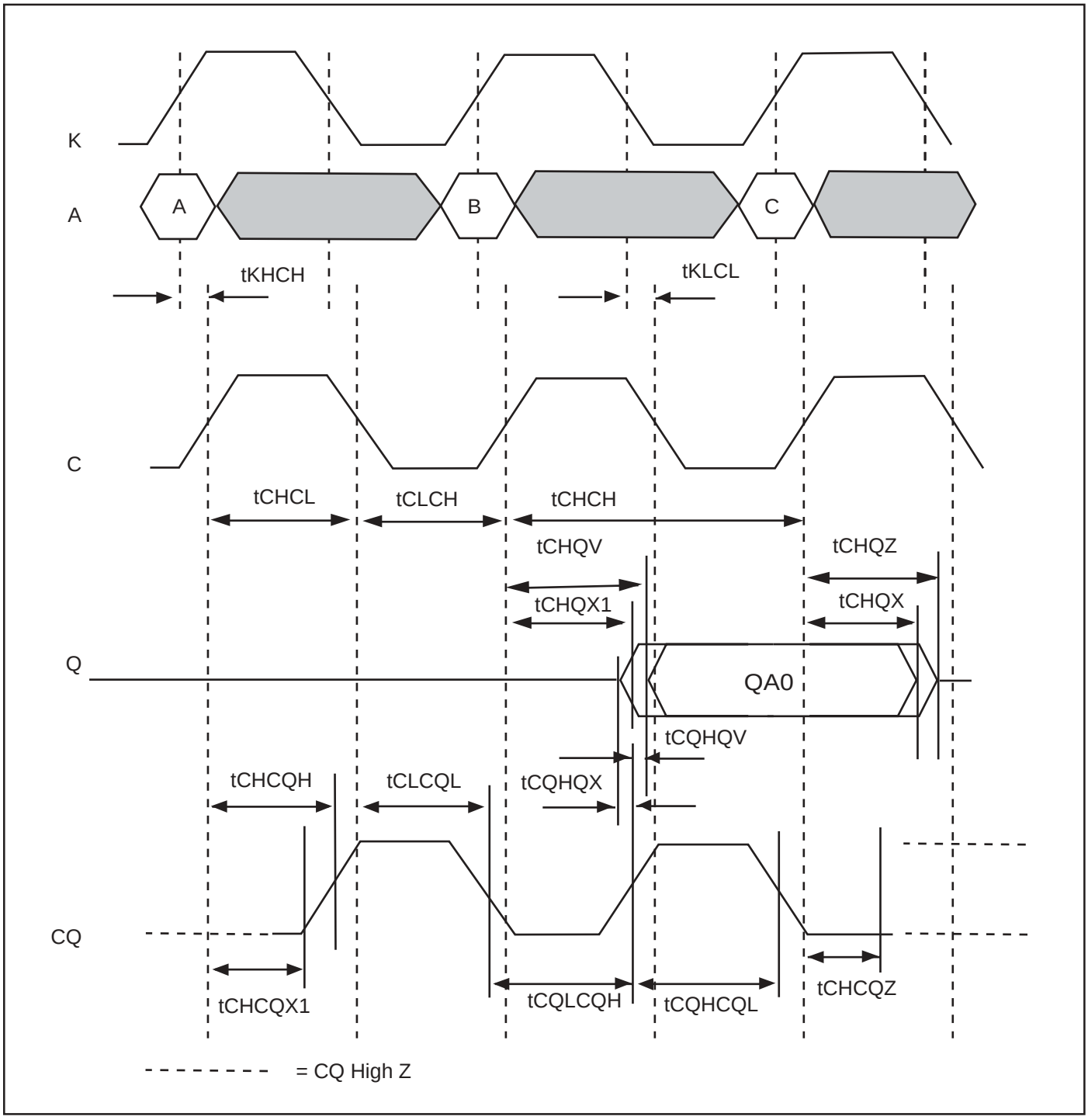
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	-333 Min	-333 Max	-300 Min	-300 Max	-250 Min	-250 Max	Unit
t_{KHKH}	Input Clock Cycle Time	3.0	—	3.3	—	4.0	—	ns
t_{CHCH}	Output Clock Cycle Time	3.0	—	3.3	—	4.0	—	ns
t_{KHKL}	Input Clock HIGH Time	1.2	—	1.3	—	1.6	—	ns
t_{CLCL}	Output Clock HIGH Time	1.2	—	1.3	—	1.6	—	ns
t_{KHKH}	Input Clock LOW Time	1.2	—	1.3	—	1.6	—	ns
t_{CLCH}	Output Clock LOW Time	1.2	—	1.3	—	1.6	—	ns
t_{KHCH}	Input Clock High to Output Clock High	0	2.0	0	2.2	0	2.6	ns
t_{KLCL}	Input Clock Low to Output Clock Low	0	2.0	0	2.2	0	2.6	ns
t_{CHQV}	Output Clock High to Output Valid	—	1.6	—	1.8	—	2.1	ns
t_{CLQV}	Output Clock Low to Output Valid	—	1.6	—	1.8	—	2.1	ns
t_{CHQZ}	Output Clock High to Output in High-Z	0.5	1.6	0.5	1.8	0.5	2.1	ns
t_{CLQX}	Output Clock Low to Output Invalid	0.5	—	0.5	—	0.5	—	ns
t_{CHQX}	Output Clock High to Output Invalid	0.5	—	0.5	—	0.5	—	ns
t_{CHQX1}	Output Clock High to Output in Low-Z	0.5	—	0.5	—	0.5	—	ns
t_{CHCQX1}	Output Clock High to Echo Clock Low-Z	0.5	—	0.5	—	0.5	—	ns
t_{CHCQH}	Output Clock High to Echo Clock High	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CLCQL}	Output Clock Low to Echo Clock Low	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CQHQX}	Echo Clock High to Output Invalid	-0.2	—	-0.2	—	-0.25	—	ns
t_{CQLQX}	Echo Clock Low to Output Invalid	-0.2	—	-0.2	—	-0.25	—	ns
t_{CQHQV}	Echo Clock High to Output Valid	—	0.2	—	0.2	—	0.25	ns
t_{CQLQX}	Echo Clock Low to Output Invalid	-0.2	—	-0.2	—	-0.25	—	ns
t_{CQLQV}	Echo Clock Low to Output Valid	—	0.2	—	0.2	—	0.25	ns
t_{KHCQZ}	Input Clock High to Echo Clock High-Z	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CHCQZ}	Output Clock High to Echo Clock High-Z	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{CQHCQL}	Echo Clock High Time	t_{CHCL} ±100 ps		t_{CHCL} ±100 ps		t_{CHCL} ±100 ps		ns
t_{CQLCQH}	Echo Clock Low Time	t_{CLCH} ±100 ps		t_{CLCH} ±100 ps		t_{CLCH} ±100 ps		ns
$t_{CQHCQL2}$	Echo Clock High Time	t_{KHKL} ±100 ps		t_{KHKL} ±100 ps		t_{KHKL} ±100 ps		ns
$t_{CQLCQH2}$	Echo Clock Low Time	t_{KLKH} ±100 ps		t_{KLKH} ±100 ps		t_{KLKH} ±100 ps		ns
t_{KHQV}	Input Clock High to Ouput Valid	—	1.6	—	1.8	—	2.1	ns
t_{KLQV}	Input Clock Low to Ouput Valid	—	1.6	—	1.8	—	2.1	ns
t_{KHQZ}	Input Clock High to Output in High-Z	0.5	1.6	0.5	1.8	0.5	2.1	ns
t_{KHQX}	Input Clock High to Output Invalid	0.5	—	0.5	—	0.5	—	ns
t_{KLQX}	Input Clock Low to Output Invalid	0.5	—	0.5	—	0.5	—	ns
t_{KHQX1}	Input Clock High to Output in Low-Z	0.5	—	0.5	—	0.5	—	ns
t_{KHCQX1}	Input Clock High to Echo Clock Low-Z	0.5	—	0.5	—	0.5	—	ns

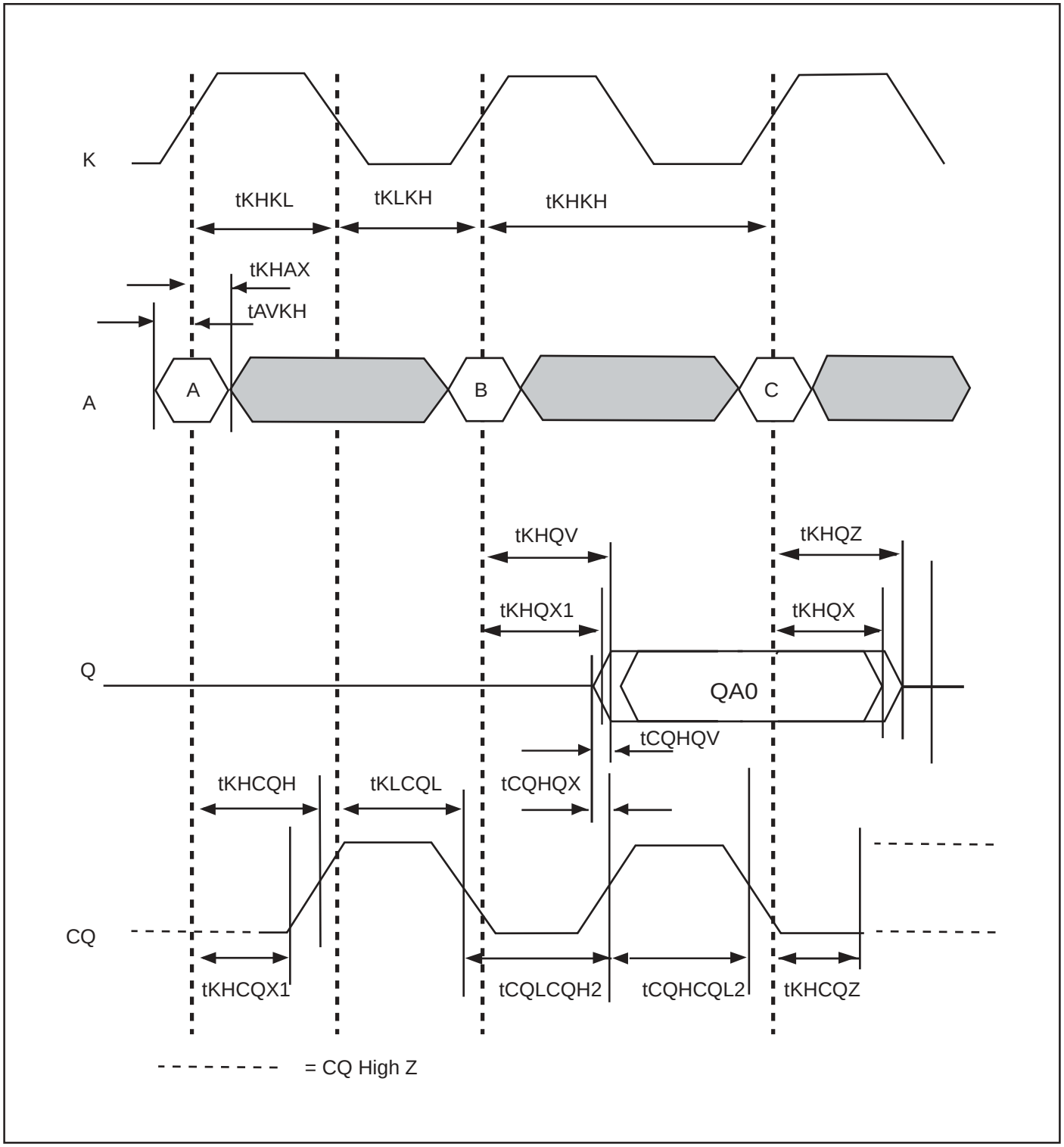
Symbol	Parameter	-333 Min	-333 Max	-300 Min	-300 Max	-250 Min	-250 Max	Unit
t_{KHCQH}	Input Clock High to Echo Clock High	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{KHCQL}	Input Clock Low to Echo Clock Low	0.5	1.5	0.5	1.7	0.5	2.0	ns
t_{AVKH}	Address Vailid to Input Clock High	0.6	—	0.7	—	0.8	—	ns
t_{AHAX}	Input Clock High to Address Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{IVKH}	$\overline{R}$,$\overline{W}$ or E Input Valid to Input Clock High	0.6	—	0.7	—	0.8	—	ns
t_{KHIX}	Input Clock High to $\overline{R}$,$\overline{W}$ or E Don't Care	0.4	—	0.4	—	0.5	—	ns
t_{DVKH}	Data In and $\overline{B}$x Valid to Input Clock High	0.32	—	0.35	—	0.45	—	ns
t_{KHDX}	Input Clk HIGH to DataIn & $\overline{B}$x Don't Care	0.27	—	0.30	—	0.35	—	ns
t_{DVKL}	Data In and $\overline{B}$x Valid to Input Clock Low	0.32	—	0.35	—	0.40	—	ns
t_{KLDX}	Input Clk Low to DataIn & $\overline{B}$x Don't Care	0.27	—	0.30	—	0.35	—	ns

Notes:
1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage $t_{CHCQZ} < t_{CHQCX}1$ and $t_{KHCQZ} < t_{KHCQX}1$.
4. Tested using AC Test Load B.

READ CYCLE TIMING USING C TO CONTROL OUTPUT DATA

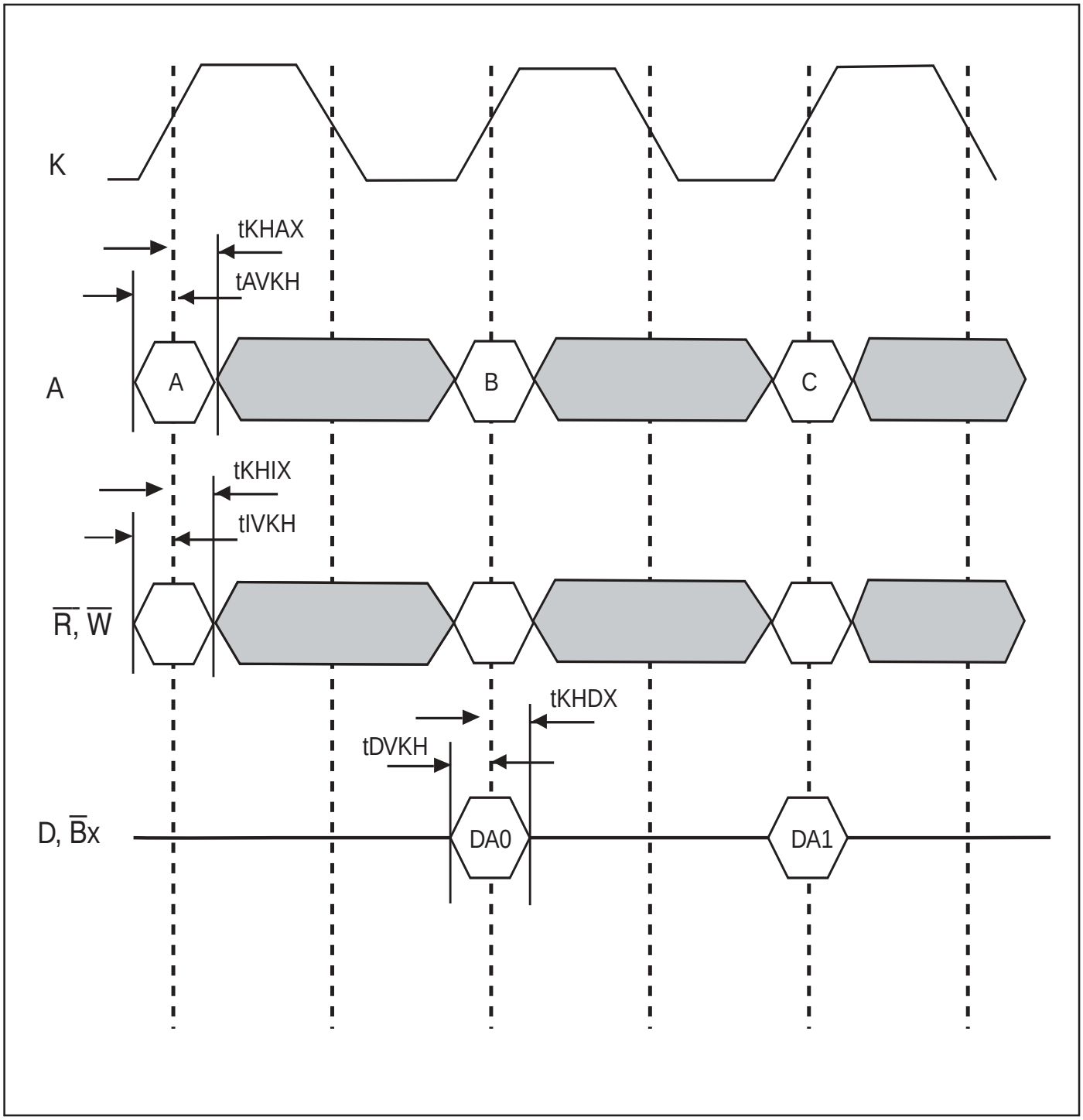


READ CYCLE TIMING USING K TO CONTROL OUTPUT DATA



Note: When K is used to control output data, C should be tied "high" (not shown).

CONTROL AND DATA IN TIMING



JTAG PORT OPERATION

Overview

The JTAG Port on this RAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Unlike JTAG implementations that have been common among SRAM vendors for the last several years, this implementation does offer a form of EXTEST, known as Clock Assisted EXTEST, reducing or eliminating the “hand coding” that has been required to overcome the test program compiler errors caused by previous non-compliant implementations.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the RAM with the JTAG Port unused, TCK should be tied Low, TDI and TMS may be left floating or tied to V_{DD}. TDO should be left unconnected.

JTAG PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP Controller. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG PORT REGISTERS

Overview

The JTAG registers, refered to as Test Access Port (TAP) registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

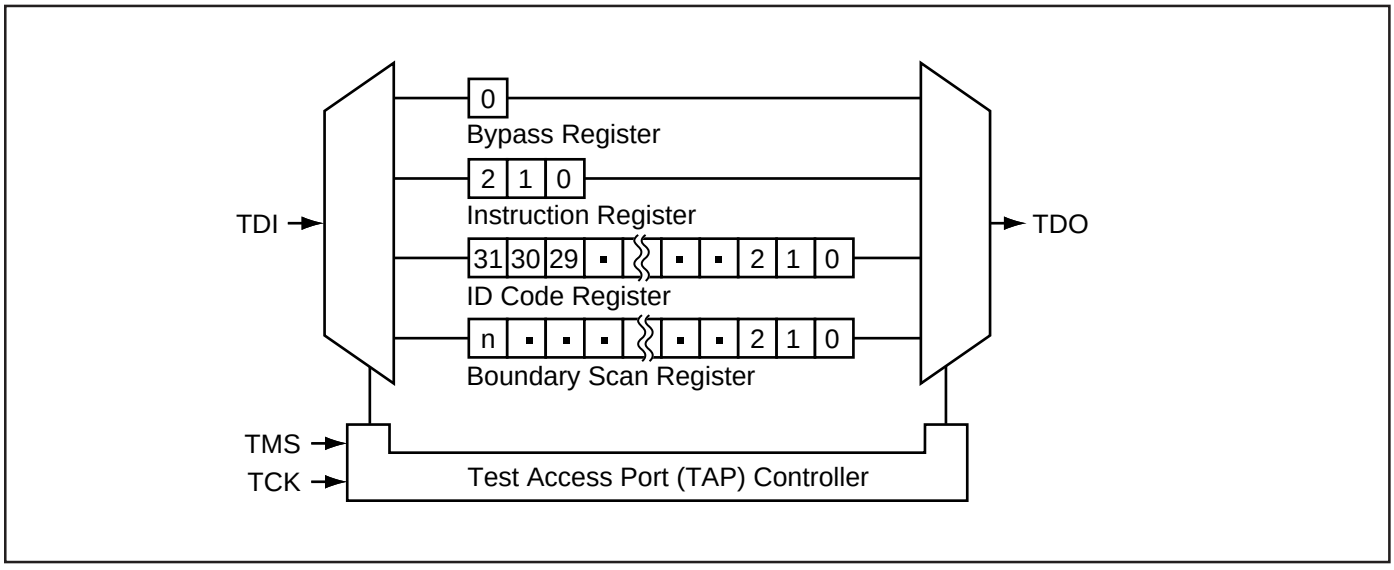
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the following Scan Order Table. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP BLOCK DIAGRAM



IDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID REGISTER CONTENTS

	Die Revision Code				Not Used												I/O Configuration				ISSI Technology JEDEC Vendor ID Code										Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	0	1	0	1	1
x36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	1	0	1	1

BOUNDARY SCAN EXIT ORDER TABLE

Order	Pin ID	Order	Pin ID	Order	Pin ID	Order	Pin ID	Order	Pin ID
1	6R	23	10K	45	9B	67	3B	89	2K
2	6P	24	9J	46	10B	68	1C	90	1K
3	6N	25	9K	47	11A	69	1B	91	2L
4	7P	26	10J	48	10A	70	3D	92	3L
5	7N	27	11J	49	9A	71	3C	93	1M
6	7R	28	11H	50	8B	72	1D	94	1L
7	8R	29	10G	51	7C	73	2C	95	3N
8	8P	30	9G	52	6C	74	3E	96	3M
9	9R	31	11F	53	8A	75	2D	97	1N
10	11P	32	11G	54	7A	76	2E	98	2M
11	10P	33	9F	55	7B	77	1E	99	3P
12	10N	34	10F	56	6B	78	2F	100	2N
13	9P	35	11E	57	6A	79	3F	101	2P
14	10M	36	10E	58	5B	80	1G	102	1P
15	11N	37	10D	59	5A	81	1F	103	3R
16	9M	38	9E	60	4A	82	3G	104	4R
17	9N	39	10C	61	5C	83	2G	105	4P
18	11L	40	11D	62	4B	84	1H	106	5P
19	11M	41	9C	63	3A	85	1J	107	5N
20	9L	42	9D	64	2A	86	2J	108	5R
21	10L	43	11B	65	1A	87	3K	109	EXTOE
22	11K	44	11C	66	2B	88	3J		1→ Active

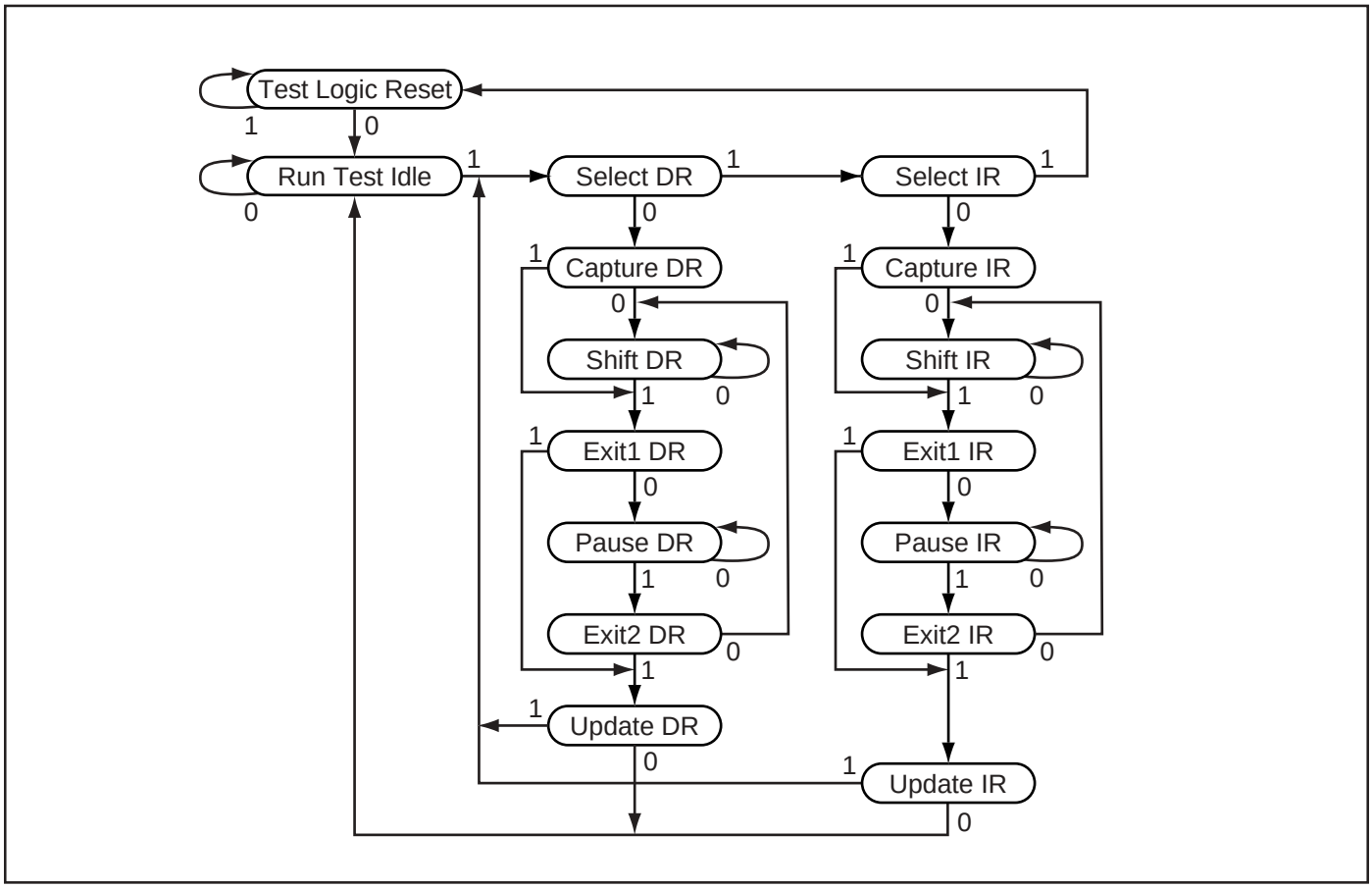
TAP CONTROLLER INSTRUCTION SET

Overview

TThere are two classes of instructions defined in the Standard 1149.1-1990; standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because one of the mandatory instructions, EXTEST, is uniquely implemented. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST but can perform the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state, the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG TAP CONTROLLER STATE DIAGRAM



INSTRUCTION DESCRIPTIONS

BYPASS

When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Some Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the BSDL file. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins. The Update-DR controller state transfers the contents of boundary scan cells into the holding register of each cell associated with an output pin on the RAM.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are sampled and transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state. Boundary Scan Register con-tents may then be shifted serially through the register using the Shift-DR command or the controller can be skipped to the Update-DR com-mand. When the controller is placed in the Update-DR state, a RAM that has a fully compliant EXTEST function drives out the value of the Boundary Scan Register location associated with which each output pin.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z/PRELOAD

The SAMPLE-Z instruction operates exactly like SAMPLE/PRELOAD except that loading the SAMPLE-Z instruction forces all the RAM's output drivers, except TDO, to an inactive drive state (High-Z).

RFU

These instructions are reserved for future use. In this device they replicate the BYPASS instruction.

JTAG TAP INSTRUCTION SET SUMMARY

Instruction	Code	Description
EXTEST(1)	000	Places the Boundary Scan Register between TDI and TDO. When EXTEST is selected, data will be driven out of the DQ pad.
IDCODE(1,2)	001	Preloads ID Register and places it between TDI and TDO.
SAMPLE-Z(1)	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z.
RFU(1)	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.
SAMPLE/PRELOAD(1)	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.
Private(1)	101	Private instruction.
RFU(1)	110	Do not use this instruction; Reserved for Future Use.
BYPASS(1)	111	Places Bypass Register between TDI and TDO.

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in Test-Logic-Reset state.

JTAG DC RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 85°C)

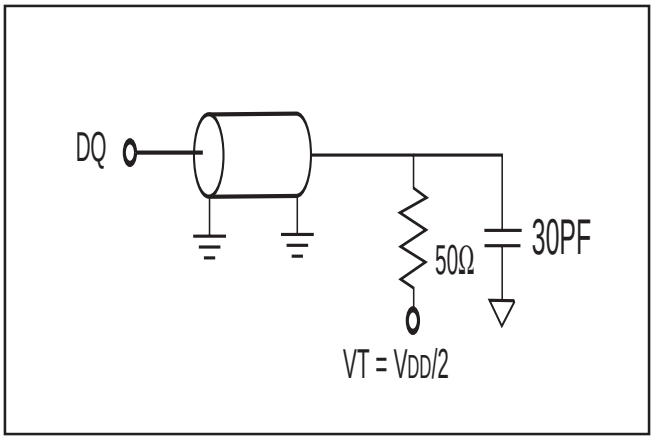
Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{TIH}	JTAG Input High Voltage(1)			0.65*V_{DD}	V_{DD} +0.3	V
V_{TIL}	JTAG Input Low Voltage(1)			-0.3	0.35*V_{DD}	V
V_{TOH}	JTAG Output High Voltage(2)	CMOS	I_{TOH} = -100µA	V_{DD}-0.1	—	V
		TTL	I_{TOH} = -8mA	V_{DD}-0.4	—	
V_{TOL}	JTAG Output Low Voltage	CMOS	I_{TOL} = 100µA	—	0.1	V
		TTL	I_{TOL} = 8mA	—	0.4	
I_{OLT}	JTAG Output Leakage Current V_{OUT} = 0V to V_{DD}		Output Disable	2	2	µA
I_{INTH}	JTAG Input Leakage Current		$V_{DD} \geq V_{IN} \geq V_{IL}$	-100	2	µA
I_{INTL}	JTAG Input Leakage Current		$0V \leq V_{IN} \leq V_{IL}$	-2	2	µA

Notes:
1. Input Under/Overshoot voltage must be -1V<Vi<V_{DD}+1V with pulse width not exceed 20% t_{TKC}.
2. The TDO output driver is erved by the V_{DD} supply

JTAG AC TEST CONDITIONS

Symbol	Parameter	Test Conditions	Unit
V_{TIH}	JTAG Input High Voltage	V_{DD}-0.2	V
V_{TIL}	JTAG Input Low Voltage	0.2	V
	JTAG Input Rise & Fall Time	1.0	V/ns
	JTAG Input Reference Level	V_{DD}/2	V
	JTAG Output Reference Level	V_{DD}/2	V
	JTAG Output Load Condition	see AC TEST LOADS	

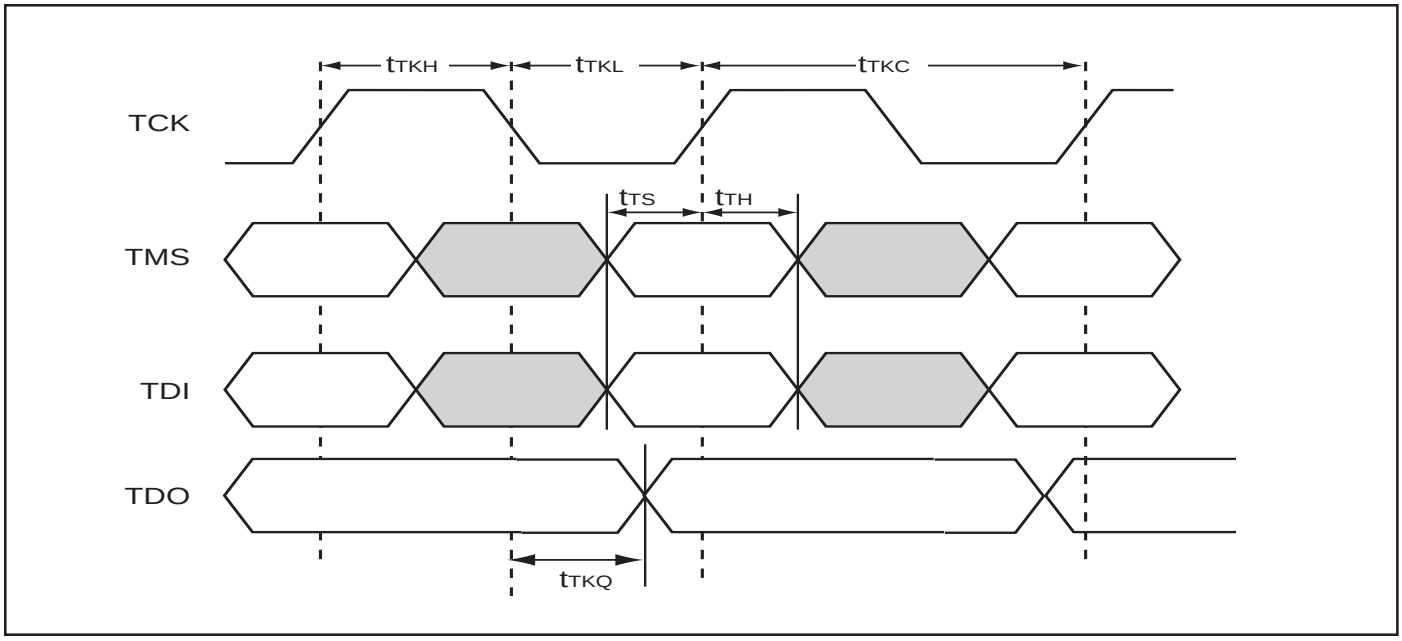
JTAG PORT AC TEST LOAD



JTAG PORT AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
t_{TKC}	TCK Cycle Time	50	—	ns
t_{TKQ}	TCK LOW to TDO Valid	—	20	ns
t_{TKH}	TCK HIGH Pulse Width	20	—	ns
t_{TKL}	TCK LOW Pulse Width	20	—	ns
t_{TS}	TDI & TMS Set Up Time	10	—	ns
t_{TH}	TDI & TMS Hold Time	10	—	ns

JTAG PORT TIMING DIAGRAM



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

	Frequency	Order Part No.	Package
x18	250	IS61LSSS102418-250B	209-pin BGA
	300	IS61LSSS102418-300B	209-pin BGA
	333	IS61LSSS102418-333B	209-pin BGA
x36	250	IS61LSSS51236-250B	209-pin BGA
	300	IS61LSSS51236-300B	209-pin BGA
	333	IS61LSSS51236-333B	209-pin BGA

Industrial Range: -40°C to +85°C

	FrequencySpeed (ns)	Order Part No.	Package
		TBD	

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