

AN2640K

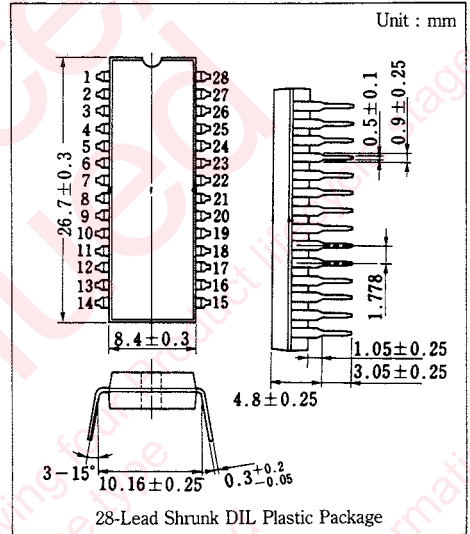
VHD Video Disc Player Chroma and Luminance Processing Circuit

Outline

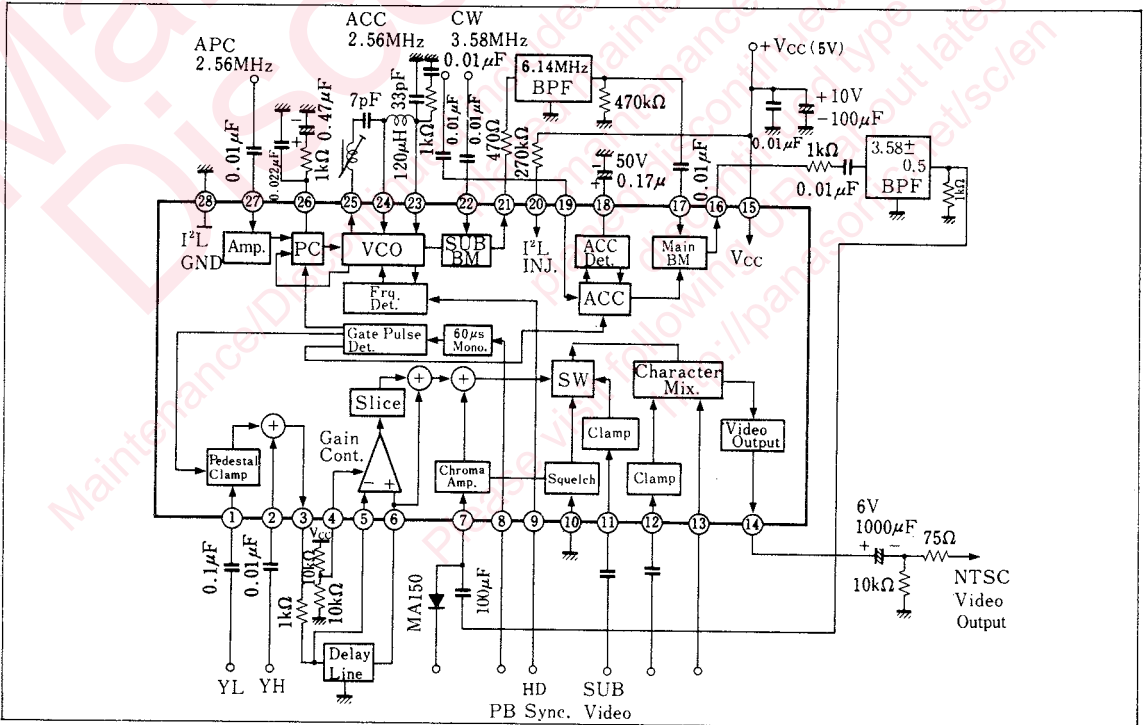
The AN2640K is an integrated circuit designed for VHD-system video disk player. It has functions for chroma signal processing and luminance signal processing.

Features

- 5.0V supply voltage operation
- Frequency conversion from 2.56MHz carrier to 3.58MHz carrier
- Built-in automatic chroma control circuit
- Luminance signal processing
- Video output



Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

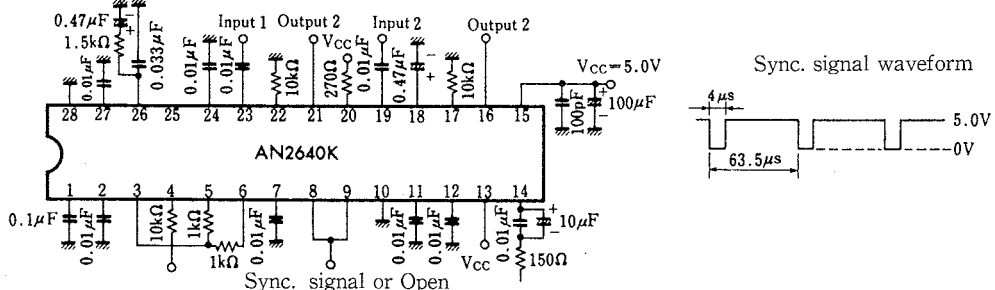
| Item | Symbol | Rating | Unit |
|-------------------------------|------------------|----------|------|
| Supply voltage | V _{CC} | 6.0 | V |
| Supply current | I _{CC} | 110 | mA |
| Power dissipation | P _D | 660 | mW |
| Operating ambient temperature | T _{opr} | -20~+70 | °C |
| Storage temperature | T _{stg} | -55~+150 | °C |

■ Electrical Characteristics (Ta=25°C)

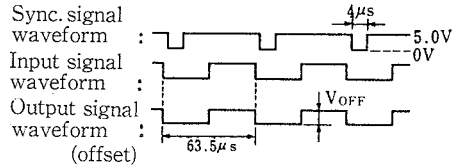
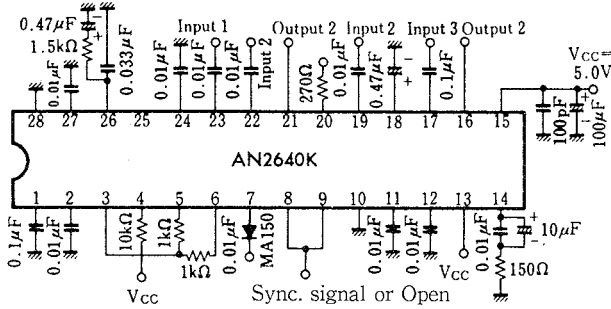
| Item | Symbol | Test Circuit | Condition | min. | typ. | max. | Unit |
|-------------------------------|--------------------|--------------|---|------|------|------|-------------------|
| Total circuit current | I _{tot} | | V _{CC} =5.0V | 50 | 70 | 86 | mA |
| Terminal voltage | V ₂₋₁₀ | | V _{CC} =5.0V | 2.5 | 3 | 3.5 | V |
| Terminal voltage | V ₇₋₁₀ | | V _{CC} =5.0V | 2.5 | 3 | 3.5 | V |
| Terminal voltage | V ₈₋₁₀ | | V _{CC} =5.0V | 2.4 | 2.7 | 3.1 | V |
| Terminal voltage | V ₉₋₁₀ | | V _{CC} =5.0V | 2.4 | 2.7 | 3.1 | V |
| Terminal voltage | V ₁₇₋₁₀ | | V _{CC} =5.0V | 2.8 | 3.6 | 4.4 | V |
| Terminal voltage | V ₁₉₋₁₀ | | V _{CC} =5.0V | 2.2 | 2.8 | 3.5 | V |
| Terminal voltage | V ₂₂₋₁₀ | | V _{CC} =5.0V | 2.8 | 3.5 | 4.2 | V |
| Terminal voltage | V ₂₃₋₁₀ | | V _{CC} =5.0V | 2.2 | 2.7 | 3.3 | V |
| Terminal voltage | V ₂₄₋₁₀ | | V _{CC} =5.0V | 2.2 | 2.7 | 3.3 | V |
| Terminal voltage | V ₂₇₋₁₀ | | V _{CC} =5.0V | 2.4 | 3.1 | 3.7 | V |
| Sub balanced modulator gain | G _{SBM} | 1 | V _{CC} =5.0V, Input: 2.56MHz, 180mVrms | 2.3 | 5 | 6.4 | dB |
| ACC output | A _{AC1} | 1 | V _{CC} =5.0V, Input: 2.56MHz, 70mVrms | 195 | 261 | 350 | mVrms |
| ACC max. gain | G _{AC2} | 1 | V _{CC} =5.0V, Input: 2.56MHz, 10mVrms | 14.5 | 17.5 | 20.5 | dB |
| Sub balanced modulator offset | V _{OFF1} | 2 | V _{CC} =5.0V, Input: 15.7kHz, 1.0V _{P-P} | | 16 | 80 | mV _{P-P} |
| Main balanced modulator | V _{OFF2} | 2 | V _{CC} =5.0V, Input: 15.7kHz, 1.0V _{P-P} | | 43 | 250 | mV _{P-P} |
| Clamp voltage | V _{CL} | 2 | V _{CC} =5.0V | 1.55 | 1.89 | 2.55 | V |
| Video signal select offset | V _{OFF3} | 2 | V _{CC} =5.0V, Input: 15.7kHz, 2.0V _{P-P} | 310 | 520 | 750 | mV _{P-P} |
| APC lock | V _{APC} | 3 | V _{CC} =5.0V, Input: 2.557MHz, 70mVrms | | 12 | 50 | mVrms |
| Freq. detection 1 | A _{FD1} | 4 | V _{CC} =5.0V, Input: 2.568MHz, 180mVrms | 200 | 283 | 400 | mV _{P-P} |
| Freq. detection 2 | A _{FD2} | 4 | V _{CC} =5.0V, Input: 2.547MHz, 180mVrms | 200 | 291 | 400 | mV _{P-P} |
| Sub video output | A _{SV} | 4 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 0.98 | 1.31 | 1.54 | V _{P-P} |
| White char. output | A _W | 4 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 0.93 | 1.44 | 1.87 | V _{P-P} |
| Y _L output | A _{YL} | 5 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 1.05 | 1.32 | 1.6 | V _{P-P} |
| Black char. output | A _{BL} | 5 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 0.55 | 0.75 | 0.95 | V _{P-P} |
| Aperture op. min. | A _{AP1} | 5 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 200 | 290 | 390 | mV _{P-P} |
| Aperture op. max. | A _{AP2} | 5 | V _{CC} =5.0V, Input: 15.7kHz, 0.35V _{P-P} | 1 | 1.26 | 1.5 | V _{P-P} |
| Y _H gain | G _{YH} | 5 | V _{CC} =5.0V, Input: 3.58MHz, 90mVrms | 8.9 | 11.4 | 14.1 | dB |
| Chroma gain | G _{CH} | 5 | V _{CC} =5.0V, Input: 3.58MHz, 35mVrms | 13.5 | 15.9 | 18.6 | dB |

Test Circuit 1 (G_{SBM}, A_{AC1}, A_{AC2})

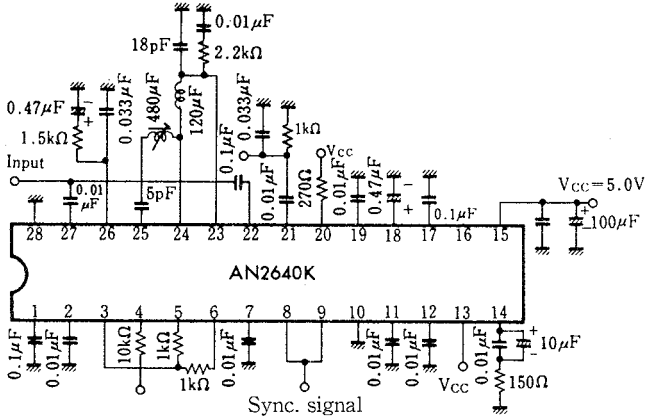
Note) Operating supply voltage range



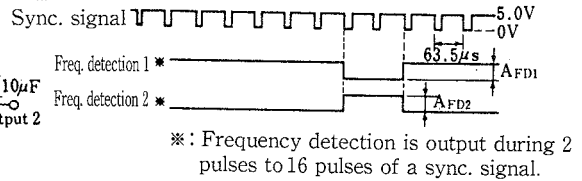
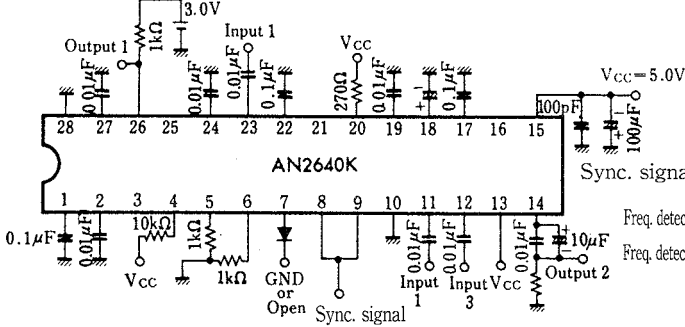
Test Circuit 2 (V_{OFF1} , V_{OFF2} , V_{CL} , V_{OFF3})



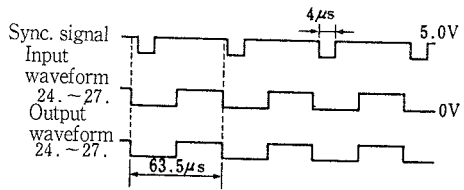
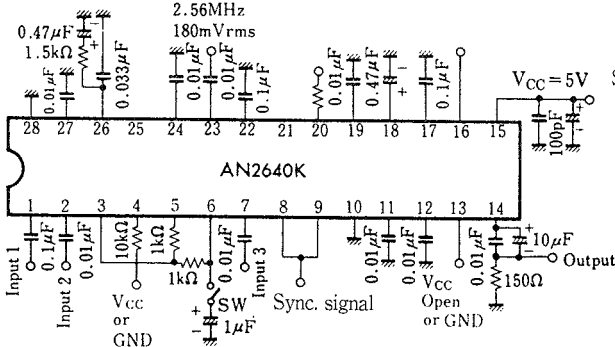
Test Circuit 3 (V_{APC})



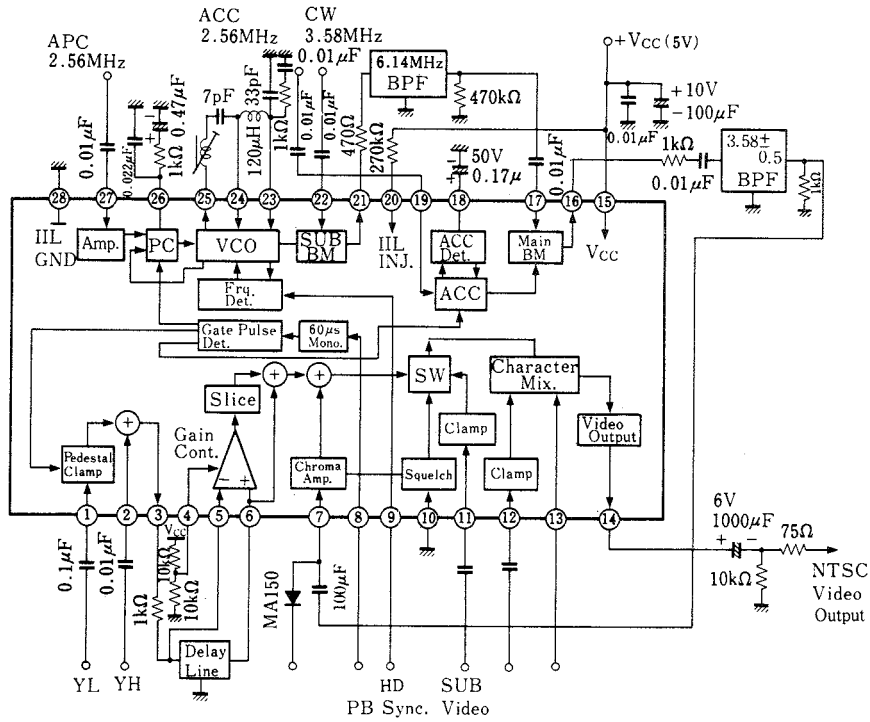
Test Circuit 4 (A_{FD1} , A_{FD2} , A_{SV} , A_W)



Test Circuit 5 (A_{YL} , A_{BL} , A_{AP1} , A_{AP2} , G_{YH} , G_{CH})



■ Application Circuit



■ Pin

| Pin No. | Pin Name | Pin No. | Pin Name |
|---------|--------------------------|---------|---------------------------------------|
| 1 | Y _L Input | 15 | Vcc |
| 2 | Y _H Input | 16 | Main Balanced Modulator Output |
| 3 | Y Output | 17 | Main Balanced Modulator Carrier Input |
| 4 | Aperture Gain Control | 18 | ACC Detector Output |
| 5 | Aperture Input | 19 | ACC Input |
| 6 | Y Input | 20 | IIL Injector |
| 7 | Chroma and Squelch Input | 21 | Sub Balanced Modulator Output |
| 8 | Playback Sync. Input | 22 | Sub Balanced Modulator Carrier Input |
| 9 | HD Pulse Input | 23 | VCO Input |
| 10 | GND | 24 | VCO Input |
| 11 | Sub Video Input | 25 | VCO Output |
| 12 | White Character Input | 26 | Loop Filter |
| 13 | Black Frame Input | 27 | APC Chroma Input |
| 14 | Video Output | 28 | GND |

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