IS61C1024H

128K x 8 HIGH-SPEED CMOS STATIC RAM

JANUARY 1996

FEATURES

- High-speed access time: 15, 20, 25 ns
- Low active power: 750 mW (typical)
- Low standby power: 2 mW (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply

DESCRIPTION

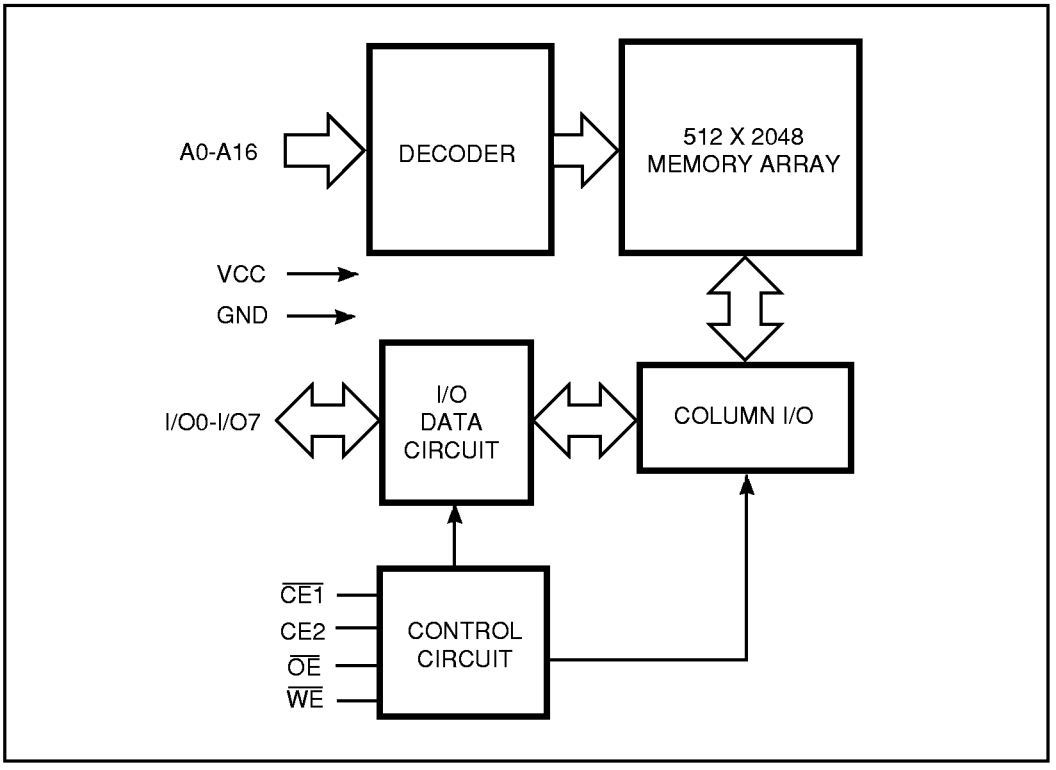
The *ISSI* IS61C1024H is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C1024H is available in 32-pin 300-mil and 400-mil plastic SOJ packages.

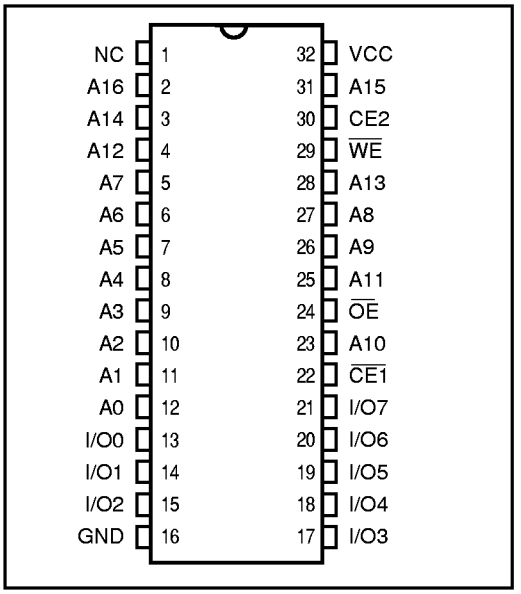
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

PIN CONFIGURATION
32-Pin SOJ



OPERATING RANGE

Range	Ambient Temperature	Vcc[1]
Commercial	0°C to +70°C	5V ± 10%

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–5	5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–5	5	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

			-15 ns		-20 ns		-25 ns		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	—	220	—	190	—	180	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL}, f = 0	—	60	—	60	—	60	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1}$ ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	—	50	—	50	—	50	mA

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	15	—	20	—	25	ns
t_{ACE2}	CE2 Access Time	—	15	—	20	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	7	—	9	—	9	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	6	0	7	0	10	ns
t_{LZCE1}[2]	$\overline{CE1}$ to Low-Z Output	2	—	3	—	3	—	ns
t_{LZCE2}[2]	CE2 to Low-Z Output	2	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE1}$ or CE2 to High-Z Output	0	8	0	9	0	10	ns
t_{PU}[3]	$\overline{CE1}$ or CE2 to Power-Up	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE1}$ or CE2 to Power-Down	—	12	—	18	—	20	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

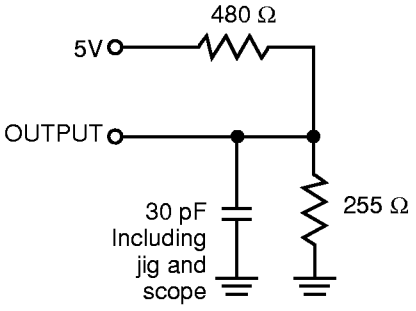


Figure 1a.

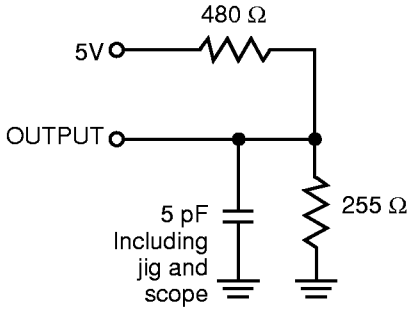
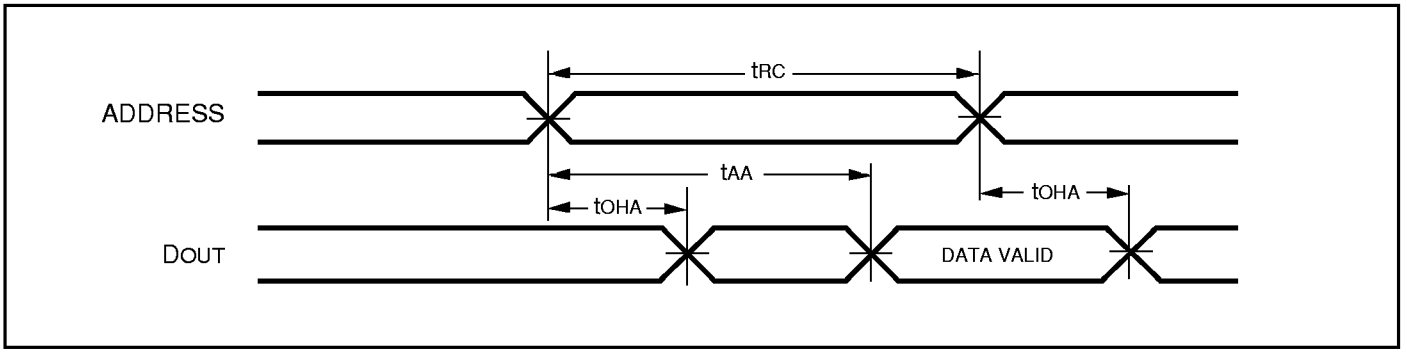


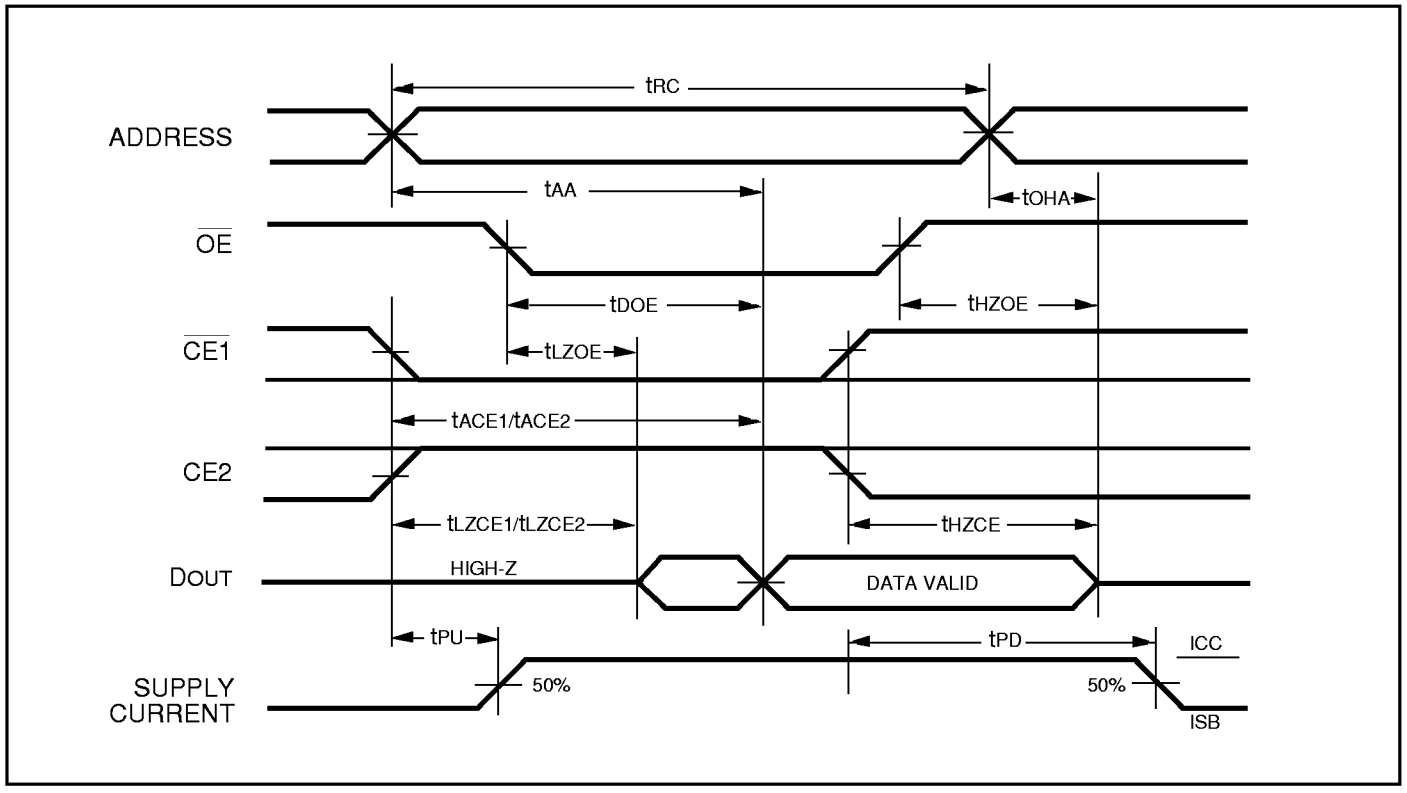
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

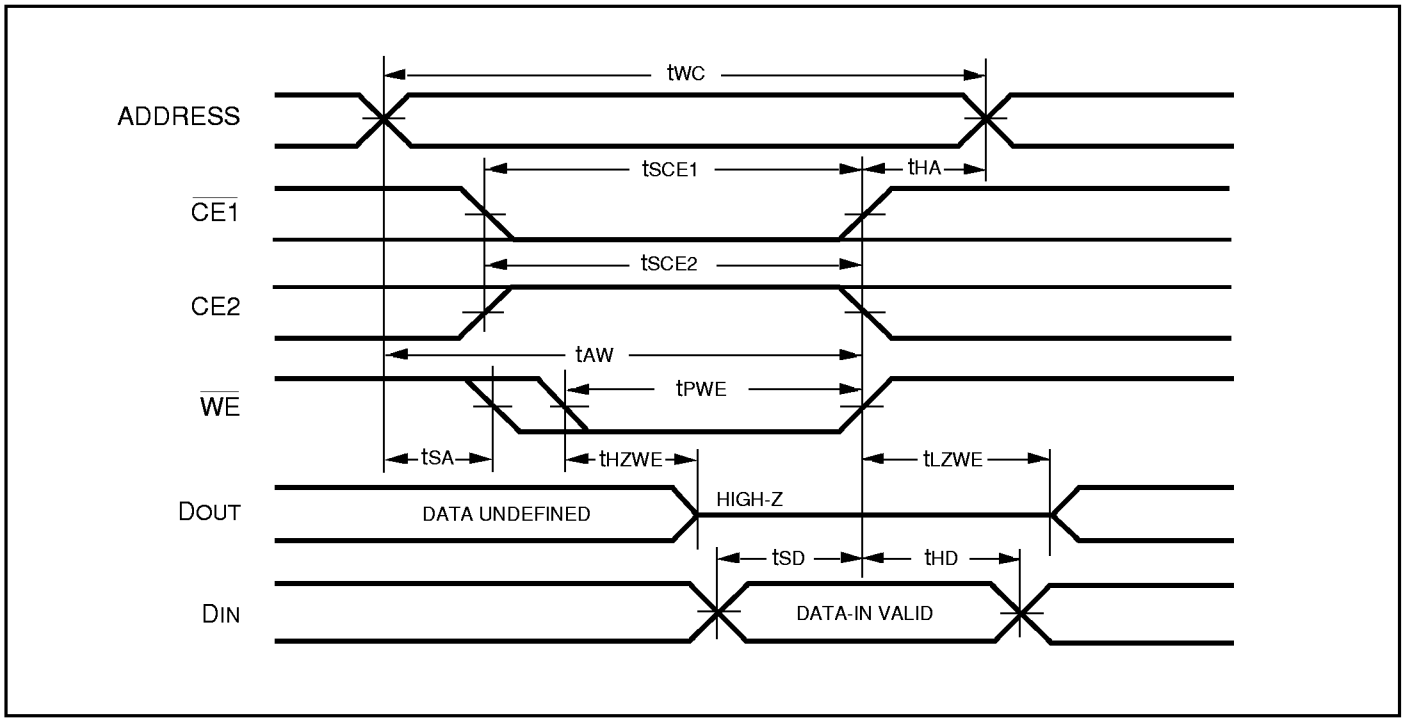
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	12	—	15	—	20	—	ns
t_{SCE2}	CE2 to Write End	12	—	15	—	20	—	ns
t_{AW}	Address Setup Time to Write End	12	—	15	—	20	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	10	—	12	—	15	—	ns
t_{SD}	Data Setup to Write End	8	—	10	—	12	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	7	—	10	—	12	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	ns

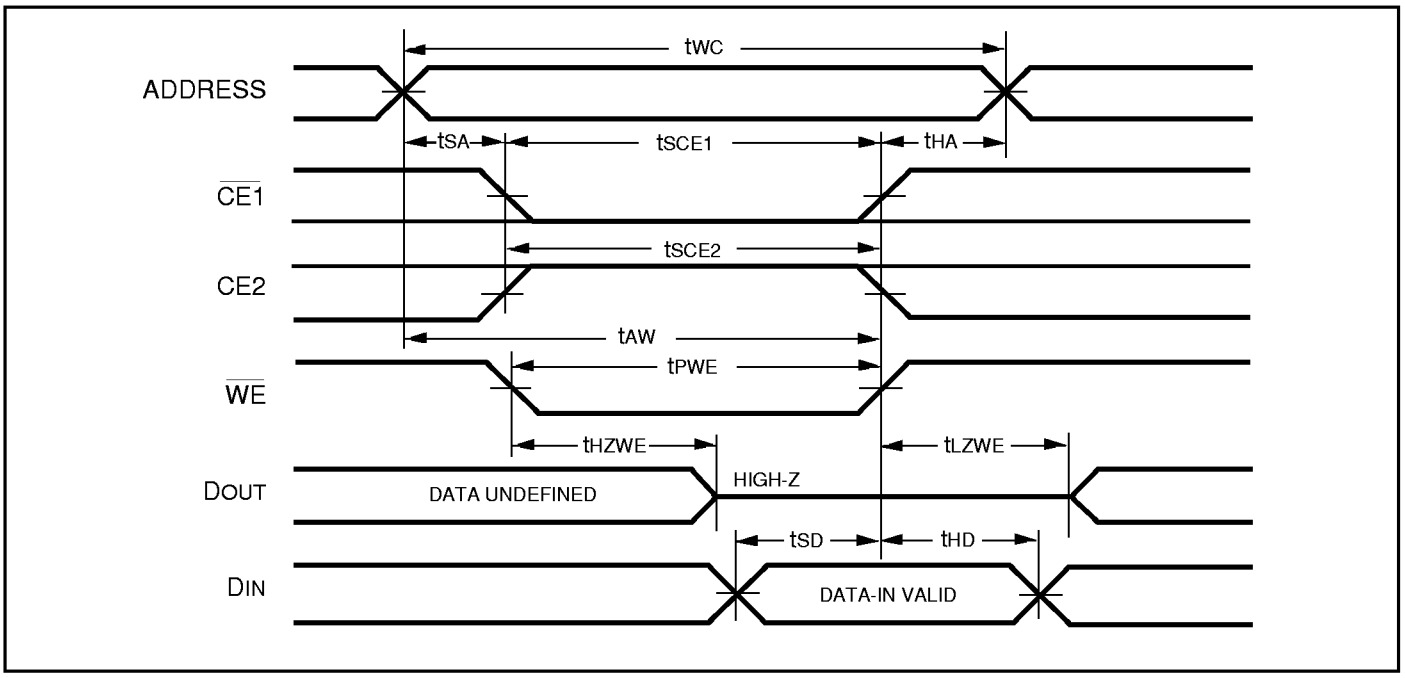
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)[1,2]



Notes:

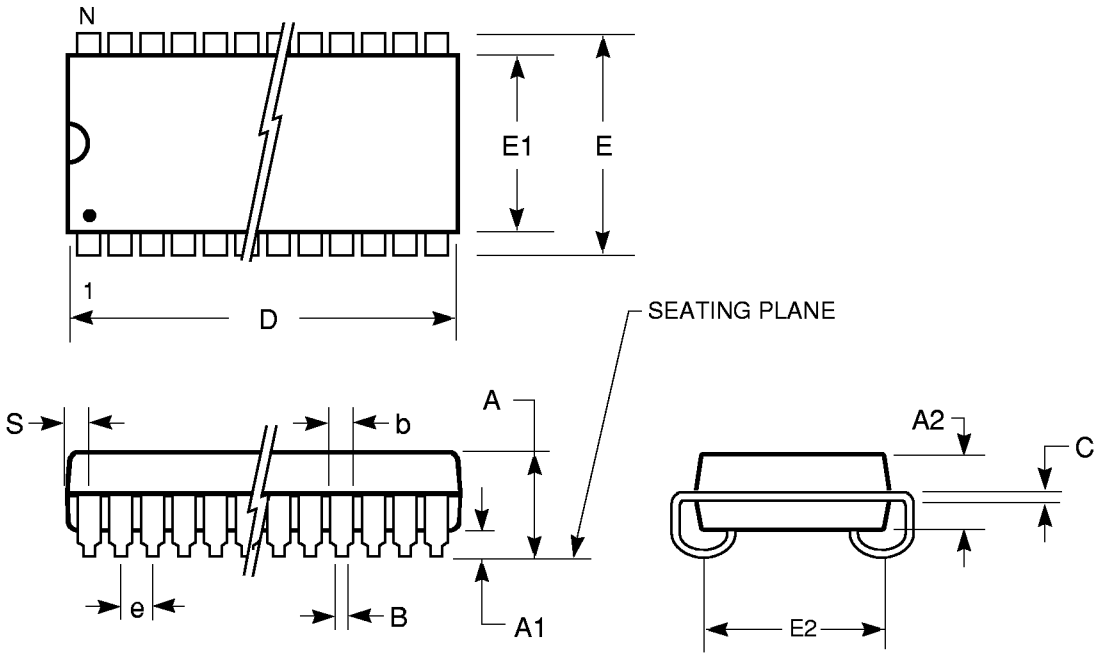
1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
15	IS61C1024H-15J	300-mil Plastic SOJ
15	IS61C1024H-15K	400-mil Plastic SOJ
20	IS61C1024H-20J	300-mil Plastic SOJ
20	IS61C1024H-20K	400-mil Plastic SOJ
25	IS61C1024H-25J	300-mil Plastic SOJ
25	IS61C1024H-25K	400-mil Plastic SOJ

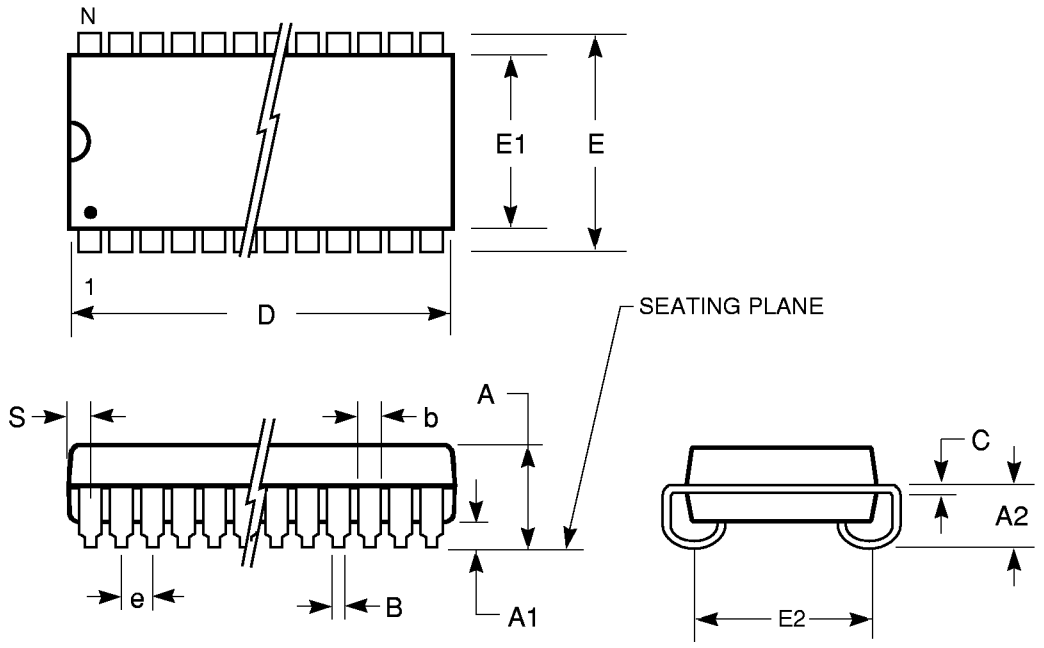
300-mil Plastic SOIC (J-Bend)
Package Code: J



300-mil Plastic SOIC (J-bend) (J)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	28		32	
A	0.128	0.140	—	0.140
A1	0.020	0.030	0.020	—
A2	0.095	0.105	0.095	0.105
B	0.016	0.022	0.016	0.022
b	0.026	0.032	0.026	0.032
C	0.008	0.014	0.008	0.014
D	0.700	0.730	0.815	0.835
E	0.321	0.347	0.325	0.345
E1	0.292	0.305	0.295	0.305
E2	0.245	0.285	0.247	0.287
e	0.050 BSC		0.050 BSC	
S	0.023	0.045	0.023	0.035

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

400-mil Plastic SOIC (J-Bend)
Package Code: K



400-mil Plastic SOIC (J-bend) (K)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	28		32	
A	0.128	0.148	0.131	0.145
A1	0.025	—	0.025	—
A2	0.082	—	0.082	—
B	0.016	0.020	0.013	0.021
b	0.026	0.032	0.024	0.032
C	0.007	0.0125	0.006	0.012
D	0.720	0.730	0.820	0.830
E	0.435	0.445	0.430	0.445
E1	0.395	0.405	0.395	0.405
E2	0.360	0.380	0.354	0.380
e	0.050 BSC		0.050 BSC	
S	—	0.035	—	0.045

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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