ANALOG DEVICES

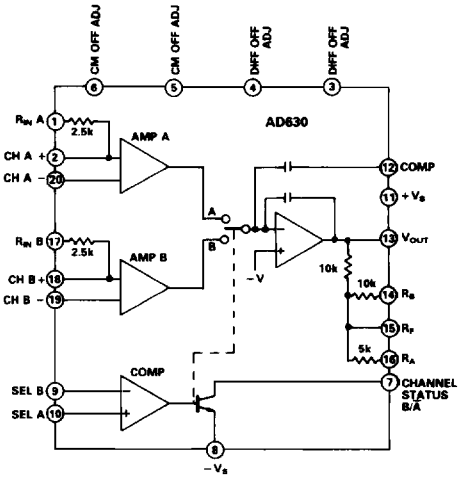
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth
Chips Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active. This device is now available to Standard Military Drawing (DESC) numbers 5962–8980701RA and 5962–89807012A.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

AD630—SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise noted)

Model	AD630J/A			AD630K/B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	μV
Input Offset Voltage										
T_{min} to T_{max}[2]			800			160			1000	μV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window										
T_{min} to T_{max}[2]			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[3]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/μs
Settling Time to 0.1% (20V step)		3			3			3		μs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ										
T_{min} to T_{max}[2]	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package	0		+70	0		+70		N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C

NOTES

[1]If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2]These parameters are guaranteed but not tested for J and K grades. For A, B and S grades they are tested.

[3]I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[4]Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/μs.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

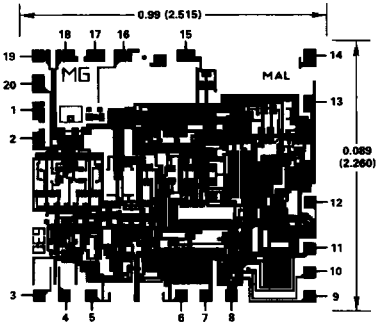
Supply Voltage	±18V
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature, Ceramic Package	−65°C to +150°C
Storage Temperature, Plastic Package	−55°C to +125°C
Lead Temperature, 10 sec. Soldering	+300°C
Max Junction Temperature	+150°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
20-Pin Plastic DIP (N)	24°C/W	61°C/W
20-Pin Ceramic DIP (D)	35°C/W	120°C/W
20-Pin Leadless Chip Carrier (E)	35°C/W	120°C/W

CHIP METALIZATION AND PINOUT

Dimensions shown in inches and (mm).
Contact factory for latest dimensions

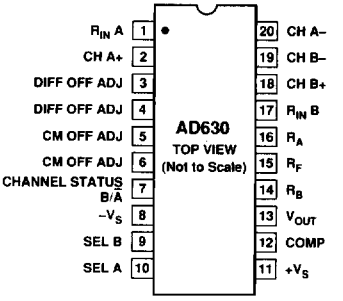


CHIP AVAILABILITY

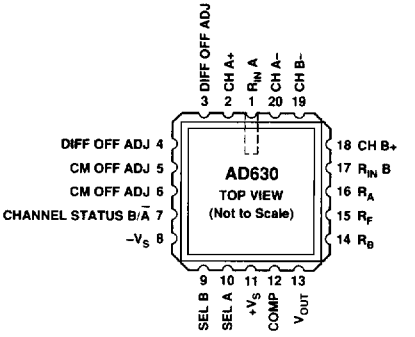
The AD630 is available in laser trimmed, passivated chip form. The figure shows the AD630 metalization pattern, bonding pads and dimensions. AD630 chips are available; consult factory for details.

PIN CONFIGURATIONS

20-Pin Plastic DIP (N-20)
20-Pin Side Brazed DIP (D-20)



20-Contact LCC (E-20A)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD630JN	0°C to +70°C	Plastic DIP	N-20
AD630KN	0°C to +70°C	Plastic DIP	N-20
AD630AD	−25°C to +85°C	Side Brazed DIP	D-20
AD630BD	−25°C to +85°C	Side Brazed DIP	D-20
AD630SD	−55°C to +125°C	Side Brazed DIP	D-20
AD630SD/883B	−55°C to +125°C	Side Brazed DIP	D-20
5962-8980701RA	−55°C to +125°C	Side Brazed DIP	D-20
AD630SE/883B	−55°C to +125°C	LCC	E-20A
5962-89807012A	−55°C to +125°C	LCC	E-20A
AD630J Chip	0°C to +70°C	Chip	
AD630S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

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