AMD

Am29F004B

4 Megabit (512 K x 8-Bit)
CMOS 5.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 Volt single power supply operation**
  - — Minimizes system-level power requirements
- **High performance**
  - — Access times as fast as 55 ns
- **Manufactured on 0.32 µm process technology**
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby mode current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
  - — Supports full chip erase
  - — Sector Protection features:
  - — A hardware method of locking a sector to prevent any program or erase operations within that sector
  - — Sectors can be locked in-system or via programming equipment
  - — Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- *Minimum 1,000,000 write cycle guarantee per sector*
- **Package options**
  - — 32-pin PDIP
  - — 32-pin PLCC
- **Compatibile with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **20-year data retention at 125°C**

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GENERAL DESCRIPTION

The Am29F004B consists of 4 Mbit, 5.0 volt-only Flash memory devices organized as 524,288 bytes. The data appears on DQ0–DQ7. The device is offered in 32-pin PLCC and 32-pin PDIP packages. This device is designed to be programmed in-system with the standard system 5.0 volt VCC supply. A 12.0 volt VPP is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 55, 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29F004B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm-an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm–an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector** protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers a **standby mode** as a power-saving feature. Once the system places the device into the standby mode power consumption is greatly reduced.

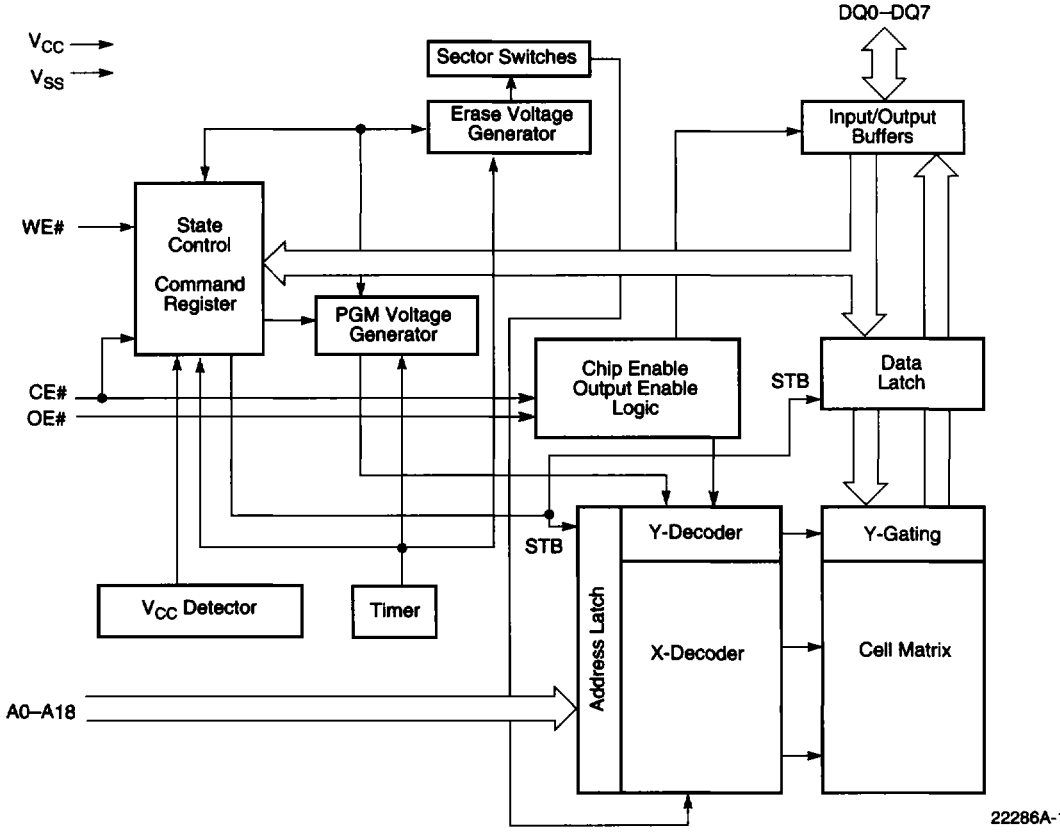
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

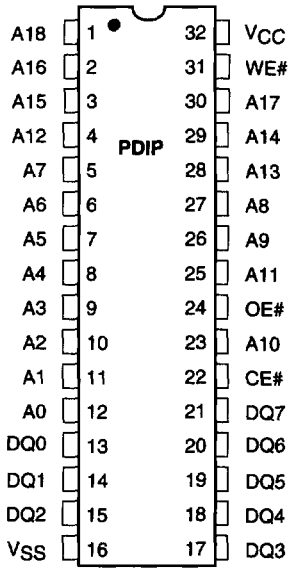
Family Part Number		Am29F004B			
Speed Option	V_{CC} = 5.0 V ± 5%	-55			
	V_{CC} = 5.0 V ± 10%		-70	-90	-120
Max access time, ns (t_{ACC})		55	70	90	120
Max CE# access time, ns (t_{CE})		55	70	90	120
Max OE# access time, ns (t_{OE})		30	30	35	50

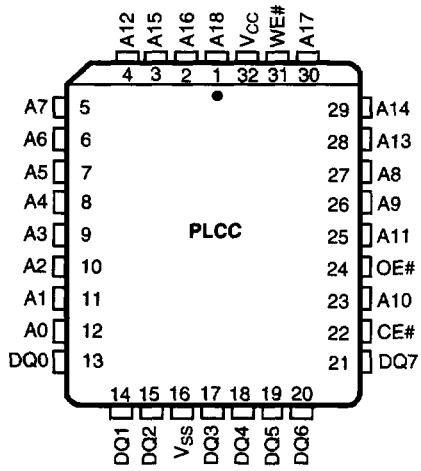
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS





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PIN CONFIGURATION

A0–A18 = 19 addresses

DQ0–DQ7 = 8 data inputs/outputs

CE# = Chip enable

OE# = Output enable

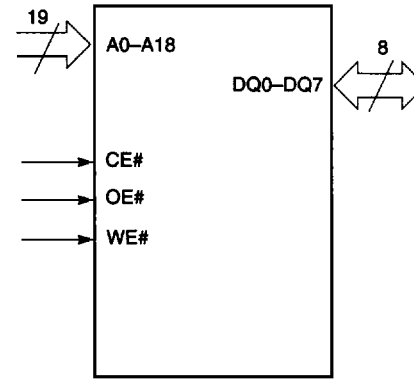
WE# = Write enable

V_{CC} = +5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)

V_{SS} = Device ground

NC = Pin not connected internally

LOGIC SYMBOL



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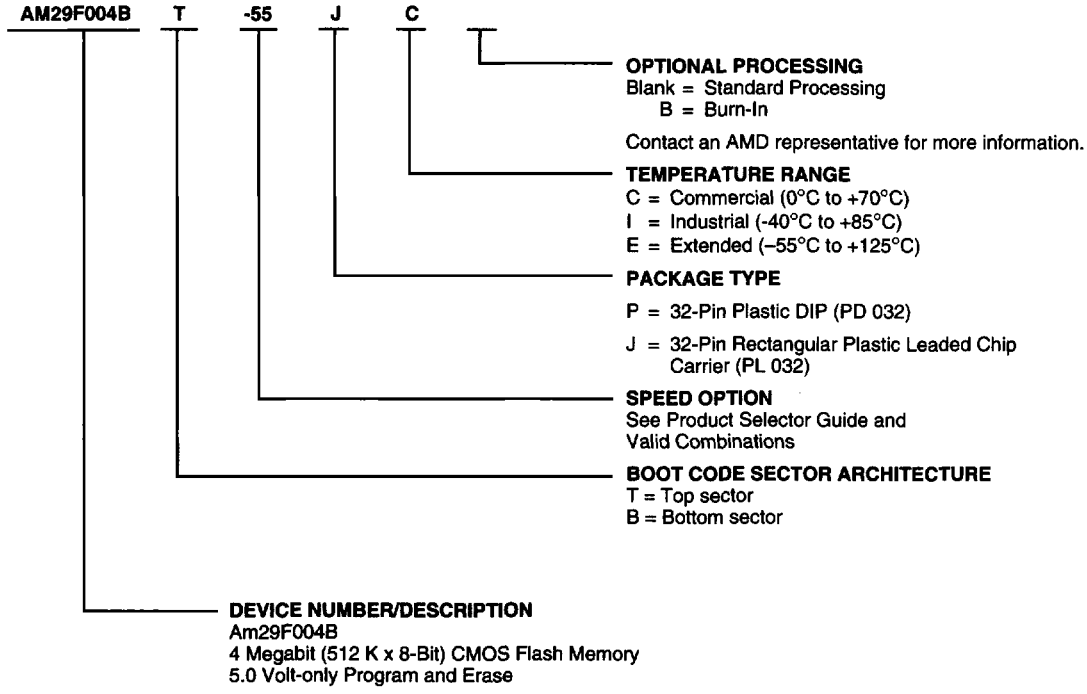
ORDERING INFORMATION

Standard Product

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29F004BT-55 AM29F004BB-55 AM29F004BT-70 AM29F004BB-70	PC, PI, JC, JI
AM29F004BT-90 AM29F004BB-90	PC, PI, PE, JC, JI, JE
AM29F004BT-120 AM29F004BB-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.