National Semiconductor

ADVANCE INFORMATION
March 1994

NM28F010
1-Mbit (131,072-Word x 8-Bit) CMOS FLASH

General Description

The NM28F010 is a 1,048,576-bit FLASH Electrically Erasable and Programmable non-volatile Memory device. The NM28F010 stores data reliably even after 10,000 program and erase cycles. The NM28F010 features single command control for read, chip erase, and programming operations to allow ease of use for on-board programming.

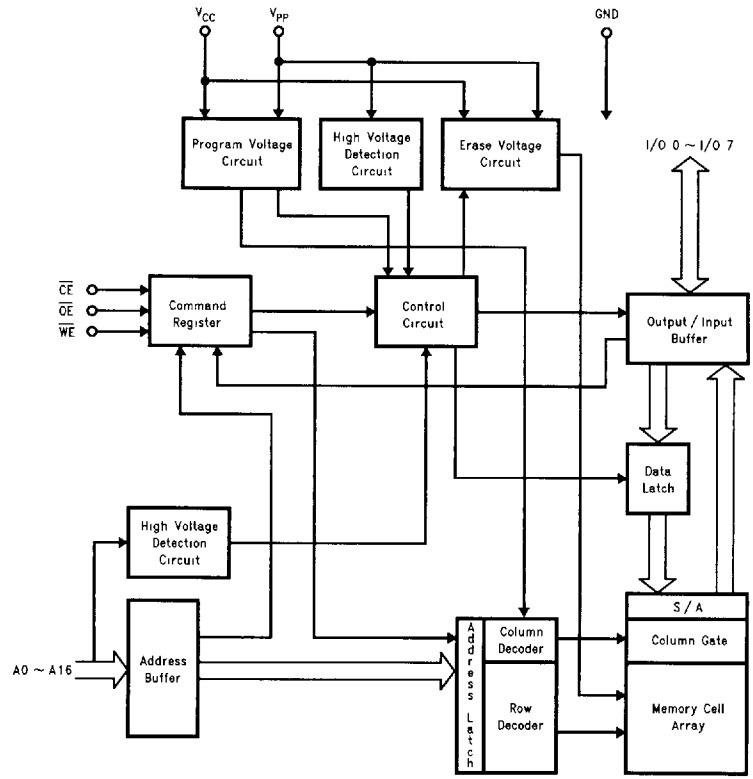
The NM28F010 is ideally suited for applications such as firmware storage, BIOS, engine control, and wireless communication—where EPROM has been used in the past.

The NM28F010 is available in either a 32-pin plastic DIP, SOP, PLCC, or forward and reverse bend TSOP packages to suit a variety of applications.

Features

- Power supply: V_{PP} = 12V ±0.6V
  V_{CC} = 5V ±0.25V
- Mode: Read/Reset
  Program (byte)
  Chip Erase
- Mode Control: command input
- Program: 10 μs typical per byte
  (loops = 10 μs x 25 max.)
- Erase: 1 sec typical per chip
  (loops = 10 ms x 1,000 max.)
- W/E Cycles: 10,000 cycles minimum target
- Access Time: 100 ns/120 ns
- Power Dissipation: Operating = 30 mA
  Standby = 100 μA
- Packages available: 32-pin DIP, SOP, TSOP, TRSOP, PLCC
- Pin compatible with NM27C010 EPROM

Functional Diagram

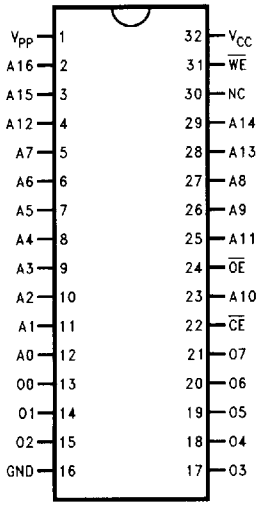


TL/D/11872-4

 TL/D/11872 6501126 0069931 638 RRD-B20M34/Printed in U S A

Connection Diagrams

Dual-In-Line Package (N)
Small Outline Package (M)



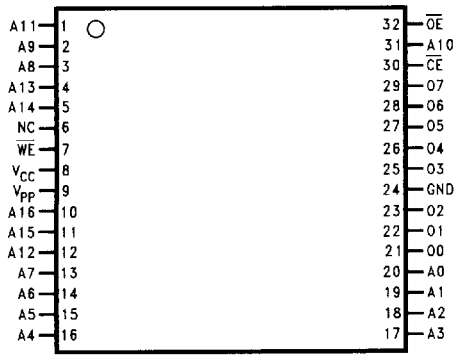
TL/D/11872-1

Top View

Pin Names

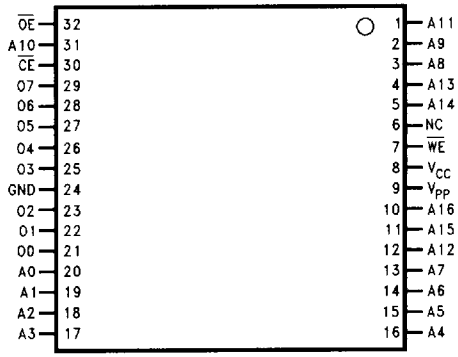
A0–16	Address Input
O0–07	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
NC	Non Connection
V_{PP}	Program/Erase Supply
V_{CC}	Supply (5V)
GND	Ground

TSOP Package (T)



TL/D/11872-2

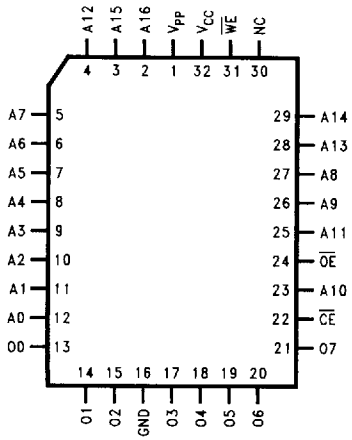
Reversed TSOP Package (TR)



TL/D/11872-3

Connection Diagrams (Continued)

PLCC Package (V)



TL/D/11872–16

Ordering Information

COMMERCIAL TEMPERATURE RANGE
(0°C to +70°C) V_{CC} = 5.0V ±5%

Parameter/Order Number	Access Time (ns)
NM28F010 N, M, V, T, TR 10	100
NM28F010 N, M, V, T, TR 12	120
NM28F010 N, M, V, T, TR 15	150

NM 28F 010 T 10

National Memory
NOR FLASH

Access Time
10 = 100 ns
12 = 120 ns
15 = 150 ns

Package Type
N = PDIP
M = SOP
V = PLCC
T = TSOP
TR = Reversed TSOP

Density
010 = 1 Mbit
040 = 4 Mbit

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.6V− +7.0V
Program/Erase Supply Voltage (V_{PP})	−0.6V− +14.0V
Input Voltoge (V_{IN})	−0.6V− +7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V− +7.0V
Power Dissipation (P_D)	1.0W
Soldering Temperature Time (T_{SOLDER})	260°C/sec.−10°C/sec.
Storage Temperature (T_{STG})	−55°C− +150°C
Operating Temperature (T_{OPR})	0°C− +70°C
Erase/Program Cycling Capability (N_{EW})	10,000 Cycles
Input Voltage (A9) (V_{ID})	−0.6V− +13.5V

AC Electrical Characteristics

READ OPERATION T_A = 0°C− +70°C, V_{CC} = 5V ±5%, V_{PP} = 0V−V_{CC} or 12.0V ±5%

Symbol	Parameter	100			120			Units
		Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	100			120			ns
t_{ACC}	Address Access Time			100			120	
t_{CE}	$\overline{CE}$ Access Time			100			120	
t_{OE}	$\overline{OE}$ Access Time			40			50	
t_{CEE}	$\overline{CE}$ to Output Low Z	0			0			
t_{OEE}	$\overline{OE}$ to Output Low Z	0			0			
t_{OH}	Output Data Hold Time	0			0			
t_{DF1}	$\overline{CE}$ to Output High Z			30			30	
t_{DF2}	$\overline{OE}$ to Output High Z			30			30	

AC Test Condition

- Output Load: 1 TTL Gate and C_L = 100 pF
- Input Pulse Rise and Fall Time (10% ~ 90%): 5 ns Max.
- Input Pulse Level: 0.6V/2.4V
- Timing Measurement Reference Level: Input 0.8V/2.0V, Output 0.8V/2.0V

AC Electrical Characteristics (Continued)

COMMAND CONTROL OPERATION $T_A = 0°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 12.0V \pm 5\%$

Symbol	Parameter	100			120			Units
		Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Setup Time	0			0			ns
t_{AH}	Address Hold Time	50			60			
t_{CES}	$\overline{CE}$ Setup Time ($\overline{WE}$ Control)	0			0			
t_{CEH}	$\overline{CE}$ Hold Time ($\overline{WE}$ Control)	0			0			
t_{OES}	$\overline{OE}$ Setup Time	0			0			
t_{OEH}	$\overline{OE}$ Hold Time	0			0			
t_{WES}	$\overline{WE}$ Setup Time ($\overline{CE}$ Control)	0			0			
t_{WEH}	$\overline{WE}$ Hold Time ($\overline{CE}$ Control)	0			0			
t_{DS}	Data Setup Time	40			50			
t_{DH}	Data Hold Time	0			0			
t_{WELH}	$\overline{WE}$ Low Level Hold Time	50			60			
t_{WEHH}	$\overline{WE}$ High Level Hold Time	20			20			
t_{CEHL}	$\overline{CE}$ Low Level Hold Time	50			60			
t_{CEHH}	$\overline{CE}$ High Level Hold Time	20			20			
t_{CMC}	Command Cycle Time	100			120			
t_{PH}	Program Hold Time	9	10		9	10		μs
t_{PRV}	Program Recovery Time	6			6			
t_{EH}	Erase Hold Time	9	10		9	10		ms
t_{ERV}	Erase Recovery Time	6			6			μs
t_{ACC}	Address Access Time			100			120	ns
t_{CE}	$\overline{CE}$ Access Time			100			100	
t_{OE}	$\overline{OE}$ Access Time			40			50	
t_{CEE}	$\overline{CE}$ to Output Low Z	0		40	0		50	
t_{OEE}	$\overline{OE}$ to Output Low Z	0			0			
t_{OH}	Output Data Hold Time	0			0			
t_{DF1}	$\overline{CE}$ to Output High Z			30			30	
t_{DF2}	$\overline{OE}$ to Output High Z			30			30	
t_{VC}	Verify Cycle Time	100			120			
t_{RC}	Read Cycle Time	100			120			

DC Electrical Characteristics $T_A = 0°C \sim +70°C, V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	μA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		−0.5	0.8	
V_{OH}	Output High Voltage	$I_{OH} = -0.40$ mA	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = +2.10$ mA		0.4	
I_{CC01}	V_{CC} Read Average Current (Read/Signature Read)	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{cycle} = t_{RC}$ (min) cycle		30	mA
I_{CC02}	V_{CC} Programming Average Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{cycle} = 9\ \mu s$		10	
I_{CC03}	V_{CC} Erase Average Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA		15	
I_{CC04}	V_{CC} Program Verify Average Current	$V_{IN} = V_{IN}/V_{IL}$, $I_{OUT} = 0$ mA		15	
I_{CC05}	V_{CC} Erase Verify Average Current	$V_{IN} = V_{IN}/V_{IL}$, $I_{OUT} = 0$ mA		15	
I_{CCS1}	V_{CC} Standby Current (Read)	$\overline{CE} = V_{IH}$		1	
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$		100	μA
I_{PPS}	V_{PP} Standby Current	$0V \le V_{PP} \le 6.5V$		±10	
		$11.4V \le V_{PP} \le 12.6V$		200	
I_{PP1}	V_{PP} Read Average Current	$0V \le V_{PP} \le 6.5V$, $V_{IN} = V_{IH}/V_{IL}$		±10	
		$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		200	
I_{PP2}	V_{PP} Programming Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		30	mA
I_{PP3}	V_{PP} Erase Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		30	
I_{PP4}	V_{PP} Program Verify Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		1	
I_{PP5}	V_{PP} Erase Verify Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		1	
I_{ID}	A9 Pin High Voltage Input Current	$11.4V \le V_{ID} \le 12.6V$		200	μA

Capacitance* $T_A = 25°C, f = 1$ MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		10	12	pF

*This parameter is periodically sampled and is not 100% tested.

DC and Operating Characteristics $T_A = 0°C - +70°C$

Symbol	Parameter	Min	Max	Units
V_{CC}	V_{CC} Supply Voltage	4.75	5.25	V
V_{ID}	A9 Input High Voltage (during ID Read)	11.4	12.6	
V_{PPL}	V_{PP} Supply Voltage (during Read Operation)	0	6.5	
V_{PPH}	V_{PP} Supply Voltage (during Erase/Program Operations)	11.4	12.6	

Mode Selection

Mode		Pin							
		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Address	I/O	V_{CC}	V_{PP}	Power
Read	Read	L	H	L	Read Address	Data Output	5V	0 ~ V_{CC} or 12V	Active
	Output Diselect	L	*	H	*	High Impedance			
	Standby	H	*	*	*				Standby
Command Input	$\overline{WE}$ Control	L	⊓	H	(Note 1)	Command Data	5V	12V	Active
	$\overline{CE}$ Control	⊓	L	H	(Note 1)				
Program/Erase		*	H	H	*				
Program/Erase Verify		L	H	L	(Note 1)	Data Output			
ID Read		L	H	L	"0"/"1"	Code Output			

Note 1: Shown as Command Definition Table and Operation Timing Chart

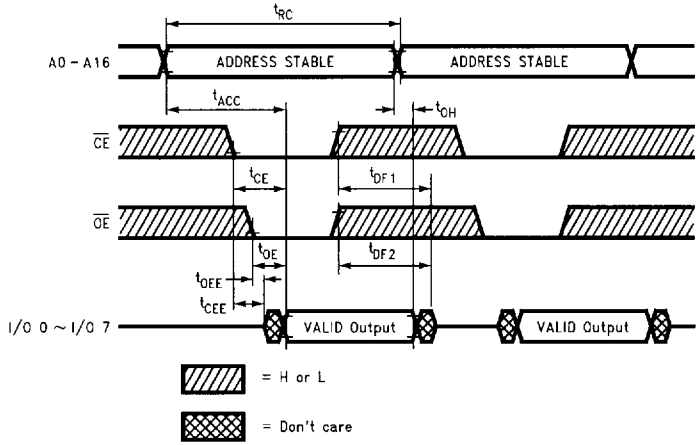
*H or L

Command Definition Table

Function	Bus Cycle	1st Bus Cycle			2nd Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H			
ID Read	2	WRITE	*	90H	READ	0000/1H	Mfg/Dev ID
Chip Erase	2	WRITE	*	20H	WRITE	*	20H
Erase Verify	2	WRITE	Byte Address	A0H	READ	*	EV Data
Program Setup/Begin	2	WRITE	*	40H	WRITE	Byte Address	WR Data
Program Verify	2	WRITE	Byte Address	C0H	READ	*	WV Data
Reset	2	WRITE	*	FFH	WRITE	*	FFH

*H or L

Waveform for Read Operations



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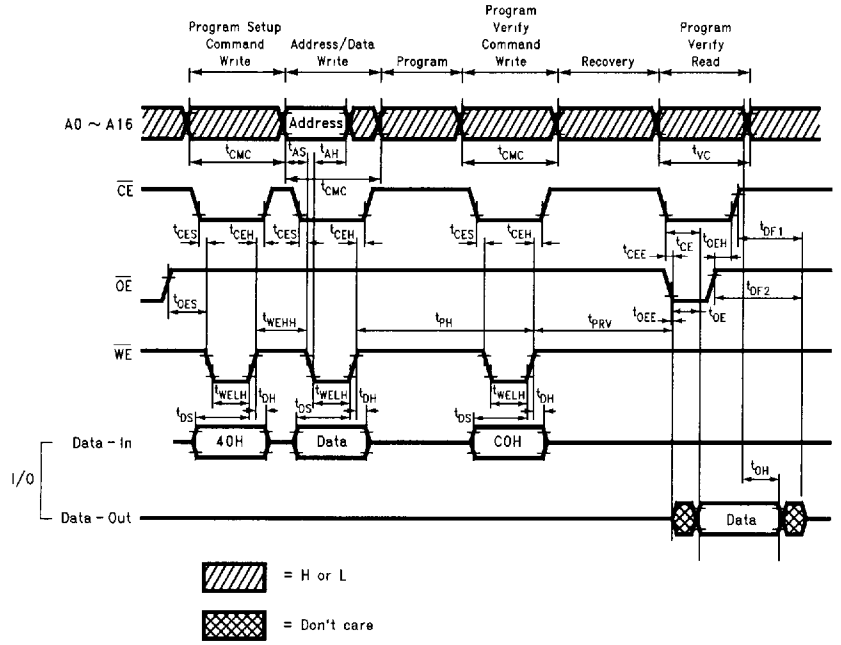
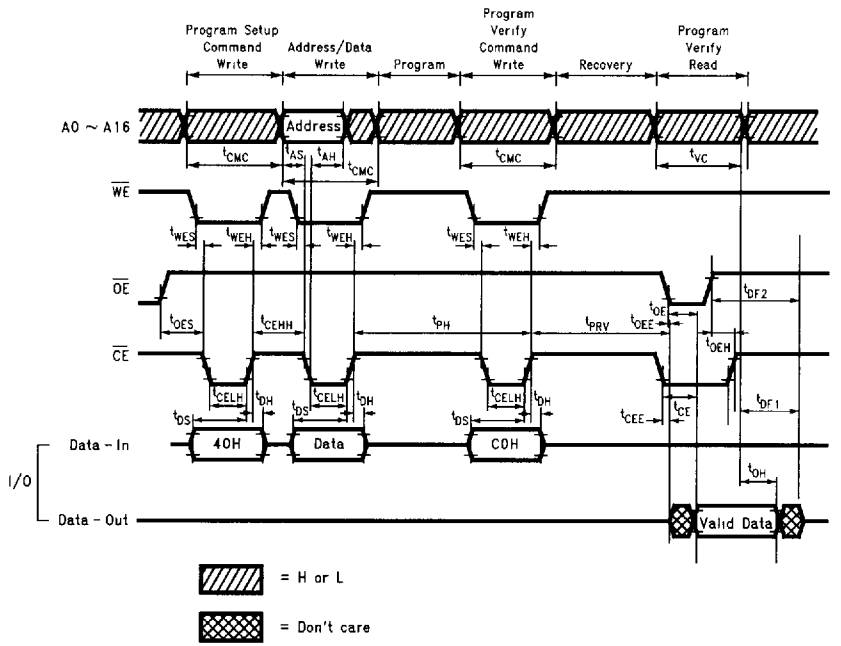
Program Operation Timing Chart

• $\overline{WE}$ Control



TL/D/11872–6

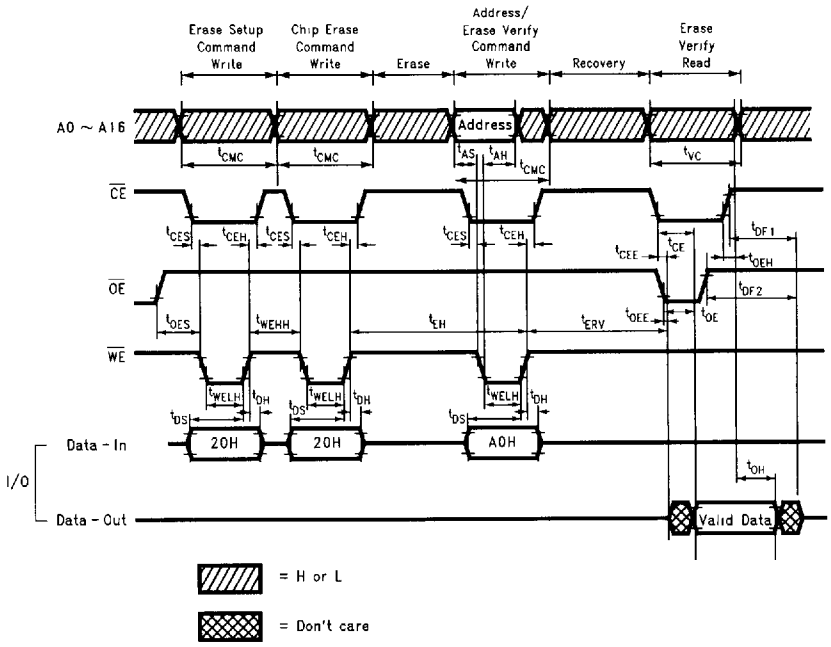
• $\overline{CE}$ Control



TL/D/11872–7

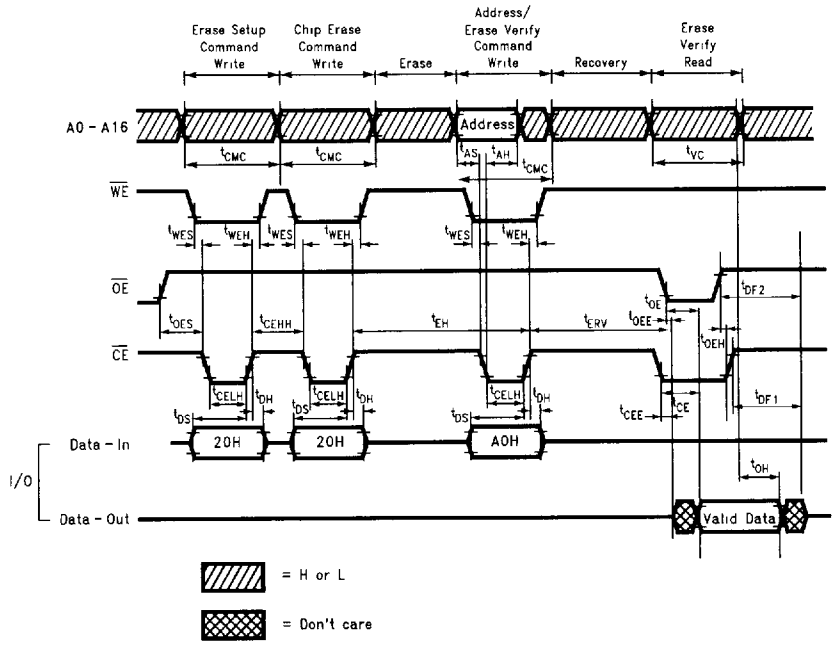
Chip Erase Operation Timing Chart

• $\overline{WE}$ Control



TL/D/11872-8

• $\overline{CE}$ Control



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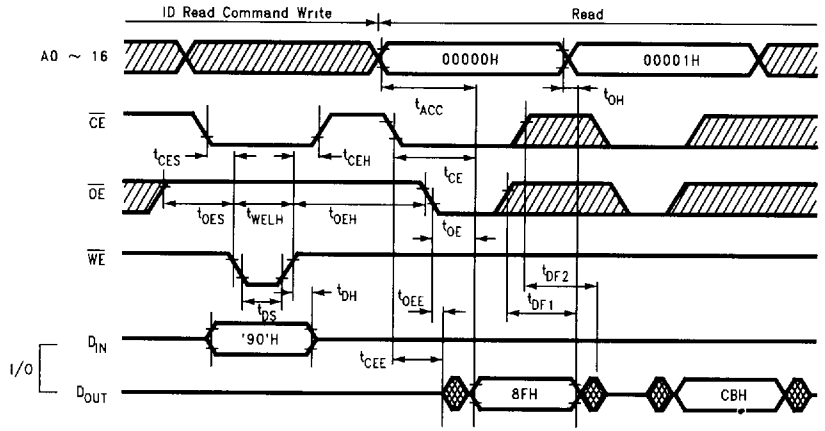
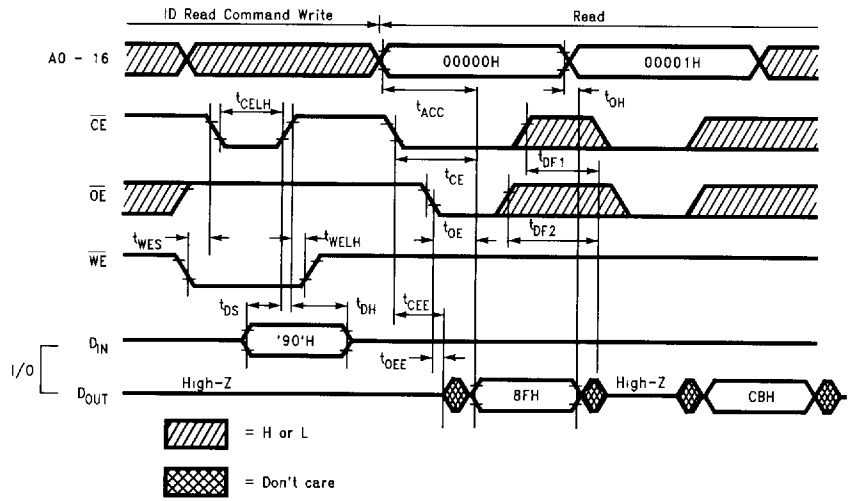
ID Read Operation Timing Chart

• $\overline{WE}$ Control



TL/D/11872–10

• $\overline{CE}$ Control



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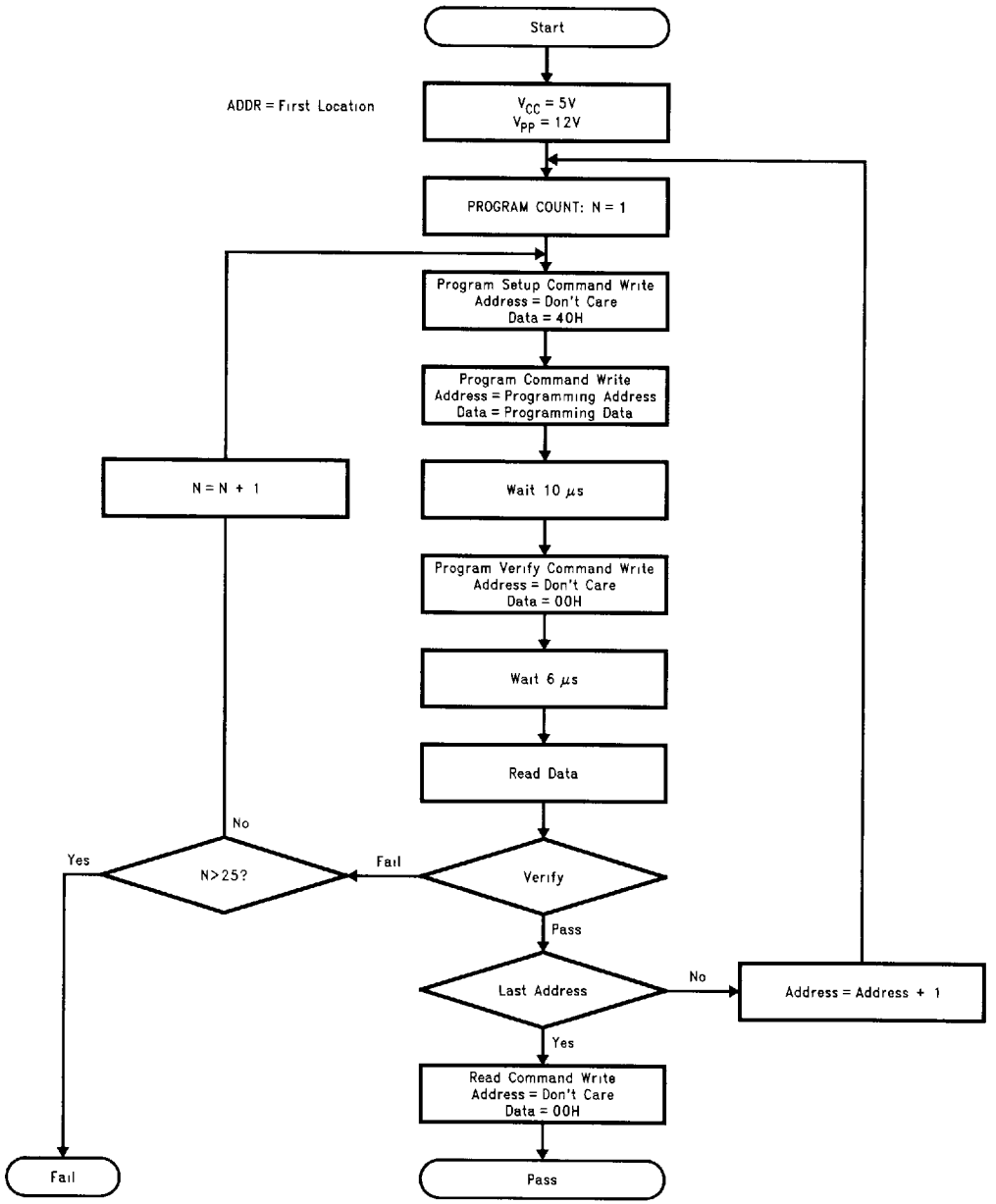
Programming Flow Chart



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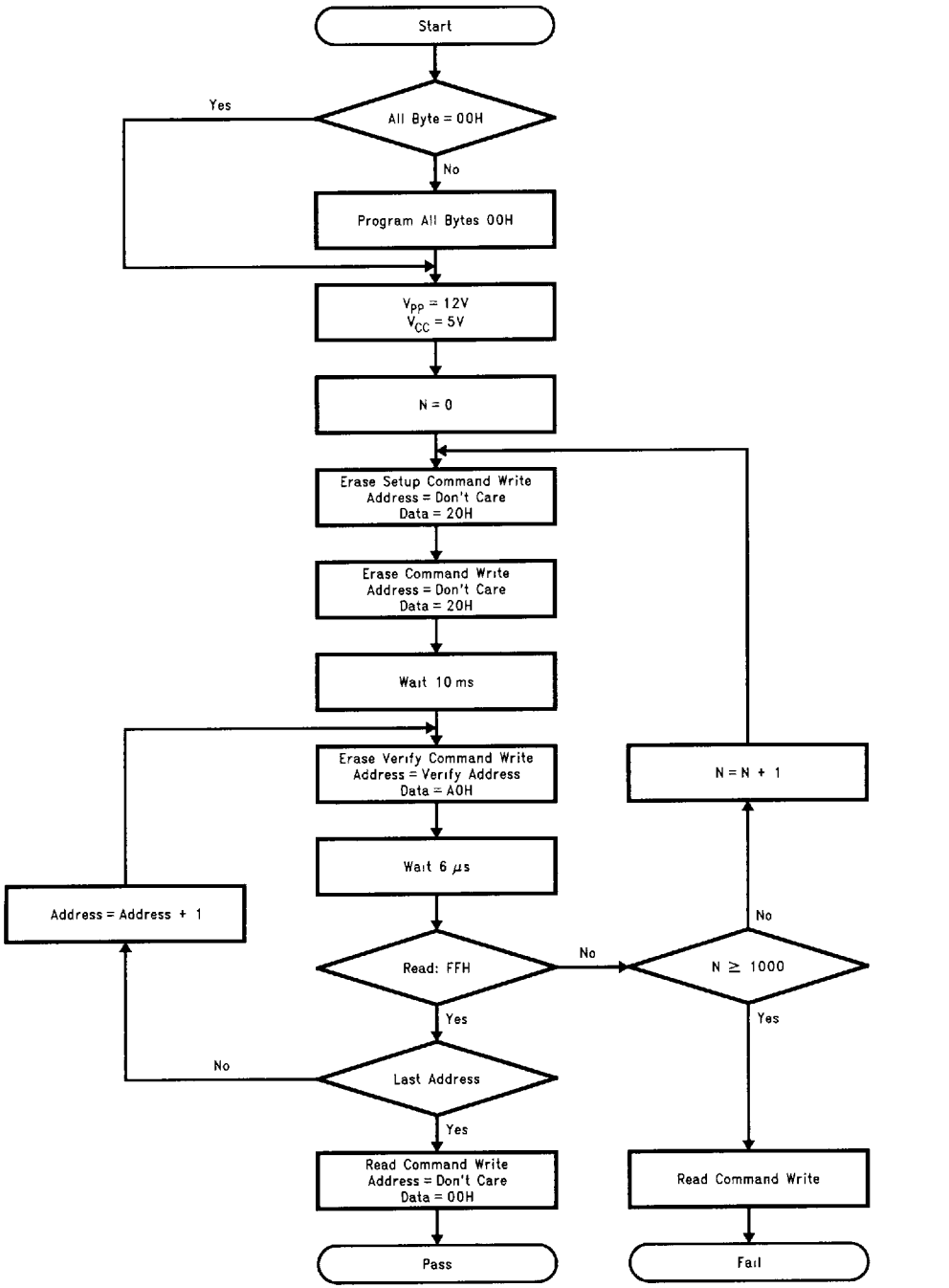
Chip Erase Flow Chart



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Operating Mode

The NM28F010 features seven modes of operation: Read, ID Read, Program, Program-Verify, Chip Erase, Erase-Verify, and Reset. Each mode is selected by a command input through the I/O pins.

READ MODE

When the device is set to read mode, it acts as an asynchronous ROM with the access time of 100 ns/120 ns. The device enters read mode regardless of a read command input in the case of $V_{PP} = 0 \sim V_{CC}$. The read command (00H) is required to set the read mode in the case of V_{PP} = 12V. The device is automatically set to read mode after V_{PP} transitions from $0 \sim V_{CC}$ to 12V.

ID READ MODE

The ID read mode is utilized for recognizing the device type. The ID read mode is set by a "90H" command input with V_{PP} = 12V. The "0" address data indicates the manufacturer code (8FH) while "1" address data indicates the device code (CBH). The access time of the ID read is the same as a normal read operation. The ID mode can also be set by applying V_{IH} to the A9 pin at $V_{CC} = 0 \sim V_{CC}$. The manufacturer code is read out at A10–16 = V_{IL} and A0–8 = 000H while the device code is read out at A10–16 = V_{IL} and A0–8 = 001H.

PROGRAM MODE

The program mode is set by entering a "40H" command input at V_{PP} = 12V. The next bus cycle will latch the input data and program address. The program operation is enabled at the end of this second bus cycle. The program operation can be terminated by either entering a program-verify command (C0H) or the reset command (FFH).

PROGRAM-VERIFY MODE

The program-verify mode is used to verify that the data was successfully programmed into the device. The program-verify mode is set by a "C0H" command input during the program operation. The programmed data is read out at the next bus cycle.

CHIP ERASE MODE

The chip erase mode is set by a "20H" command input. The device executes the erase operation by a succeeding "20H" command input at the next cycle. This second latch cycle is needed to prevent accidental erasure of data due to external noise. The chip erase operation is terminated by either the erase-verify command (A0H) or the reset command (FFH).

ERASE-VERIFY MODE

The erase-verify mode is used to verify that the data was successfully erased from the device. The erase-verify mode is set by a "A0H" command input. The data at the address specified, during the command input cycle, is read out at the next bus cycle.

RESET MODE

The reset mode is used to abort a program or erase operation and return the device to a known state. The reset operation is activated after two successive "FFH" command inputs. The device returns to the read mode after 6 μs of recovery time.

Program, Erase Operation

PROGRAM OPERATION

The program operation is executed by entering two successive command input cycles. The first cycle is used to input a "40H" command and the second cycle to enter the program address and data. The program operation starts from the rising edge of $\overline{WE}$ at the end of the second cycle and finishes with the rising edge of $\overline{WE}$ during the program-verify command input cycle. Although this time period needs to be externally controlled to be within the 10 μs requirement, the program operation is stopped by an internal timer, 10 μs after the program operation starts. The device then enables to acquire the next program-verify command. The program address is acquired at the falling edge of $\overline{WE}$ and data is acquired at the rising edge of $\overline{WE}$ in the second bus cycle. The program-verify operation can be executed 6 μs after the rising edge of $\overline{WE}$ in the program-verify command cycle. The program operation completes when the output data from program-verify coincides with the input data. The program loop can be implemented a maximum of 25 times until coincidence. (Refer to the program operation flow chart.)

CHIP ERASE OPERATION

The device must be pre-programmed to set all bits to "0" before a chip erase operation can be performed.

The chip erase operation is executed by two succeeding input command cycles of "20H". The operation starts from the rising edge of $\overline{WE}$ after the second erase command input and finishes at the rising edge of $\overline{WE}$ in the erase-verify command (A0H) cycle.

Although this time period needs to be externally controlled to be within the 10 ms requirement, the erase operation is stopped by internal timer 10 ms after the program operation starts. The device then enables to acquire the next erase-verify command. The erase-verify operation can be executed 6 μs after the rising edge of $\overline{WE}$ in the erase-verify command cycle. The address of the data to be verified is latched at the falling edge of $\overline{WE}$ and the verify command is latched at the rising edge of $\overline{WE}$ in the erase-verify cycle. If the verified output data is "FFH", the address is incremented until the last address. If the data is not "FFH", the erase operation is reexecuted until success or up to 1000 times maximum. (Refer to chip erase flow chart).

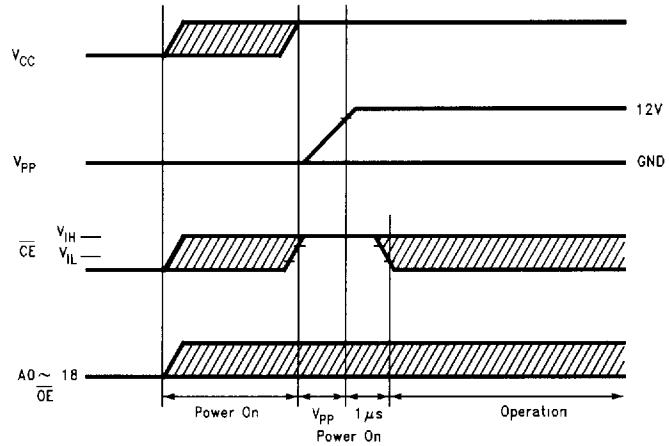
Power On/Off Sequence

The following sequences are needed to protect against data corruption during power on and off conditions:

POWER ON: V_{PP} must be applied only after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high.

POWER OFF: V_{PP} must be turned off after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high. V_{CC} can only be turned off after V_{PP} has reached 0V.

(1) Supply Power on Sequence



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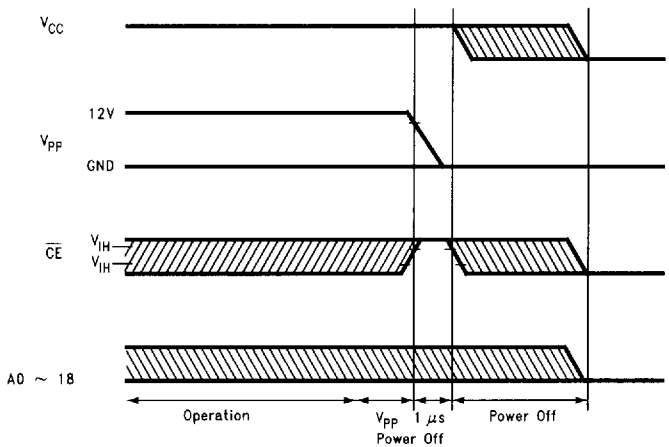
(2) Supply Power down Sequence



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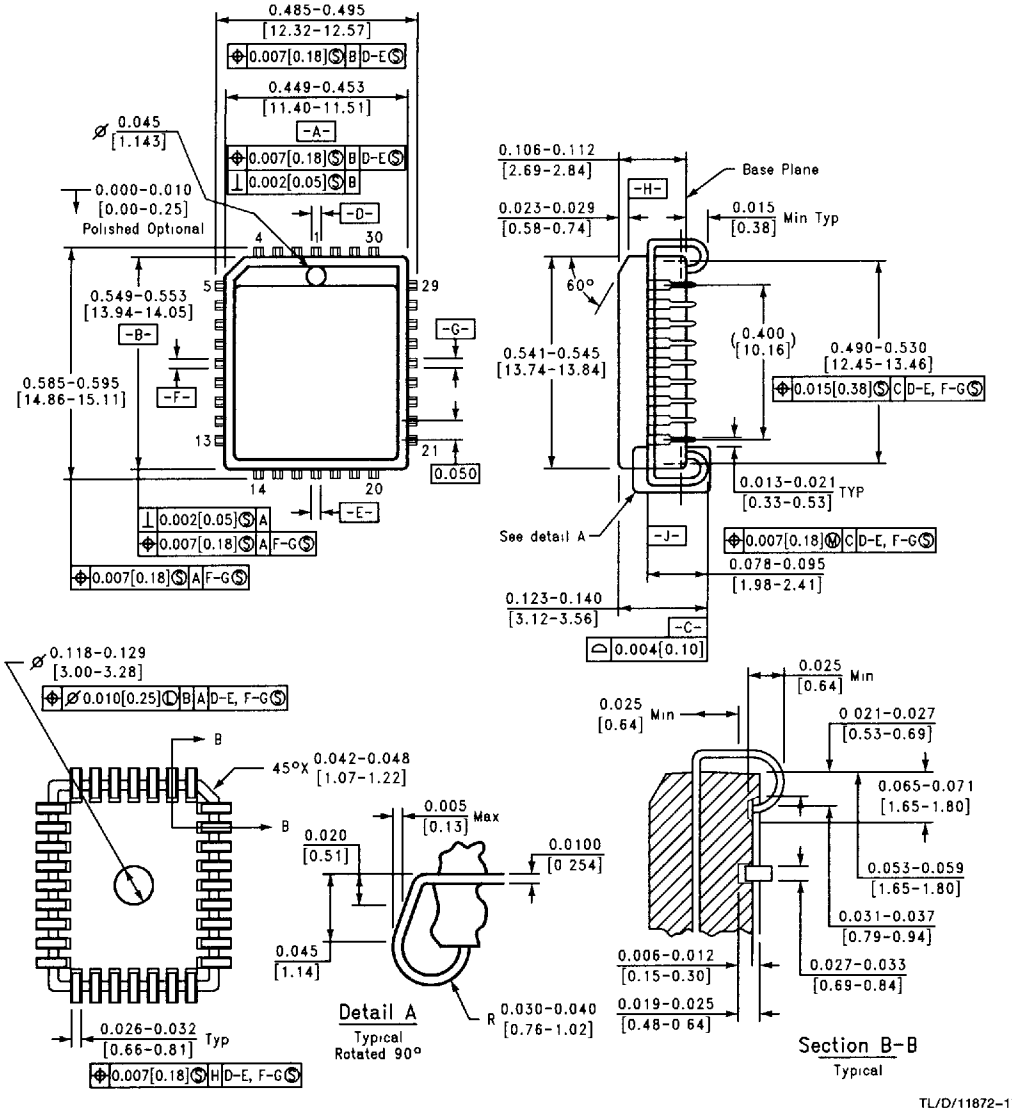
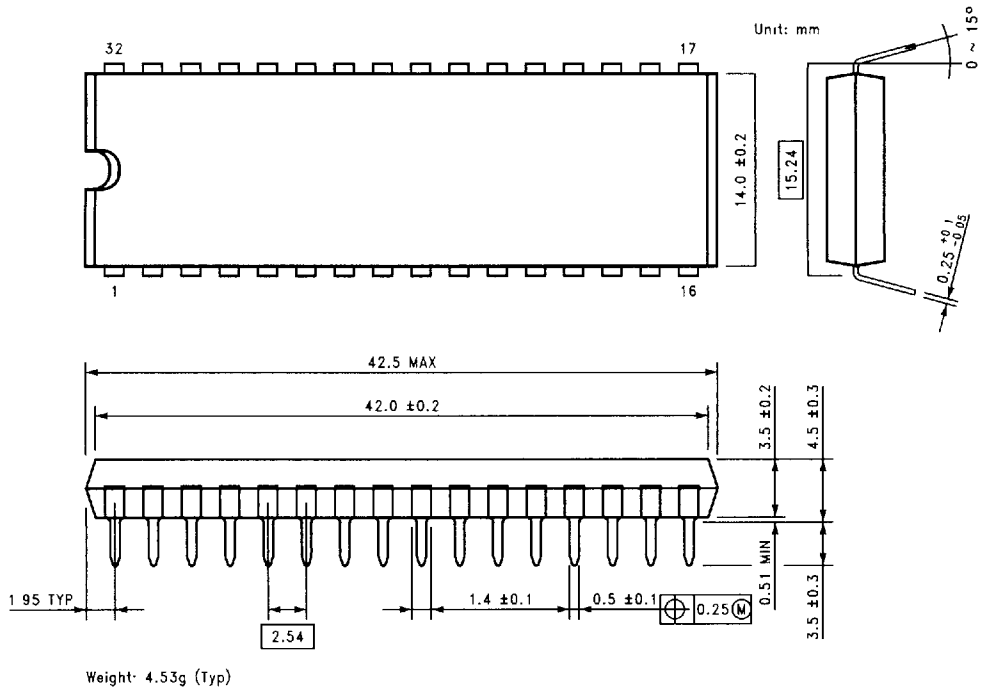
Physical Dimensions inches (millimeters)



TL/D/11872-17

32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM28F010VXXX

Physical Dimensions millimeters (Continued)

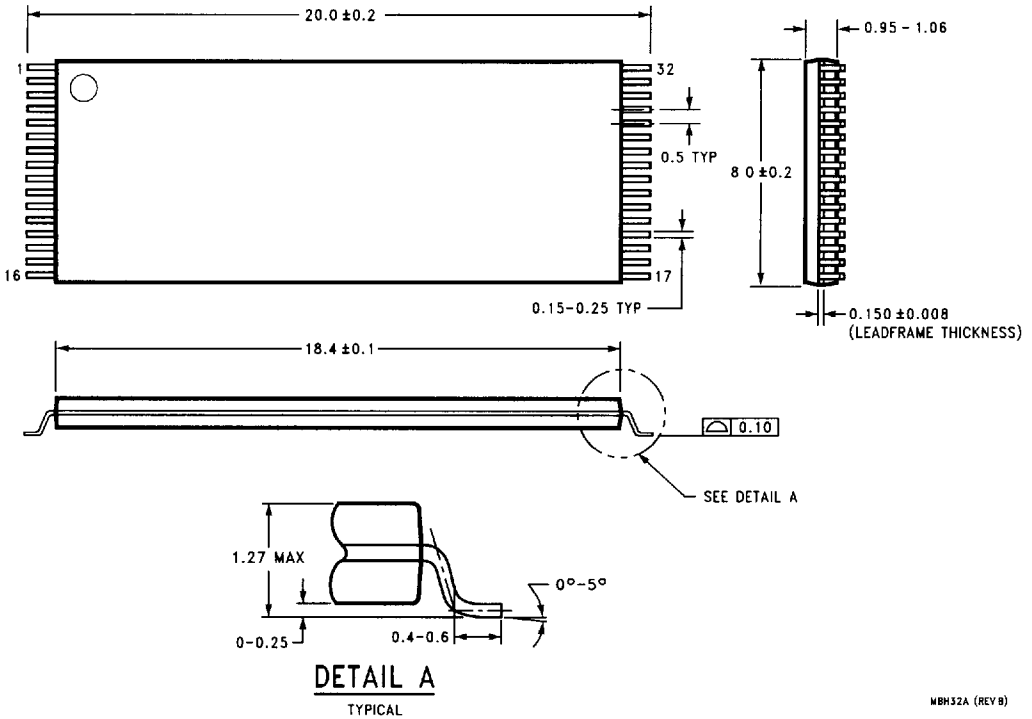


Weight: 4.53g (Typ)

TL/D/11872–18

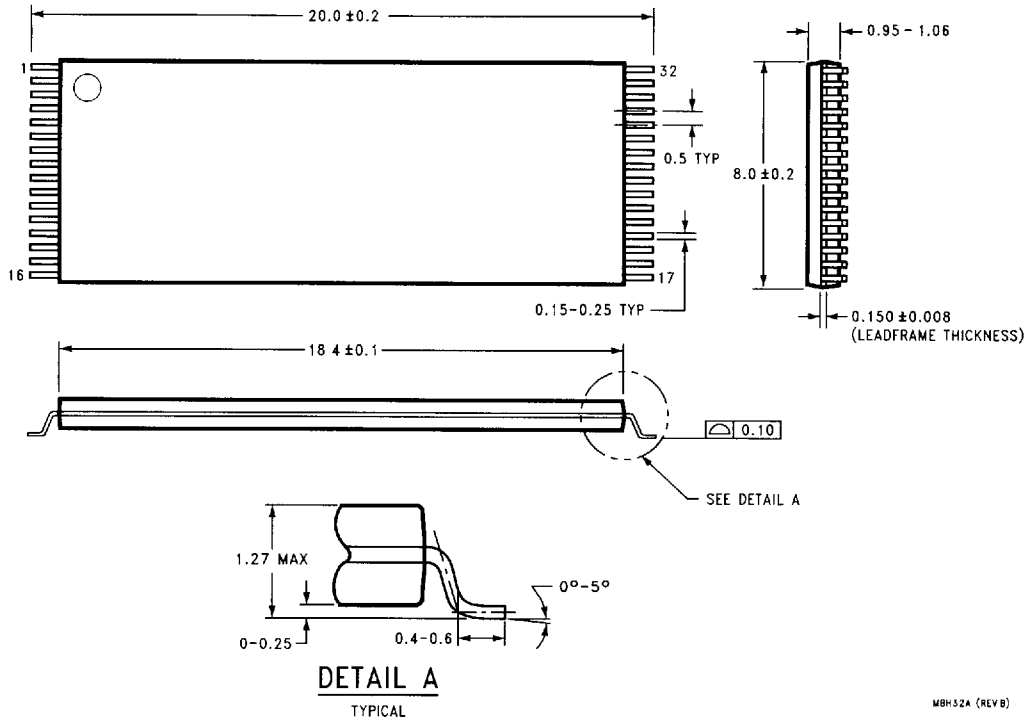
32-Lead Plastic Dual-In-Line Package (N)
Order Number NM28F010NXXX

Physical Dimensions millimeters (Continued)



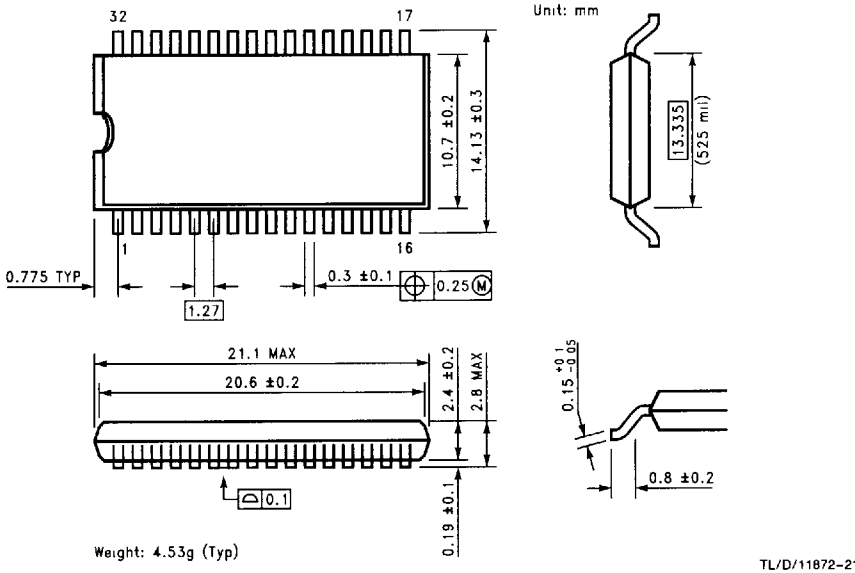
32-Lead Thin Small Outline Package (T)
Order Number NM28F010TXXX

Physical Dimensions millimeters (Continued)



32-Lead Reversed Thin Small Outline Package (TR)
Order Number NM28F010TRXXX

Physical Dimensions millimeters (Continued)



TL/D/11872-21

32-Lead Plastic Small Outline Package (M)
Order Number NM28F010MXXX

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Australia
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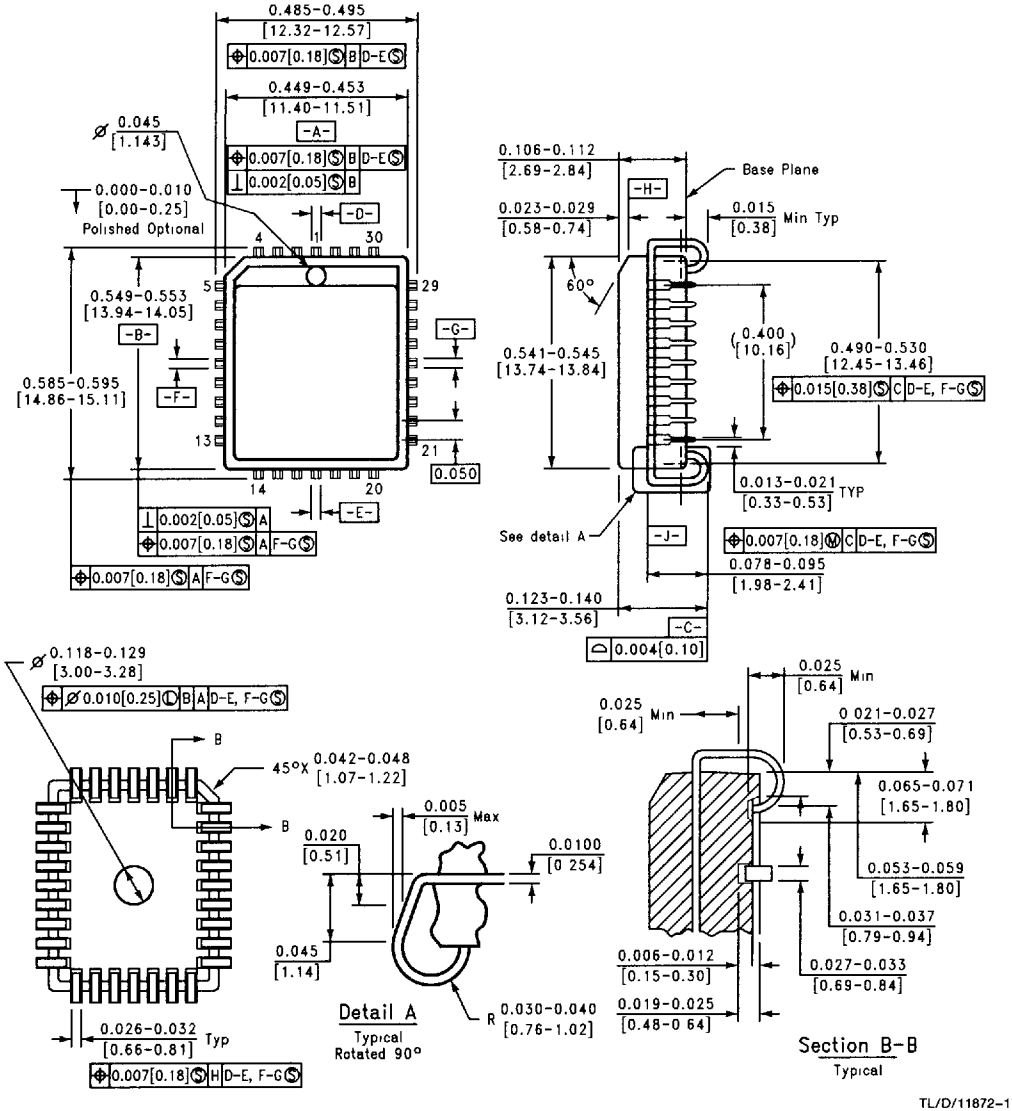
Fax (3) 558-9998

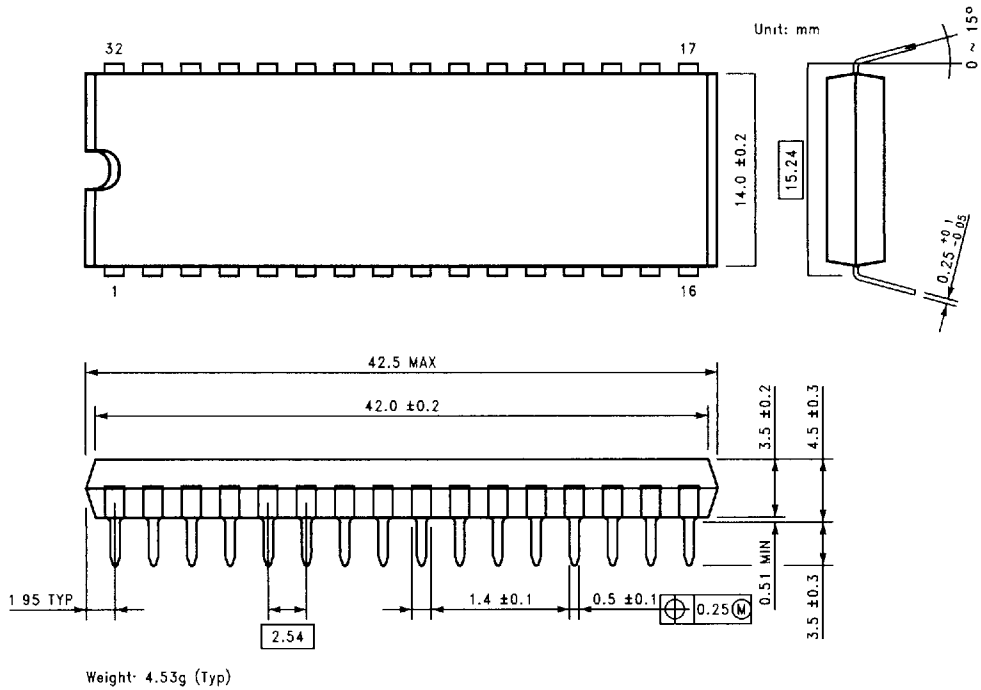
Physical Dimensions inches (millimeters)



TL/D/11872-17

32-Lead Plastic Leaded Chip Carrier (PLCC)
Order Number NM28F010VXXX

Physical Dimensions millimeters (Continued)

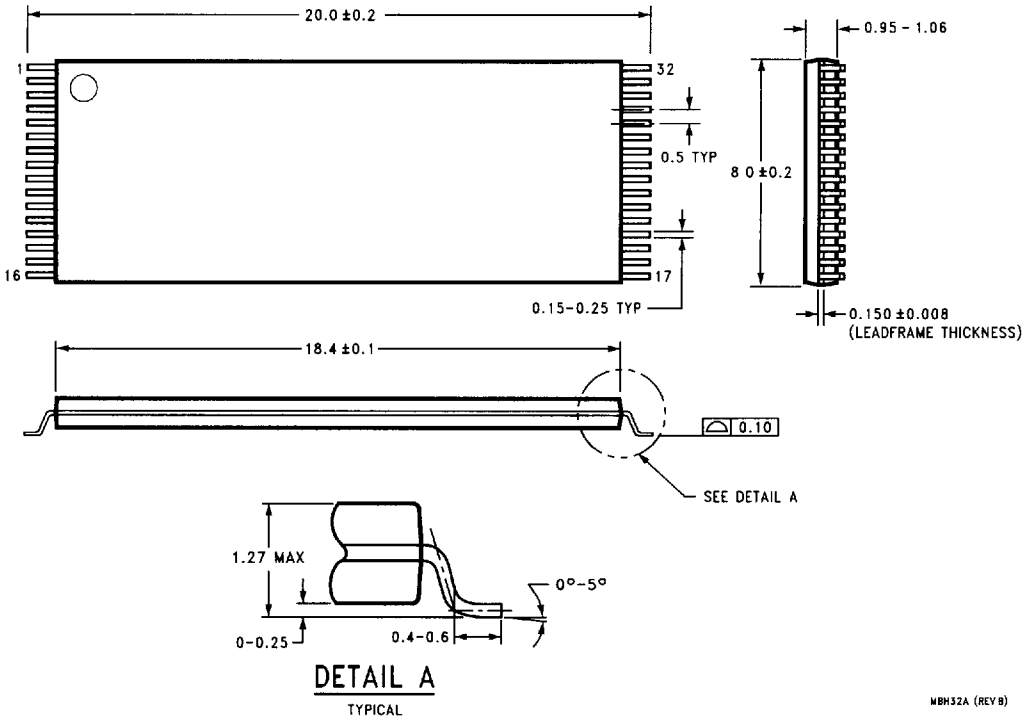


Weight: 4.53g (Typ)

TL/D/11872–18

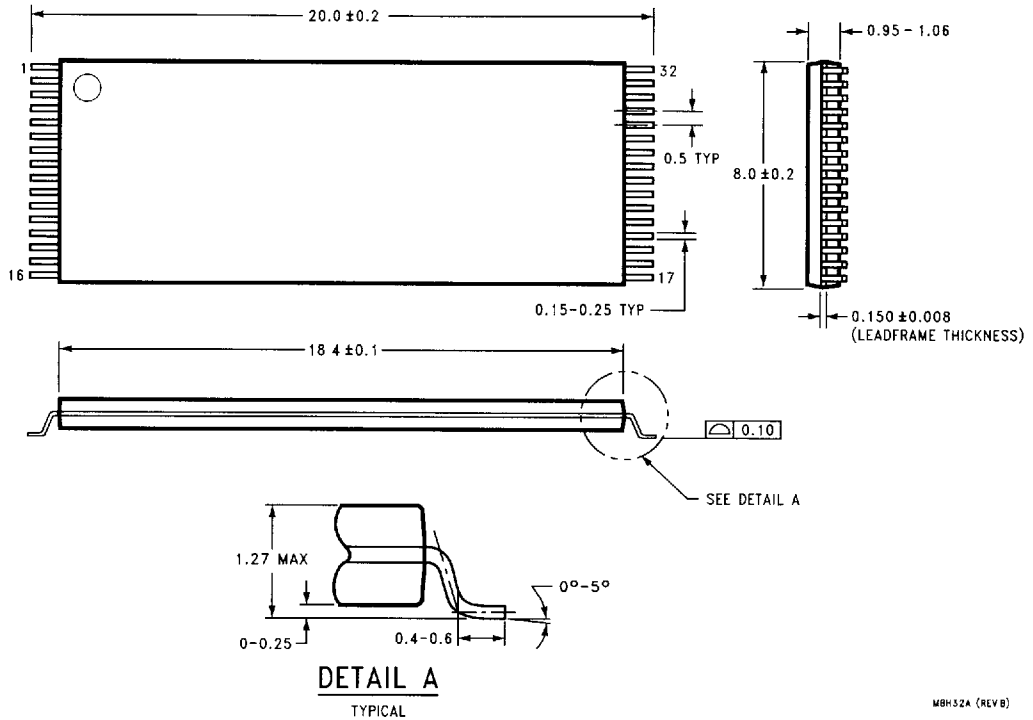
32-Lead Plastic Dual-In-Line Package (N)
Order Number NM28F010NXXX

Physical Dimensions millimeters (Continued)



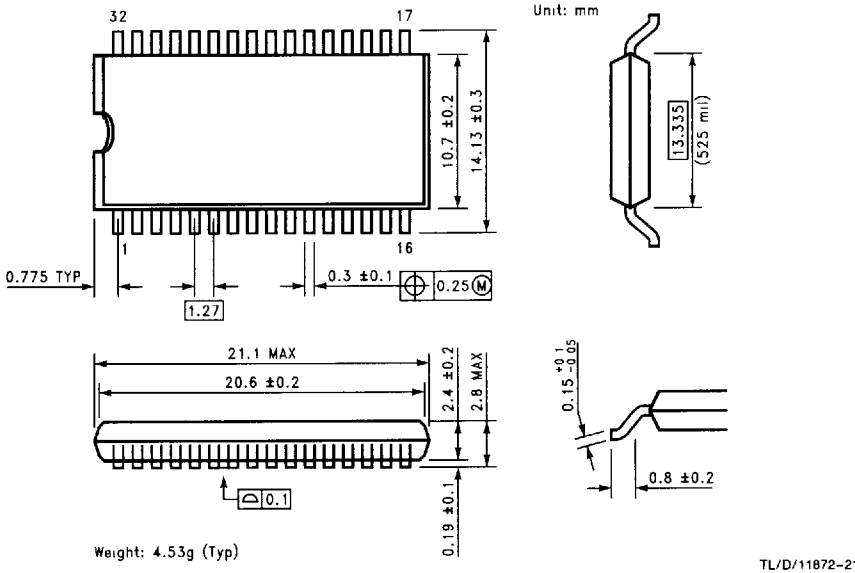
32-Lead Thin Small Outline Package (T)
Order Number NM28F010TXXX

Physical Dimensions millimeters (Continued)



32-Lead Reversed Thin Small Outline Package (TR)
Order Number NM28F010TRXXX

Physical Dimensions millimeters (Continued)



TL/D/11872-21

32-Lead Plastic Small Outline Package (M)
Order Number NM28F010MXXX

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