Features

Density "Doubler"

- 32Meg x 32 and 32 Meg x 36 organization
- Fast Page Mode Operation (FPM)
- CAS-before RAS refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Buffered Address & Write enable lines
- Fast access and cycle time - 60ns and 70ns
- JEDEC Standard 72 pin SIMM
- Single +5Volt ±10%
- On Board Decoupling Capacitors
- 4k Refresh Cycle

Pin Configurations and Block Diagram

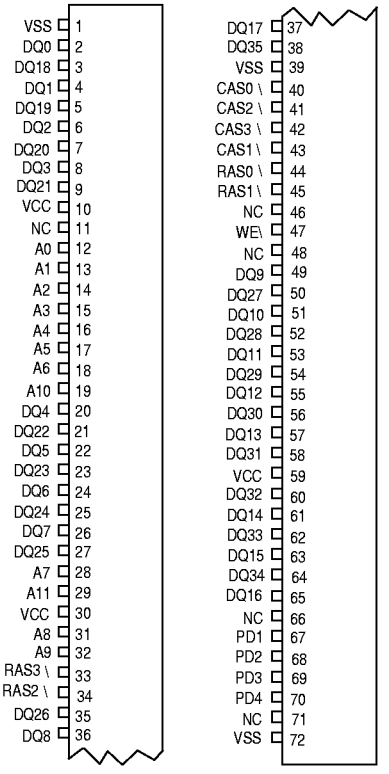
A0 - A11	Address Inputs
$\overline{CAS}$ 0-3	Column Address Strobe
$\overline{RAS}$ 0-3	ROW Address Strobe
$\overline{W}$	Write Control Input
DQ0-DQ35*	Data Input/Output
VCC	Power 5V ±10%
VSS	Ground
NC	No Connection

* On x32 version DQ8, DQ17, DQ26, DQ35 are no connects.

*FRAMM™ Technology produced under license from Dynamem, Inc.

32 Megx32 / 32Megx36
High Density DRAM Simm

The EDI4F3232F and EDI4F3632F are organized as 32 Meg x 32 and 32 Meg x 36 respectively. Both modules are part of EDI's High Density DRAM SIMM Product line which utilizes a multi-layer, rigid flex FR4 substrate.
Both DRAM modules meet the industry standard 72 pin JEDEC SIMM modules. The 128 Megabyte module measures only 1.750 inches in height and 0.325 inches thick (max). The module is well suited for applications requiring large memory arrays and provides up to 4 times the density of currently available DRAM SIMMs in only a single socket. The EDI4F3232F is assembled using (64) 16 Megx1 Fast Page Mode DRAMs and the EDI4F3632F is assembled using (72) 16 Meg x 1 Fast Page Mode DRAMs. Both modules are available with access times of 60 and 70ns.



	PD1	PD2	PD3	PD4
60ns	OPEN	VSS	OPEN	OPEN
70ns	OPEN	VSS	VSS	OPEN

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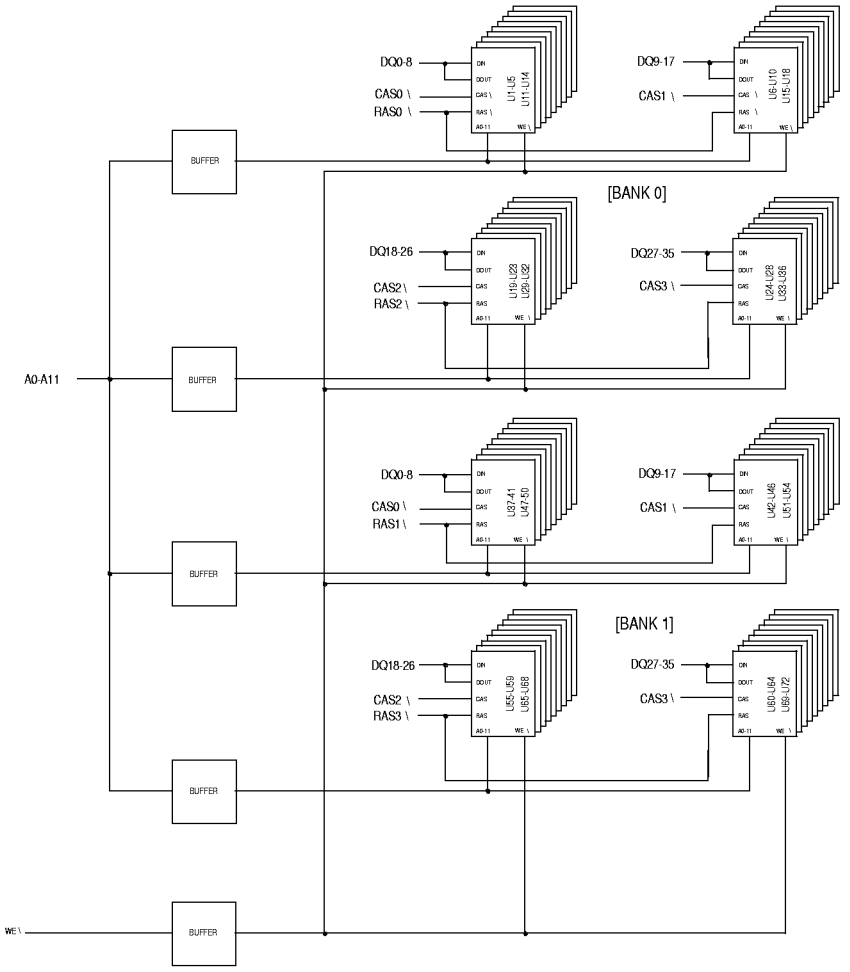
Pin Configurations and Block Diagram

EDI4F3632F



Note: For x32 version, DQ8, DQ17, DQ26 and DQ 35 are no connects.

Absolute Maximum Ratings*

Parameter	Symbol	Rating 5V	Units
Voltage on any pin relative to VSS	VIN,VOUT	-1.0 to +7.0	V
Voltage on VCC supply relative to VSS	VCC	-1.0 to +7.0	V
Storage Temperature	TSTG	-40 to +125	°C
Power Dissipation	PD	17	W
Short Circuit Output Current	IOS	50	mA

*Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (Voltages referenced to VSS, TA = 0 to 70°C)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Ground	VSS	0	0	0	V
Input High Voltage	VIH	2.4	-	VCC+1[2]	V
Input Low Voltage	VIL	-1.0[2]	-	0.8	V

Notes: 1. VCC +2.0V/20ns(5V), Pulse width is measured at VCC.
2. -2.0V/20ns, Pulse width is measured at VSS.

DC and Operating Characteristics

(EDI4F3632F, 32 Meg x 36)
(Recommended operating conditions unless otherwise noted)

Parameter	Sym	Conditions	60ns		70ns		Units
			Min	Max	Min	Max	
Operating Current	ICC1*	RAS+CAS cycling @ tRC=min		3052		2700	mA
Standby Current	ICC2	RAS=CAS=W=VIH		144		144	mA
RAS-Only Refresh Current	ICC3*	CAS=VIH, RAS cycling @ TRC=min		3052		2700	mA
Fast Page Mode Current	ICC4*	RAS=VIL,CAS, Address cycling @ TPC=min		2700		2350	mA
Standby Current	ICC5	RAS=CAS=W=VCC-0.2V		72		72	mA
CAS-Before-RAS Refresh Current	ICC6*	RAS and CAS cycling @ TRC=min		3052		2700	mA
Input Leakage Current Address	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±10	±10	±10	±10	µA
Input Leakage Current RAS 0-3, CAS 0-3	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±50	±50	±50	±50	µA
Input Leakage Current W\	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±10	±10	±10	±10	µA
Output Leakage Current	IOL	Data out is disabled, 0V<VOUT<VCC	±20	±20	±20	±20	µA
Output High Voltage Level	VOH	IOH=-5mA	2.4		2.4		V
Output Low Voltage Level	VOL	IOL = 4.2mA		0.4		0.4	V

DC and Operating Characteristics

(EDI4F3232F, 32 Meg x 32)
(Recommended operating conditions unless otherwise noted)

Parameter	Sym	Conditions	60ns		70ns		Units
			Min	Max	Min	Max	
Operating Current	ICC1*	RAS+CAS cycling @ tRC=min		2800		2500	mA
Standby Current	ICC2	RAS=CAS=W=VIH		128		128	mA
RAS-Only Refresh Current	ICC3*	CAS=VIH, RAS cycling @ TRC=min		2800		2500	mA
Fast Page Mode Current	ICC4*	RAS=VIL,CAS, Adress cycling @ TPC=min		2400		2100	mA
Standby Current	ICC5	RAS=CAS=W=VCC-0.2V		64		64	mA
CAS-Before-RAS Refresh Current	ICC6*	RAS and CAS cycling @ TRC=min		2800		2500	mA
Input Leakage Current Address	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±10	±10	±10	±10	µA
Input Leakage Current RAS 0-3, CAS 0-3	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±50	±50	±50	±50	µA
Input Leakage Current W\	IIL	Any input 0<VIN<VCC+0.5V all other pins not under test = 0 Volts	±10	±10	±10	±10	µA
Output Leakage Current	IOL	Data out is disabled, 0V<VOUT<VCC	±20	±20	±20	±20	µA
Output High Voltage Level	VOH	IOH=-5mA	2.4		2.4		V
Output Low Voltage Level	VOL	IOL = 4.2mA		0.4		0.4	V

* Note: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3, and ICC6, address can be changed maximum once while RAS=VIL. In ICC4, address can be changed maximum once within one fast page mode cycle time, TPC.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Typ	Unit
Input Capacitance (Address)	CA	15	pF
Input Capacitance (W)	CW	30	pF
Input Capacitance (RAS)	CR	85	pF
Input Capacitance (CAS)	CC	85	pF
Output Capacitance	CDQ	50	pF

AC Characteristics

(0°C≤TA≤70°C, See note 1)
(Test condition: VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V)

Parameter	Symbol	60ns Min	60ns Max	70ns Min	70ns Max	Units	Notes
Random read or write cycle time	TRC	110		130		ns	
Read-modify-write cycle time	TRWC	130		155		ns	
Access time from $\overline{RAS}$	TRAC		60		70	ns	3,4,9
Access time from $\overline{CAS}$	TCAC		15		20	ns	3,4
Access time from column address	TAA		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	TCLZ	0		0		ns	3
Output buffer turn-off delay	TOFF	0	15	0	20	ns	5
Transition time (rise and fall)	TT	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	TRP	40		50		ns	
$\overline{RAS}$ pulse width	TRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	TRSH	15		20		ns	
$\overline{CAS}$ hold time	TCSH	60		70		ns	
$\overline{CAS}$ pulse width	TCAS	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	TRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	TRAD	10	25	10	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	TCRP	5		5		ns	
Row address set-up time	TASR	5		5		ns	
Row address hold time	TRAH	10		10		ns	
Column address set-up time	TASC	5		5		ns	
Column address hold time	TCAH	10		15		ns	
Column address to $\overline{RAS}$ lead time	TRAL	35		40		ns	
Read command set-up time	TRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	TRCH	0		0		ns	7
Read command hold time referenced to$\overline{RAS}$	TRRH	0		0		ns	7
Write command hold time	TWCH	10		15		ns	
Write command pulse width	TWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	TRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	TCWL	15		20		ns	

See Notes on Page 6.

AC Characteristics

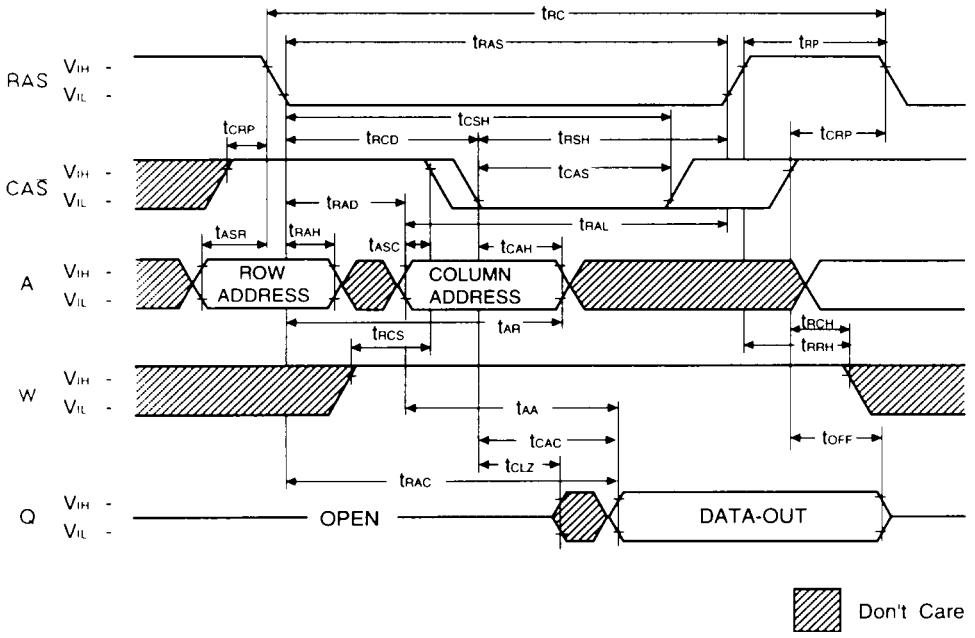
(0°C≤TA≤70°C, See note 1)
(Test condition (5V device): VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V)

Parameter	Symbol	60ns Min	60ns Max	70ns Min	70ns Max	Units	Notes
Data set-up time	TDS	0		0		ns	8
Data hold time	TDH	10		15		ns	8
Refresh period	TREF		64		64	ms	
Write Command set-up time	TWCS	0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	TCWD	15		20		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	TRWD	60		70		ns	6
Column address to $\overline{W}$ delay time	TAWD	25		30		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	TCPWD	35		40		ns	
$\overline{CAS}$ set-up time $\overline{CAS}$-before-$\overline{RAS}$ refresh	TCSR	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	TCHR	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	TRPC	5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	TCPT	20		30		ns	
Access time from $\overline{CAS}$ precharge	TCPA		35		40	ns	3
Fast page mode cycle time	TPC	40		45		ns	
Fast page mode read-modify-write cycle time	TPRWC	60		70		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	TCP	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	TRASP	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	TRHCP	35		40		ns	

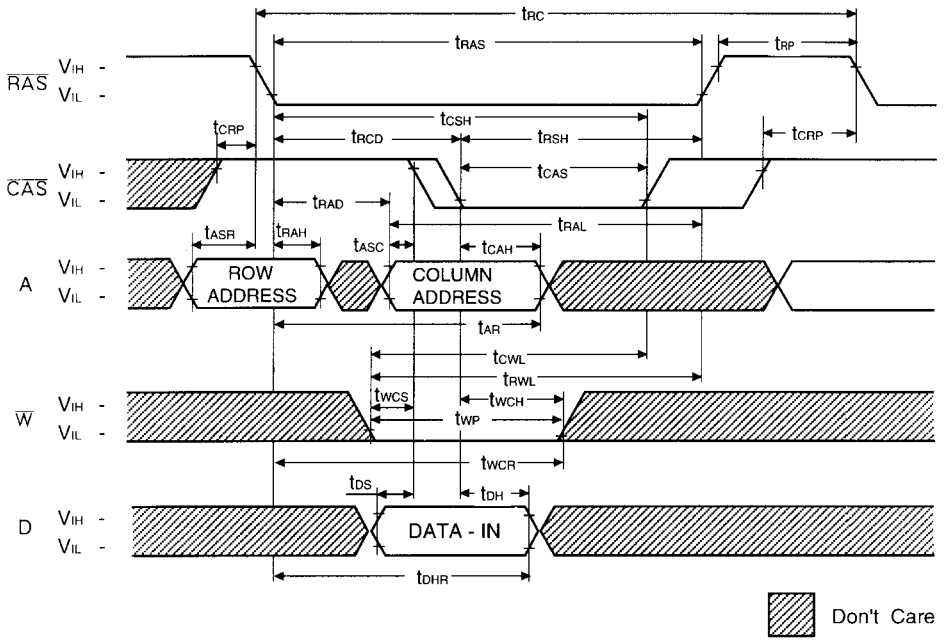
Notes:
1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load of equivalent to 2 TTL(5V device) loads and 100pF.
4. Operation within the TRCD(max) limit insures that TRAC(max) can be met. TRCD(max) is specified as a reference point only. If TRCD is greater than the specified TRCD(max) limit, then access time is controlled exclusively by TCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
6. TWCS, TRWD, TCWD, TAWD and TCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If TWCS≥TWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If TCWD≥TCWD(min), TRWD≥TRWD(min), TAWD≥TAWD(min) and TCPWD≥TCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either TRCH or TRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the TRAD(max) limit insures that TRAC(max) can be met. TRAD(max) is specified as a reference point only. If TRAD is greater than the specified TRAD (max) limit, then access time is controlled by TAA.

Timing Diagrams

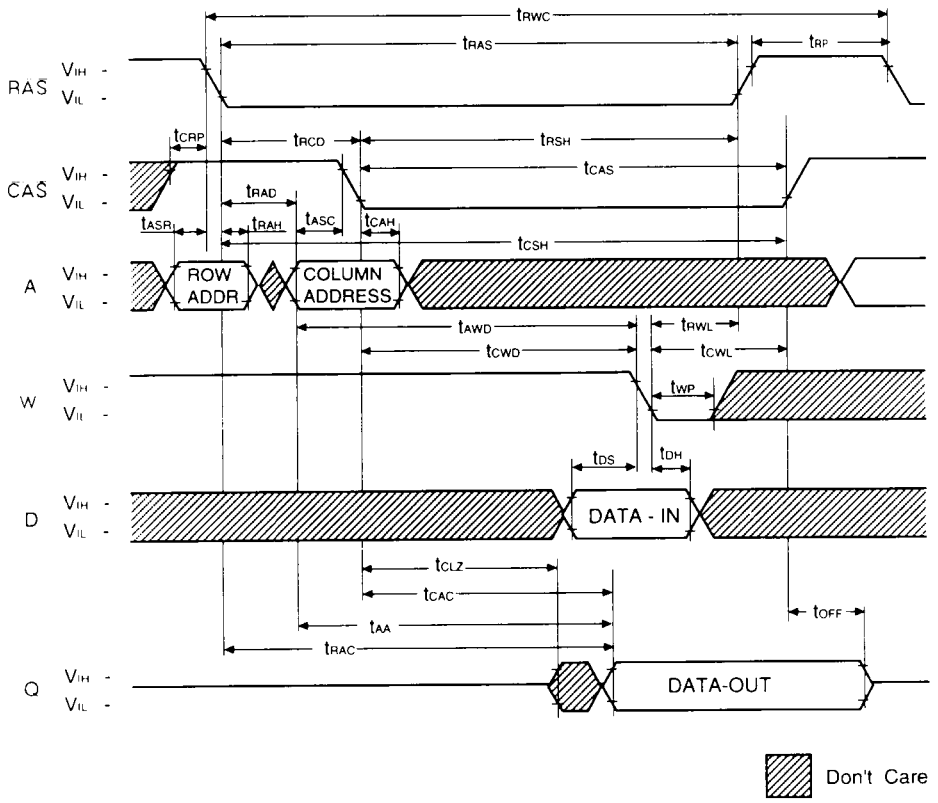
READ CYCLE



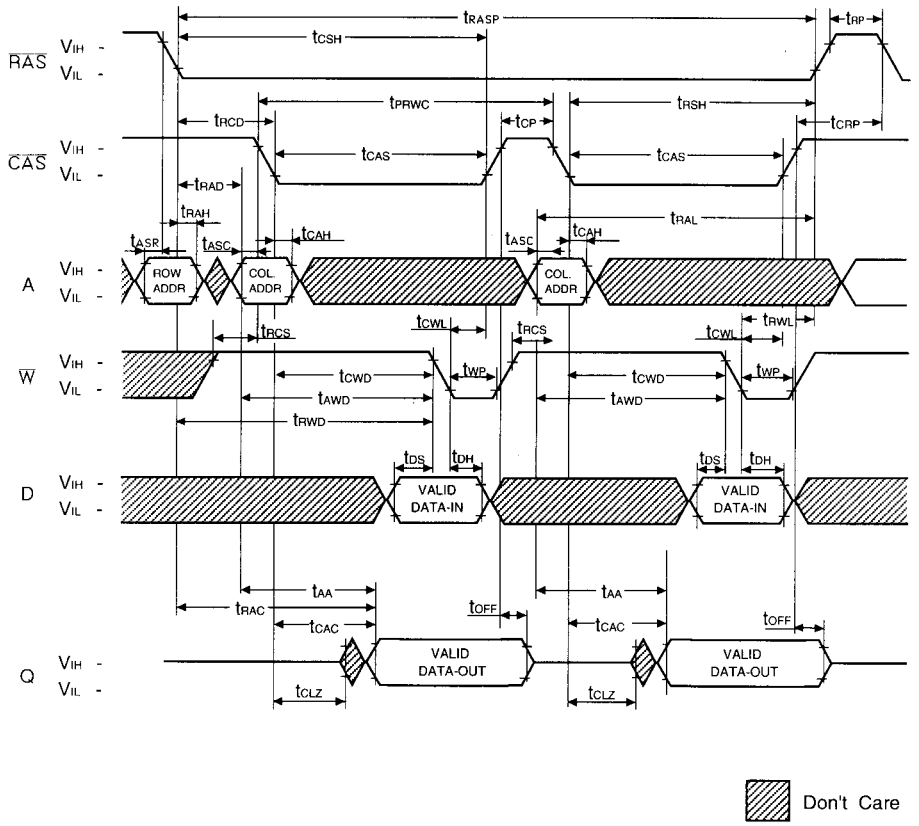
WRITE CYCLE (EARLY WRITE)



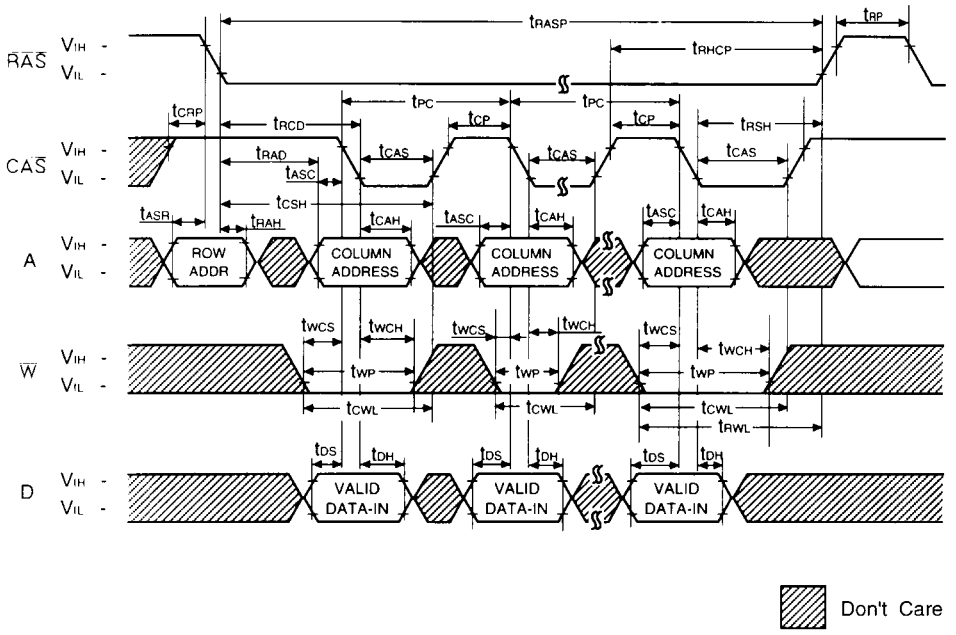
READ-WRITE / READ - MODIFY - WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

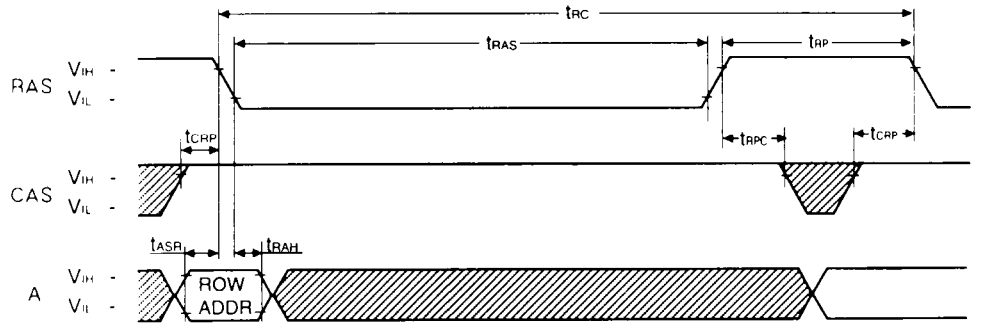


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



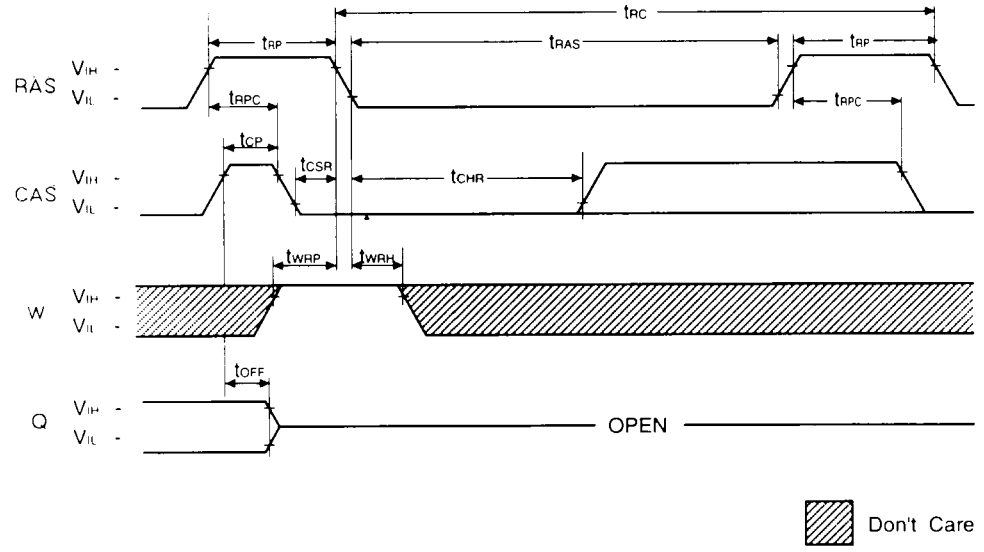
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : W D_{IN} = Don't care
D_{OUT} = Open

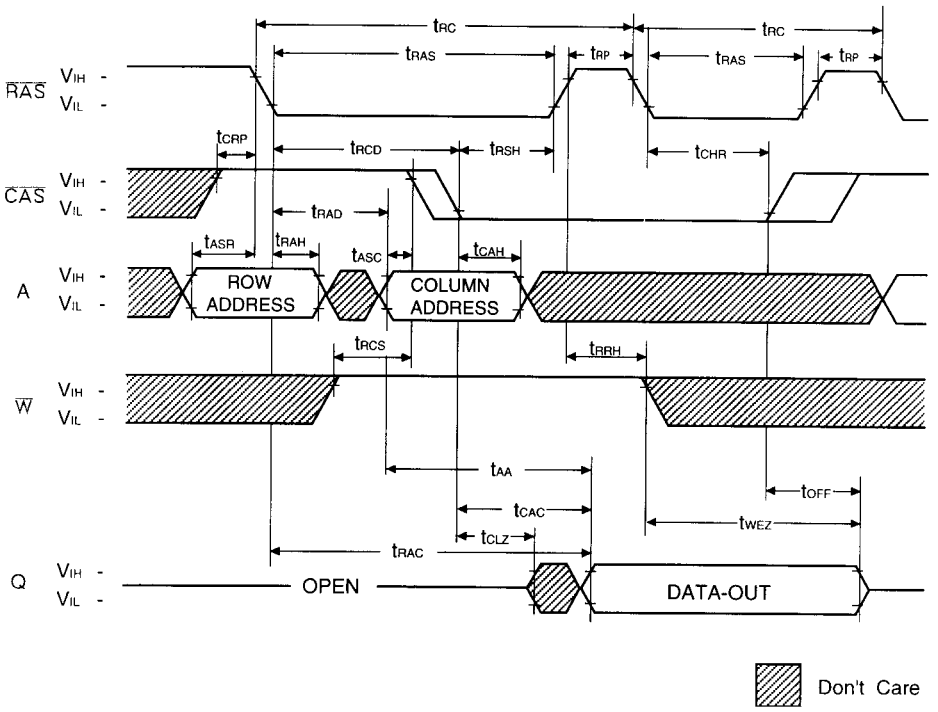


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : A = Don't Care

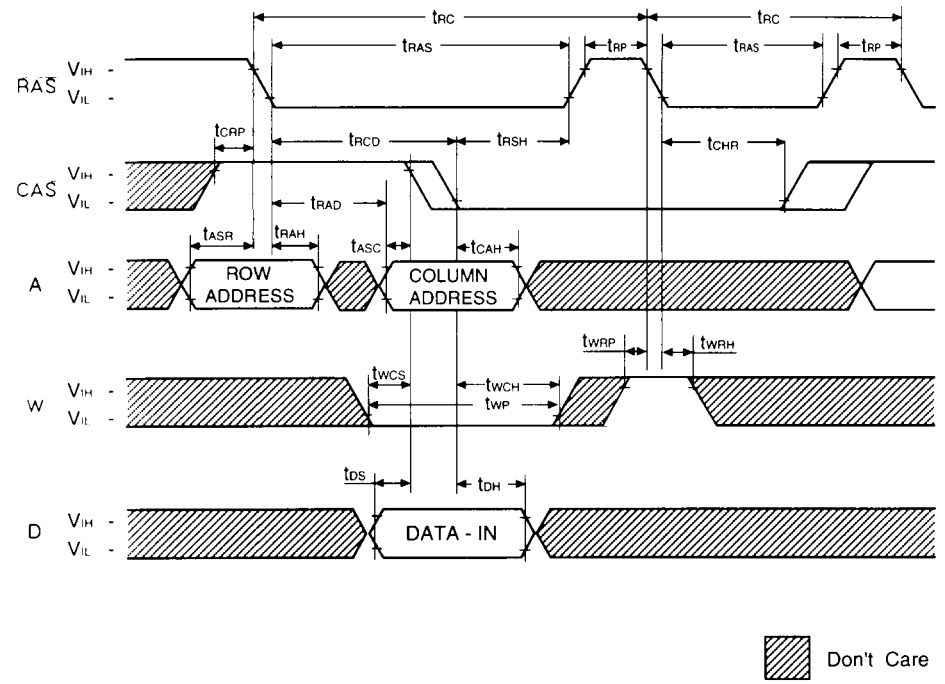


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



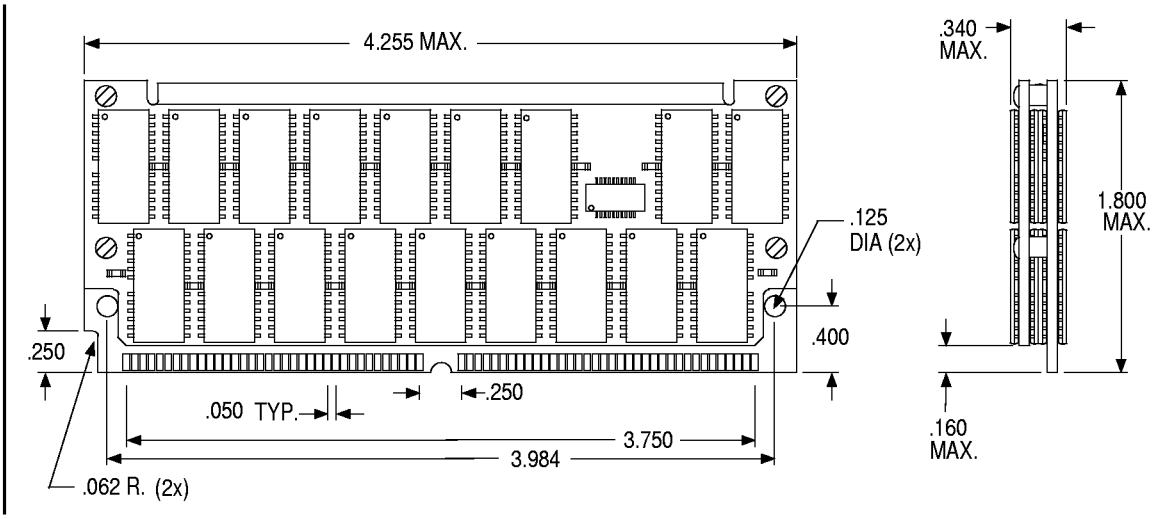
Ordering Information

Part Number	Organization	Speed (ns)	Package No.
EDI4F3632F6M	32Meg x 36	60	378
EDI4F3632F7M	32Meg x 36	70	378
EDI4F3232F6M	32Meg x 32	60	378
EDI4F3232F7M	32Meg x 32	70	378

Note: Gold Contacts available. Change from EDI4F to EDI4G.

Package Description

Package No. 378



Only x36 version shown for clarity, eight components depopulated for x32 version.

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