Precision Low Noise JFET Operational Amplifiers

ISL28110, ISL28210

The ISL28110, ISL28210, are single and dual JFET amplifiers featuring low noise, high slew rate, low input bias current and offset voltage, making them the ideal choice for high impedance applications where precision and low noise are important. The combination of precision, low noise, and high speed combined with a small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision medical and analytical instrumentation, sensor conditioning, precision power supply controls, industrial controls and photodiode amplifiers.

The ISL28110 single amplifier is available in the 8 Ld SOIC, TDFN, and MSOP packages. The ISL28210 dual amplifier is available in the 8 Ld SOIC and TDFN packages. All devices are offered in standard pin configurations and operate over the extended temperature range from -40°C to +125°C.

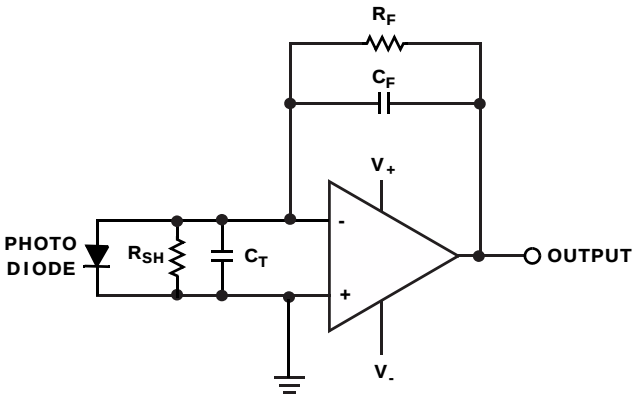
Features

- Wide Supply Range. . . . . .9V to 40V
- Low Voltage Noise . . . . . 6nV/√Hz
- Input Bias Current 2pA
- High Slew Rate. 23V/µs
- High Bandwidth 12.5MHz
- Low Input Offset . . . . . .300µV, Max
- Offset Drift . . . . . Grade C 10µV/°C
- Low Current Consumption 2.55mA
- Operating Temperature Range . . . -40°C to +125°C
- Small Package Offerings in Single, and Dual
- Pb-Free (RoHS compliant)

Applications* (see page 16)

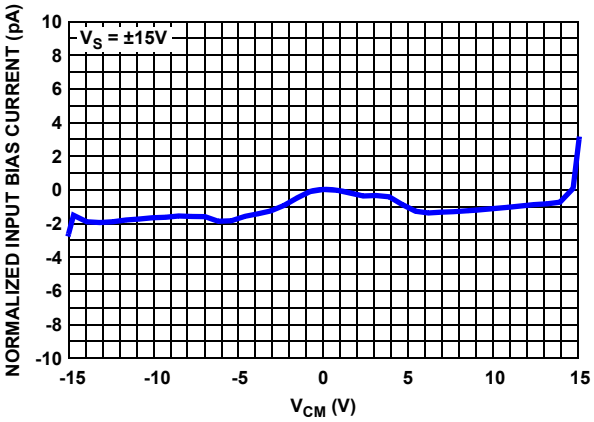
- Precision Instruments
- Photodiode Amplifiers
- High Impedance Buffers
- Medical Instrumentation
- Active Filter Blocks
- Industrial Controls

Typical Application



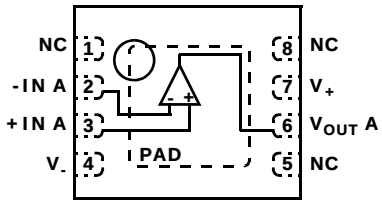
BASIC APPLICATION CIRCUIT - PHOTODIODE AMPLIFIER

Input Bias Current vs Common Mode Input Voltage

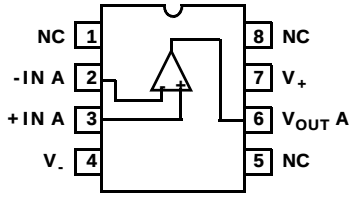


Pin Configurations

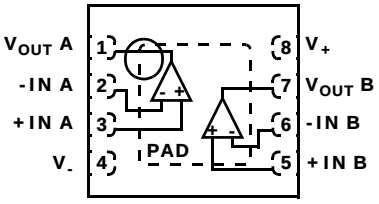
ISL28110
(8 LD TDFN)
TOP VIEW



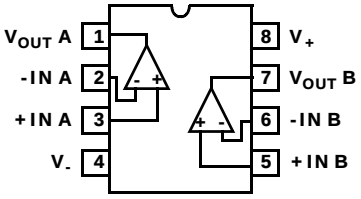
ISL28110
(8 LD, SOIC, MSOP)
TOP VIEW



ISL28210
(8 LD TDFN)
TOP VIEW

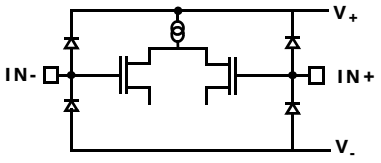


ISL28210
(8 LD SOIC)
TOP VIEW

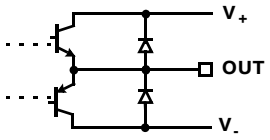


Pin Descriptions

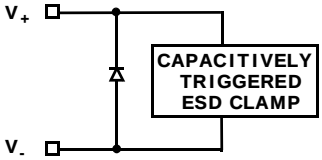
ISL28110 (8 Ld TDFN)	ISL28110 (8 Ld SOIC, 8 Ld MSOP)	ISL28210 (8 Ld TDFN)	ISL28210 (8 Ld SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	3	3	+IN A	Circuit 1	Amplifier A non-inverting input
2	2	2	2	-IN A	Circuit 1	Amplifier A inverting input
6	6	1	1	V_{OUT} A	Circuit 2	Amplifier A output
4	4	4	4	V_-	Circuit 3	Negative power supply
		5	5	+IN B	Circuit 1	Amplifier B non-inverting input
		6	6	-IN B	Circuit 1	Amplifier B inverting input
		7	7	V_{OUT} B	Circuit 2	Amplifier B output
7	7	8	8	V_+	Circuit 3	Positive power supply
1, 5, 8	1, 5, 8					No connect
PAD		PAD		PAD		Thermal Pad is electrically isolated from active circuitry. Pad can float, connect to Ground or to a potential source that is free from signals or noise sources.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TCV_{OS} (µV/°C)	PACKAGE (Pb-free)	PKG. DWG. #
Coming Soon ISL28110FBZ	28110 FBZ -C	10 (C Grade)	8 Ld SOIC	M8.15E
ISL28210FBZ	28210 FBZ -C	10 (C Grade)	8 Ld SOIC	M8.15E
Coming Soon ISL28110FRTZ	-C 8110	10 (C Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28210FRTZ	-C 8210	10 (C Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28110FRTBZ	8110	4 (B Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28210FRTBZ	8210	4 (B Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28110FBBZ	28110 FBZ -C	4 (B Grade)	8 Ld SOIC	M8.15E
Coming Soon ISL28210FBBZ	28210 FBZ	4 (B Grade)	8 Ld SOIC	M8.15E
Coming Soon ISL28110FUBZ	8110Z	4 (B Grade)	8 Ld MSOP	M8.118
Coming Soon ISL28110FUZ	8110Z	10 (C Grade)	8 Ld MSOP	M8.118

NOTES:

1. Add "-T7", "-T13" or "-T7A" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28110, ISL28210. For more information on MSL please see techbrief TB363.

Absolute Voltage Ratings

Maximum Supply Voltage 42V
Maximum Supply Turn On Voltage Slew Rate 1V/µs
Maximum Differential Input Voltage 33V
Min/Max Input Voltage . . . . . V_- - 0.5V to V_+ + 0.5V
Max/Min Input current for input voltage >V+ or <V- . ±20mA
Output Short-Circuit Duration
(1 output at a time) . . . . . Indefinite
ESD Ratings
Human Body Model 4000V
Machine Model 400V
Charged Device Model 2000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (Notes 5, 7)		
ISL28110	125	70
ISL28210	120	50
8 Ld TDFN (Notes 4, 6)		
ISL28110	48	7.8
ISL28210	46	4.5
8 Ld MSOP (Notes 5, 7)		
ISL28110	158	60

Ambient Operating Temperature Range . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_S = ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-300		300	µV
		-40°C ≤ T_A ≤ +125°C	**-1300**		**1300**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	-40°C ≤ T_A ≤ +125°C		**1**	**10**	µV/C
I_B	Input Bias Current (Note 9)		-2	±0.3	2	pA
		-40°C < T_A < +60°C	-4.5		4.5	pA
		-40°C < T_A < +85°C	-50		50	pA
		-40°C ≤ T_A ≤ +125°C	**-245**		**245**	pA
I_{OS}	Input Offset Current (Note 9)		-1	±0.15	1	pA
		-40°C < T_A < +60°C	-2.25		2.25	pA
		-40°C < T_A < +85°C	-30		30	pA
		-40°C ≤ T_A ≤ +125°C	**-105**		**105**	pA
$C_{IN-DIFF}$	Differential Input Capacitance			8.3		pF
C_{IN-CM}	Common Mode Input Capacitance			11.8		pF
$R_{IN-DIFF}$	Differential Input Resistance			530		GΩ
R_{IN-CM}	Common Mode Input Resistance			560		GΩ
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- + 1.5		V_+ - 1.5	V
			V_- + 2.5		**V_+ - 2.5**	V

Electrical Specifications V_S = ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
CMRR	Common Mode Rejection Ratio	V_{CM} = -3.5V to +3.5V		90		dB
		V_{CM} = -2.5V to +2.5V	**88**	**100**		dB
A_{VOL}	Open-loop Gain	R_L = 10kΩ to ground V_O = -3V to +3V	165	240		V/mV
			155			V/mV
DYNAMIC PERFORMANCE						
GBWP	Gain-bandwidth Product	G = 100, R_L = 100kΩ, C_L = 4pF	11	12.5		MHz
SR	Slew Rate, V_{OUT} 20% to 80%	G = -1, R_L = 2kΩ		23		V/µs
THD+N	Total Harmonic Distortion + Noise	G = 1, f = 1kHz, $4V_{P-P}$, R_L = 2kΩ		0.0002		%
		G = 1, f = 1kHz, $4V_{P-P}$, R_L = 600Ω		0.0003		%
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = $4V_{P-P}$, R_L = 2kΩ to V_{CM}		0.4		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = $4V_{P-P}$, R_L = 2kΩ to V_{CM}		1		µs
NOISE PERFORMANCE						
e_{nP-P}	Peak-to-Peak Input Voltage Noise	0.1Hz to 10Hz		580		nV_{P-P}
e_n	Input Voltage Noise Spectral Density	f = 10Hz		14		nV/√Hz
		f = 100Hz		7		nV/√Hz
		f = 1kHz		6		nV/√Hz
		f = 10kHz		6		nV/√Hz
i_n	Input Current Noise Spectral Density	f = 1kHz		9		fA/√Hz
OUTPUT CHARACTERISTICS						
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ		0.8	1.0	V
					1.1	V
		R_L = 2kΩ		0.9	1.1	V
					1.2	V
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L to GND = 10kΩ		0.8	1.0	V
					1.1	V
		R_L to GND = 2kΩ		0.9	1.1	V
					1.2	V
I_{SC}	Output Short Circuit Current	R_L = 10Ω to V+. V-		±50		mA
POWER SUPPLY						
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±4.5**		**±20V**	V
PSRR	Power Supply Rejection Ratio	V_S = ± 4.5V to ±5V	102	115		dB
			100			dB
I_S	Supply Current/Amplifier			2.5	2.9	mA
					3.8	mA

Electrical Specifications V_S = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-300		300	µV
		-40°C ≤ T_A ≤ +125°C	**-1300**		**1300**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient (Grade C)	-40°C ≤ T_A ≤ +125°C		**1**	**10**	µV/C
I_B	Input Bias Current (Note 9)		5	±2	5	pA
		-40°C < T_A < +60°C	-350		350	pA
		-40°C < T_A < +85°C	-700		700	pA
		-40°C ≤ T_A ≤ +125°C	**-3600**		**3600**	pA
I_{OS}	Input Offset Current (Note 9)		-2.5	±0.5	2.5	pA
		-40°C < T_A < +60°C	-285		285	pA
		-40°C < T_A < +85°C	-445		445	pA
		-40°C ≤ T_A ≤ +125°C	**-2000**		**2000**	pA
$C_{IN-DIFF}$	Differential Input Capacitance			8.3		pF
C_{IN-CM}	Common Mode Input Capacitance			11.8		pF
$R_{IN-DIFF}$	Differential Input Resistance			530		GΩ
R_{IN-CM}	Common Mode Input Resistance			560		GΩ
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	**V_- + 1.5**		**V_+ - 1.5**	V
CMRR	Common Mode Rejection Ratio	V_{CM} = -13.5V to +13.5V	**80**	**100**		dB
A_{VOL}	Open-loop Gain	R_L = 10kΩ to ground V_O = -12.5V to +12.5V	230	290		V/mV
		-40°C ≤ T_A ≤ +125°C	**200**			V/mV
DYNAMIC PERFORMANCE						
GBWP	Gain-bandwidth Product	G =100, R_L = 100kΩ, C_L = 4pF	11	12.5		MHz
SR	Slew Rate, V_{OUT} 20% to 80%	G = -1, R_L = 2kΩ		23		V/µs
THD+N	Total Harmonic Distortion + Noise	G = 1, f = 1kHz, 10V_{P-P}, R_L = 2kΩ		0.00025		%
		G = 1, f = 1kHz, 10V_{P-P}, R_L = 600Ω		0.0003		%
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_L = 2kΩ to V_{CM}		0.9		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_L = 2kΩ to V_{CM}		1.2		µs
NOISE PERFORMANCE						
e_{nP-P}	Peak-to-Peak Input Voltage Noise	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Input Voltage Noise Spectral Density	f = 10Hz		18		nV/√Hz
		f = 100Hz		7.8		nV/√Hz
		f = 1kHz		6		nV/√Hz
		f = 10kHz		6		nV/√Hz
i_n	Input Current Noise Spectral Density	f = 1kHz		9		fA/√Hz

Electrical Specifications V_S = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
OUTPUT CHARACTERISTICS						
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ		0.8	1.0	V
					1.1	V
		R_L = 2kΩ		0.9	1.1	V
					1.2	V
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L to GND = 10kΩ		0.8	1.0	V
					1.1	V
		R_L to GND = 2kΩ		0.9	1.1	V
					1.2	V
I_{SC}	Output Short Circuit Current	R_L = 10Ω to V+. V-		±50		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	102	115		dB
			100			dB
I_S	Supply Current/Amplifier			2.55	3.1	mA
					3.9	mA

NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Limits established by characterization and are not production tested.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified.

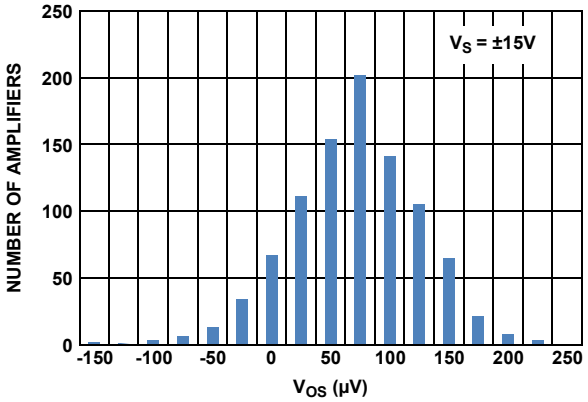


FIGURE 1. INPUT OFFSET VOLTAGE (V_{OS}) DISTRIBUTION

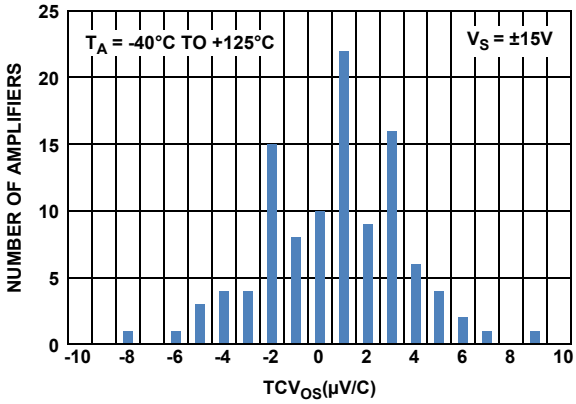


FIGURE 2. T_CV_{OS} DISTRIBUTION, -40°C to +125°C

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

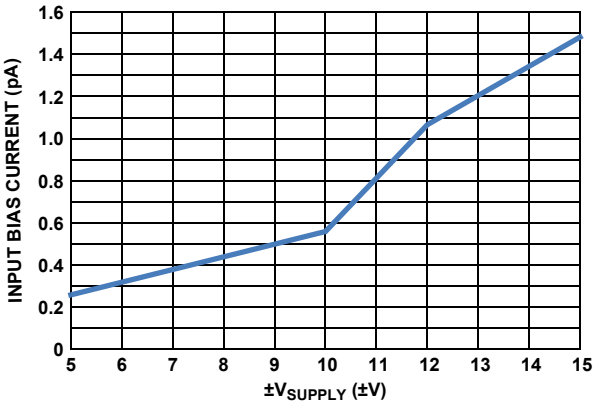


FIGURE 3. INPUT BIAS CURRENT (I_B) vs SUPPLY VOLTAGE

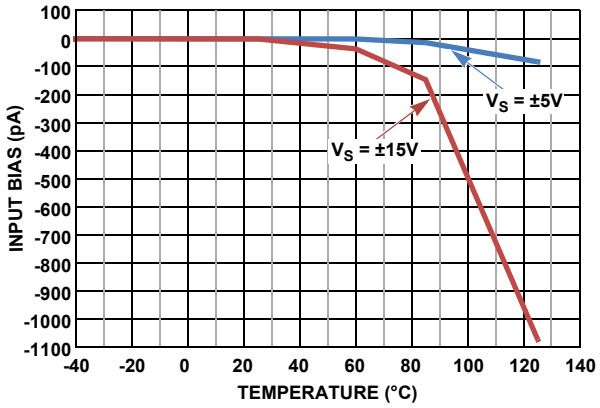


FIGURE 4. INPUT BIAS CURRENT (I_B) vs TEMPERATURE

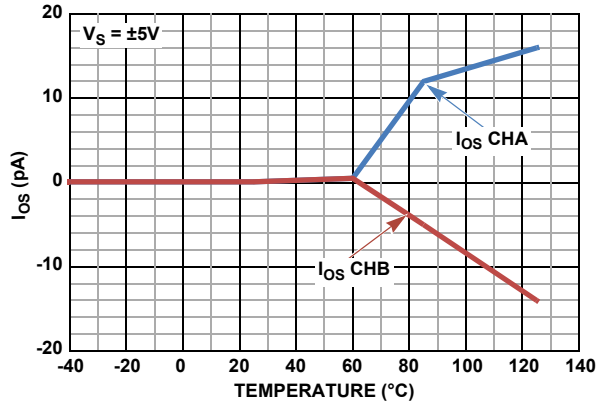


FIGURE 5. ISL28210 INPUT OFFSET CURRENT (I_{OS}) vs TEMPERATURE, V_S = ± 5V

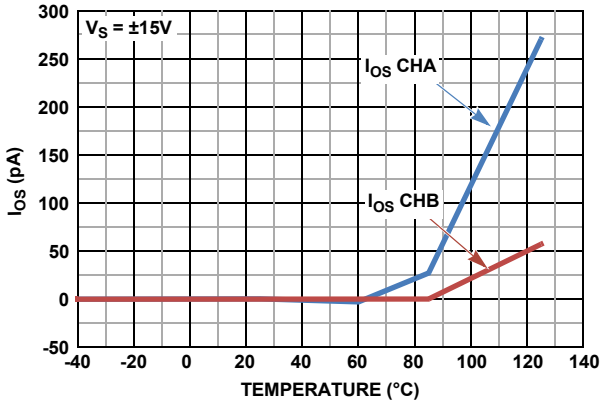


FIGURE 6. ISL28210 INPUT OFFSET CURRENT (I_{OS}) vs TEMPERATURE, V_S = ± 15V

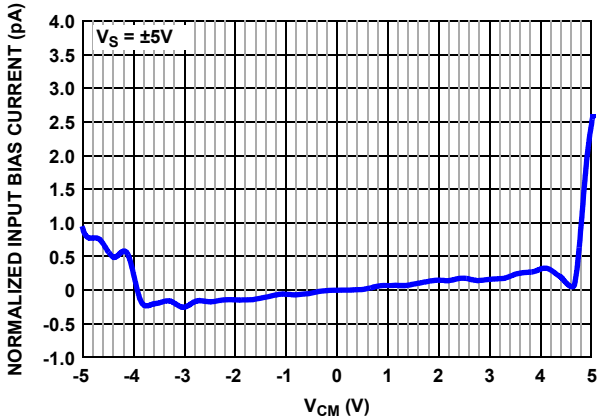


FIGURE 7. NORMALIZED INPUT BIAS CURRENT (I_B) vs INPUT COMMON MODE VOLTAGE (V_{CM}), V_S = ± 5V

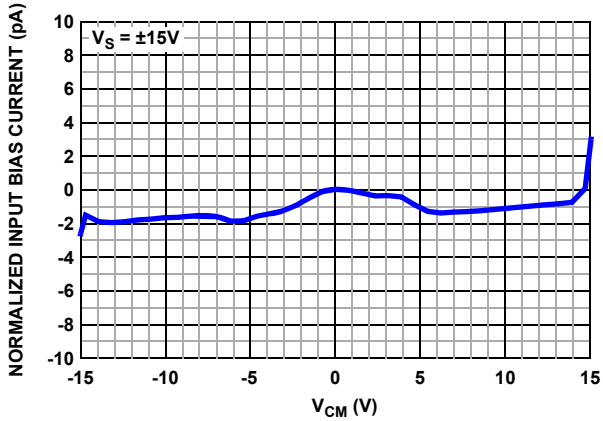


FIGURE 8. NORMALIZED INPUT BIAS CURRENT (I_B) vs INPUT COMMON MODE VOLTAGE (V_{CM}), V_S = ± 15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

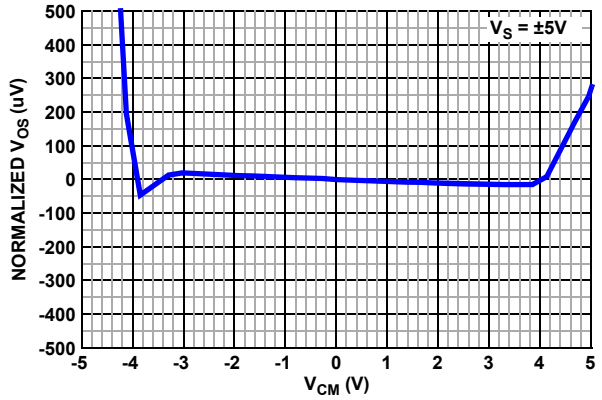


FIGURE 9. NORMALIZED INPUT OFFSET VOLTAGE (V_{OS}) vs INPUT COMMON MODE VOLTAGE (V_{CM}), V_S = ± 5V

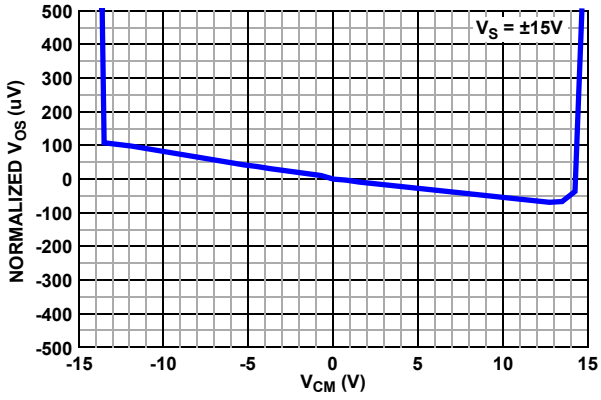


FIGURE 10. NORMALIZED INPUT OFFSET VOLTAGE (V_{OS}) vs INPUT COMMON MODE VOLTAGE (V_{CM}), V_S = ± 15V

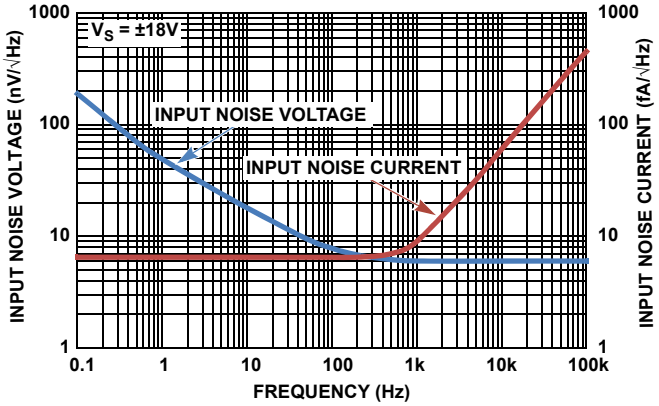


FIGURE 11. INPUT NOISE VOLTAGE (e_n) AND CURRENT (i_n) vs FREQUENCY, V_S = ±18V

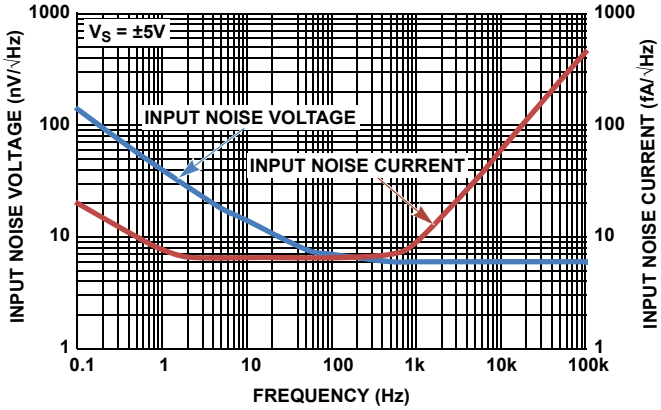


FIGURE 12. INPUT NOISE VOLTAGE (e_n) AND CURRENT (i_n) vs FREQUENCY, V_S = ±5V

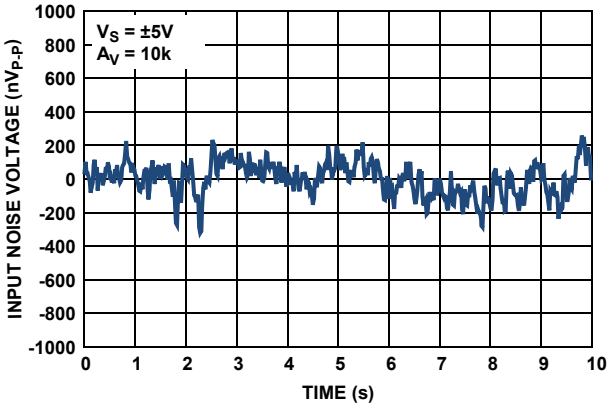


FIGURE 13. 0.1Hz TO 10Hz V_{P-P} NOISE VOLTAGE, V_S = ±5V

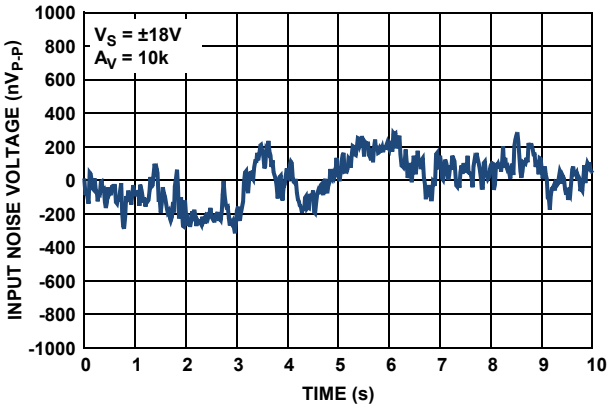


FIGURE 14. 0.1Hz TO 10Hz V_{P-P} NOISE VOLTAGE, V_S = ±18V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

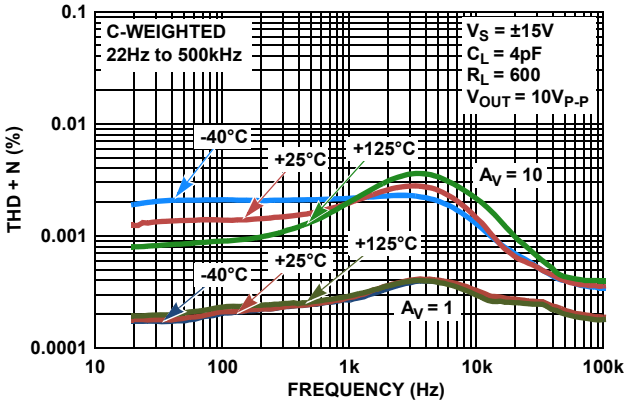


FIGURE 15. THD+N vs FREQUENCY vs TEMPERATURE, A_V = 1, 10, V_{OUT} = 10V_{P-P}, R_L = 600Ω

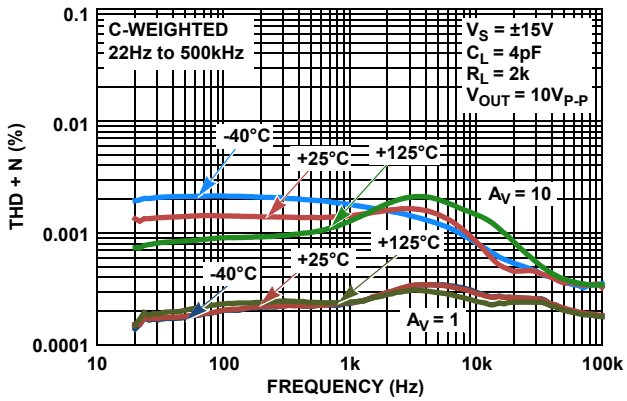


FIGURE 16. THD+N vs FREQUENCY vs TEMPERATURE, V_{OUT} = 10V_{P-P}, R_L = 2kΩ

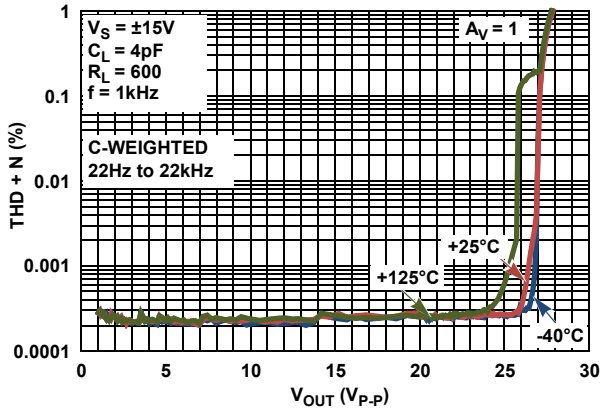


FIGURE 17. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1 f = 1kHz, R_L = 600Ω

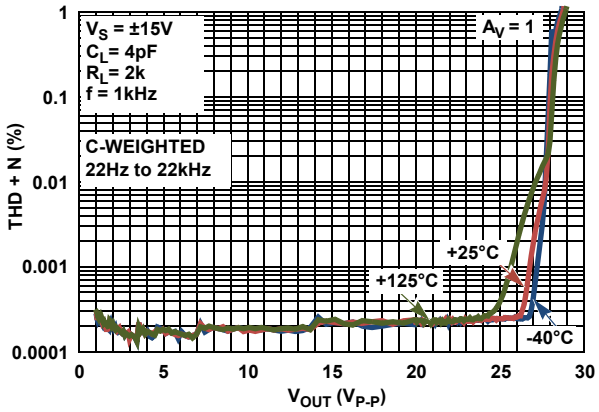


FIGURE 18. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1 f =1kHz, R_L = 2kΩ

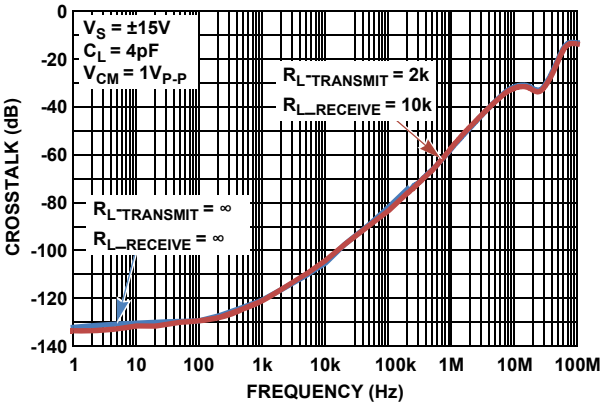


FIGURE 19. CROSSTALK vs FREQUENCY

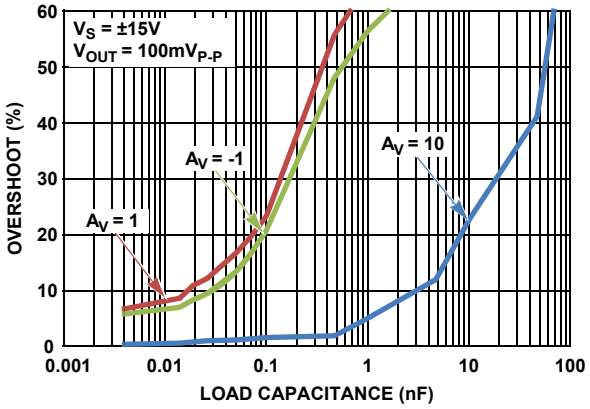


FIGURE 20. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE (C_L)

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

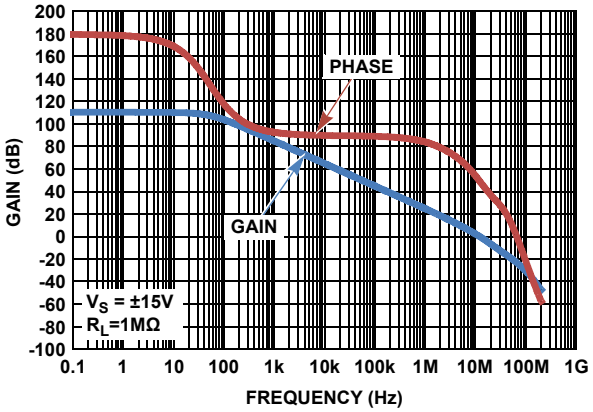


FIGURE 21. OPEN LOOP GAIN-PHASE vs FREQUENCY

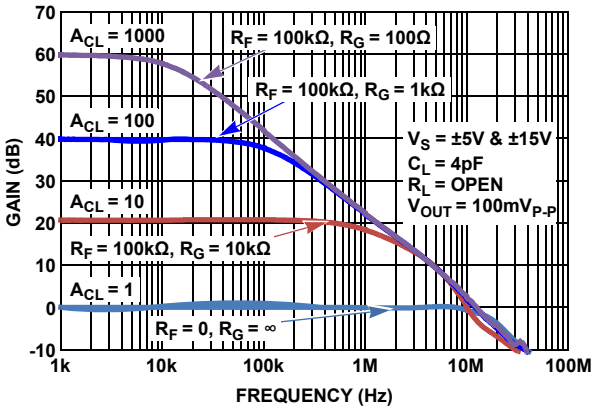


FIGURE 22. CLOSED LOOP GAIN vs FREQUENCY

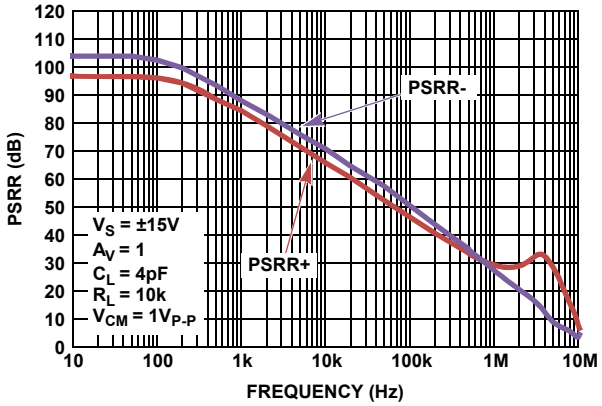


FIGURE 23. POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY

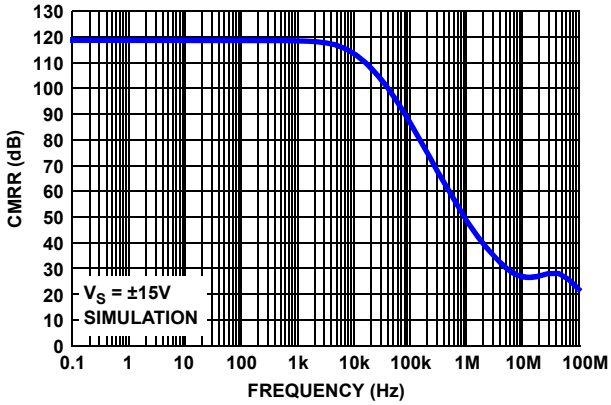


FIGURE 24. COMMON-MODE REJECTION RATIO (CMRR) vs FREQUENCY

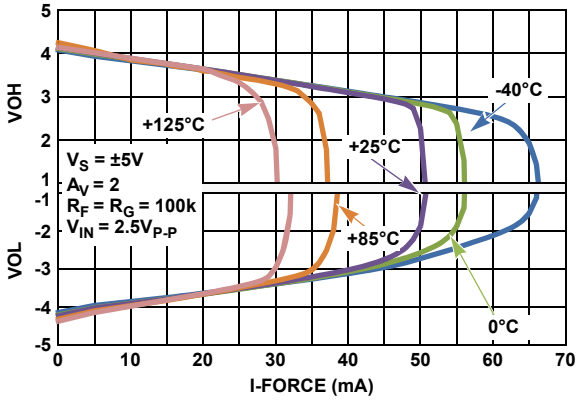


FIGURE 25. OUTPUT VOLTAGE (V_{OUT}) vs OUTPUT CURRENT (I_{OUT}) vs TEMPERATURE, V_S = ±5V

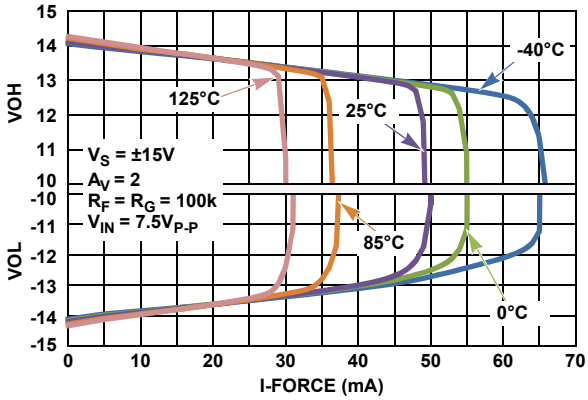


FIGURE 26. OUTPUT VOLTAGE (V_{OUT}) vs OUTPUT CURRENT (I_{OUT}) vs TEMPERATURE, V_S = ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

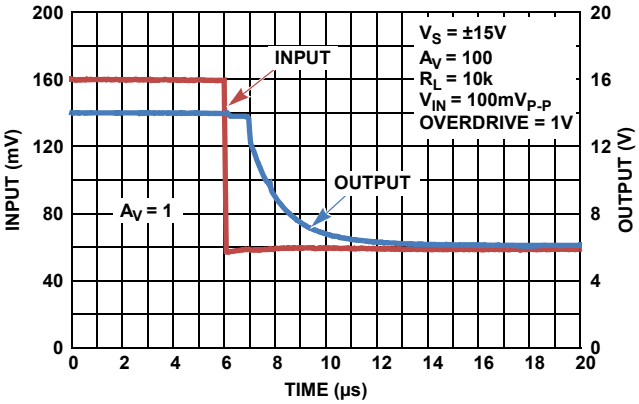


FIGURE 27. POSITIVE OUTPUT OVERLOAD RECOVERY TIME

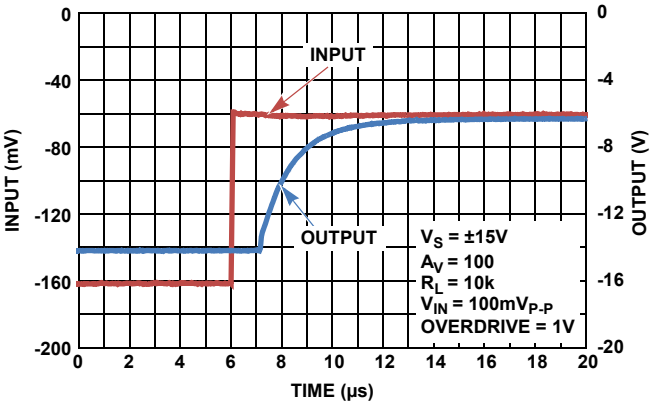


FIGURE 28. NEGATIVE OUTPUT OVERLOAD RECOVERY TIME

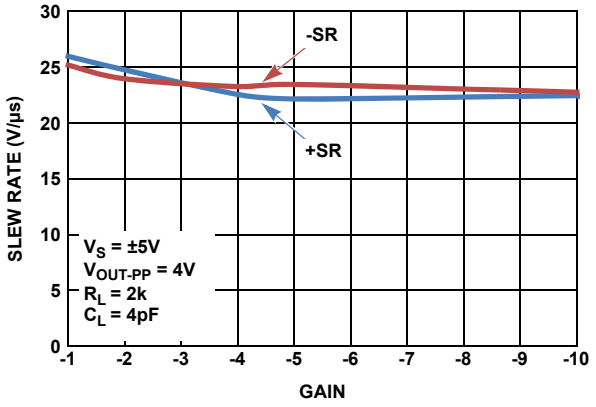


FIGURE 29. SLEW RATE vs INVERTING CLOSED LOOP GAIN, V_S = ±5V

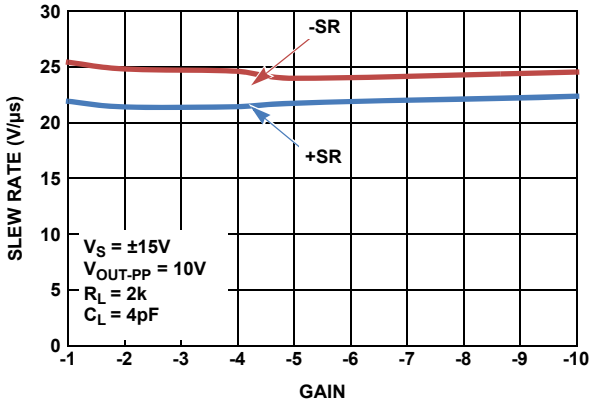


FIGURE 30. SLEW RATE vs INVERTING CLOSED LOOP GAIN, V_S = ±15V

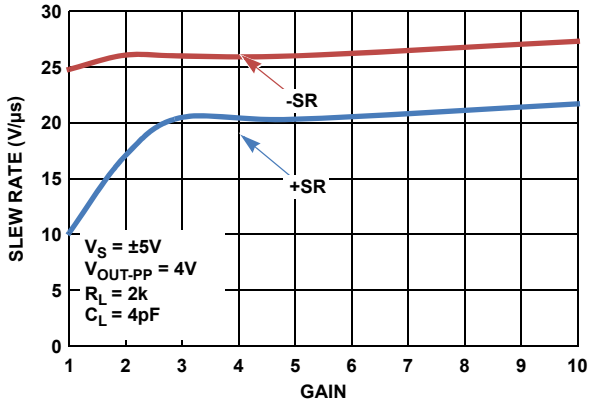


FIGURE 31. SLEW RATE vs NON-INVERTING CLOSED LOOP GAIN, V_S = ±5V

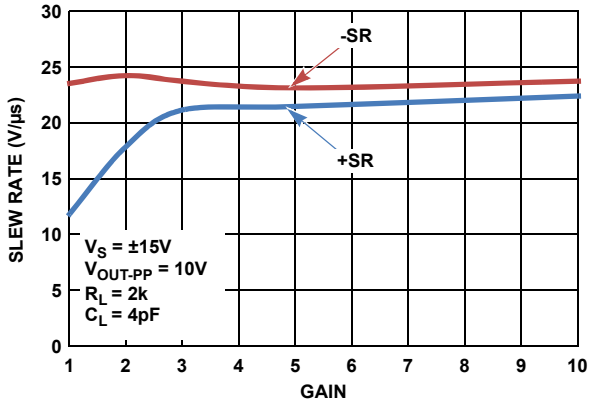


FIGURE 32. SLEW RATE vs NON-INVERTING CLOSED LOOP GAIN, V_S = ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, RL = Open, T = +25°C, unless otherwise specified. **(Continued)**

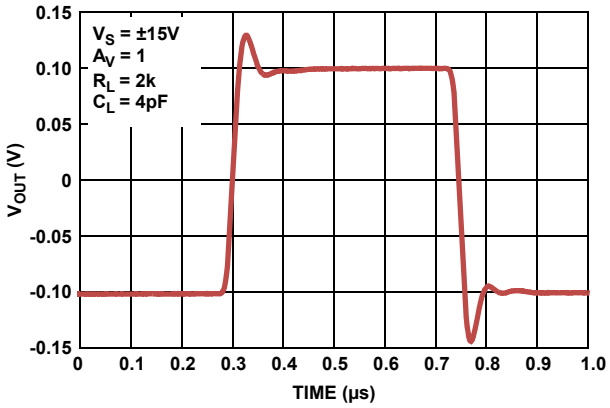


FIGURE 33. SMALL SIGNAL TRANSIENT RESPONSE

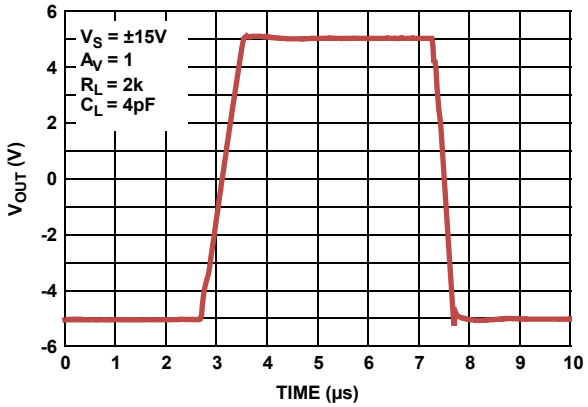


FIGURE 34. LARGE SIGNAL UNITY GAIN TRANSIENT RESPONSE

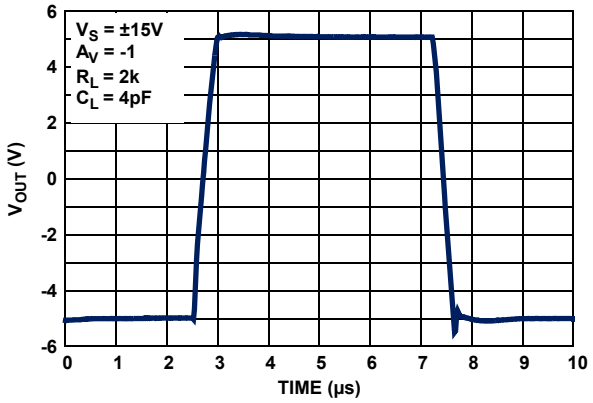


FIGURE 35. LARGE SIGNAL 10V STEP RESPONSE A_V = -1

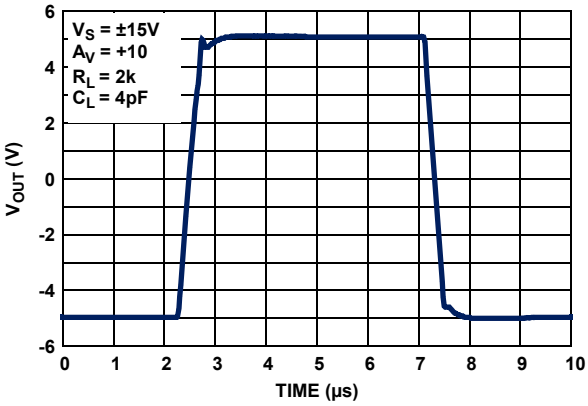


FIGURE 36. LARGE SIGNAL 10V STEP RESPONSE A_V = +10

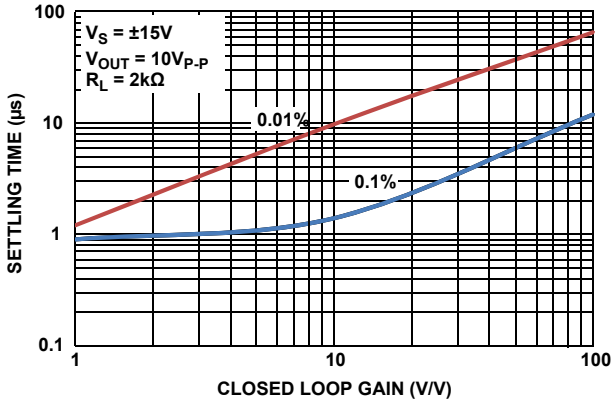


FIGURE 37. SETTLING TIME (t_S) vs CLOSED LOOP GAIN

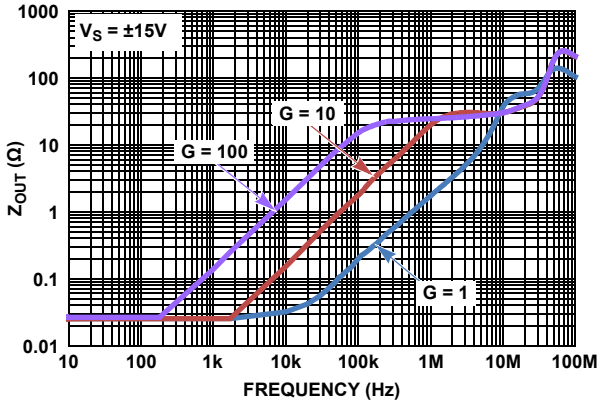


FIGURE 38. Z_{OUT} vs FREQUENCY

Applications Information

Functional Description

The ISL28110 and ISL28210 are single and dual 12.5 MHz precision JFET input op amps. These devices are fabricated in the PR40 Advanced SOI bipolar-JFET process to ensure latch-free operation. The precision JFET input stage provides low input offset voltage (300µV max @ +25°C), low input voltage noise (6nV/√Hz), and input current noise that is very low with virtually no 1/f component. A high current complementary NPN/PNP emitter-follower output stage provides high slew rate and maintains excellent THD+N performance into heavy loads (0.0003% @ $10V_{P-P}$ @ 1kHz into 600Ω).

Operating Voltage Range

The devices are designed to operate over the 9V (±4.5V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). The JFET input stage maintains high impedance over a maximum input differential voltage range of ±33V. Internal ESD protection diodes clamp the non-inverting and inverting inputs to one diode drop above and below the V+ and V- the power supply rails ("Pin Descriptions" on page 2, CIRCUIT 1).

Input ESD Diode Protection

The JFET gate is a reverse-biased diode with >33V reverse breakdown voltage which enables the device to function reliably in large signal pulse applications without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. No special input signal restrictions are needed for power supply operation up to ±15V, and input signal distortion caused by nonlinear clamps under high slew rate conditions are avoided. For power supply operation greater than ±16V (>32V), the internal ESD clamp diodes alone cannot clamp the maximum input differential signal to the power supply rails without the risk of exceeding the 33V breakdown of the JFET gate. Under these conditions, differential input voltage limiting is necessary to prevent damage to the JFET input stage.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current limiting resistors may be needed at each input terminal (see Figure 39 $R_{IN}+$, $R_{IN}-$) to limit current through the power supply ESD diodes to 20mA.

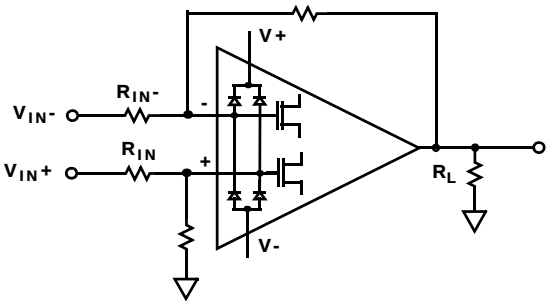


FIGURE 39. INPUT ESD DIODE CURRENT LIMITING

JFET Input Stage Performance

The ISL28110, ISL28210 JFET input stage has the linear gain characteristics of the MOSFET but can operate at high frequency with much lower noise. The reversed-biased gate PN gate junction has significantly lower gate capacitance enabling input slew rates that rival op amps using bipolar input stages. The added advantage for high impedance, precision amplifiers is the lack of a significant 1/f component of current noise (Figures 11, 12) as there is virtually no gate current.

The input stage JFETs are bootstrapped to maintain a constant JFET drain to source voltage which keeps the JFET gate currents and input stage frequency response nearly constant over the common mode input range of the device. These enhancements provide excellent CMRR, AC performance and very low input distortion over a wide temperature range. The common mode input performance for offset voltage and bias current is shown in FIGURE 40. Note that the input bias current remains low even after the maximum input stage common mode voltage is exceeded (as indicated by the abrupt change in input offset voltage).

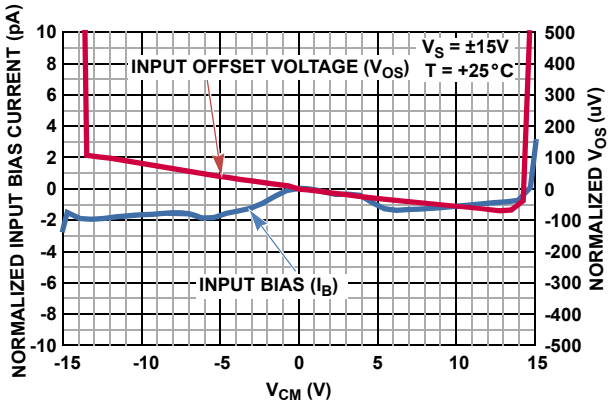


FIGURE 40. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

Output Drive Capability

The complementary bipolar emitter follower output stage features low output impedance (Figure 40) and is capable of substantial current drive over the full temperature range (Figures 25, 26) while driving the output voltage close to the supply rails. The output current is internally limited to approximately ±50mA at +25°C. The amplifiers can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28110 and ISL28210 are immune to output phase reversal, out to 0.5V beyond the rail (V_{ABS} MAX) limit. Beyond these limits, the device is still immune to reversal to 1V beyond the

rails but damage to the internal ESD protection diodes can result unless these input currents are limited.

Maximizing Dynamic Signal Range

The amplifiers maximum undistorted output swing is a figure of merit for precision, low distortion applications. Audio amplifiers are a good example of amplifiers that require low noise and low signal distortion over a wide output dynamic range. When these applications operate from batteries, raising the amplifier supply voltage to overcome poor output voltage swing has the penalty of increased power consumption and shorter battery life. Amplifiers whose input and output stages can swing closest to the power supply rails while providing low noise and undistorted performance, will provide maximum useful dynamic signal range and longer battery life.

Rail-to-rail input and output (RRIO) amplifiers have the highest dynamic signal range but their added complexity degrades input noise and amplifier distortion. Many contain two input pairs, one pair operating to each supply rail. The trade-offs for these are increased input noise and distortion caused by non-linear input bias current and capacitance when amplifying high impedance sources. Their rail-to-rail output stages swing to within a few millivolts of the rail, but output impedances are high so that their output swing decreases and distortion increases rapidly with increasing load current. At heavy load currents the maximum output voltage swing of RRO op amps can be lower than a good emitter follower output stage.

The ISL28110 and ISL28210 low noise input stage and high performance output stage are optimized for low THD+N into moderate loads over the full -40°C to +125°C temperature range. Figures 17 and 18 show the 1kHz THD+N unity gain performance vs output voltage swing at load resistances of 2kΩ and 600Ω. Figure 41 shows the unity-gain THD+N performance driving 600Ω from ±5V supplies.

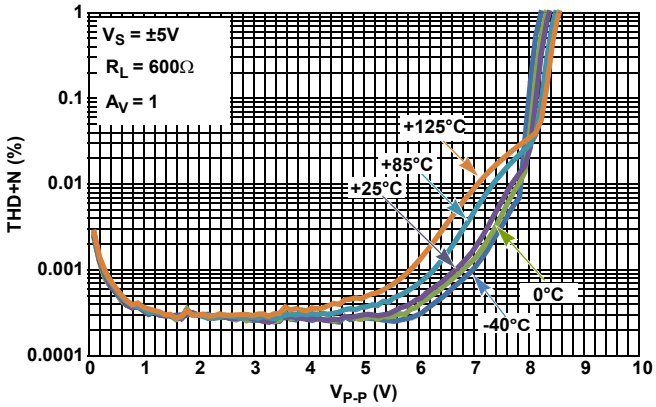


FIGURE 41. UNITY-GAIN THD+N vs OUTPUT VOLTAGE vs TEMPERATURE AT V_S = ±5V FOR 600Ω LOAD

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/13/10	FN6639.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28110, ISL28210

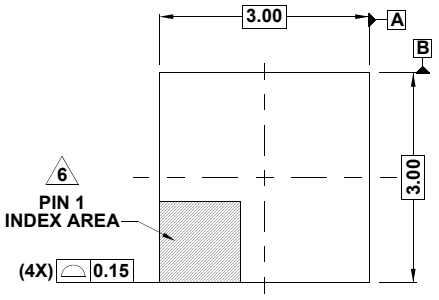
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

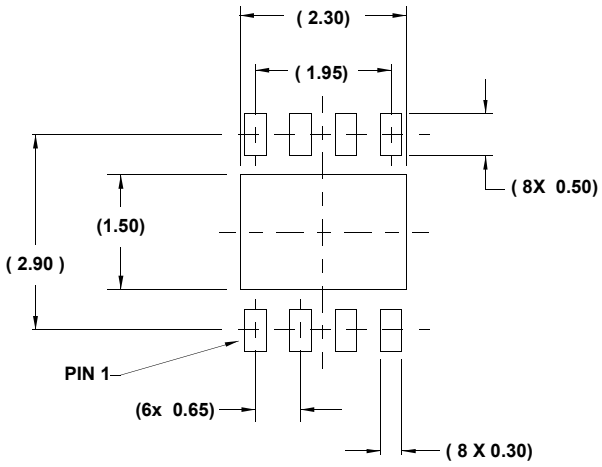
Package Outline Drawing

L8.3x3A

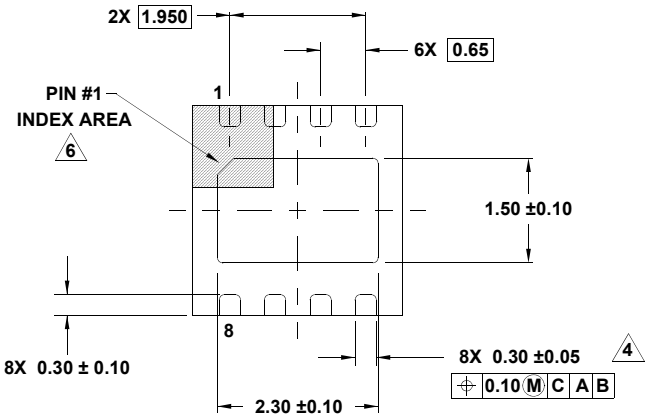
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



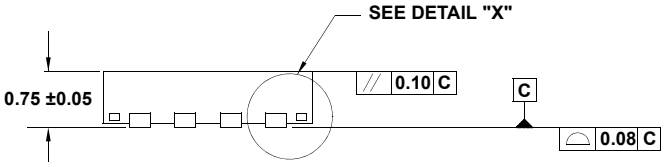
TOP VIEW



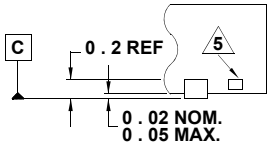
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

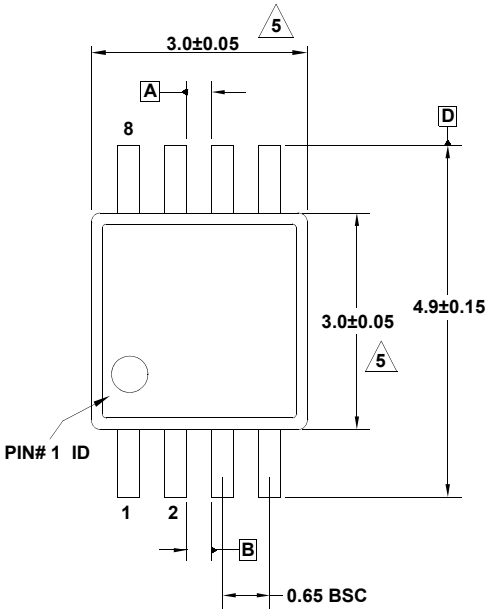
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

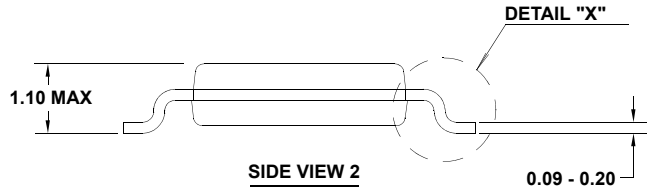
Package Outline Drawing

M8.118

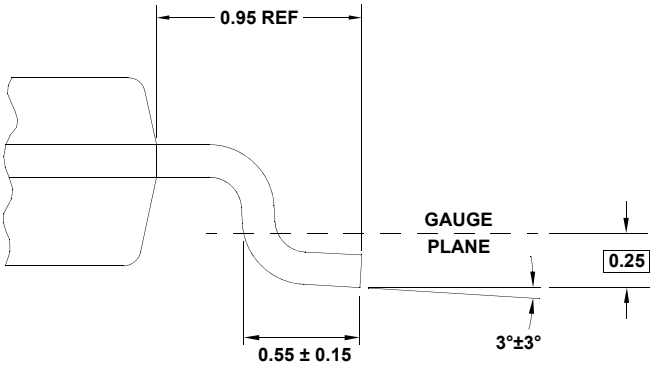
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



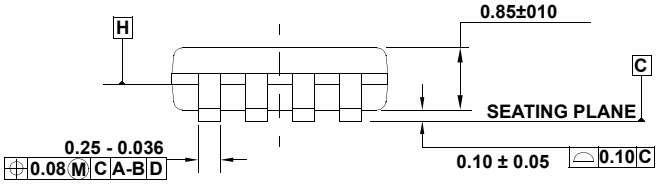
TOP VIEW



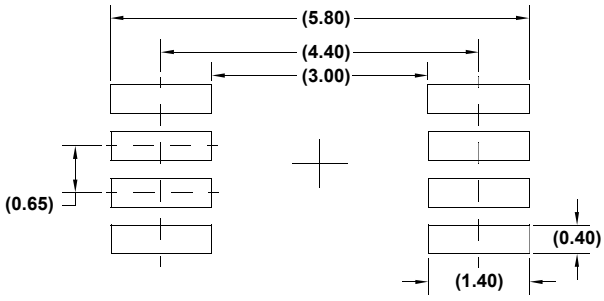
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

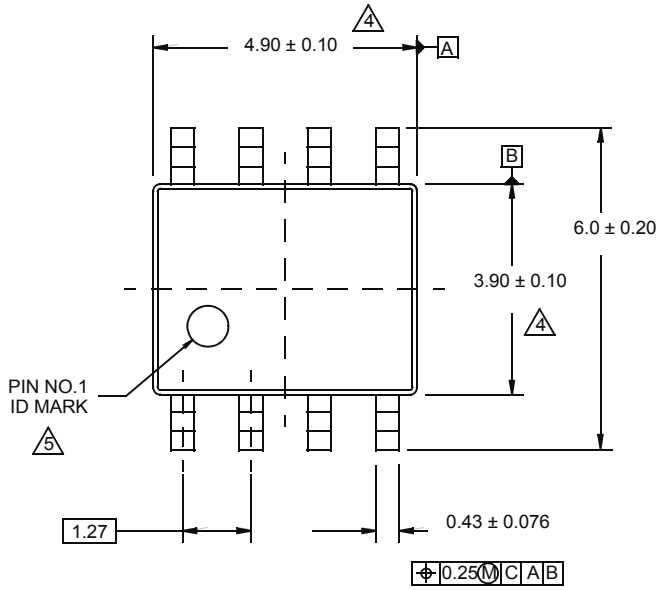
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

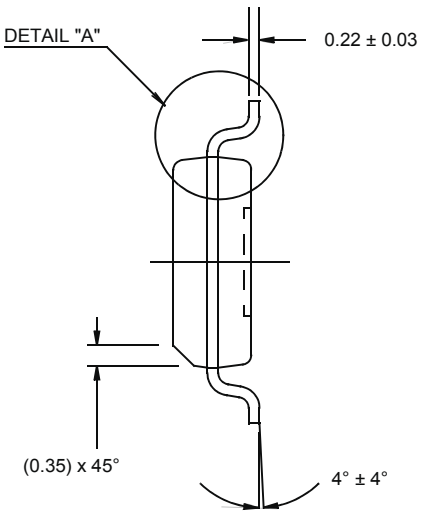
Package Outline Drawing

M8.15E

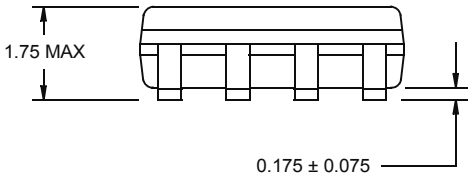
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



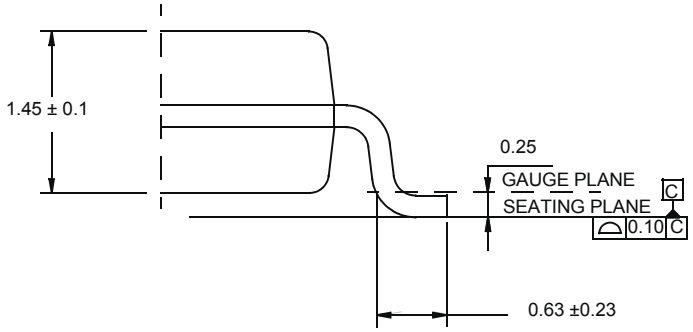
TOP VIEW



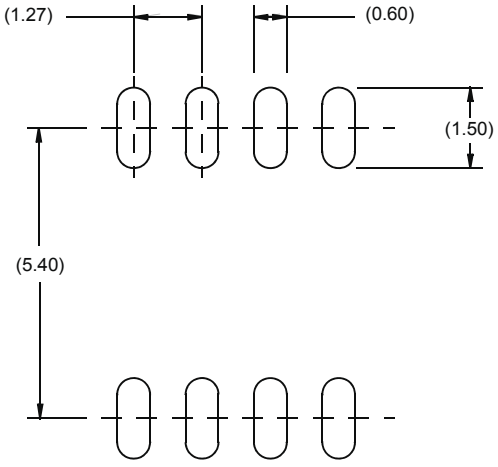
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.