Integrated Device Technology, Inc.

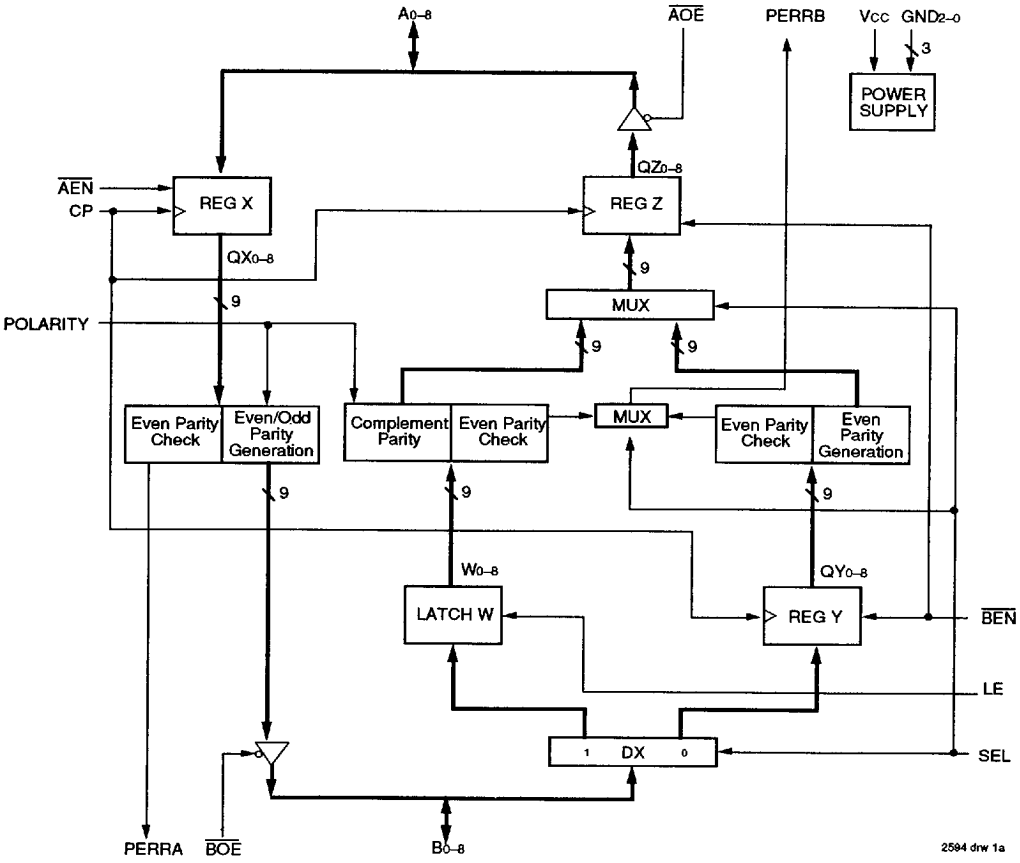
FAST CMOS OCTAL REGISTER TRANSCEIVER WITH PARITY

PRELIMINARY
IDT73210/A/B
IDT73211/A/B

FEATURES

- Two bidirectional 9-bit I/O ports
- Available in standard, A, and B speed grades
- High output drive capability: 64mA (Com'l), 48mA (Mil)
- Low CMOS power: 0.1mW typical
- Parity Generation/Checking in both directions with polarity control for A-to-B direction
- 73210/211 Single-level pipeline register from Port A to Port B
- 73210 Two level pipeline register from Port B to Port A
- 73211 Single level pipeline register from Port B to Port A
- Military product compliant to MIL-STD-883, Class B
- Available in 32-pin sidebraze DIP and surface mount 32-pin SOJ packages

IDT73210 FUNCTIONAL BLOCK DIAGRAM



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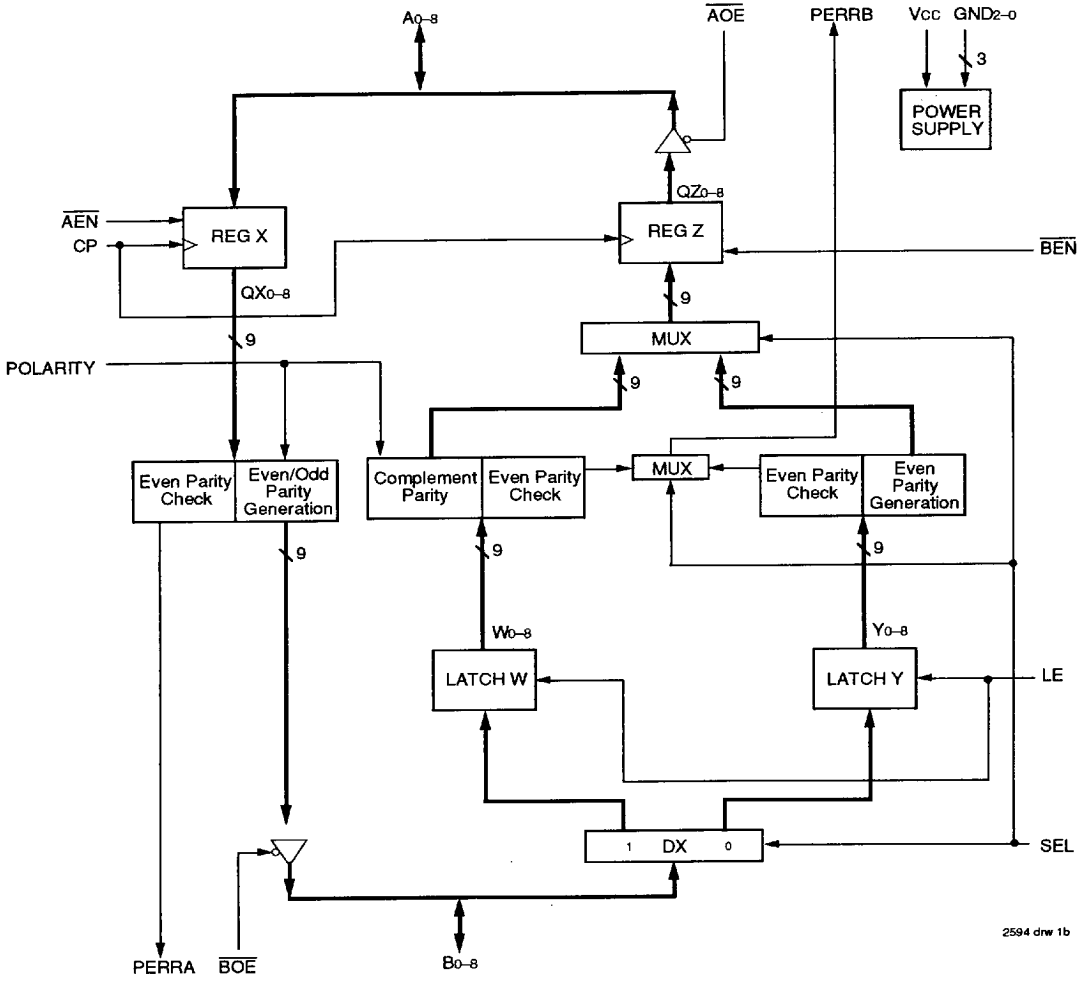
IDT73211 FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The IDT73210/211 Octal Register Transceivers with parity, are designed for high performance systems requiring bidirectional data transfer between two busses with parity support. These transceivers are offered in several speed grades to support data transfer in systems with up to 40 MHz data rates. The output buffers have high drive capability for high capacitance driving and low impedence line driving.

The IDT73210/211 Register Transceivers provide Even/Odd parity generation from Port A to Port B and Even parity generation from Port B to Port A. Even parity checking with ERROR flag is provided in both directions. The Even/Odd parity and Generate/Check options can be dynamically reconfigured.

The IDT73210/211 can be used as an interface between a cache memory and the main memory in any RISC or CISC microprocessor system. The pipelining feature makes these devices ideal for use as Read/Write buffers. They can also be used as high speed general purpose registers in any parity based system. In this application, the IDT73210/211 replace the equivalent of an FCT52 Bidirectional Register and two F280 parity generator/checker devices.

DETAILED FUNCTIONAL DESCRIPTION

Port A to Port B Path (IDT73210 and IDT73211) is comprised of a register (X), an even/odd parity generator and an even parity checker. The input data is on the A_{0-8} lines. When $\overline{AEN}$ is low, A_{0-8} is latched into Register X on the low-to-high CP transition. Even parity of the latched data is checked. If PERRA goes high, a parity error has occurred. A new parity bit, B_8, is generated. The output data bus is B_{0-8} and is enabled when $\overline{BOE}$ is low.

Port B to Port A Path (IDT73210) is comprised of a latch (W), two registers (Y and Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Register Y on the low-to-high CP transition, when $\overline{BEN}$ is low. Even parity of the registered data is checked. If PERRB goes high, a parity error has occurred. Even parity (QY_8) is generated on the contents in Register Y. When $\overline{BEN}$ is low, the contents of register Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a two clock cycle latency.

Port B to Port A Path (IDT73211) is comprised of latch (W), latch (Y), register (Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Latch Y when LE is high. Latch Y is closed when LE is low. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. Even parity (Y_8) is generated on the contents in Latch Y. When $\overline{BEN}$ is low, the contents of Latch Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a one clock cycle latency.

The power pins are Vcc and GND_{0-2}. GND_0 is internal quiet ground, GND_1 is Port B ground and GND_2 is Port A ground.

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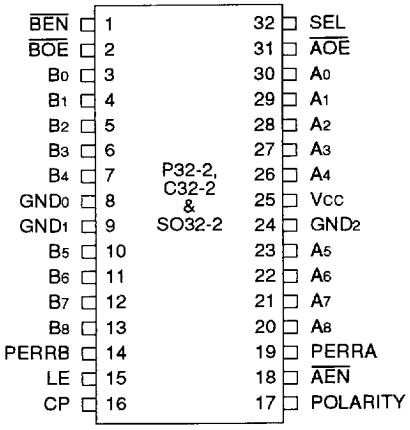
PIN CONFIGURATIONS[1]



DIP/SOJ
TOP VIEW

NOTE:
1. GND_0 is internal quiet ground
   GND_1 is B Port ground
   GND_2 is A Port ground

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{0-8}	I/O	Data Port A.
$\overline{AEN}$	I	Clock enable (active low) for the register X.
$\overline{AOE}$	I	3-state output enable for Port A.
B_{0-8}	I/O	Data Port B.
$\overline{BEN}$	I	Clock enable (active low) for the registers Y and Z.
$\overline{BOE}$	I	3-state output enable for Port B.
LE	I	Latch enable input for Latch Y/Latch W of Port B. The Latch Y/Latch W is open when LE is high. Data is latched on the high-to-low transition of LE.
SEL	I	Input selection for Port B. SEL = 0 Register Y (73210); SEL = 1 Latch W SEL = 0 Latch Y (73211);
POLARITY	I	Polarity selection input. **Polarity** — **A to B Direction** — **B to A Direction** 0 — EVEN — Pass Parity 1 — ODD — Complement Parity
PERRA	O	Parity output error for Port A.
PERRB	O	Parity output error for Port B.
CP	I	Input clock.
V_{CC}		+5 volts.
GND_{0-2}		Ground.

2594 tbl 01

OPERATING MODES SUMMARY

IDT73210/11 A TO B DIRECTION, SEL = X

Input	Reg. X	PERRA	Output (B8)	Output B0–8
A0–8	A0–8 → QX0–8 (CP = Lo to Hi) ($\overline{AEN}$ = 0)	Result of even parity check	Even/odd parity bit B8 = POLARITY XOR Even parity generate from QX0–7	QX0–8 → B0–8 ($\overline{BOE}$ = 0)

2594 tbl 02

IDT73210/1 B TO A DIRECTION WHEN SEL = 1

Input	Latch W	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → W0–8 (LE = 1)	Result of even parity check	Bit complemented by POLARITY (Even/odd parity translation)	W0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = POLARITY XOR W8	QZ0–8 → A0–8 ($\overline{AOE}$ = 0)

2594 tbl 03

IDT73210 B TO A DIRECTION WHEN SEL = 0

Input	Reg. Y	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → QY0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	Result of even parity check	Even parity generated bit	QY0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = Even parity generated from QY0–7	QZ0–8 → A0–8 ($\overline{AOE}$ = 0)

2594 tbl 04

IDT73211 B TO A DIRECTION WHEN SEL = 0

Input	Latch Y	PERRB	Reg. Z (QZ8)	Reg. Z QZ0–8	Output (A8)	Output A0–8
B0–8	B0–8 → Y0–8 (LE = 1)	Result of even parity check	Even parity generated bit	Y0–8 → QZ0–8 (CP = Lo to Hi) ($\overline{BEN}$ = 0)	A8 = Even parity generated from Y0–7	QZ0–8 → A0–8 ($\overline{AOE}$ = 0)

2594 tbl 05

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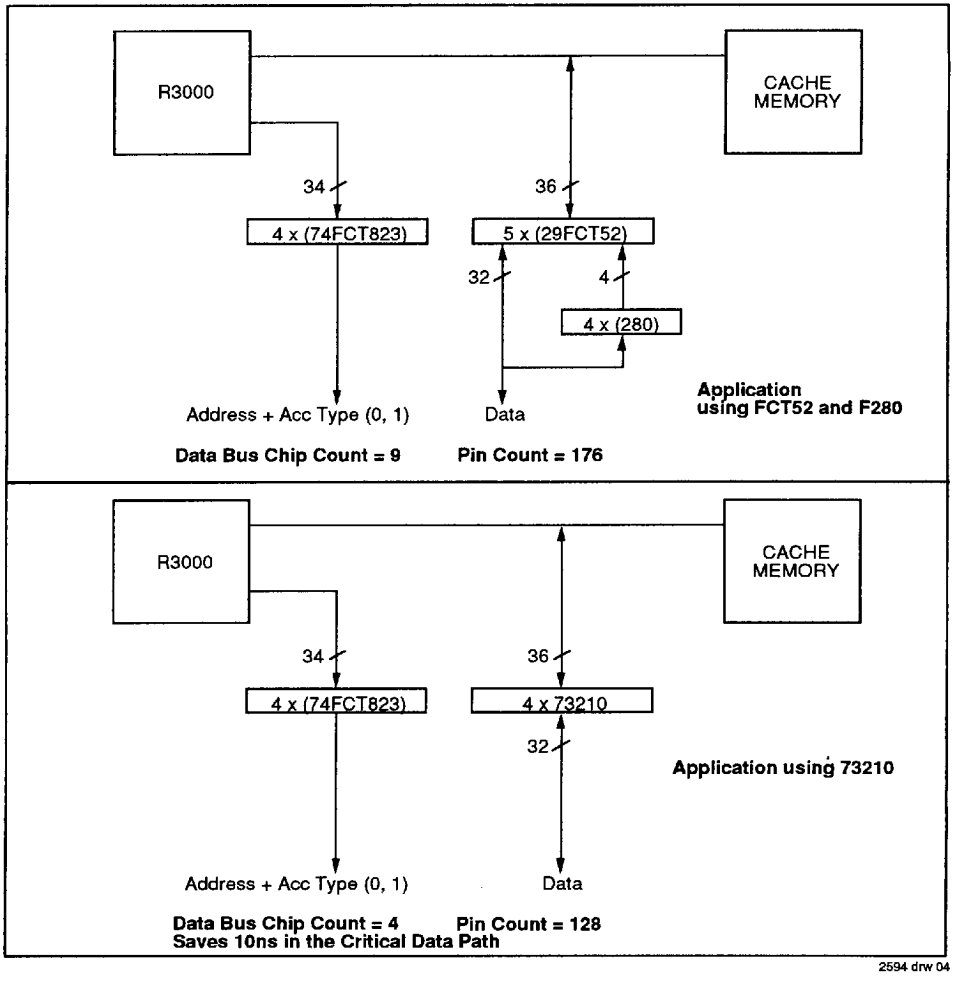

Figure 1. R3000 System with No Parity Support in Main Memory

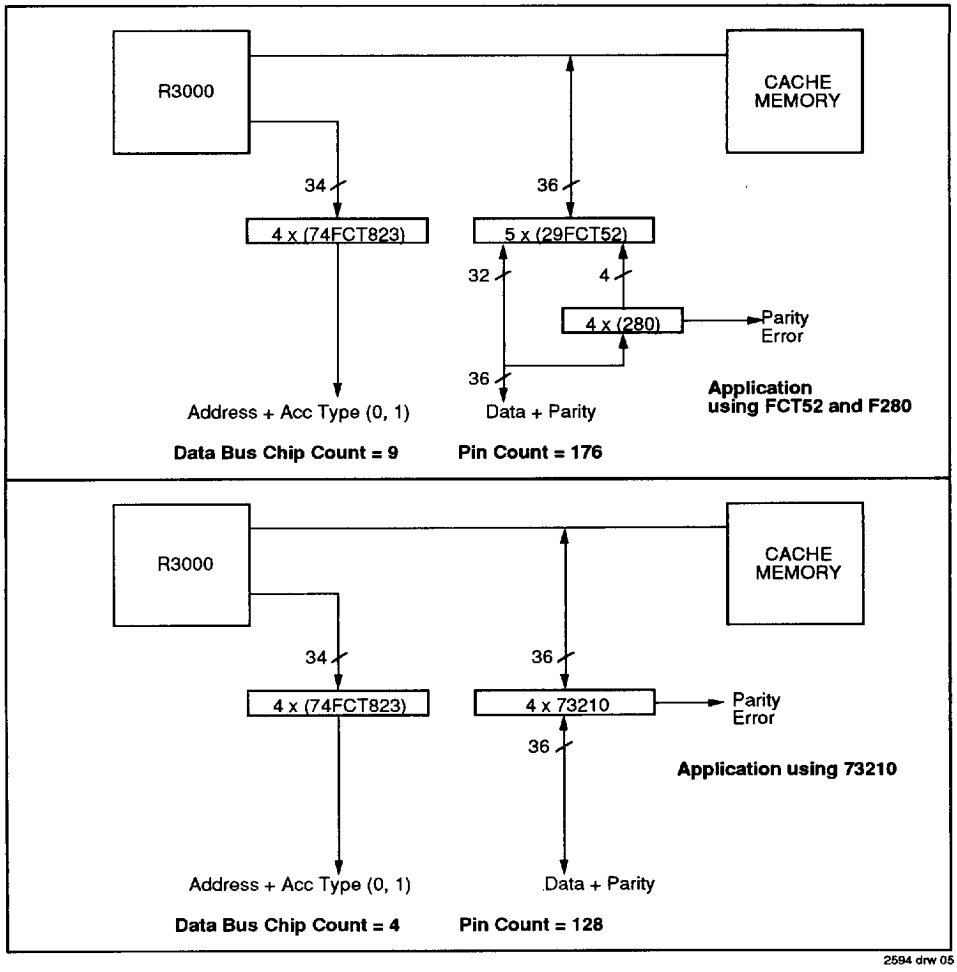

Figure 2. R3000 System with Parity Support in Main Memory

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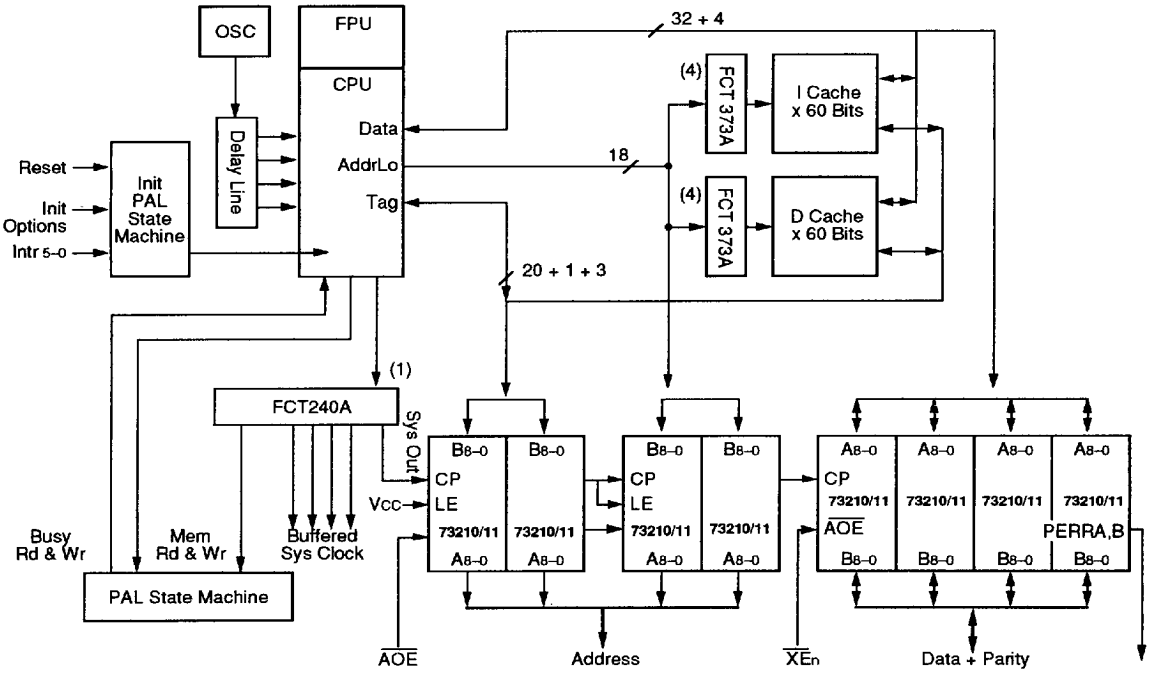

Figure 3. Read and Write Buffers Using Eight IDT73210/11

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.2	1.5	W
I_{OUT}	Total Output Current	200	250	mA

NOTE: 2594 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF
$C_{I/O}$	Input – Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2594 tbl 07

1. This parameter is not production tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.		Except I/O	—	—	10	µA
		V_I = 2.7V		I/O pins	—	—	20	
I_{IL}	Input LOW Current	V_{CC} = Max.		Except I/O	—	—	-10	µA
		V_I = 0.5V		I/O pins	—	—	-20	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA			—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		PERRA, PERRB	-30	—	-150	mA
				A_{0-8}, B_{0-8}	-20	—	-75	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.		I_{OH} = −12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	A_{0-8}	I_{OL} = 48mA MIL.	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	B_{0-8}	I_{OL} = 64mA COM'L.				
		V_{CC} = Min.	PERRA	I_{OL} = 20mA MIL.				
		V_{IN} = V_{IH} or V_{IL}	PERRB	I_{OL} = 24mA COM'L.				
V_H	Input Hysteresis for CP only	V_{CC} = 5V			—	200	—	mV

NOTES:
2594 tbl 09

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, not production tested.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 millisecond.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.02	2.0	mA
I_{CCQT}	Quiescent Power Supply Current	V_{CC} = Max.	COM'L.	—	0.3	1.0	mA/
	TTL Inputs HIGH	V_{IN} = 3.4[3]	MIL.	—	0.3	1.5	Input
I_{CCD}	Dynamic Power Supply Current[3]	V_{CC} = Max. Outputs Disabled One input toggling 50% Duty Cycle	V_{IN} = V_{CC} or GND	—	0.25	0.50	mA/ MHz/ Input
I_C	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 10 MHz 50% Duty Cycle f_i = 5 MHz	V_{IN} = V_{CC} or GND	—	18	30	mA

NOTES:
2594 tbl 08

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CCQC} + I_{CCQT} $D_H N_T$ + I_{CCD} (f_{CP}/2 + $f_i N_i$)
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP}= Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input frequency
   N_i = Number of Inputs at f_i
   f_{CP} = Clock frequency for register devices (zero for non-register devices)
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Commercial: T_A = 0°C to +70°C; V_{CC} = 5V ± 5%
Military: T_A = -55°C to +125°C; V_{CC} = 5V ± 10%,
C_L = 50pF; R_L = 500Ω

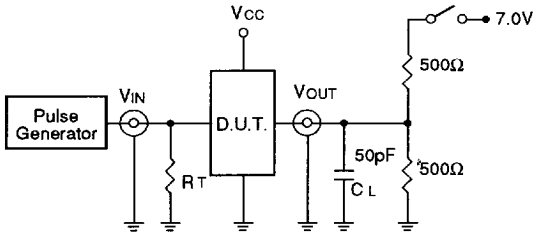
Parameter	Description	IDT73210/11				IDT73210A/11A				IDT73210B/11B				Unit
		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)	2.0	9.0	2.0	11.0	2.0	7.2	2.0	9.0	2.0	6.0	2.0	7.5	ns
t_{PHL} t_{PLH}	Propagation Del Clock to B_{0-8} ($\overline{BOE}$ = Low)	2.0	10.5	2.0	12.0	2.0	9.0	2.0	10.5	2.0	7.5	2.0	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay CP to PERRA, PERRB	2.0	10.5	2.0	12.0	2.0	9.0	2.0	10.5	2.0	7.5	2.0	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay POLARITY to B_8	2.0	9.5	2.0	11.0	2.0	8.5	2.0	9.5	2.0	7.0	2.0	8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B_{0-8} to PERRB LE = High	2.0	10.0	2.0	11.5	2.0	9.0	2.0	10.0	2.0	7.5	2.0	9.0	ns
t_S	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time to CP — A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.0	—	1.5	—	1.0	—	1.5	—	1.0	—	1.5	—	ns
	Hold Time to CP — POLARITY, SEL	1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP	1.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_S	Set-up Time B_{0-8} to LE	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_S	Set-up Time B_{0-8} to CP (Reg Z); LE = High	4.5	—	5.0	—	3.5	—	4.5	—	3.0	—	3.5	—	ns
t_H	Hold Time B_{0-8} to CP (Reg Z); LE = High	1.5	—	3.0	—	1.5	—	2.5	—	1.5	—	2.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	2.0	8.0	2.0	10.0	2.0	7.0	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	2.0	7.5	2.0	9.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.5	ns
t_{PWH} t_{PWL}	Clock Pulse Width High[2] Clock Pulse Width Low[2]	5.0 5.0	— —	5.0 5.0	— —	5.0 5.0	— —	5.0 5.0	— —	5.0 5.0	— —	5.0 5.0	— —	ns ns

NOTES:
1. All minimum limits for propagation delays are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

2594 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2594 drw 09

SWITCH POSITION

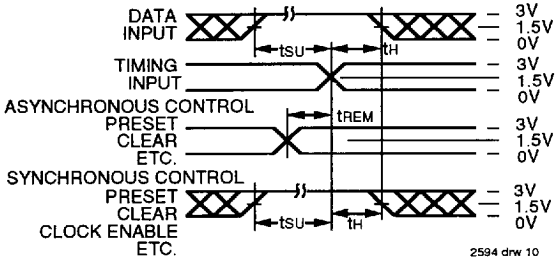
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2594 lnk 13

DEFINITIONS:

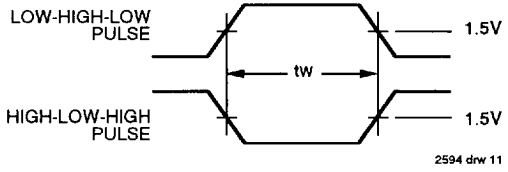
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



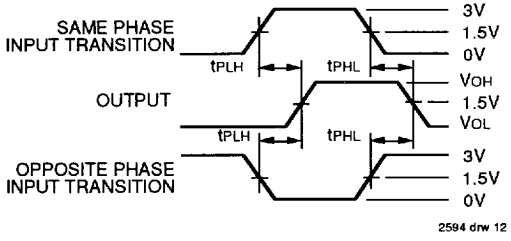
2594 drw 10

PULSE WIDTH



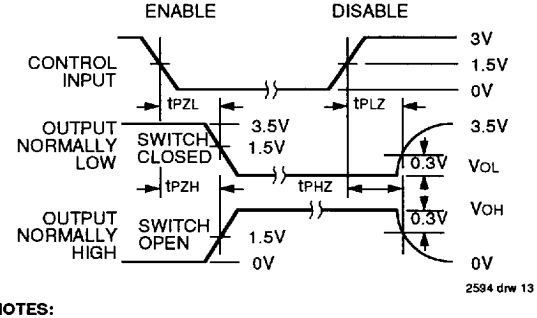
2594 drw 11

PROPAGATION DELAY



2594 drw 12

ENABLE AND DISABLE TIMES



2594 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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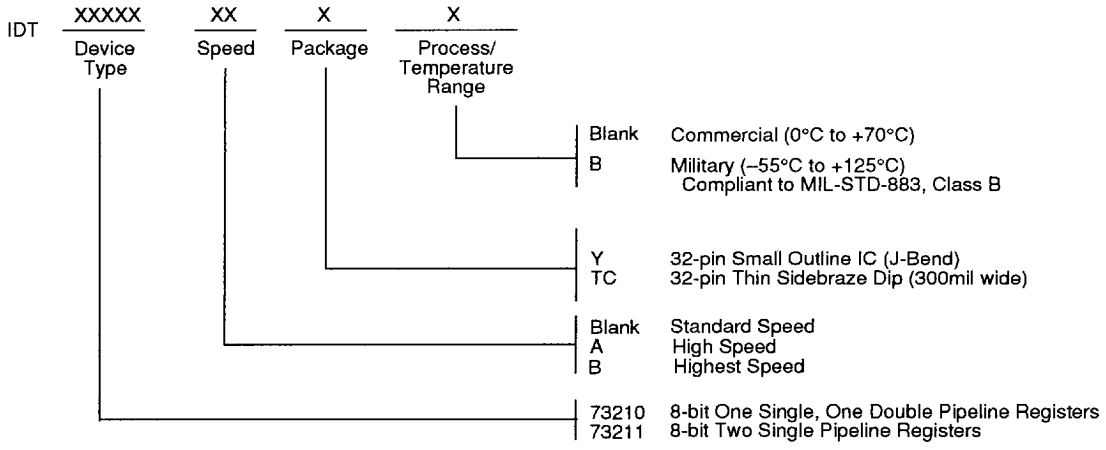
ORDERING INFORMATION



2594 drw 14