Agilent Technologies
Innovating the HP Way

Surface Mount PIN Diodes in SOT-323 (SC-70 3-Lead)

Technical Data

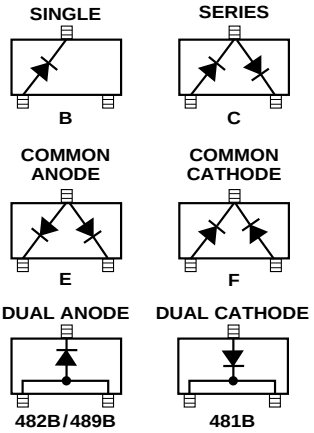
HSMP-381B/C/E/F
HSMP-386B/C/E/F
HSMP-389B/C/E/F
HSMP-481B, -482B, -489B

Features

- **Diodes Optimized for:**
  Low Current Switching
  Low Distortion Attenuating
  Ultra-Low Distortion Switching
  Microwave Frequency Operation
- **Surface Mount SOT-323 (SC-70)Package**
  Single and Pair Versions
  Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate***

* For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description/Applications

The HSMP-381B/C/E/F series is specifically designed for low distortion attenuator applications. The HSMP-386B/C/E/F series is a general purpose PIN diode designed for low current attenuators and low cost switches. The HSMP-389B/C/E/F series is optimized for switching applications where low resistance at low current, and low capacitance are required.

The HSMP-48XB series is special products featuring ultra low parasitic inductance in the SOT-323 package, specifically designed for use at frequencies which are much higher than the upper limit for conventional SOT-323 PIN diodes. The HSMP-481B diode is a low distortion attenuating PIN designed for operation to 3 GHz. The HSMP-482B diode is ideal for limiting and low inductance switching applications up to 1.5 GHz. The HSMP-489B is optimized for low current switching applications up to 3 GHz.

Absolute Maximum Ratings[1], T_C = + 25°C

Symbol	Parameter	Unit	Absolute Maximum
I_f	Forward Current (1 µs Pulse)	Amp	1
P_{iv}	Peak Inverse Voltage	V	Same as V_{BR}
T_J	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	300

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = 25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications, T_C = +25°C, each diode

PIN Attenuator Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Resistance R_T (Ω)	Maximum Total Capacitance C_T (pF)	Minimum High Resistance R_H (Ω)	Maximum Low Resistance R_L (Ω)
381B 381C 381E 381F	E0 E2 E3 E4	B C E F	Single Series Common Anode Common Cathode	100	3.0	0.35	1500	10
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_R = 0.01 mA f = 100 MHz	I_F = 20 mA f = 100 MHz

PIN General Purpose Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Typical Total Resistance R_T (Ω)		Typical Total Capacitance C_T (pF)
386B 386C 386E 386F	L0 L2 L3 L4	B C E F	Single Series Common Anode Common Cathode	50	3.0	1.5*	0.20
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 10 mA f = 100 MHz I_F = 100 mA*		V_R = 50 V f = 1 MHz

PIN Switching Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Resistance R_T (Ω)	Maximum Total Capacitance C_T (pF)
389B 389C 389E 389F	G0 G2 G3 G4	B C E F	Single Series Common Anode Common Cathode	100	2.5	0.30
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 5 mA f = 100 MHz	V_R = 5 V f = 1 MHz

Electrical Specifications, T_C = +25°C, each diode, continued

Typical Parameters

Part Number HSMP-	Total Resistance R_T (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance (pF)
381A Series 386A Series 389A Series	75 22 3.8	1500 500 200*	300 80 —	0.27 0.20 —
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA T_R = 250 mA I_F = 10 mA* I_R = 6 mA*	V_R = 10 V I_F = 20 mA 90% Recovery	50 V

Note:
1. Package marking code is laser marked.

High Frequency (Low Inductance, 500 MHz–3 GHz PIN Diodes

Part Number HSMP-	Package Marking Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)	Application
481B	EB	Dual Cathode	100	3.0	0.35	0.4	1.0	Attenuator
482B	FA	Dual Anode	50	0.6*	0.75*	1.0	1.0*	Limiter
489B	GA	Dual Anode	100	2.5**	0.33**	0.375*	1.0	Switch
Test Conditions			V_R = V_{BR} Measure I_R ≤ 10 μA	I_F = 100 mA I_F = 10 mA* I_F = 5 mA**	V_R = 50 V f = 1 MHz V_R = 20 V* V_R = 5 V**	V_R = 50 V f = 1 MHz V_R = 5 V*	f = 500 MHz–3 GHz V_R = 20 V*	

Typical Performance, T_C = 25°C

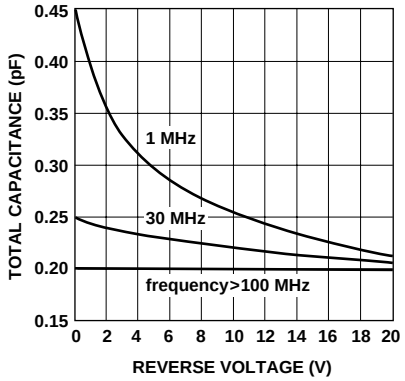


Figure 1. RF Capacitance vs. Reverse Bias, HSMP-381B/C/E/F Series.

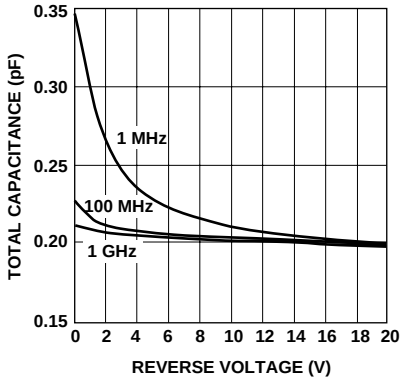


Figure 2. RF Capacitance vs. Reverse Bias, HSMP-386B/C/E/F Series.

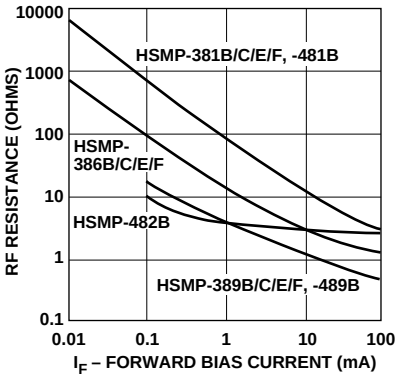


Figure 3. Total RF Resistance at 25° C vs. Forward Bias Current.

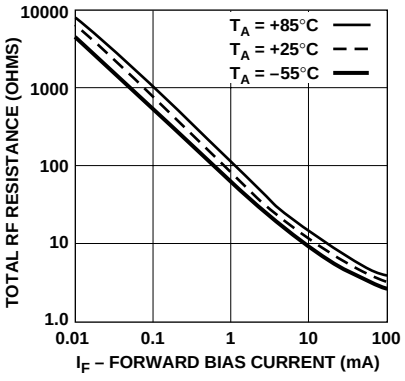


Figure 4. RF Resistance vs. Forward Bias Current for HSMP-381B/C/E/F Series and HSMP-481B.

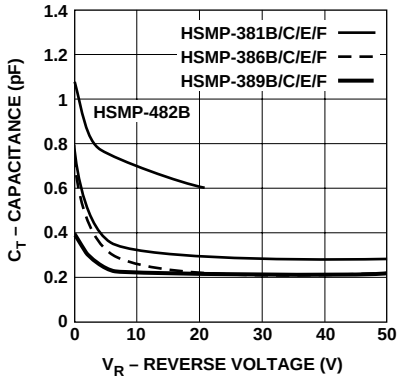


Figure 5. Capacitance vs. Reverse Voltage at 1 MHz.

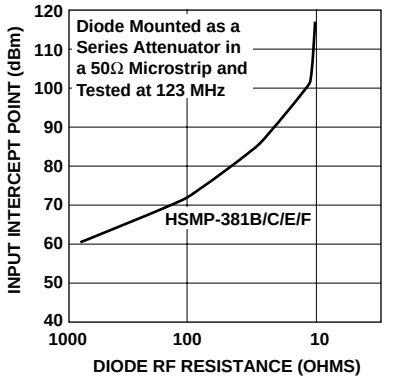


Figure 6. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuator Diodes.

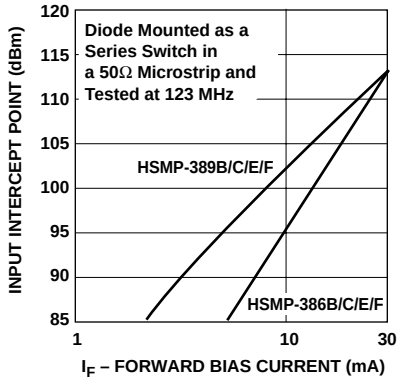


Figure 7. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

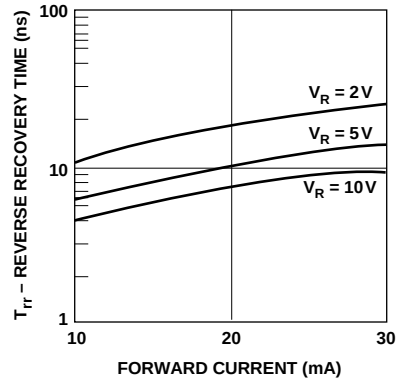


Figure 8. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-482B.

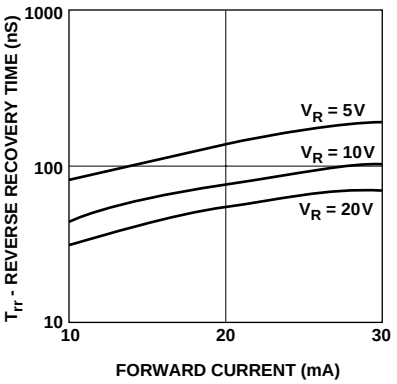


Figure 9. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-386B/C/E/F Series.

Typical Performance, T_C = 25°C

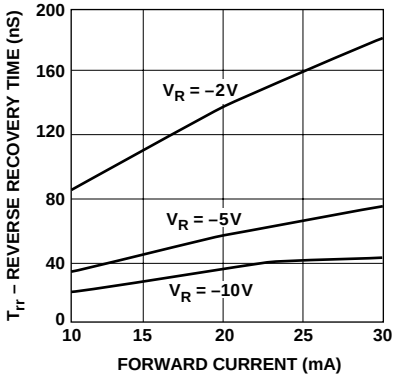


Figure 10. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-389B/C/E/F Series.

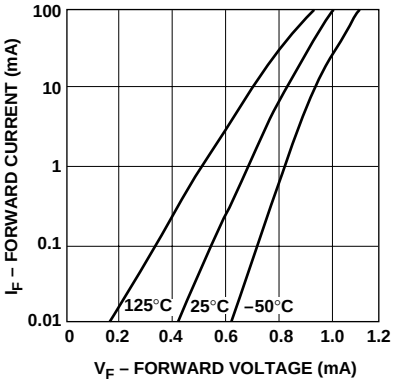


Figure 11. Forward Current vs. Forward Voltage. HSMP-381B/C/E/F Series and HSMP-481B.

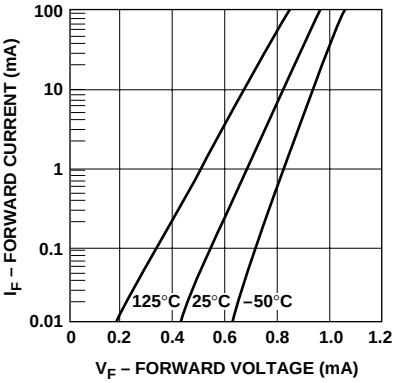


Figure 12. Forward Current vs. Forward Voltage. HSMP-482B.

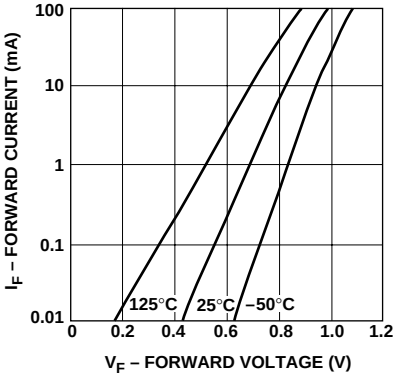


Figure 13. Forward Current vs. Forward Voltage. HSMP-386B/C/E/F Series.

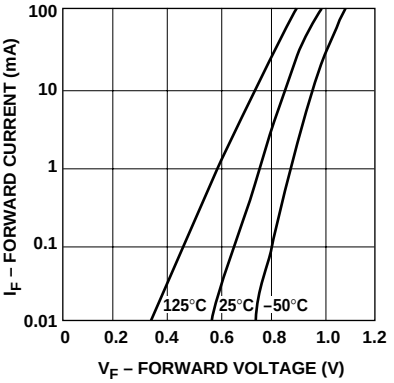


Figure 14. Forward Current vs. Forward Voltage. HSMP-389B/C/E/F Series and HSMP-489B.

Typical Applications for Multiple Diode Products

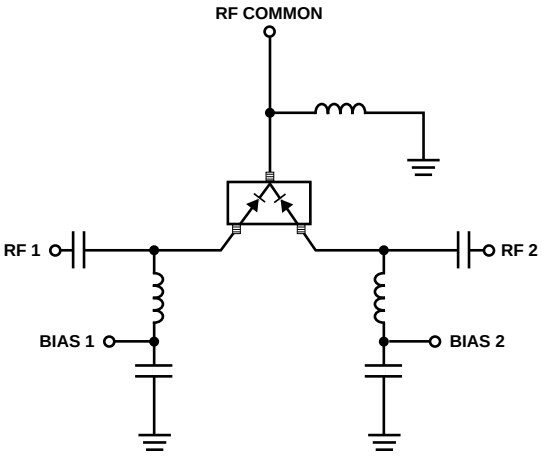


Figure 15. Simple SPDT Switch, Using Only Positive Bias Current.

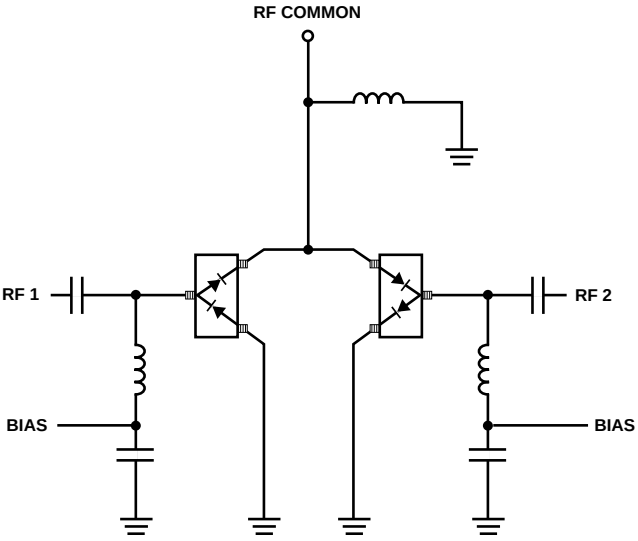


Figure 16. High Isolation SPDT Switch.

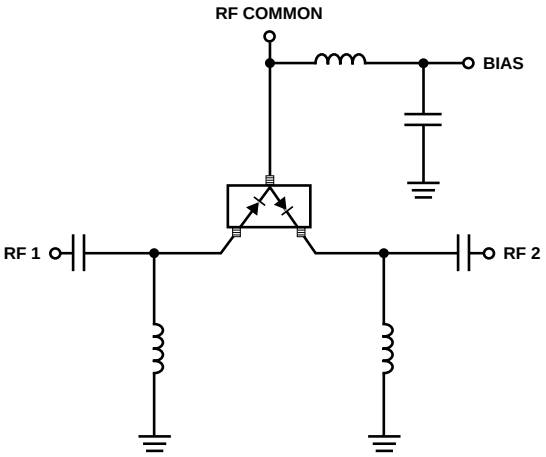


Figure 17. SPDT Switch Using Both Positive and Negative Bias Current.

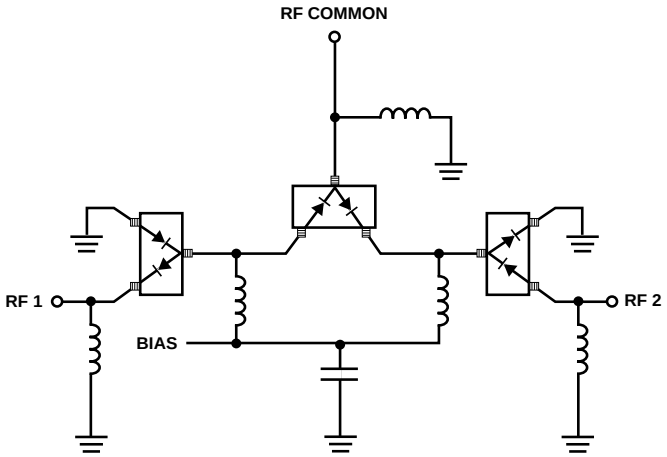


Figure 18. Very High Isolation SPDT Switch.

Typical Applications for Multiple Diode Products (continued)

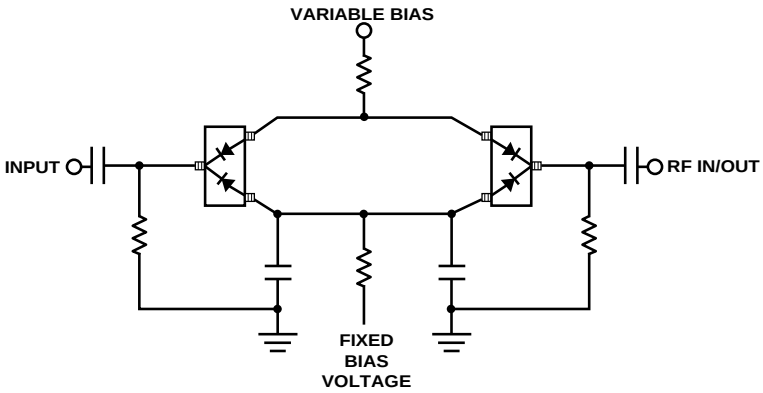


Figure 19. Four Diode π Attenuator.

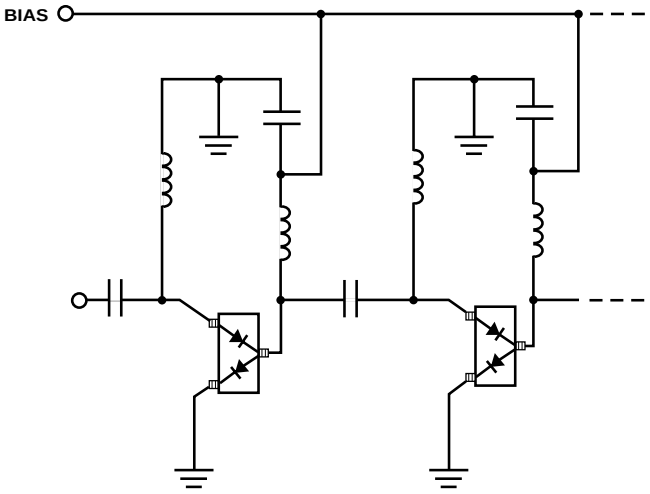


Figure 20. High Isolation SPST Switch (Repeat Cells as Required).

Typical Applications for HSMP-48XX Low Inductance Series

Microstrip Series Connection for HSMP-48XB Series

In order to take full advantage of the low inductance of the HSMP-48XB series when using them in series applications, both lead 1 and lead 2 should be connected together, as shown in Figure 21.

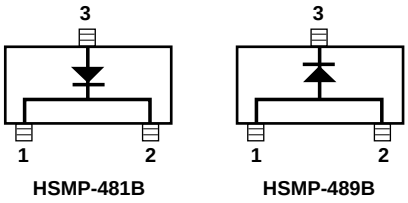


Figure 21. Internal Connections.

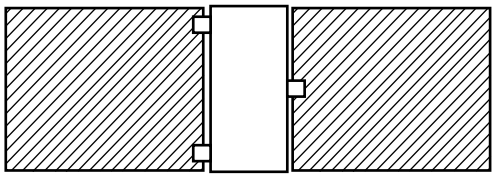


Figure 22. Circuit Layout.

Microstrip Shunt Connections for HSMP-48XB Series

In Figure 23, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-48XB series diode are placed across the resulting gap. This forces the 0.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

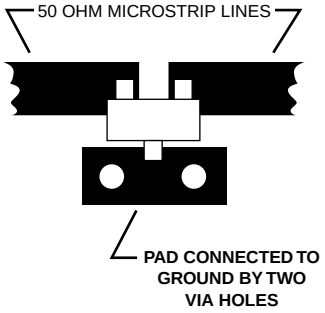


Figure 23. Circuit Layout.

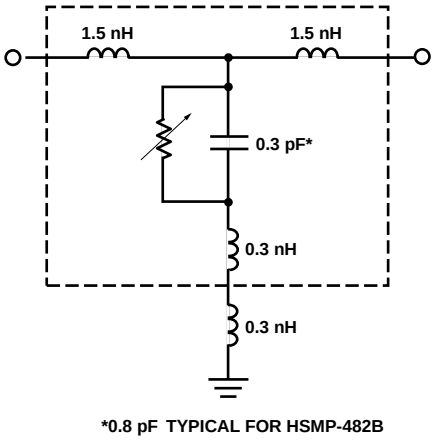


Figure 24. Equivalent Circuit.

Typical Applications for HSMP-48XX Low Inductance Series (continued)

Co-Planar Waveguide Shunt Connection for HSMP-48XB Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 25. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to a microstrip circuit.

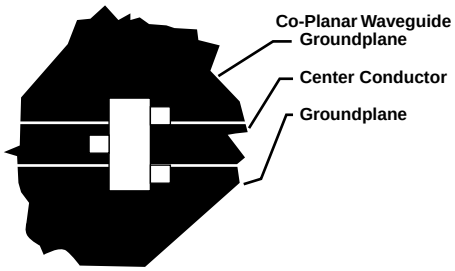


Figure 25. Circuit Layout.

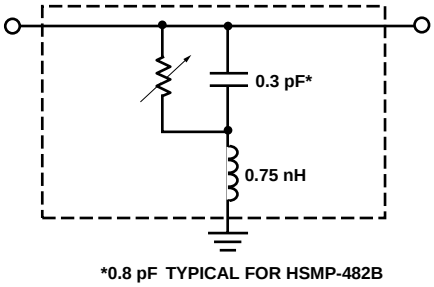


Figure 26. Equivalent Circuit.

Assembly Information

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 27 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair performance.

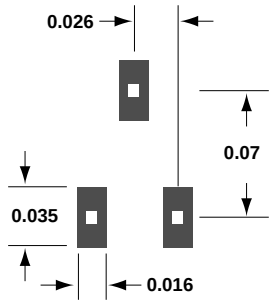


Figure 27. PCB Pad Layout (dimensions in inches).

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323 package, will reach solder reflow temperatures faster than those with a greater mass.

Agilent's SOT-323 diodes have been qualified to the time-temperature profile shown in Figure 28. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235 °C.

These parameters are typical for a surface mount assembly process for Agilent SOT-323 diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

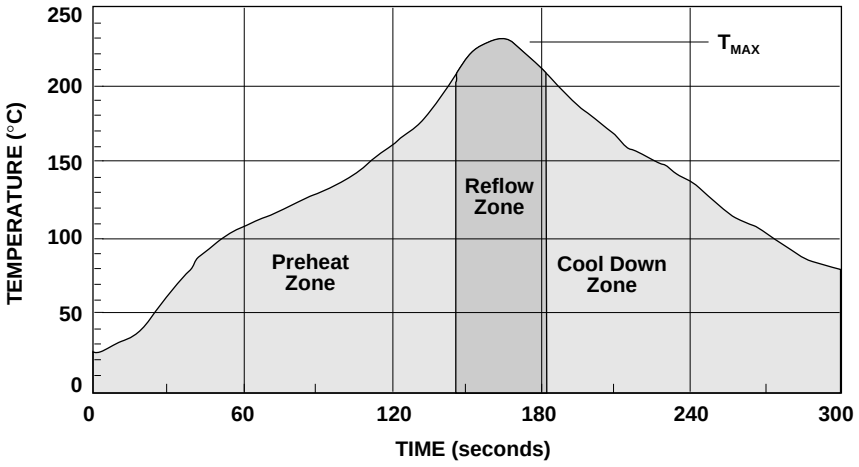
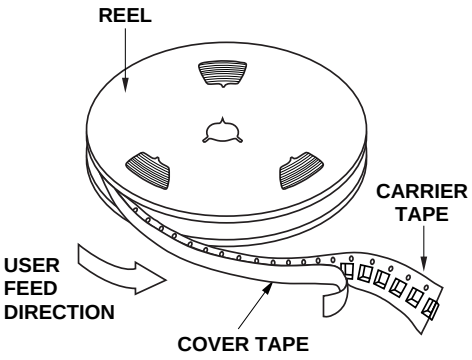
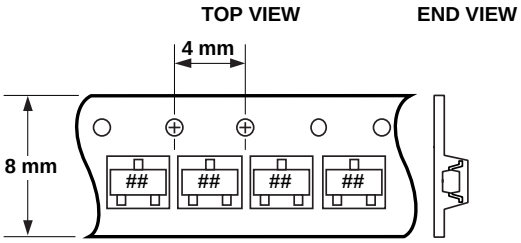


Figure 28. Surface Mount Assembly Profile.

Device Orientation

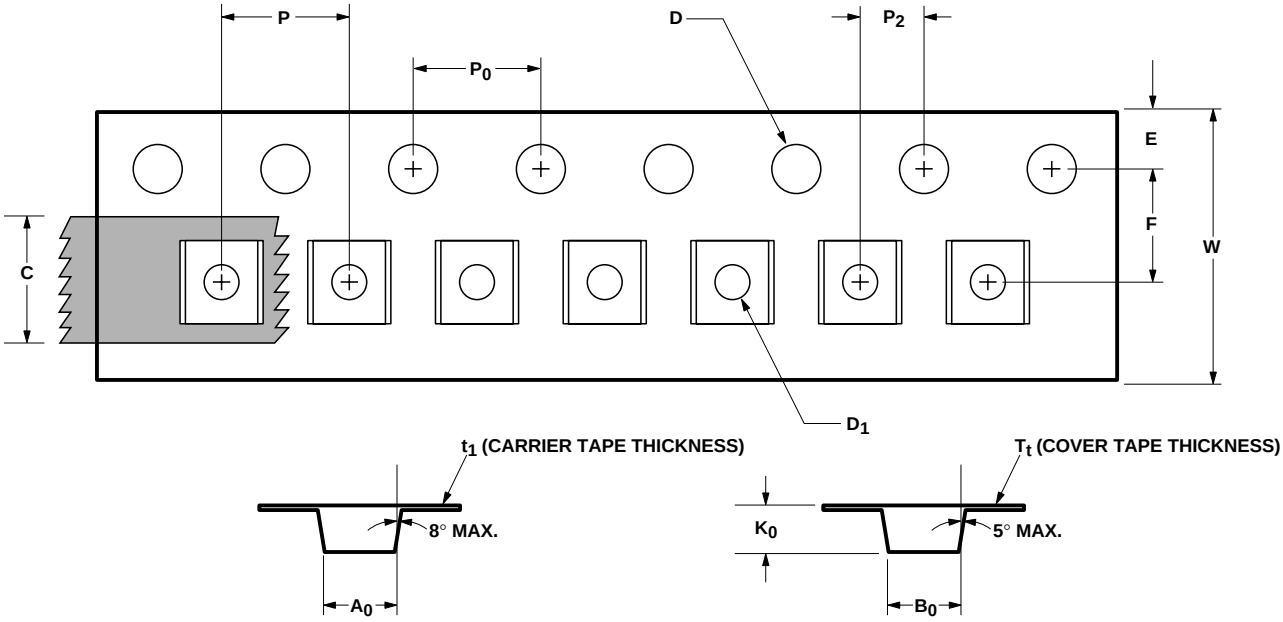




Note: "##" represents Package Marking Code.

Tape Dimensions

For Outline SOT-323 (SC-70 3 Lead)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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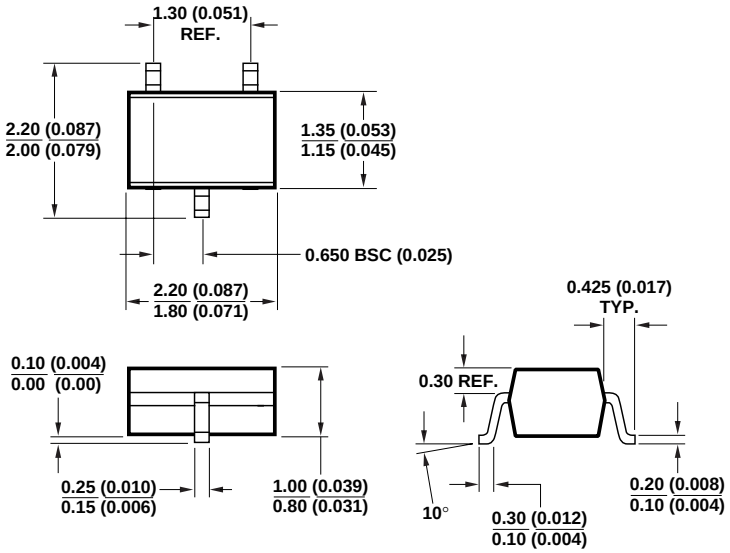
Package Dimensions

Outline SOT-323 (SC-70)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package Characteristics

Lead Material ..... Copper
Lead Finish ..... Tin-Lead 85/15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:

HSMP-38XA – XXX

- XXX: Bulk or Tape and Reel Option
- 38XA: Part Number
- HSMP: Surface Mount PIN
- Agilent

Option – BLK = Bulk, 100 pcs. per antistatic bag
Option – TR1 = Tape and Reel, 3000 devices per 7" reel

Conforms to Electronic Industries RS-481, “Taping of Surface Mounted Components for Automated Placement.” Standard Quantity is 3,000 Devices per Reel.

www.semiconductor.agilent.com
Data subject to change.

Obsoletes 5966-2323E
5967-6070E (11/99)