MX66U4000

Extra Low Power/Voltage 512k x 8 CMOS SRAM

FEATURES

- Very low operation voltage

  1.8 V

- Very low power consumption

  45mA (Max.) write current
  10mA (Max.) read current
  3uA (Typ.) CMOS standby current

- High speed access time

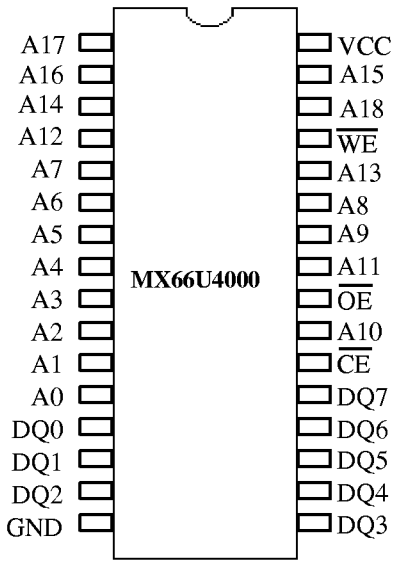
  150ns (Max.)

- Input levels are TTL-compatible
- Automatic power down when chip is deselected
- Three state outputs
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE}$/, and $\overline{OE}$/ options
- All I/O pins are 3.3V tolerant

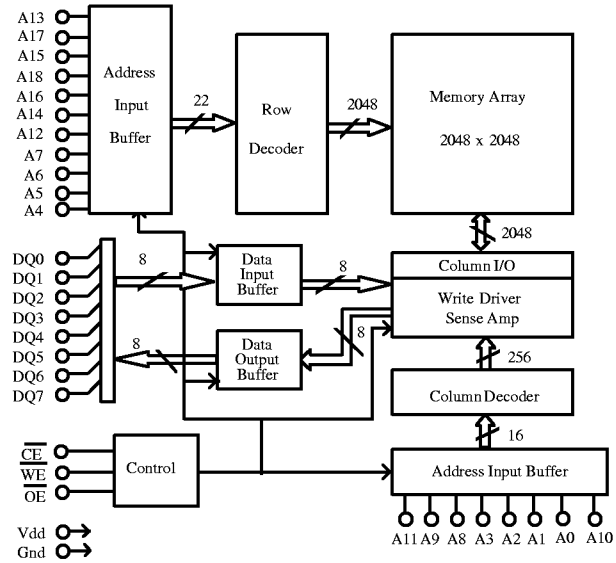
DESCRIPTION

The MX66U4000 is a high performance, extra low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from a very low range of supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 3uA and maximum access time of 150ns in 1.8V operation.
Easy memory expansion is provided by an active LOW chip enable($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The MX66U4000 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The MX66U4000 is available in the JEDEC standard 32 pin 600mil Plastic DIP, 525mil Plastic SOP, 8mmx13.4mm STSOP, and 8mmx20mm TSOP.

PIN CONFIGURATIONS



BLOCK DIAGRAM



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PIN DESCRIPTIONS

A_0-A_{18} Address Input	These 19 address input select one of the 524,288 x 8-bit words in the RAM
$\overline{CE}$ Chip Enable Input	$\overline{CE}$ is active LOW . Chip enable must be active to read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
DQ_0 - DQ_7 Data Input/Output Ports	These 8 bidirectional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
GND	Ground

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +5.5	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0° C to + 70° C	1.8V ~ 3.6V

CAPACITANCE(1) (T_A = 25° C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

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DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.5	—	+0.4	V
V_{IH}	Guaranteed Input High Voltage(2)		1.5	2.0	3.0	V
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc	—	—	1	uA
I_{OL}	Output Leakage Current	Vcc = Max, $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc	—	—	1	uA
V_{OL}	Outout Low Voltage	Vcc = Max, I_{OL} = 4mA	—	—	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -1mA	1.5	—	—	V
I_{CC}	Operating Power Supply Current	Vcc = Max, $\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, F = Fmax(3)	—	—	45	mA
I_{CCSB}	Standby Power Supply Current	Vcc = Max, $\overline{CE}$ = V_{IH}, I_{DQ} = 0mA,	—	—	0.5	mA
I_{CCSBI}	Power Down Supply Current	Vcc = Max, $\overline{CE}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≥ 0.2V	—	3	50	uA

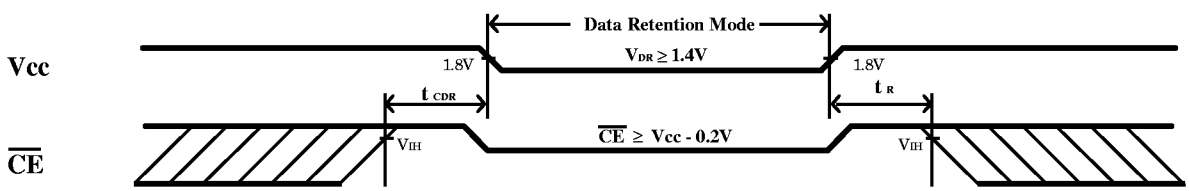
1. Typical characteristics are at Vcc = 1.8V, T_A = 25°C.
2. These are absolute valuse with respect to device ground and all overshoots due to system or tester noice are included.
3. $F_{MAX} = 1/t_{RC}$.

DATA RETENTION CHARACTERISTICS (T_A = 0 to + 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE}$ ≥Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤0.2V	1.4	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$≥Vcc -0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤.2V	—	1.5	40	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Wavform	0	—	—	ns
t_R	Operation Recovery Time		T_{RC}(2)	—	—	ns

1. Vcc = 1.8V, T_A = + 25°C
2. t_{RC} = Read Cycle Time

LOW VCC DATA RETENTION WAVEFORM (1) ($\overline{CE}$ Controlled)



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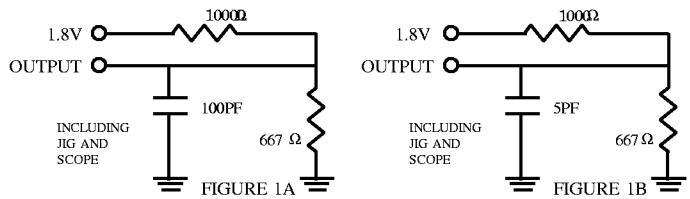
AC TEST CONDITIONS

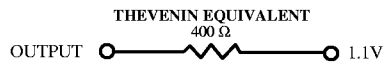
Input Pulse Levels	1.8V/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.9V

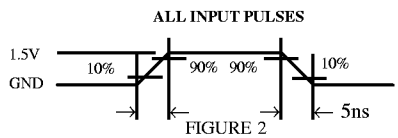
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

AC TEST LOADS AND WAVEFORMS







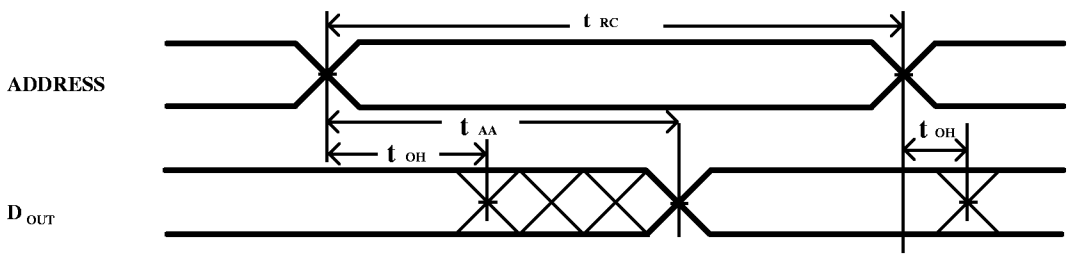
AC ELECTRICAL CHARACTERISTICS (over the operating range)
READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	MX66U4000-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	150	—	—	ns
t_{AVQV}	t_{AA}	Address Access Time	—	—	150	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time	—	—	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	—	—	100	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10	—	—	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	—	—	ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	—	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	—	35	ns
t_{AXQX}	t_{OH}	Output Disable to Output Address Change	10	—	—	ns

1. Typical characteristics are at Vcc = 1.8V, T_A = 25°C.

SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE1 (1,2,4)



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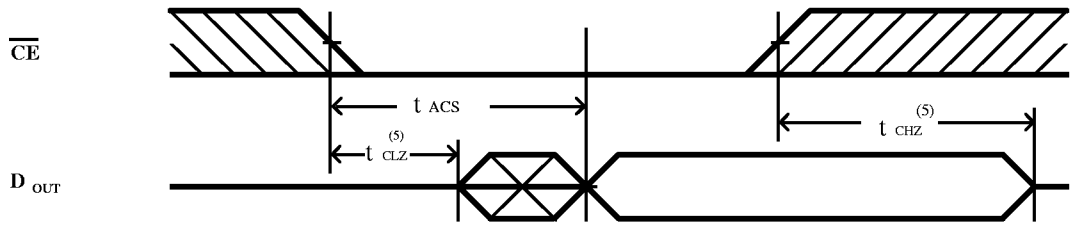
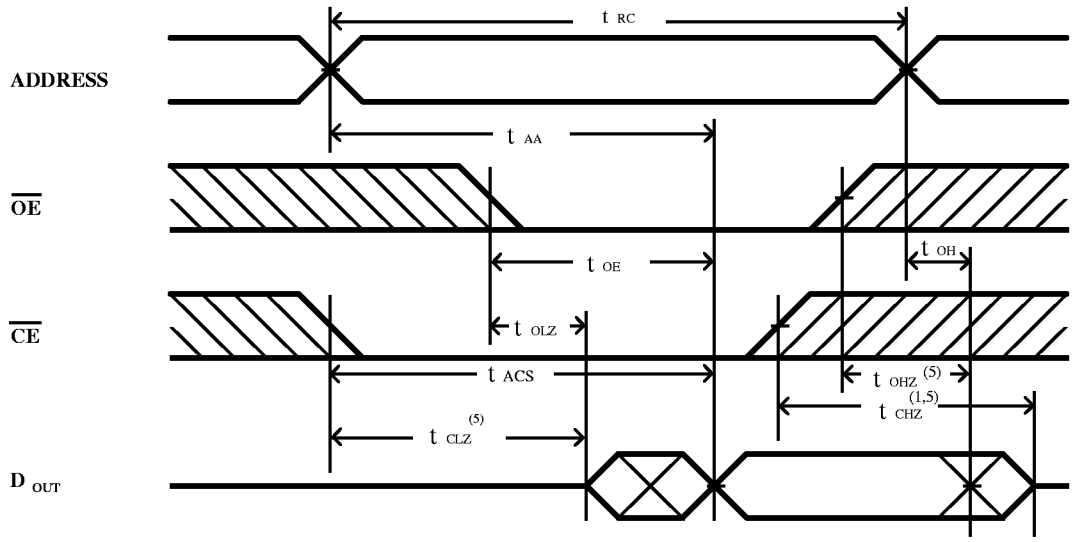
READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. $\overline{WE}$ is high for read Cycle.
2. Device is continuously selected when $\overline{CE}$ = V_{IL} .
3. Address valid prior to or coincident with $\overline{CE}$ transition low .
4. $\overline{OE}$ = V_{IL} .
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

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AC ELECTRICAL CHARACTERISTICS (over the operating range)

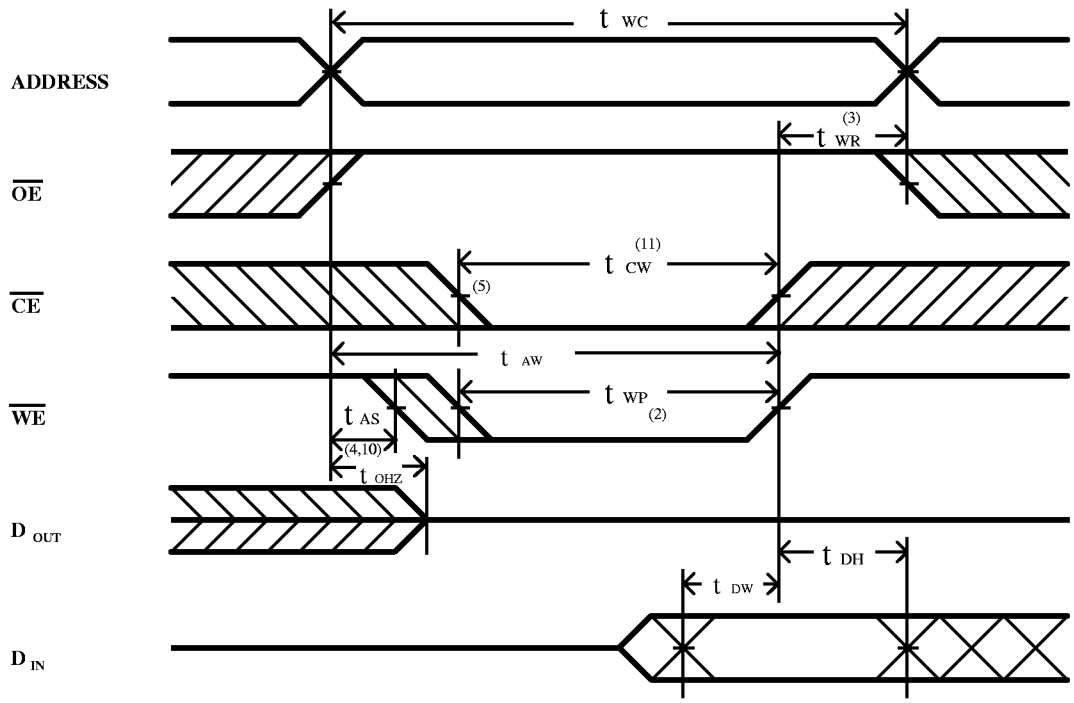
WRITE CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	MX66U4000-15 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	150	—	—	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	150	—	—	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	—	—	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	150	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width	80	—	—	ns
t_{WHAX}	t_{WR}	Write Recovery Time ($\overline{CE}$, $\overline{WE}$)	0	—	—	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	—	—	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	50	—	—	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	—	—	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	—	35	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	—	—	ns

1. Typical characteristics are at Vcc = 1.8V, T_A = 25°C.

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



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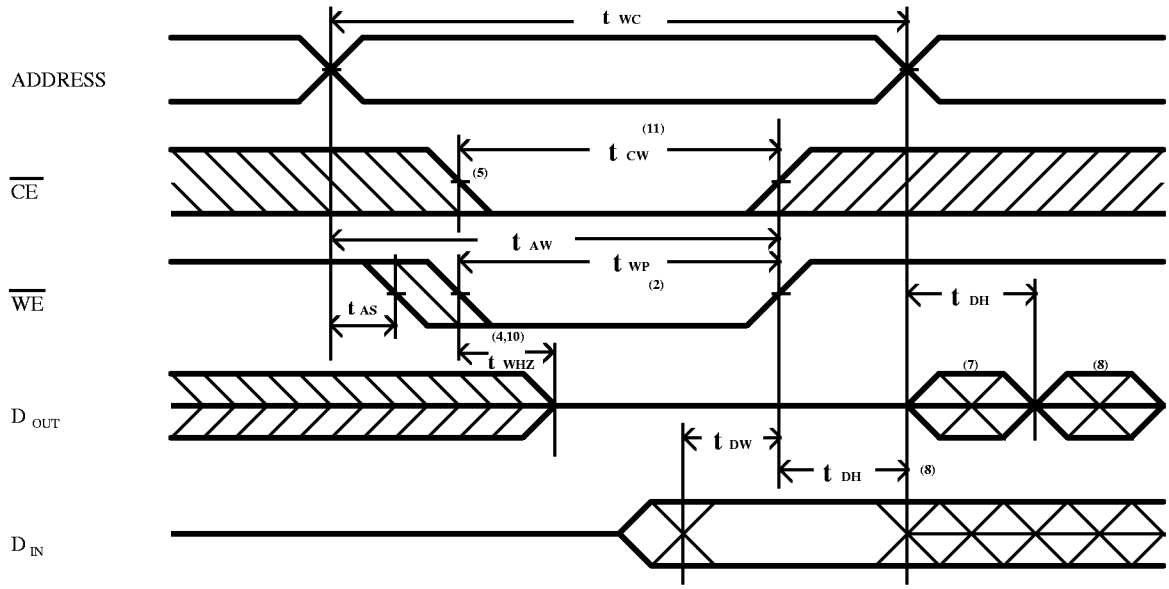
WRITE CYCLE2 (1,6)



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

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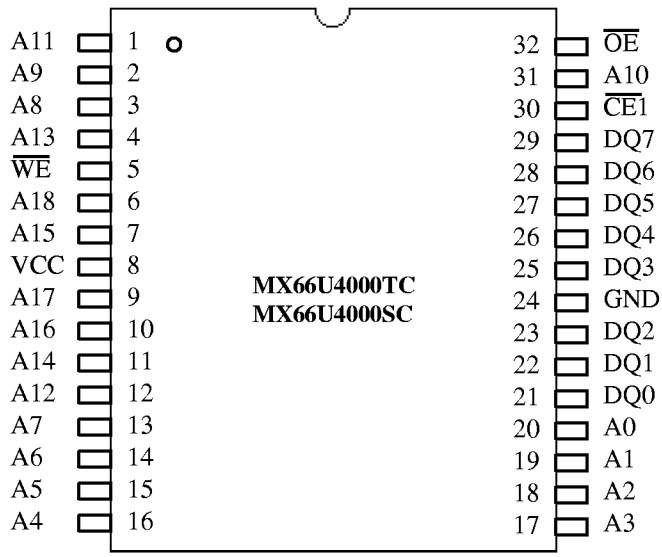
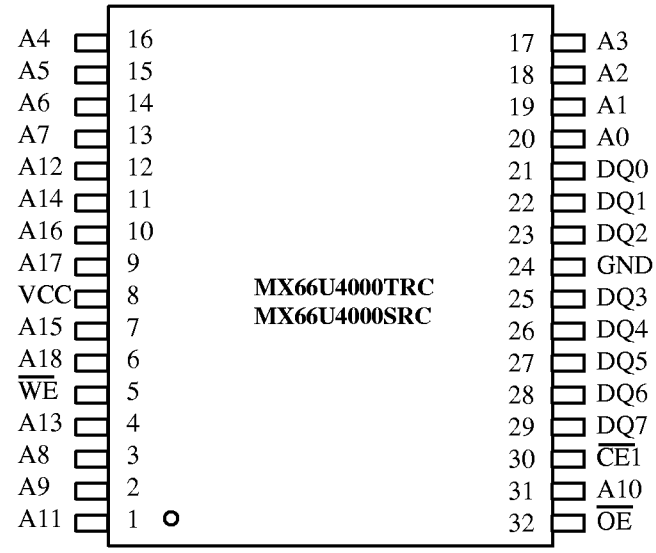
PIN CONFIGURATIONS (cont.)

32-Pin Plastic TSOP (Normal Pinouts)



Suffix-TC, SC in the package identifier

32-Pin Plastic TSOP (Reverse Pinouts)



Suffix-TRC, SRC in the package identifier

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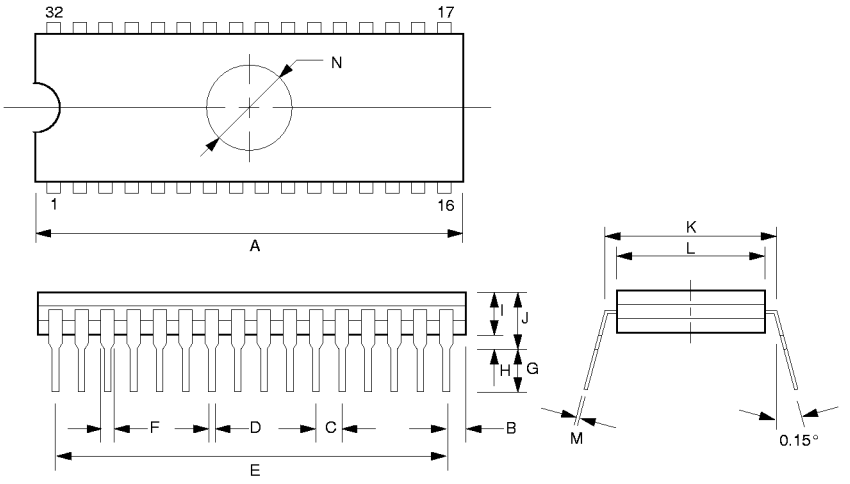
PACKAGE INFORMATION

32-PIN CERDIP(MSI) WITH WINDOW (600mil)

ITEM	MILLIMETERS	INCHES
A	42.26 max	1.665 max
B	1.90 ± .38	.075 ± .015
C	2.54 [TP]	.100 [TP]
D	.46 [REF]	.018 [REF]
E	38.07	1.500
F	1.42 [REF]	.056 [REF]
G	3.43 ± .38	.135 ± .015
H	.96 ± .43	.038 ± .017
I	4.06	.160
J	5.00	.203
K	15.58 ± .13	.614 ± .005
L	13.20 ± .38	.520 ± .015
M	.25 [REF]	.010 [REF]
N	ø8.12	ø.320

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.