HT163A

Dot Matrix LCD Controller and Driver

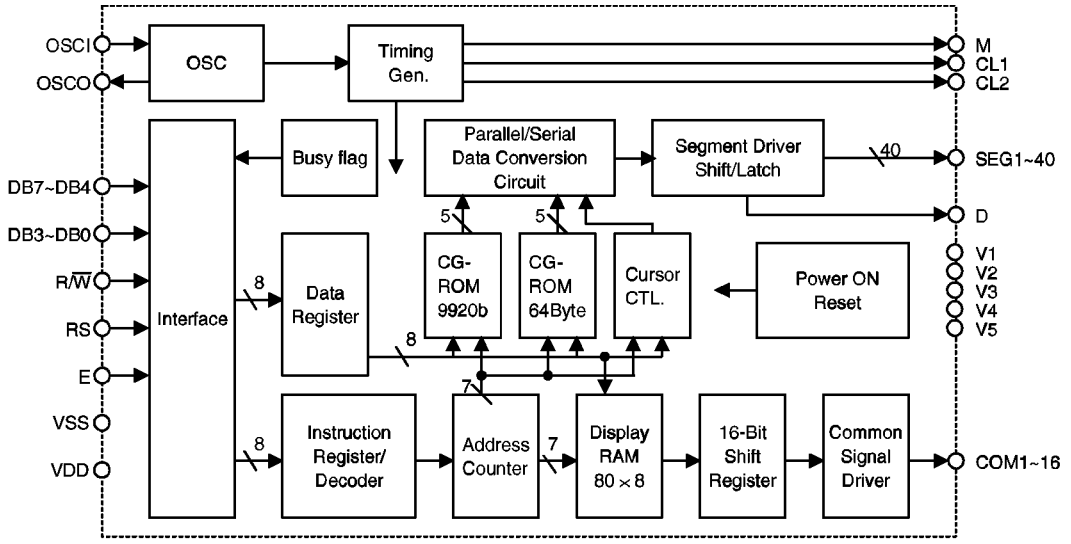
Features

- Low power operating voltage: 2.7V to 5.5V
- Internal LCD driver: 16 commons and 40 segments (segment can be extended by HT1602L/HT1608/HT1608L/HT1609L)
- 4-bit or 8-bit interface function
- Interface bus clock rating: 4 MHz (V_{DD}=5V)
- Built-in 80×8 bits display RAM
- 9920-bit character generator ROM for a total of 240 character fonts
  - 208 character fonts (5×8)
  - 32 character fonts (5×10)
- Character generator RAM
  - 8 character fonts (5×8)
  - 4 character fonts (5×10)
- Programmable duty cycles
  - 1/8 duty for one line of 5×8 dots with cursor
  - 1/11 duty for one line of 5×10 dots with cursor
  - 1/16 for two lines of 5×8 dots with cursor
- Built-in oscillator circuit with external resistor
- Powerful instruction set: Display clear, display on/off, cursor home, cursor on/off, display character blink, cursor shift, display shift
- Built-in power on reset function
- Low power consumption

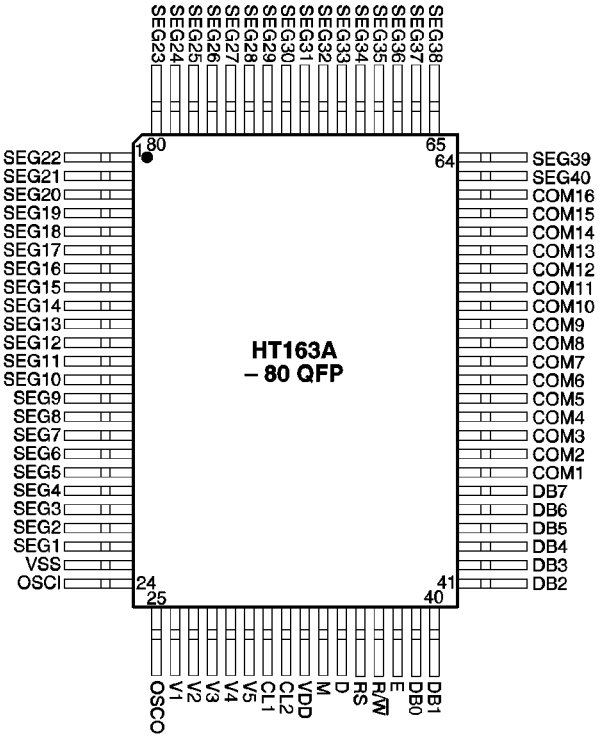
General Description

The HT163A is a dot matrix LCD controller and driver LSI with low power consumption and fabricated by CMOS technology. It can operate with either a 4-bit or an 8-bit microcontroller at high speed clock rating. The HT163A built-in CGROM and CGRAM provide user-friendly interface for the programmer. It contains 208 5×8 dot character fonts and 32 5×10 dot character fonts for a total of 240 different character fonts.

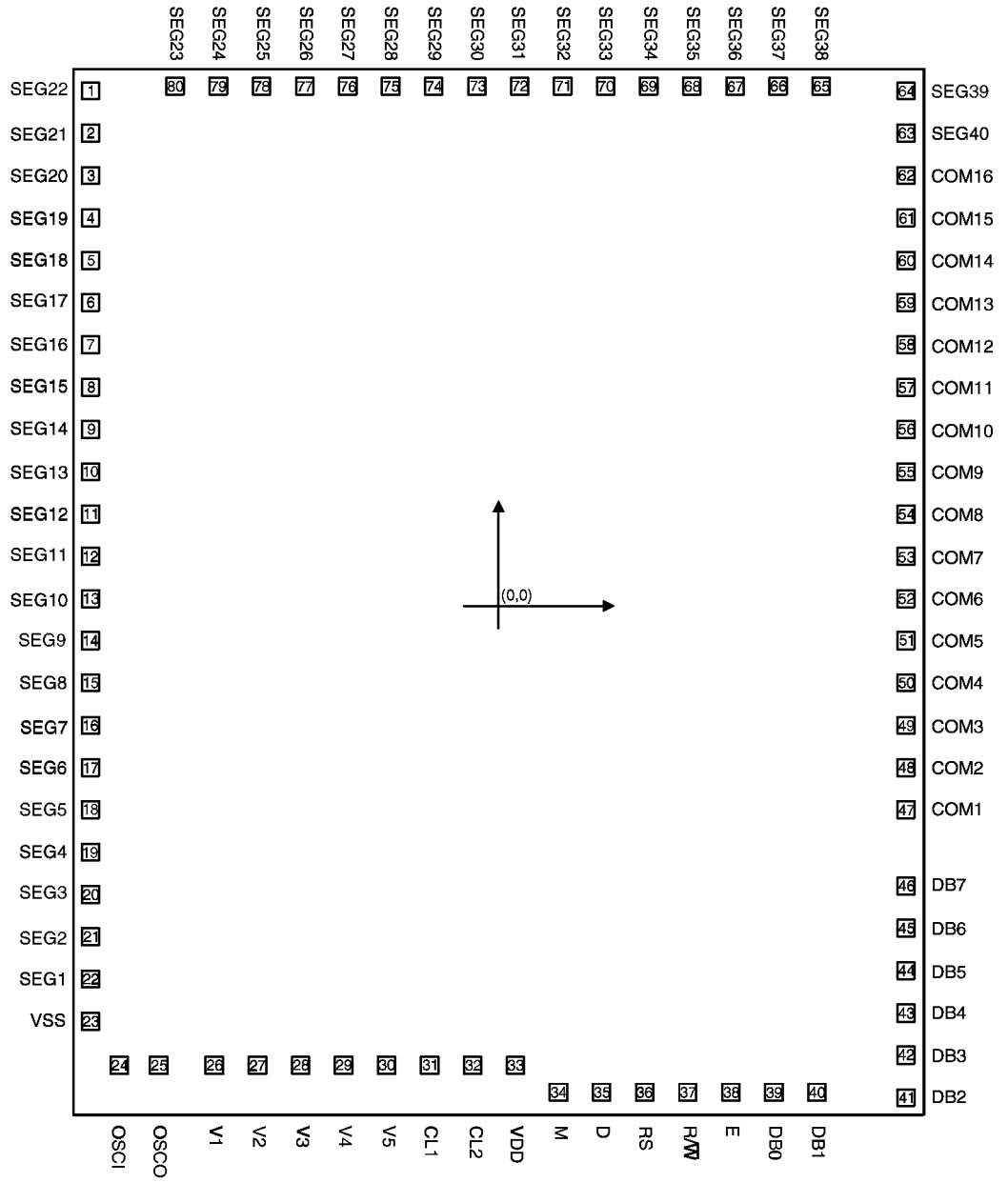
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 104×134 (mil)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1183.70	1521.30	41	1183.70	–1453.70
2	–1183.70	1396.30	42	1183.70	–1328.70
3	–1183.70	1271.30	43	1183.70	–1203.70
4	–1183.70	1146.30	44	1183.70	–1078.70
5	–1183.70	1021.30	45	1183.70	–953.70
6	–1183.70	896.30	46	1183.70	–828.70
7	–1183.70	771.30	47	1183.70	–603.70
8	–1183.70	646.30	48	1183.70	–478.70
9	–1183.70	521.30	49	1183.70	–353.70
10	–1183.70	396.30	50	1183.70	–228.70
11	–1183.70	271.30	51	1183.70	–103.70
12	–1183.70	146.30	52	1183.70	21.30
13	–1183.70	21.30	53	1183.70	146.30
14	–1183.70	–103.70	54	1183.70	271.30
15	–1183.70	–228.70	55	1183.70	396.30
16	–1183.70	–353.70	56	1183.70	521.30
17	–1183.70	–478.70	57	1183.70	646.30
18	–1183.70	–603.70	58	1183.70	771.30
19	–1183.70	–728.70	59	1183.70	896.30
20	–1183.70	–853.70	60	1183.70	1021.30
21	–1183.70	–978.70	61	1183.70	1146.30
22	–1183.70	–1103.70	62	1183.70	1271.30
23	–1183.70	–1228.70	63	1183.70	1396.30
24	–1121.90	–1357.10	64	1183.70	1521.30
25	–985.90	–1357.10	65	937.50	1535.90
26	–824.60	–1357.10	66	812.50	1535.90
27	–699.60	–1357.10	67	687.50	1535.90
28	–574.60	–1357.10	68	562.50	1535.90
29	–449.60	–1357.10	69	437.50	1535.90
30	–324.60	–1357.10	70	312.50	1535.90
31	–199.60	–1357.10	71	187.50	1535.90
32	–74.60	–1357.10	72	62.50	1535.90
33	50.40	–1357.10	73	–62.50	1535.90
34	175.40	–1437.10	74	–187.50	1535.90
35	300.40	–1437.10	75	–312.50	1535.90
36	425.40	–1437.10	76	–437.50	1535.90
37	550.40	–1437.10	77	–562.50	1535.90
38	675.40	–1437.10	78	–687.50	1535.90
39	800.40	–1437.10	79	–812.50	1535.90
40	925.40	–1437.10	80	–937.50	1535.90

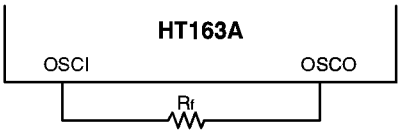
Pad Description

Pad No.	Pad Name	I/O	Description
1~22	SEG22~SEG1	O	LCD driver output for segment signal
23	VSS	—	Ground
24 25	OSCI OSCO	I O	Connects external resistor for RC Oscillator circuit
26~30	V1~V5	P	Power supply for LCD driver level
31	CL1	O	Clock to latch serial data send to the extension driver
32	CL2	O	Clock to shift serial data
33	VDD	—	Power supply for logic circuit
34	M	O	The alternating signal to convert LCD drive waveform to AC
35	D	O	Character pattern data corresponding to each segment signal, "0" is Non-selected, "1" is Selected
36	RS	I	Register select signal "0" : Instruction register (for write) Busy flag, address counter (for read) "1" : Data register, (for read and write)
37	R/$\overline{W}$	I	Select read or write "0" : Write "1" : Read
38	E	I	Start data Read/Write
39~42	DB0~DB3	I/O	Low order bidirectional tri-state data bus pins for transmitting and receiving data between the MPU and the HT163A. These pins are not used during 4-bit operation
43~46	DB4~DB7	I/O	High order bidirectional tri-state data bus pins for transmitting and receiving data between the MPU and the HT163A. The DB7 pin can be used as a busy flag
47~62	COM1~16	O	LCD driver output for common signal
63~80	SEG40~23	O	LCD driver output for segment signal

Notes:

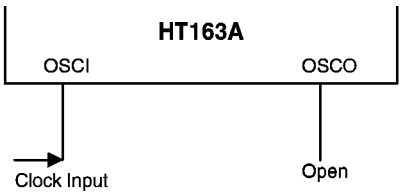
1. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained

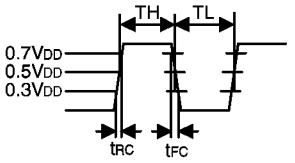
A. Internal oscillator operation using oscillation resistor R_f



R_f= 91kΩ±2% (V_{DD}=5V)
R_f= 75kΩ±2% (V_{DD}=3V)

B. External clock operation

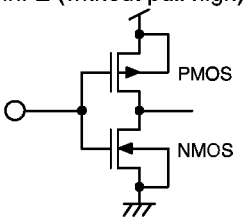




$$\text{Duty}=\frac{TH}{TH+TL}\times 100\%$$

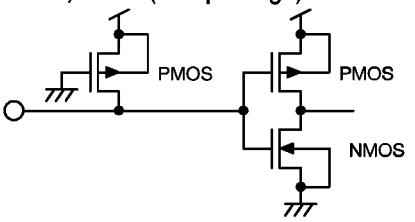
2. Two clock options:

Pin: E (without pull high)



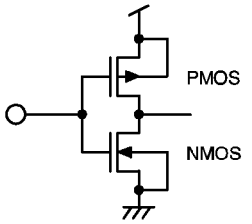
3. Input terminal:

Pin: RS, R/WB (with pull high)

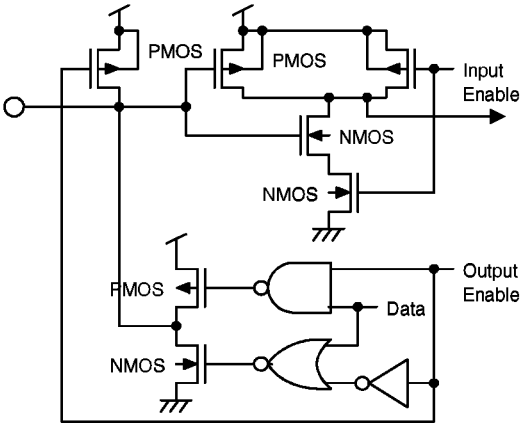


4. Output terminal:

Pin: CL1, CL, M, D



5. I/O terminal: (DB0~DB7)



Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –40°C to 125°C

Operating Temperature ..... –20°C to 75°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}= 4.5V~5.5V operation Ta=–20 to 75°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	4.5	—	5.5	V
V_{LCD}	LCD Driving Voltage	4.5V~5.5V	V_{DD}–V5	3.0	—	5.5	V
I_{DD}	Power Consumption	4.5V~5.5V	f_{OSC}=270kHz	—	0.35	0.6	mA
V_{IH1}	Input High Voltage (except OSCI)	4.5V~5.5V	—	2.2	—	V_{DD}	V
V_{IL1}	Input Low Voltage (except OSCI)	4.5V~5.5V	—	–0.3	—	0.6	V
V_{IH2}	Input High Voltage (OSCI)	4.5V~5.5V	—	V_{DD} –1.0	—	V_{DD}	V
V_{IL2}	Input Low Voltage (OSCI)	4.5V~5.5V	—	—	—	1.0	V
V_{OH1}	Output High Voltage (DB0~DB7)	4.5V~5.5V	I_{OH}=–0.2mA (DB0~DB7)	2.4	—	—	V
V_{OL1}	Output Low Voltage (DB0~DB7)	4.5V~5.5V	I_{OL}=1.2mA (DB0~DB7)	—	—	0.4	V
V_{OH2}	Output High Voltage (except DB0~DB7)	4.5V~5.5V	I_{OH}=–0.04mA (except DB0~DB7)	0.9V_{DD}	—	—	V
V_{OL2}	Output Low Voltage (except DB0~DB7)	4.5V~5.5V	I_{OL}=0.04mA (except DB0~DB7)	—	—	0.1V_{DD}	V
R_{COM}	Driver on Resistor	4.5V~5.5V	V_{LCD}=4V, I_{COM}=0.05mA (Between VDD, V1, V4, V5 and each COM pin)	—	—	20	kΩ
R_{SEG}	Driver on Resistor	4.5V~5.5V	V_{LCD}=4V, I_{SEG}=0.05mA (Between VDD, V1, V4, V5 and each SEG pin)	—	—	30	kΩ
I_{LEAK}	Input Leakage Current	4.5V~5.5V	V_{IN}=0 to V_{DD}	–1	—	1	μA
R_{PH}	Pull-high Resistance	5V	V_{DD}=5V	100	40	20	kΩ

V_{DD}=2.7V~4.5V operation Ta=–20 to 75°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.5	V
V_{LCD}	LCD Driving Voltage	2.7V~4.5V	V_{DD}–V5	2.7	—	5.5	V
I_{DD}	Power Consumption	2.7V~4.5V	f_{OSC}=270kHz	—	0.15	0.3	mA
V_{IH1}	Input High Voltage (except OSCI)	2.7V~4.5V	—	0.7V_{DD}	—	V_{DD}	V
V_{IL1}	Input Low Voltage (except OSCI)	2.7V~4.5V	—	–0.3	—	0.55	V
V_{IH2}	Input High Voltage (OSCI)	2.7V~4.5V	—	0.7V_{DD}	—	V_{DD}	V
V_{IL2}	Input Low Voltage (OSCI)	2.7V~4.5V	—	—	—	0.2V_{DD}	V
V_{OH1}	Output High Voltage (DB0~DB7)	2.7V~4.5V	I_{OH}=–0.2mA (DB0~DB7)	0.7V_{DD}	—	—	V
V_{OL1}	Output Low Voltage (DB0~DB7)	2.7V~4.5V	I_{OL}=1.2mA (DB0~DB7)	—	—	0.2V_{DD}	V
V_{OH2}	Output High Voltage (except DB0~DB7)	2.7V~4.5V	I_{OH}=–0.04mA (except DB0~DB7)	0.8V_{DD}	—	—	V
V_{OL2}	Output Low Voltage (except DB0~DB7)	2.7V~4.5V	I_{OL}=0.04mA (except DB0~DB7)	—	—	0.2V_{DD}	V
R_{COM}	Driver on Resistor	2.7V~4.5V	V_{LCD}=4V, I_{COM}=0.05mA (Between VDD, V1, V4, V5 and each COM pin)	—	—	20	kΩ
R_{SEG}	Driver on Resistor	2.7V~4.5V	V_{LCD}=4V, I_{SEG}=0.05mA (Between VDD, V1, V4, V5 and each SEG pin)	—	—	30	kΩ
I_{LEAK}	Input Leakage Current	2.7V~4.5V	V_{IN}=0 to V_{DD}	–1	—	1	μA
R_{PH}	Pull-high Resistance	3V	V_{DD}=3V	500	100	45	kΩ

A.C. Characteristics

V_{DD}=4.5V~5.5V operation Ta=–20 to 75°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{OSC}	Clock Oscillator Frequency	5V	R_f=91kΩ	190	270	350	kHz
f_C	External Clock Frequency	4.5V~5.5V	—	125	250	350	kHz
t_{RC}	External Clock Rise Time	4.5V~5.5V	—	—	—	0.2	μs
t_{FC}	External Clock Fall Time	4.5V~5.5V	—	—	—	0.2	μs
Duty	External Clock Duty	4.5V~5.5V	—	45	50	55	%
t_C	E Cycle Time	4.5V~5.5V	Write Mode	500	—	—	ns
t_R, t_F	E Rise/Fall Time	4.5V~5.5V	Write Mode	—	—	20	ns
t_W	E Pulse Width	4.5V~5.5V	Write Mode	230	—	—	ns
t_{SU1}	R/$\overline{W}$ and RS Setup Time	4.5V~5.5V	Write Mode	40	—	—	ns
t_{H1}	R/$\overline{W}$ and RS Hold Time	4.5V~5.5V	Write Mode	10	—	—	ns
t_{DSW}	Data Setup Time	4.5V~5.5V	Write Mode	60	—	—	ns
t_{DHW}	Data Hold Time	4.5V~5.5V	Write Mode	10	—	—	ns
t_C	E Cycle Time	4.5V~5.5V	Read Mode	500	—	—	ns
t_R, t_F	E Rise/Fall Time	4.5V~5.5V	Read Mode	—	—	20	ns
t_W	E Pulse Width	4.5V~5.5V	Read Mode	230	—	—	ns
t_{SU2}	R/$\overline{W}$ and RS Setup Time	4.5V~5.5V	Read Mode	40	—	—	ns
t_{H2}	R/$\overline{W}$ and RS Hold Time	4.5V~5.5V	Read Mode	10	—	—	ns

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{DDR}	Data Output Delay Time	4.5V~5.5V	Read Mode	—	—	120	ns
t_{DHR}	Data Hold Time	4.5V~5.5V	Read Mode	5	—	—	ns
t_{CW}	Clock Pulse Width	4.5V~5.5V	Interface with driver	800	—	—	ns
t_R, t_F	Clock Rise/Fall Time	4.5V~5.5V	Interface with driver	—	—	100	ns
t_{CSU}	Clock Setup Time	4.5V~5.5V	Interface with driver	500	—	—	ns
t_{SU}	Data Setup Time	4.5V~5.5V	Interface with driver	300	—	—	ns
t_{DH}	Data Hold Time	4.5V~5.5V	Interface with driver	300	—	—	ns
t_{DM}	M Delay Time	4.5V~5.5V	Interface with driver	–1000	—	1000	ns

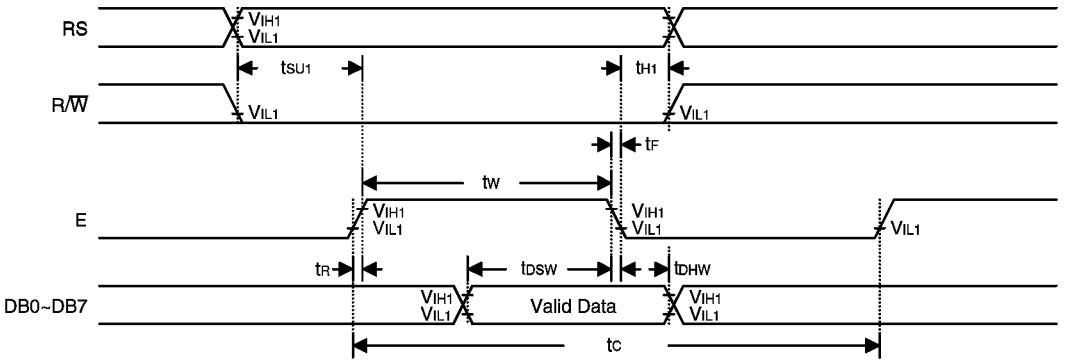
V_{DD}=2.7V~4.5V operation Ta=–20 to 75°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{OSC}	Clock Oscillator Frequency	3V	R_f=75kΩ	190	270	350	kHz
f_C	External Clock Frequency	2.7V~4.5V	—	125	250	350	kHz
t_{RC}	External Clock Rise Time	2.7V~4.5V	—	—	—	0.2	μs
t_{FC}	External Clock Fall Time	2.7V~4.5V	—	—	—	0.2	μs
Duty	External Clock Duty	2.7V~4.5V	—	45	50	55	%
t_C	E Cycle Time	2.7V~4.5V	Write Mode	1000	—	—	ns
t_R, t_F	E Rise/Fall Time	2.7V~4.5V	Write Mode	—	—	25	ns
t_W	E Pulse Width	2.7V~4.5V	Write Mode	450	—	—	ns

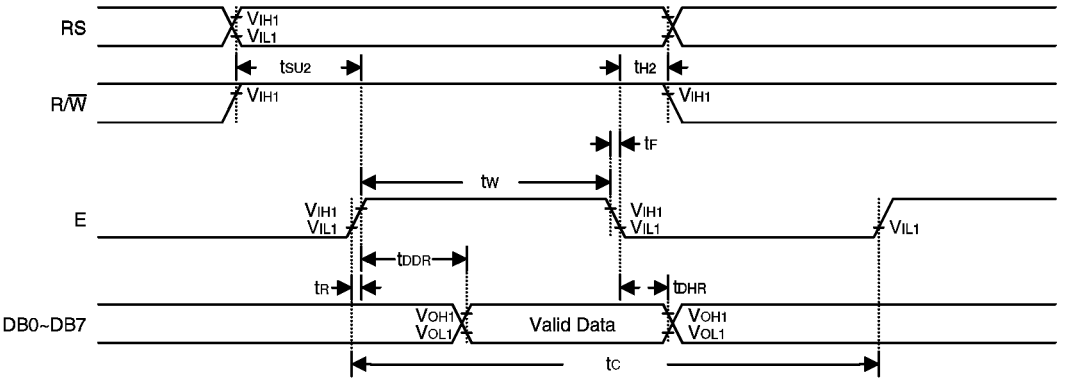
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{SU1}	R/$\overline{W}$ and RS Setup Time	2.7V~4.5V	Write Mode	60	—	—	ns
t_{H1}	R/$\overline{W}$ and RS Hold Time	2.7V~4.5V	Write Mode	20	—	—	ns
t_{DSW}	Data Setup Time	2.7V~4.5V	Write Mode	195	—	—	ns
t_{DHW}	Data Hold Time	2.7V~4.5V	Write Mode	10	—	—	ns
t_C	E Cycle Time	2.7V~4.5V	Read Mode	1000	—	—	ns
t_R, t_F	E Rise/Fall Time	2.7V~4.5V	Read Mode	—	—	25	ns
t_W	E Pulse Width	2.7V~4.5V	Read Mode	450	—	—	ns
t_{SU2}	R/$\overline{W}$ and RS Setup Time	2.7V~4.5V	Read Mode	60	—	—	ns
t_{H2}	R/$\overline{W}$ and RS Hold Time	2.7V~4.5V	Read Mode	20	—	—	ns
t_{DDR}	Data Output Delay Time	2.7V~4.5V	Read Mode	—	—	360	ns
t_{DHR}	Data Hold Time	2.7V~4.5V	Read Mode	5	—	—	ns
t_{CW}	Clock Pulse Width	2.7V~4.5V	Interface with driver	800	—	—	ns
t_R, t_F	Clock Rise/Fall Time	2.7V~4.5V	Interface with driver	—	—	200	ns
t_{CSU}	Clock Setup Time	2.7V~4.5V	Interface with driver	500	—	—	ns
t_{SU}	Data Setup Time	2.7V~4.5V	Interface with driver	300	—	—	ns
t_{DH}	Data Hold Time	2.7V~4.5V	Interface with driver	300	—	—	ns
t_{DM}	M Delay Time	2.7V~4.5V	Interface with driver	–1000	—	1000	ns

Timing Diagrams

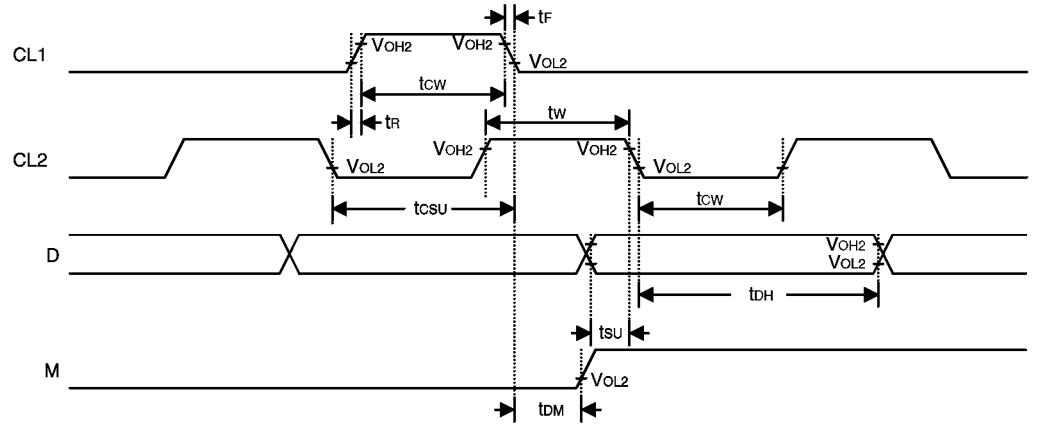
• Write mode timing diagram



• Read mode timing diagram

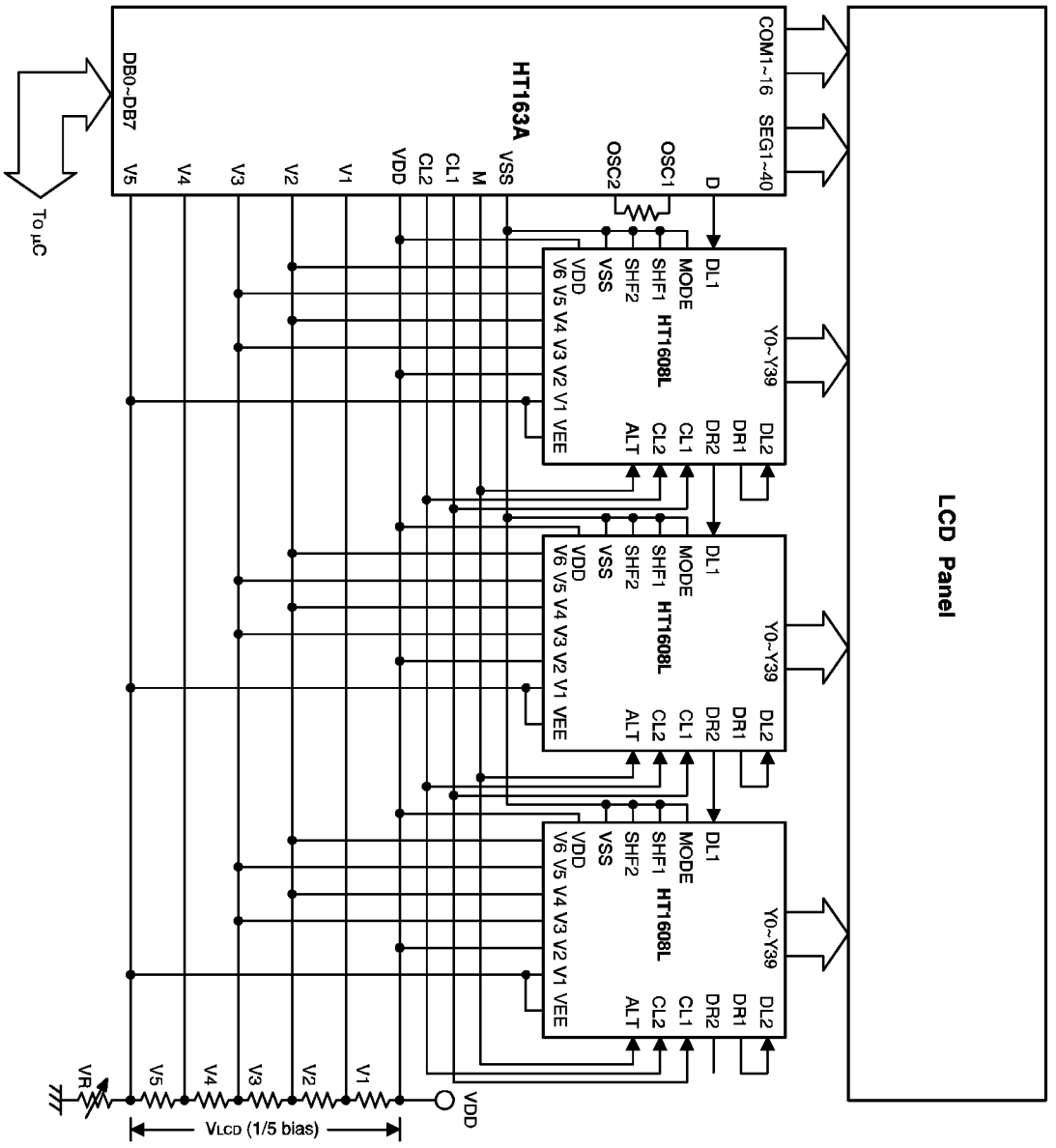


• Interface mode with external driver timing diagram



Functional Description

The HT163A LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver HT1608, HT1608L or HT1602L. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display.



The HT163A has two kinds of interface type with MPU: 4-bit and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. It can receive both instructions and data from the MPU. Some instructions set the operation modes, such as function mode, data entry mode, display mode, read or write both data and address etc.

Instruction Table

Instruction	Instruction Code										Description	Execution time (f_{OSC}=270 kHz)
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.	1.52ms
Display Return home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to it's original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable. I/D: 1-Increment 0-Decrement SH: 1-Display, Shift on	37μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit. D: 1-On, 0-Off C: 1-On, 0-Off B: 1-On, 0-Off	37μs

Instruction	Instruction Code										Description	Execution time (f_{OSC}=270 kHz)
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data. S/C: 0-Cursor move 1-Display R/L: 0-Shift to the left 1-Shift to the right	37μs
Function set	0	0	0	0	1	DL	N	F	X	X	Set interface data length, DL: 0-4 bits/1-8 bits numbers of display line, N: 0-1 line/1-2 lines display font type. F: 0-5×7dots 1-50-5×10 dots	37μs
Set CGRAM address	0	0	0	1	AD5	AD4	AD3	AD2	AD1	AD0	Set CGRAM address in address counter	37μs
Set DDRAM address	0	0	1	A6	AD5	AD4	AD3	AD2	AD1	AD0	Set DDRAM address in address counter	37μs
Read busy flag and address	0	1	BF	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Whether during internal operation or not, can be known by reading BF. The contents of address counter can also be read. BF: 0-Can accept Instruction 1-Internally operating	0μs
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM,DDRAM/CGRAM	43μs
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM DDRAM/CGRAM	43μs

* "X": don't care

- The character generator ROM (CGROM) generates 5×8 dot or 5×10 dot character patterns from 8-bit character codes. It can generate 208 5×8 dot character patterns and 32 5×10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

- Example of correspondence between address data and character pattern (5×8 dots)

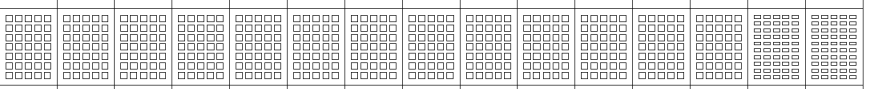
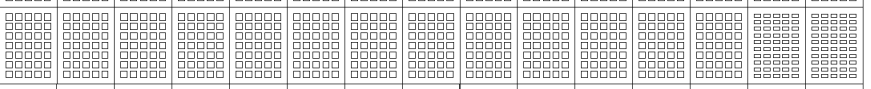
EPROM Address												Data				
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	LSB O0
								0	0	0	0	1	0	0	0	0
								0	0	0	1	1	0	0	0	0
								0	0	1	0	1	0	1	1	0
								0	0	1	1	1	1	0	0	1
								0	1	0	0	1	0	0	0	1
								0	1	0	1	1	0	0	0	1
								0	1	1	0	1	1	1	1	0
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0 ← Cursor position
								1	0	0	0	0	0	0	0	0
								1	0	0	1	0	0	0	0	0
								1	0	1	0	0	0	0	0	0
								1	0	1	1	0	0	0	0	0
								1	1	0	0	0	0	0	0	0
								1	1	0	1	0	0	0	0	0
								1	1	1	0	0	0	0	0	0
								1	1	1	1	0	0	0	0	0

Character Code Line Position

- Example of correspondence between address data and character pattern (5×10 dots)

EPROM Address												Data				
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	LSB O0
								0	0	0	0	0	0	0	0	0
								0	0	0	1	0	0	0	0	0
								0	0	1	0	0	1	1	0	1
								0	0	1	1	1	0	0	1	1
								0	1	0	0	1	0	0	0	1
								0	1	0	1	1	0	0	0	1
								0	1	1	0	0	1	1	1	1
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1
								1	0	0	0	0	0	0	0	1
								1	0	0	1	0	0	0	0	1
								1	0	1	0	0	0	0	0	0 ← Cursor position
								1	0	1	1	0	0	0	0	0
								1	1	0	0	0	0	0	0	0
								1	1	0	1	0	0	0	0	0
								1	1	1	0	0	0	0	0	0
								1	1	1	1	0	0	0	0	0

Character Code Line Position

Upper 4 bits / Lower 4 bits	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

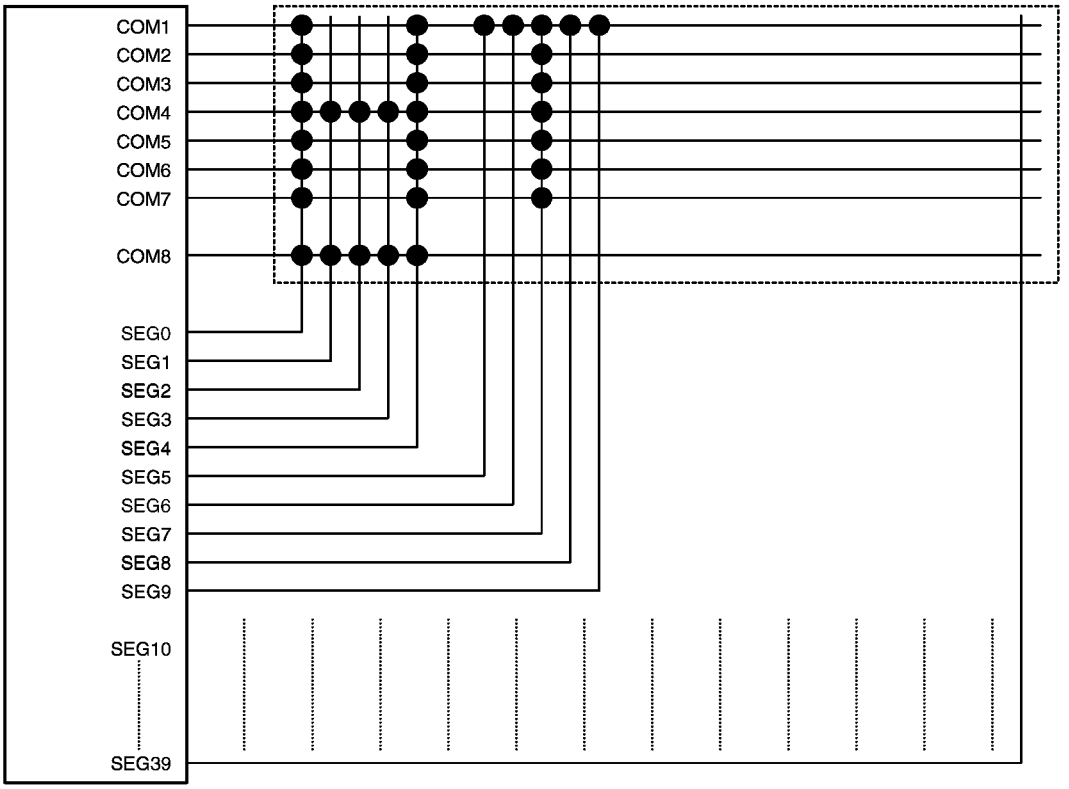
• Character codes and character patterns (ROM code: H00)

Upper 4 bits / Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

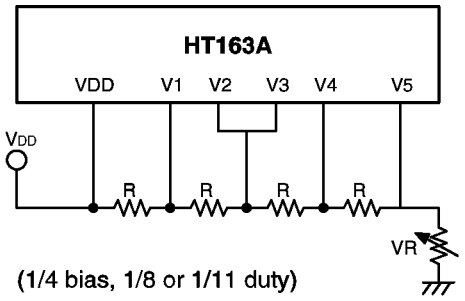
Application Circuits

Number of Lines	Character Font	Number of Common	Duty	Bias
1	5×8 dots+cursor	8	1/8	1/4
1	5×10 dots+cursor	11	1/11	1/4
2	5×8 dots+cursor	16	1/16	1/5

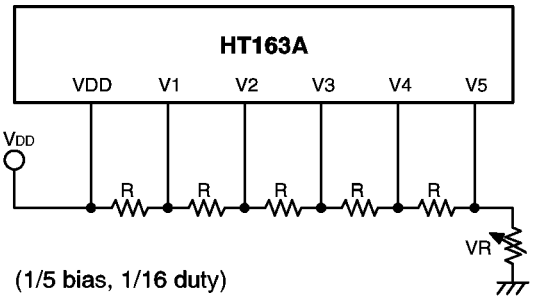
• LCD panel (5×8 dots, 8 characters × 1 line)



Bias voltage divider circuit

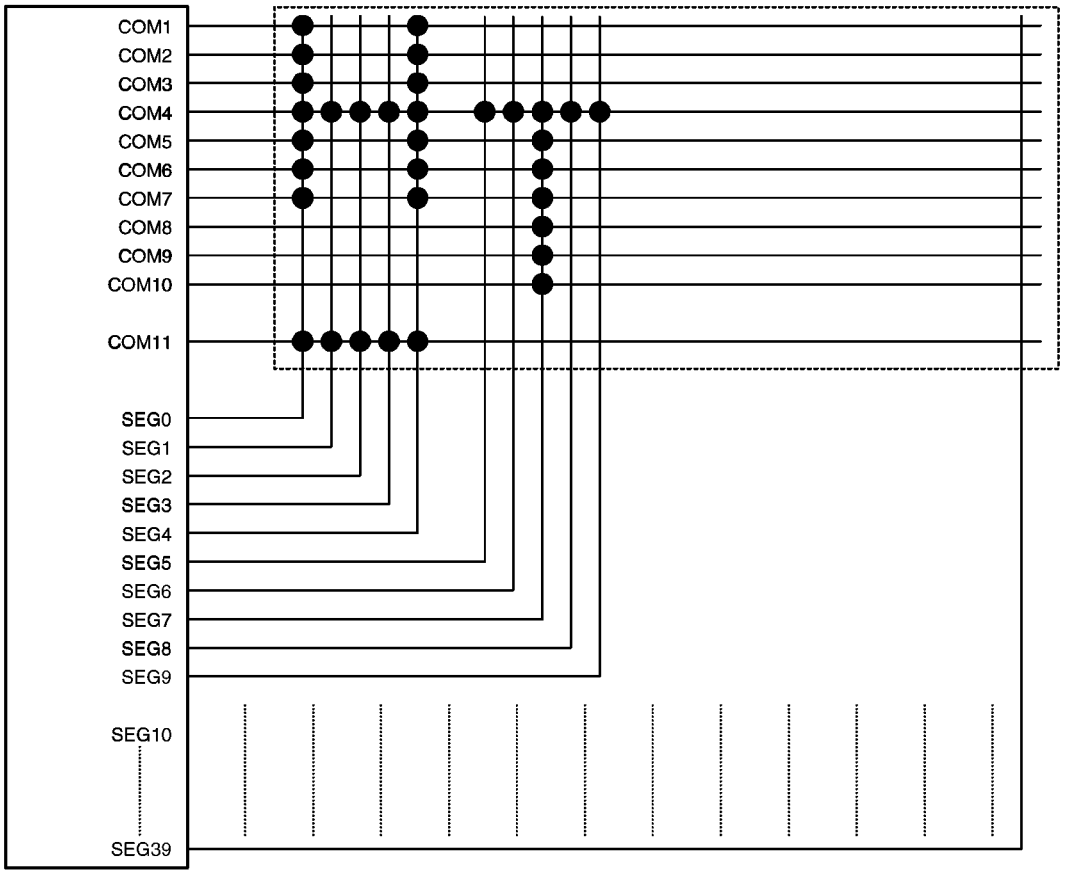


(1/4 bias, 1/8 or 1/11 duty)



(1/5 bias, 1/16 duty)

• LCD panel (5×10 dots, 8 characters × 1 line)



• LCD panel (5×8 dots, 8 characters × 2 lines)