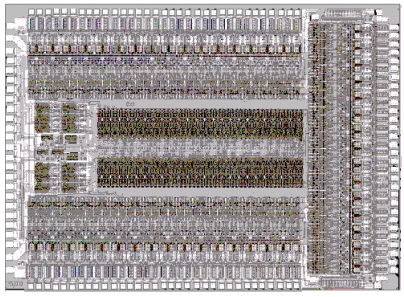
STV7610A

PLASMA DISPLAY PANEL DATA DRIVER

FEATURES

- 96 Output- Plasma Display Driver
- 100 V Absolute Maximum Rating
- 5 V Supply for Logic
- -70/+90 mA Source/sink Output MOS
- 6 bit Cascadable Data Bus (20 MHz)
- Blank, Polarity Control
- BCD Technology
- Packaging TQFP144 or Dic



DIE
ORDER CODE: STV7610A/WAF(1)
(1): Unsawn tested wafer

DESCRIPTION

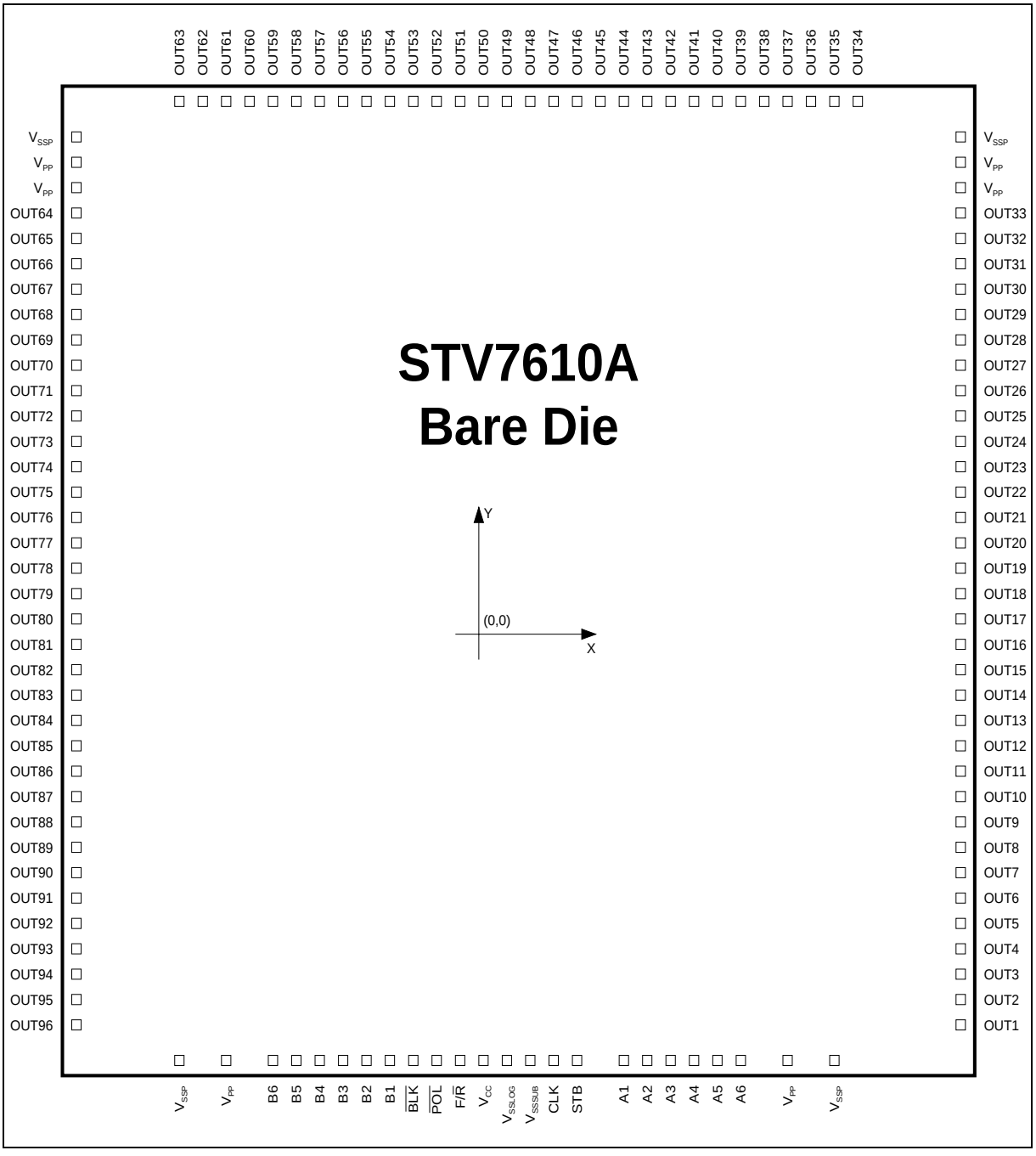
The STV7610A is a BCD data driver for Plasma Display Panel (PDP). Using a 6-bit wide cascadable data bus, it addresses 96 high current & high voltage outputs. By serially connecting several STV7610A, any horizontal pixel definition can be performed. The 20 MHz shift clock gives an equivalent 120 MHz shift register. The STV7610A is supplied with a separated 90 V power output supply and a 5 V logic supply. All command inputs are CMOS compatible.

version 4.7

Table of Contents

PIN CONNECTIONS

(DIE Pinout)



PAD COORDINATES

(in µm)

Pad positions from the middle of the top side

Name	Center		Size	
	X	Y	X	Y
OUT 48	74.0	3034.0	80.0	90.0
OUT 47	210.0	3034.0	80.0	90.0
OUT 46	346.0	3034.0	80.0	90.0
OUT 45	482.0	3034.0	80.0	90.0
OUT 44	618.0	3034.0	80.0	90.0
OUT 43	754.0	3034.0	80.0	90.0
OUT 42	890.0	3034.0	80.0	90.0
OUT 41	1026.0	3034.0	80.0	90.0
OUT 40	1162.0	3034.0	80.0	90.0
OUT 39	1298.0	3034.0	80.0	90.0
OUT 38	1434.0	3034.0	80.0	90.0
OUT 37	1570.0	3034.0	80.0	90.0
OUT 36	1706.0	3034.0	80.0	90.0
OUT 35	1842.0	3034.0	80.0	90.0
OUT 34	1993.0	3034.0	80.0	90.0

Pad positions along the right side

Name	Centre		Size	
	X	Y	X	Y
V_{SSP}	2116.0	2795.0	90.0	80.0
V_{PP}	2029.8	2496.5	90.0	90.0
V_{PP}	2041.5	1843.0	90.0	80.0
OUT 33	2117.0	1580.0	90.0	80.0
OUT 32	2117.0	1444.0	90.0	80.0
OUT 31	2117.0	1308.0	90.0	80.0
OUT 30	2117.0	1172.0	90.0	80.0
OUT 29	2117.0	1036.0	90.0	80.0
OUT 28	2117.0	900.0	90.0	80.0
OUT 27	2117.0	764.0	90.0	80.0
OUT 26	2117.0	628.0	90.0	80.0
OUT 25	2117.0	492.0	90.0	80.0
OUT 24	2117.0	356.0	90.0	80.0
OUT 23	2117.0	220.0	90.0	80.0
OUT 22	2117.0	84.0	90.0	80.0
OUT 21	2117.0	-52.0	90.0	80.0
OUT 20	2117.0	-188.0	90.0	80.0
OUT 19	2117.0	-324.0	90.0	80.0
OUT 18	2117.0	-460.0	90.0	80.0
OUT 17	2117.0	-596.0	90.0	80.0
OUT 16	2117.0	-732.0	90.0	80.0
OUT 15	2117.0	-868.0	90.0	80.0
OUT 14	2117.0	-1004.0	90.0	80.0
OUT 13	2117.0	-1140.0	90.0	80.0
OUT 12	2117.0	-1276.0	90.0	80.0
OUT 11	2117.0	-1412.0	90.0	80.0
OUT 10	2117.0	-1548.0	90.0	80.0
OUT 9	2117.0	-1684.0	90.0	80.0
OUT 8	2117.0	-1820.0	90.0	80.0
OUT 7	2117.0	-1956.0	90.0	80.0
OUT 6	2117.0	-2092.0	90.0	80.0
OUT 5	2117.0	-2228.0	90.0	80.0
OUT 4	2117.0	-2364.0	90.0	80.0
OUT 3	2117.0	-2500.0	90.0	80.0
OUT 2	2117.0	-2636.0	90.0	80.0
OUT 1	2117.0	-2832.0	90.0	80.0

Pad positions along the bottom side

Name	Centre		Size	
	X	Y	X	Y
V_{SSP}	1904.0	-3034.0	80.0	90.0
V_{PP}	1698.0	-3034.0	80.0	90.0
A6	1499.0	-3034.0	80.0	90.0
A5	1349.0	-3034.0	80.0	90.0
A4	1199.0	-3034.0	80.0	90.0
A3	1049.0	-3034.0	80.0	90.0
A2	899.0	-3034.0	80.0	90.0
A1	749.0	-3034.0	80.0	90.0
STB	449.0	-3034.0	80.0	90.0
CLK	299.0	-3034.0	80.0	90.0
GNDsub	156.5	-3034.0	80.0	90.0

Name	Centre		Size	
	X	Y	X	Y
GND	3.0	-3034.0	80.0	90.0
V_{CC}	-158.0	-3034.0	80.0	90.0
F/$\overline{R}$	-299.0	-3034.0	80.0	90.0
POL	-449.0	-3034.0	80.0	90.0
BLK	-599.0	-3034.0	80.0	90.0
B1	-749.0	-3034.0	80.0	90.0
B2	-899.0	-3034.0	80.0	90.0
B3	-1049.0	-3034.0	80.0	90.0
B4	-1199.0	-3034.0	80.0	90.0
B5	-1349.0	-3034.0	80.0	90.0
B6	-1499.0	-3034.0	80.0	90.0
V_{PP}	-1698.0	-3034.0	80.0	90.0
V_{SSP}	-1904.0	-3034.0	80.0	90.0

Pad Positions along the left side

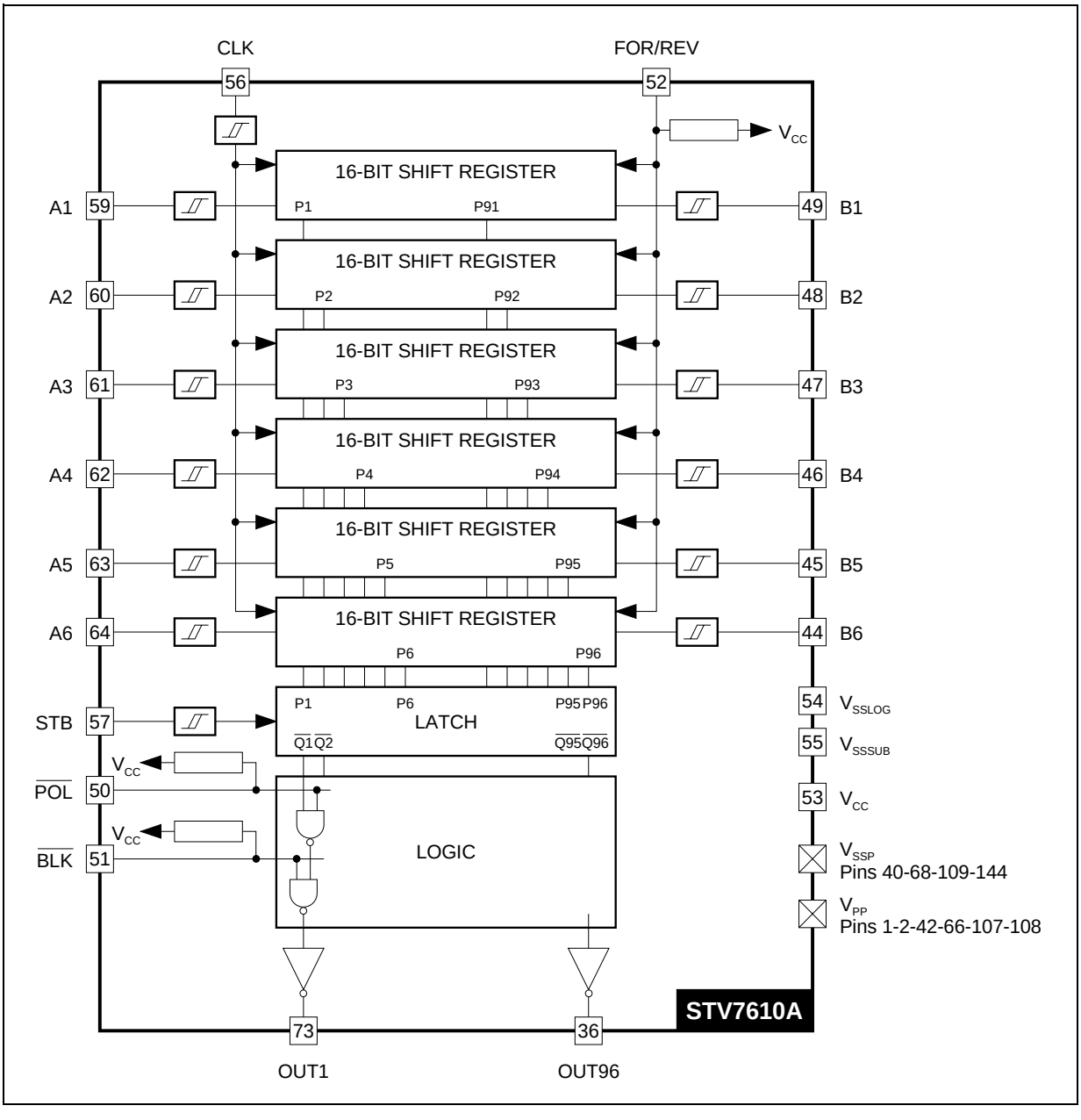
Name	Centre		Size	
	X	Y	X	Y
OUT 96	-2117.0	-2832.0	90.0	80.0
OUT 95	-2117.0	-2636.0	90.0	80.0
OUT 94	-2117.0	-2500.0	90.0	80.0
OUT 93	-2117.0	-2364.0	90.0	80.0
OUT 92	-2117.0	-2228.0	90.0	80.0
OUT 91	-2117.0	-2092.0	90.0	80.0
OUT 90	-2117.0	-1956.0	90.0	80.0
OUT 89	-2117.0	-1820.0	90.0	80.0
OUT 88	-2117.0	-1684.0	90.0	80.0
OUT 87	-2117.0	-1548.0	90.0	80.0
OUT 86	-2117.0	-1412.0	90.0	80.0
OUT 85	-2117.0	-1276.0	90.0	80.0
OUT 84	-2117.0	-1140.0	90.0	80.0
OUT 83	-2117.0	-1004.0	90.0	80.0
OUT 82	-2117.0	-868.0	90.0	80.0
OUT 81	-2117.0	-732.0	90.0	80.0
OUT 80	-2117.0	-596.0	90.0	80.0
OUT 79	-2117.0	-460.0	90.0	80.0
OUT 78	-2117.0	-324.0	90.0	80.0

Name	Centre		Size	
	X	Y	X	Y
OUT 77	-2117.0	-188.0	90.0	80.0
OUT 76	-2117.0	-52.0	90.0	80.0
OUT 75	-2117.0	84.0	90.0	80.0
OUT 74	-2117.0	220.0	90.0	80.0
OUT 73	-2117.0	356.0	90.0	80.0
OUT 72	-2117.0	492.0	90.0	80.0
OUT 71	-2117.0	628.0	90.0	80.0
OUT 70	-2117.0	764.0	90.0	80.0
OUT 69	-2117.0	900.0	90.0	80.0
OUT 68	-2117.0	1036.0	90.0	80.0
OUT 67	-2117.0	1172.0	90.0	80.0
OUT 66	-2117.0	1308.0	90.0	80.0
OUT 65	-2117.0	1444.0	90.0	80.0
OUT 64	-2117.0	1580.0	90.0	80.0
V_{PP}	-2041.5	1843.0	90.0	80.0
V_{PP}	-2029.8	2496.5	90.0	80.0
V_{SSP}	-2116.0	2795.0	90.0	80.0

Pad Positions along the top side

Name	Centre		Size	
	X	Y	X	Y
OUT 63	-1980.0	3034.0	80.0	90.0
OUT 62	-1830.0	3034.0	80.0	90.0
OUT 61	-1694.0	3034.0	80.0	90.0
OUT 60	-1558.0	3034.0	80.0	90.0
OUT 59	-1422.0	3034.0	80.0	90.0
OUT 58	-1286.0	3034.0	80.0	90.0
OUT 57	-1150.0	3034.0	80.0	90.0
OUT 56	-1014.0	3034.0	80.0	90.0
OUT 55	-878.0	3034.0	80.0	90.0
OUT 54	-742.0	3034.0	80.0	90.0
OUT 53	-606.0	3034.0	80.0	90.0
OUT 52	-470.0	3034.0	80.0	90.0
OUT 51	-334.0	3034.0	80.0	90.0
OUT 50	-198.0	3034.0	80.0	90.0
OUT 49	-62.0	3034.0	80.0	90.0

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The STV7610A contains all the logic and the power circuits necessary to drive the columns of a Plasma Display Panel (P. D. P.). The binary value of each pixel of the displayed line is loaded into the shift register. Data are input in a 6-bit wide data bus to A1 - A6 input (case of forward shift mode). Data are shifted at each low to high transition of the CLK shift clock. After 16 shifts the first data are available on B1 - B6 outputs. These B1 - B6 outputs can be used to cascade several drivers to perform any horizontal resolution. The forward/reverse (F/$\overline{R}$) input is used to select the direction of the shift register, A1 - A6 and B1 - B6 data bus input/output status is set according to the selected direction. F/$\overline{R}$= H, A is an input and B is an output.

Serial inputs, CLK, STB inputs are Smith trigger inputs. If not used in the application, Blanking ($\overline{BLK}$), Polarity ($\overline{POL}$ are internally pulled to level “H”. The maximum frequency of the shift clock is 20 MHz. This leads to an equivalent 120 MHz serial shift register.

On low level of STB, data is transferred from shift register to the latch stage. Data will not be refreshed as long as STB is kept high.

Blanking input ($\overline{BLK}$) forces the power outputs to low level when pulled low. All the power outputs are set at high level when the Polarity command ($\overline{POL}$) is pulled low and the Blanking ($\overline{BLK}$) input is at high level.

V_{SSSUB} and V_{SSLOG} must be connected as close as possible to the logical reference ground of the application.

Shift Register Truth Table

Input		Input/Output		Shift Register Function
F/$\overline{R}$	**CLK**	**A**	**B**	**Output Q**
H	Rise	IN	OUT	Forward shift
H	H or L	IN	OUT	Steady
L	Rise	OUT	IN	Reverse shift
L	H or L	OUT	IN	Steady

Power Output Truth Table

Qn	STB	$\overline{BLK}$	$\overline{POL}$	Driver Output	Comments
X	X	L	X	L	Output low
X	X	H	L	H	Output high
X	H	H	H	Qn	Data latched
L	L	H	H	L	Data copied
H	L	H	H	H	Data copied

Note 1 Qn+1 = A1, Qn + 2 = A2, Qn + 3 = A3, Qn + 4 = A4, Qn + 5 = A5, Qn + 6 = A6, n = [0,6,12,18,...,90]

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply Range (Pin 53)	-0.3, +7	V
OUTi	Output Pins (4 to 36, 73 to 105, 112 to 141)	-0.3, +100	V
V_{IN}	Logic Input Voltage (Pins 50, 51, 52, 56, 57, 59 to 64)	-0.3, $+V_{CC}$ +0.3	V
V_{OUT}	Logic Output Voltage (Pin 44 to 49)	-0.3, $+V_{CC}$ + 0.3	V
I_{POUT}	Driver Output Current (Note 2) (Note 4) (Note 5)	-150/ +150	mA
I_{DOUT}	Diode Output Current (Note 3) (Note 4) (Note 5)	-200/ +300	mA
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	-20, +85	°C
T_{stg}	Storage Temperature	-50, +150	°C

Note 2 Through one power output (all power outputs).

Note 3 Through one power output for all power outputs (see Test Diagram) with Junction temperature lower or equal than $T_j$max.

Note 4 These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

Note 5 Transient current. Spike current duration inferior to 300ns.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, V_{PP} = 90 V, V_{SSP} = 0 V, V_{SSLOG} = 0 V, V_{SSSUB} = 0 V, T_{amb} = 25°C, f_{CLK} = 20 MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current (all inputs high)		-	-	100	µA
I_{CCL}	Logic Dynamic Supply Current	f_{CLK} = 20 MHz	-	26	-	mA
V_{PP}	Power Output Supply Voltage		15	-	90	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	µA
OUTPUT (V_{PP} = 15 V to 90 V)						
OUT 1- OUT 96						
V_{POUTH}	Power Output Voltage Drop (High Level) (versus V_{PP})	I_{POUTH} = - 30 mA I_{POUTH} = - 45mA	- -	4.0 4.5	6.0 6.5	V V
V_{POUTL}	Power Output Voltage Drop (Low Level)	I_{POUTL} = + 30 mA	-	1.6	4	V
V_{DOUTH}	Output Diode Voltage (High Level)	I_{DOUTH} = +45 mA (Figure 2)	-	1.05	4	V
V_{DOUTL}	Output Diode Low Level	I_{DOUTL} = - 30mA (Figure 2)	-	-0.95	-4	V
A1-A6, B1-B6						
V_{OH}	Logic Output (High Level)	I_{OH} = -1 mA	4	4.2	-	V
V_{OL}	Logic Output (Low Level)	I_{OL} = +1 mA	-	0.12	0.4	V
INPUT						
CLK, F/$\overline{R}$, STB, $\overline{POL}$, $\overline{BLK}$, A1-A6, B1-B6						
V_{IH}	Input Voltage (High Level)		0.8 V_{CC}	-	-	V
V_{IL}	Input Voltage (Low Level)		-	-	0.2V_{CC}	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	-	-	10	µA
I_{IL}	Low Level Input Current CLK, A1-A6, B1-B6, STB, F/$\overline{R}$, $\overline{BLK}$, $\overline{POL}$	V_{IL} = 0 V	 - -	 - -	 -10 -40	 µA µA

AC TIMINGS REQUIREMENTS

(V_{CC} = 4.5 V to 5.5 V, T_{amb} = -20 to +85°C, input signals max leading edge & trailing edge (t_R, t_F) = 10 ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WHCLK}	Duration of clock (CLK) pulse at high level	15	-	-	ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	15	-	-	ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	10	-	-	ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	10	-	-	ns
t_{SFR}	Forward/$\overline{reverse}$ (F/$\overline{R}$) Set-up Time before clock (low to high) transition	100	-	-	ns
t_{DSTB}	Minimum Delay to latch $\overline{STB}$ after clock (low to high) transition	10	-	-	ns
t_{SSTB}	Minimum Delay to latch $\overline{STB}$ before clock (low to high) transition	10	-	-	ns
t_{STB}	Latch $\overline{STB}$ Low Level Pulse Duration	20	-	-	ns
t_{BLK}	Blanking $\overline{BLK}$ Pulse Duration	500	-	-	ns
t_{POL}	Polarity $\overline{POL}$ Pulse Duration	500	-	-	ns

AC TIMINGS CHARACTERISTICS

(V_{CC} = 5 V, V_{PP} = 90 V, V_{SPP} = 0 V, V_{SSLOG} = 0 V, V_{SSSUB} = 0 V, T_{amb} = 25°C)

($V_{IL(Max.)}$ = 0.2 Vcc, $V_{IH(Min.)}$ = 0.8 V_{CC}, V_{OH} = 4.0V, V_{OL} = 0.4 V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data clock Period	50	-	-	ns
t_{RDAT}	Logical Data Output Rise Time (CL=10pF)	-	12	20	ns
t_{FDAT}	Logical Data Output Fall Time (CL=10pF)	-	11	20	ns
t_{PHL1} t_{PLH1}	Delay of logic data output (high to low transition) after clock (CLK) transition Note 6 Delay of logic data output (low to high transition) after clock (CLK) transition Note 6	15 15	35 35	50 50	ns ns
t_{PHL2} t_{PLH2}	Delay of power output change (high to low transition) after clock (CLK) transition Delay of power output change (low to high transition) after clock (CLK) transition	- -	135 80	180 180	ns ns
t_{PHL3} t_{PLH3}	Delay of power output change (high to low transition) after Latch (STB) transition Delay of power output change (low to high transition) after Latch (STB) transition	- -	115 70	165 165	ns ns
t_{PHL4} t_{PLH4}	Delay of power output change (high to low transition) to Blank or Polarity ($\overline{BLK}$,$\overline{POL}$) transition Delay of power output change (low to high transition) to Blank or Polarity ($\overline{BLK}$,$\overline{POL}$) transition	- -	100 55	160 160	ns ns
t_{ROUT}	Power Output Rise Time (Note 7)	-	50	150	ns
t_{FOUT}	Power Output Fall Time (Note 7)	-	80	200	ns

Note 6 For IC in cascading configuration and in case a time delay is inserted on the clock signal of the cascaded IC, the maximum value of this time delay must be set at the minimum value of t_{PHL1}, t_{PLH1} (Figure 7).

Note 7 One output among 96, loading capacitor C_L = 50pF, other outputs at low level.

Figure 1: AC Characteristics Waveform

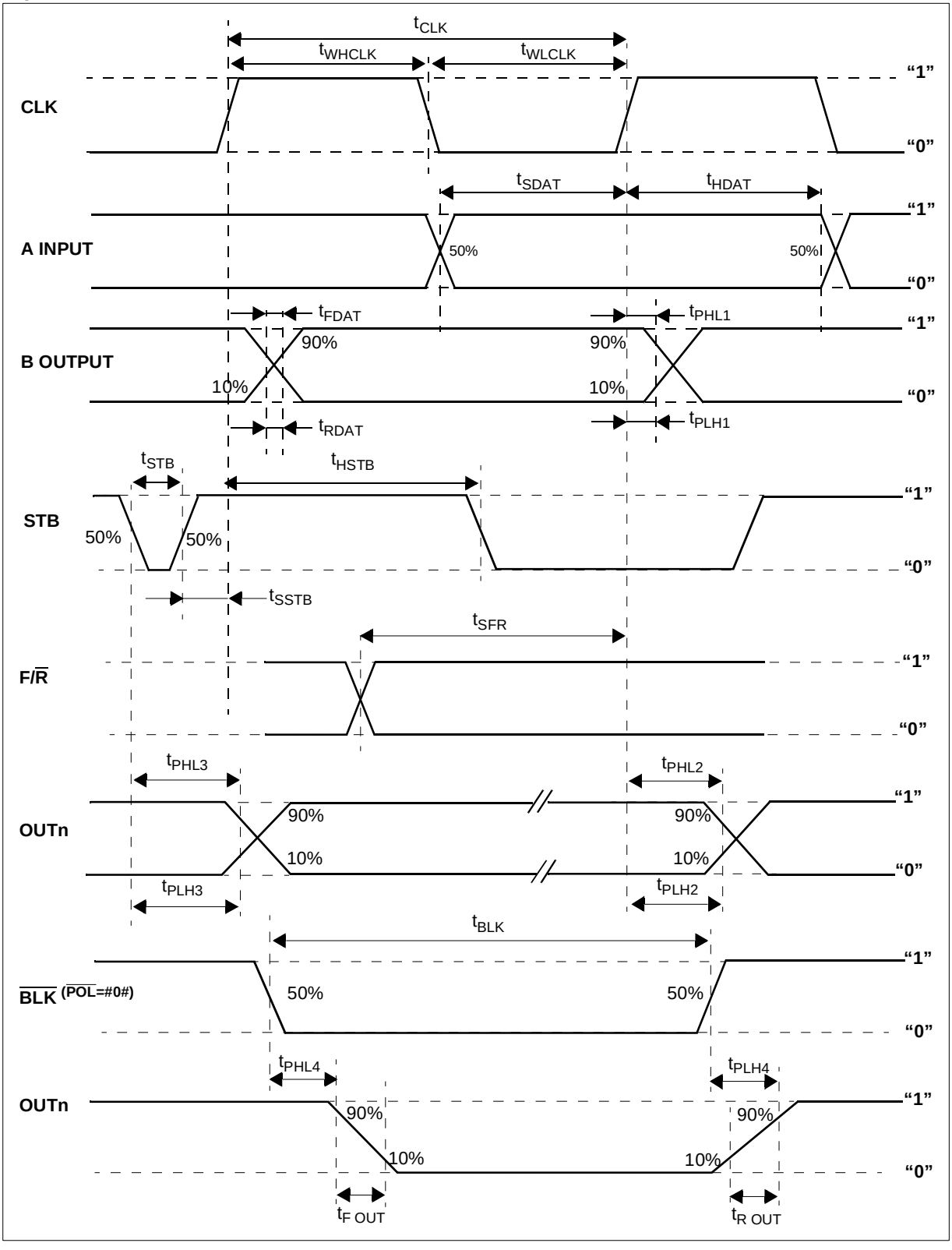
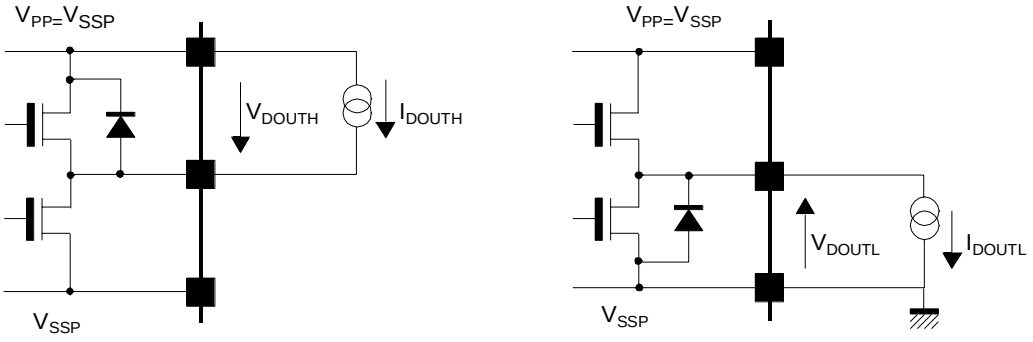


Figure 2: Test Configuration



Output sinking current as positive value, sourcing current as negative value

INPUT/OUTPUT SCHEMATICS

Figure 3: $\overline{POL}$, $\overline{BLK}$, F/$\overline{R}$ Input

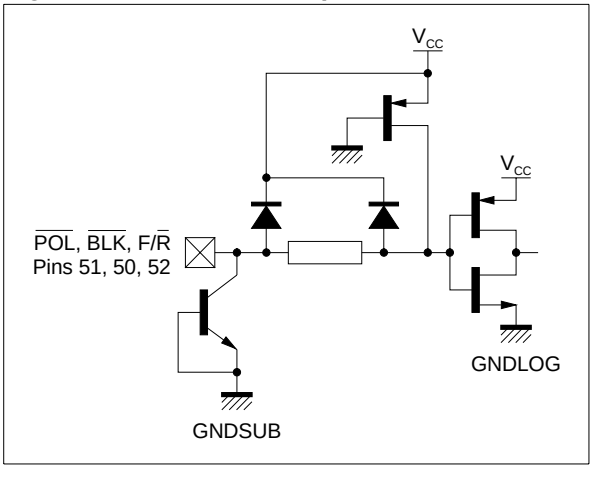


Figure 4: CLK, STB Input

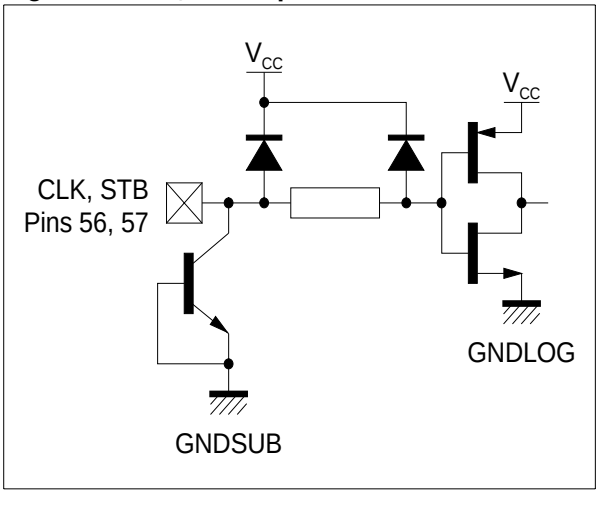


Figure 5: A1 to A6, B1 to B6

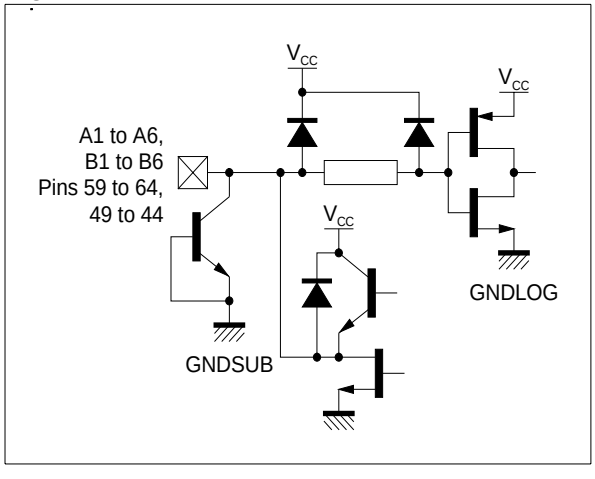


Figure 6: Power Output

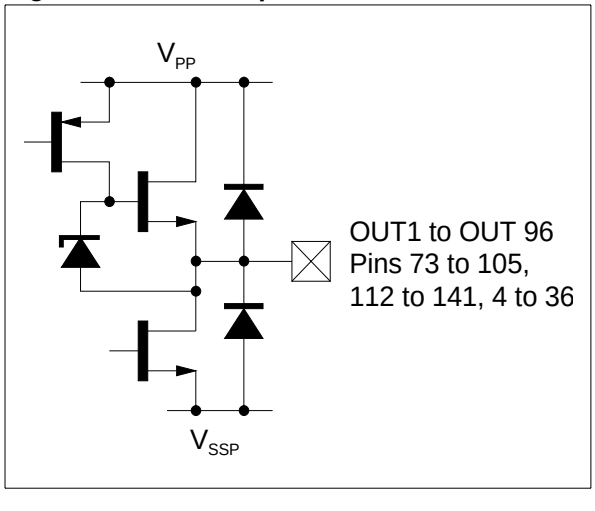
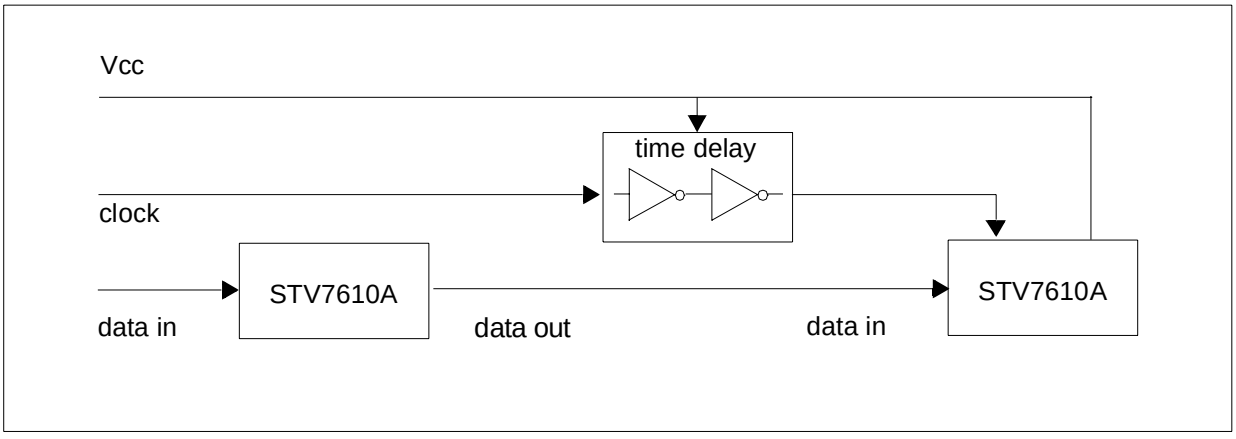


Figure 7: IC cascading mode suggestion



TESTED WAFER DISCLAIMER

All wafers are tested and guaranteed to comply with all datasheet limits up to the point of wafer sawing for a period of ninety (90) days from the delivery date.

We remind you that it is the customer's responsibility to test and qualify their application in which the die is used. ST Microelectronics is ready to support the customer when qualifying the product.