ExpressLane PEX 8114BC
PCI Express-to-PCI/PCI-X Bridge
Data Book

Version 3.0

January 2007

Website www.plxtech.com

Technical Support www.plxtech.com/support

Phone 800 759-3735

408 774-9060

FAX 408 774-2169

Copyright Information

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Revision History

Version	Date	Description of Changes
1.0	June, 2006	Initial production release, Silicon Revision BA.
1.1	August, 2006	Added notes regarding NT mode errata. Revised Register 17-12, offset 30h **Expansion ROM Base Address**. Updated miscellaneous electrical specifications. Added pull-up information for JTAG_TCK, and removed pull-up information from EE_PR# and all Hot Plug outputs. Moved thermal resistance information to Chapter 20 (from Chapter 19) and added heat sink-related information. Miscellaneous corrections throughout the data book.
2.0	December, 2006	Production release, Silicon Revision BB. Removed support for Silicon Revision BA and Non-Transparent mode. Miscellaneous corrections and enhancements throughout data book.
3.0	January, 2007	Production release, Silicon Revision BC.

Preface

The information contained in this document is subject to change without notice. This document is periodically updated as new information is made available.

Audience

This data book provides the functional details of the PLX ExpressLane PEX 8114BC PCI Express-to-PCI/PCI-X Bridge, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc.

  870 W Maude Avenue, Sunnyvale, CA 94085 USA

  Tel: 800 759-3735 (domestic only) 408 774-9060, Fax: 408 774-2169, www.plxtech.com

  – *PEX 8114BC Design Checklist Application Note*
  – *PEX 8114BC Errata*

  The PLX PEX 8114 Toolbox includes other PEX 8114 documentation as well.
- PCI Special Interest Group (PCI-SIG)

  3855 SW 153rd Drive, Beaverton, OR 97006 USA

  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com

  – *PCI Local Bus Specification, Revision 2.3*
  – *PCI Local Bus Specification, Revision 3.0*
  – *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
  – *PCI Express Card Electromechanical (CEM) Specification, Revision 1.1*
  – *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  – *PCI Bus Power Management Interface Specification, Revision 1.2*
  – *PCI Hot Plug Specification, Revision 1.1*
  – *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
  – *PCI-X Addendum to PCI Local Bus Specification, Revision 1.0b*
  – *PCI-X Addendum to PCI Local Bus Specification, Revision 2.0a*
  – *PCI Express Base Specification, Revision 1.0a*
  – *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
  – *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a*
- The Institute of Electrical and Electronics Engineers, Inc.

  445 Hoes Lane, Piscataway, NJ 08854-4141 USA

  Tel: 800 701-4333 (domestic only) or 732 981-0060, Fax: 732 981-9667, www.ieee.org

  – *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  – *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  – *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*
  – *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*

Supplemental Documentation Abbreviations

In this data book, shortened titles are provided to the previously listed documents. The following table defines these abbreviations.

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI ExpressCard CEM r1.0a	*PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a*
PCI ExpressCard CEM r1.1	*PCI Express Card Electromechanical (CEM) Specification, Revision 1.1*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Mgmt. r1.2	*PCI Bus Power Management Interface Specification, Revision 1.2*
PCI Hot Plug r1.1	*PCI Hot Plug Specification, Revision 1.1*
PCI Standard Hot Plug Controller and Subsystem r1.0	*PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
PCI-X r1.0b	*PCI-X Addendum to PCI Local Bus Specification, Revision 1.0b*
PCI-X r2.0a	*PCI-X Addendum to PCI Local Bus Specification, Revision 2.0a*
PCI Express r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express-to-PCI/PCI-X Bridge r1.0	*PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*

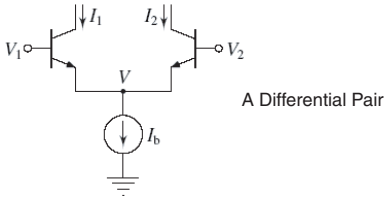
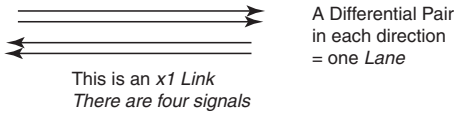
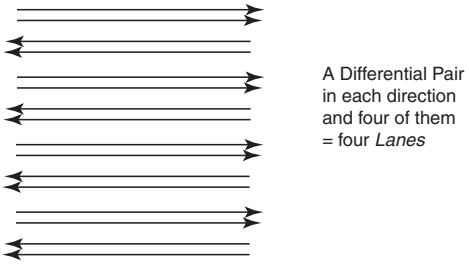
Data Assignment Conventions

Data Width	PEX 8114 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	DWORD/DWord

Terms and Abbreviations

The following table defines common terms and abbreviations used in this document. Terms and abbreviations defined in the *PCI Express r1.0a* are not included in this table.

Terms and Abbreviations	Definition
#	Active-Low signal.
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges signal receipt.
ADB	Allowable Disconnect Boundary.
ADQ	Allowable Disconnect Quantity. In the PCI Express interface, the ADQ is a buffer size, which is used to indicate memory requirements or reserves.
BAR	Base Address Register.
BCR	Bridge Control Register of the Type 1 CSR space.
Bridge, Transparent	Provides connectivity from the Conventional PCI or PCI-X Bus system to the PCI Express hierarchy or subsystem. The bridge not only converts the physical bus to PCI Express point-to-point signaling, it also translates the PCI or PCI-X Bus protocol to PCI Express protocol. The Transparent bridge allows the Address domain on one side of the bridge to be mapped into the CPU system hierarchy on the primary side of the bridge.
Cold Reset	A "Fundamental Reset" following the application of power.
Completer	Device addressed by a requester.
CPL	Completion Transaction.
CRC	Cyclic Redundancy Check
CSR	Configuration Status Register; Control and Status Register; Command and Status Register.
DL_Down	Data Link Layer is down (a PCI Express link/port status).
DLLP	Data Link Layer Packet (originate at the Data Link Layer); allow Flow Control (FCx DLLPs) to acknowledge packets (ACK and NAK DLLPs); and Power Management (PMx DLLPs).
DW	DWord.
ECC	Error Checking and Correction.
EEPROM	Electrically Erasable Programmable Read-Only Memory.
Endpoint	Device, other than the Root Complex and switches that are requesters or completers of PCI Express transactions. • Endpoints can be PCI Express endpoints or Conventional PCI endpoints. • Conventional PCI endpoints support I/O and Locked transaction semantics. PCI Express endpoints do not.
FCP	Flow Control Packet devices on each link exchange FCPs, which carry *Header* and *Data Payload* credit information for one of three packet types – Posted requests, Non-Posted requests, and Completions.
Fundamental Reset	The mechanism of setting or returning all registers and state machines to default/initial conditions, as defined in all PCI Express, PCI, PCI-X and Bridge specifications. This mechanism is implemented by way of the PEX_PERST# Input ball/signal.
Host	A Host computer provides services to computers that connect to it on a network. It is considered in charge over the remainder of devices connected on the bus.
Hot Reset	A reset propagated in-band across a Link using a Physical Layer mechanism (Training Sequence).

Terms and Abbreviations	Definition
I	CMOS Input.
I/O	CMOS Bi-Directional Input/Output.
INCH	Ingress Credit Handler.
ITCH	Internal Credit Handler.
Lane	Differential signal pair in each direction.
Layers	PCI Express defines three layers: • ***Transaction Layer –*** Provides assembly and disassembly of TLPs, the major components of which are Header, Data Payload, and an optional Digest Field. • ***Data Link Layer –*** Provides link management and data integrity, including error detection and correction. Defines the data control for PCI Express. • ***Physical Layer –*** Appears to the upper layers as *PCI*. Connects the lower protocols to the upper layers.
Link	Physical connection between two devices that consists of x*N* ***lanes***. • A x1 link consists of 1 Transmit and 1 Receive signal, where each signal is a differential pair. This is one lane. There are four lines or signals in a x1 link. • A x4 link contains four lanes or four differential signal pairs for each direction, for a total of 16 lines or signals.   
LLIST	Link List.
LVDSRn	Differential low-voltage, high-speed, LVDS negative Receiver Inputs.
LVDSRp	Differential low-voltage, high-speed, LVDS positive Receiver Inputs.
LVDSTn	Differential low-voltage, high-speed, LVDS negative Transmitter Outputs.
LVDSTp	Differential low-voltage, high-speed, LVDS positive Transmitter Outputs.

Terms and Abbreviations	Definition
MAM	Master Abort Mode.
MSI	Message Signaled Interrupt.
MWI	Memory Write and Invalidate.
NAK	Negative Acknowledge.
Non-Posted Request Packet	Packet transmitted by a requester that has a Completion packet returned by the associated completer.
NPR	Non-Posted Request.
NS	No Snoop.
O	CMOS Output.
OD	Open Drain Output.
Packet Types	There are three packet types: • ***TLP***, Transaction Layer Packet • ***DLLP***, Data Link Layer Packet • ***PLP***, Physical Layer Packet
PCI	Peripheral Component Interconnect. A PCI Bus is a high-performance, 32- or 64-bit bus. It is designed to use with devices that contain high-bandwidth requirements; *for example*, the display subsystem. A PCI Bus is an I/O bus that can be dynamically configured.
PCI	PCI/PCI-X Compliant.
PCI-X	Peripheral Component Interconnect. An extension to PCI, designed to address the need for the increased bandwidth of PCI devices.
PEX	PCI Express.
Port	Interface between a PCI Express component and the link, and consists of transmitters and receivers. • An ***ingress*** port receives a packet. • An ***egress*** port that transmits a packet.
Posted Request Packet	Packet transmitted by a requester that does have a Completion packet returned by the associated completer.
PR	Posted Request.
PU	Signal is internally pulled up.
QoS	Quality of Service.
RC	Root Complex. Device that connects the CPU and Memory subsystem to the PCI Express fabric, which supports one or more PCI Express ports.
RCB	Read Completion Boundary.
Requester	Device that originates a transaction or places a transaction sequence into the PCI Express fabric.
RO	Relaxed Ordering.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RX	Receiver.
SOPS	Station Operations block.

Terms and Abbreviations	Definition
Sticky bits	Status bits that are reset to default on a fundamental reset. Sticky bits are not modified or initialized by a reset, except a fundamental reset. Devices that consume AUX power preserve register values when AUX power consumption is enabled (by way of AUX power or PME Enable). HwInit, ROS, R/WS. and R/W1CS CSR types. (Refer to Table 14-2 for CSR type definitions.)
STRAP	Strapping pads must be tied High to VDD33 or Low to VSS on the board.
STS	PCI-X Sustained Three-State Output, driven High for One CLK before Float.
Switch	Device that appears to software as two or more logical PCI-to-PCI bridges.
TC	Traffic Class.
TLP	Translation Layer Packet.
TP	Totem Pole.
TS	Three-State Bi-Directional.
TX	Transceiver.
VC	Virtual Channel.
Warm Reset	“Fundamental Reset” without cycling the supplied power.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXp[3:0]	When the signal name appears in all CAPS, with the primary port description listed first, field [3:0] indicates the number of signal balls/pads assigned to that port. The lowercase "p = positive" or "n = negative" suffix indicates the differential pair of signal, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to memory sizes (binary notation)
1Fh	h = suffix which identifies hex values. Each prefix term is equivalent to a 4-bit binary value (nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 or 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes)
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	DWord (32 bits) is the primary register size in these devices.
Reserved	Do not modify ***reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.

Contents

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Registers

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Chapter 1 Introduction

1.1 Features

The PLX ExpressLane™ PEX 8114 PCI Express-to-PCI/PCI-X Bridge supports the following features:

- Four full-duplex PCI Express Lanes
- 8b/10b encoding, 2.5 Gbps bandwidth
- Four integrated SerDes on bridge
- x1, x2, or x4 port lane width, established during link auto-negotiation
- Lane reversal
- Lane polarity inversion
- Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3
- PCI Express 256-byte Maximum Payload Size
- Read Completion supported for all eight (8) traffic classes
- One Virtual Channel (VC0)
- TLP Digest
- End-to-end CRC checking
- Data poisoning
- Baseline and Advanced Error Reporting capability
- SPI/serial EEPROM for initialization
- JTAG
- PCI Bus Clock Master and Slave
- Data rates
  - Conventional PCI – 25, 33, 50, and 66 MHz
  - PCI-X – 50, 66, 100, and 133 MHz
- Arbitration
  - Internal arbitration (four REQ/GNT external pairs) that can be enabled or disabled
  - External arbitration accepted
- Message Signaled Interrupts (MSI)
- 64-bit data width
- Dual Address Cycles (DAC)
- 64-bit addressing as Master and Slave
- Maximum 4-KB Master Writes and Reads on PCI-X Bus
- Eight outstanding Split transactions on primary side, and eight outstanding Split transactions on secondary side
- Address stepping and IDSEL stepping
- One Type 1 Configuration Space Header
- Forward and Reverse Transparent Bridge modes (primary or secondary interface)
- All Completions to PCI Express transactions are assigned to the Traffic Class on which they originated
- Clocks up to four external PCI/PCI-X devices
- Prefetchable Memory Address range

- Transaction Ordering and Deadlock Avoidance rules
- Oversubscribe and Flood modes
- ECC checking on destination packet RAM
- Standard 256-ball PBGA package (17 x 17 mm)
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 2.3 (PCI r2.3)*
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.0a (PCI ExpressCard CEM r1.0a)*
  - *PCI Express Card Electromechanical (CEM) Specification, Revision 1.1 (PCI 2.0 CEM r1.1)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1 (PCI-to-PCI Bridge r1.1)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI Hot Plug Specification, Revision 1.1 (PCI HotPlug 1.1)*
  - *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0 (Hot Plug r1.0)*
  - *PCI-X Addendum to PCI Local Bus Specification, Revision 1.0b (PCI-X r1.0b)*
  - *PCI-X Addendum to PCI Local Bus Specification, Revision 2.0a (PCI-X r2.0a)*
  - *PCI Express Base Specification, Revision 1.0a (PCI Express Base 1.0a)*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 (PCI Express-to-PCI/PCI-X Bridge r1.0)*
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990 (IEEE Standard 1149.1-1990)*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1993)*
  - *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions (IEEE Standard 1149.1-1990)*
  - *IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*

1.2 PEX 8114 Serial PCI Express to PCI/PCI-X Bridge

The PEX 8114 is a high-performance bridge that enables designers to migrate Conventional PCI and PCI-X Bus interfaces to the new advanced serial PCI Express.

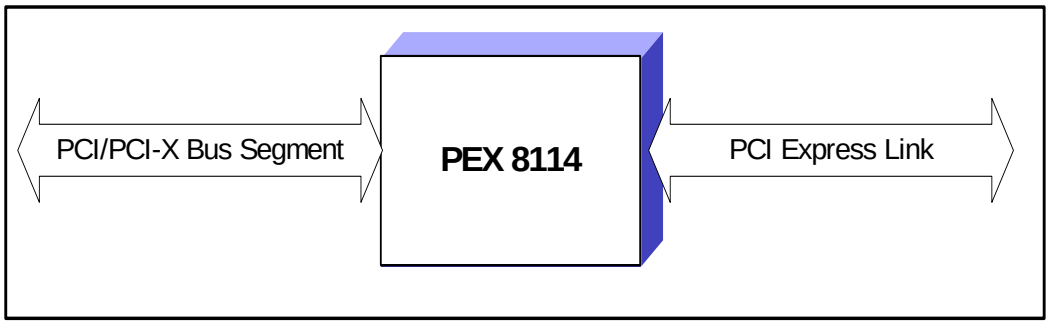
This simple two-port device is equipped with a standard, but flexible, PCI Express port that scales from 2.5 to 10 Gbps maximum bit rate. Supporting standard PCI Express signaling, these bandwidths are achieved with the lowest possible ball count (16 balls), using LVDS technology.

The single parallel bus segment supports the advanced PCI-X protocol. Conventional PCI and PCI-X interfaces can reach 8-Gbps bandwidth, using a 64-bit wide parallel data path at a clock frequency of 133 MHz.

While both sides of the bridge are evenly matched, the PEX 8114 also supports internal queues with Flow Control (FC) features to optimize throughput and traffic flow.

The PEX 8114 is available in a standard 256-ball Plastic Ball Grid Array (BGA) package. The small footprint and low-power consumption make the PEX 8114 an ideal bridge for use on adapter board, daughter board, add-on module, and backplane designs, as well as on larger planar boards.

Figure 1-1. PEX 8114 – Two-Port Device



1.2.1 Introduction to PEX 8114 Operation

The PEX 8114 is a PCI Express-to-PCI-X bridge that provides a functional link from a PCI or PCI-X Bus segment to a PCI Express port. This port can be configured as x1, x2, or x4 2.5 Gbps lanes. The PCI Express port conforms to the *PCI Express r1.0a.*

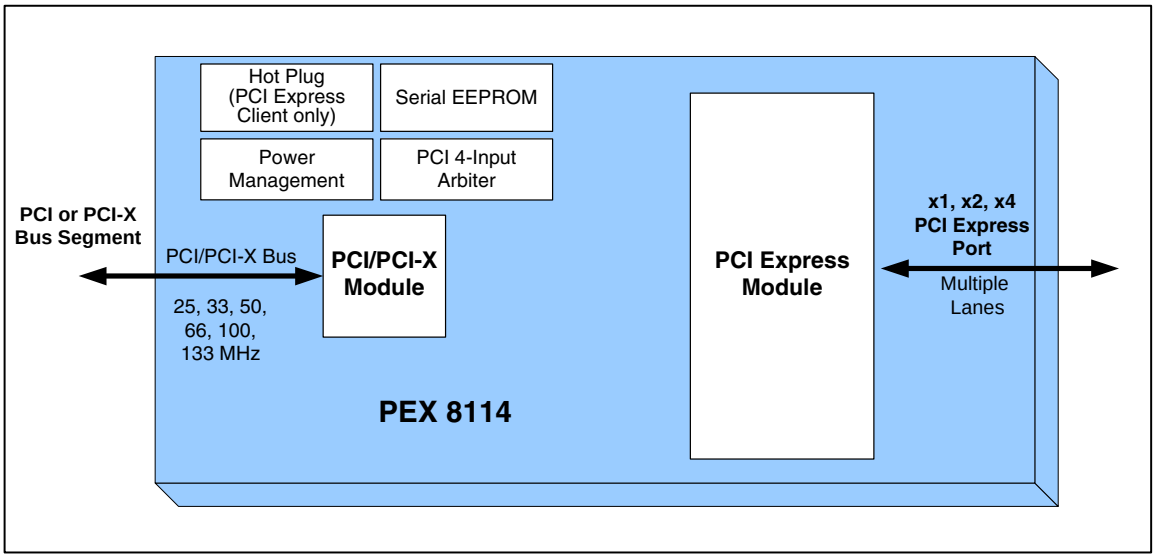
Data received by the PCI/PCI-X input from an external PCI/PCI-X Bus is delivered to the PCI Express port.

There are several Data Transfer modes that the PEX 8114 supports as it transfers data between PCI-X and PCI Express.The PEX 8114 can operate as a Forward or Reverse bridge (by way of ball strap).

- As a *Forward bridge*, Configuration accesses are transmitted from the PCI Express Root Complex
- As a *Reverse bridge*, Configuration accesses are transmitted from the PCI-X Bus
- In addition to Forward and Reverse bridging, the PEX 8114 also operates as a Transparent bridge:
  - If a Type 1 Configuration access is seen, if it matches the host secondary bus, the Type 1 Configuration access is changed to a Type 0 Configuration access and accepted
  - If the Type 1 Configuration access is for some destination further down the bus hierarchy, the Type 1 Configuration access is maintained and passed along

Figure 1-2 provides a PEX 8114 top-level block diagram.

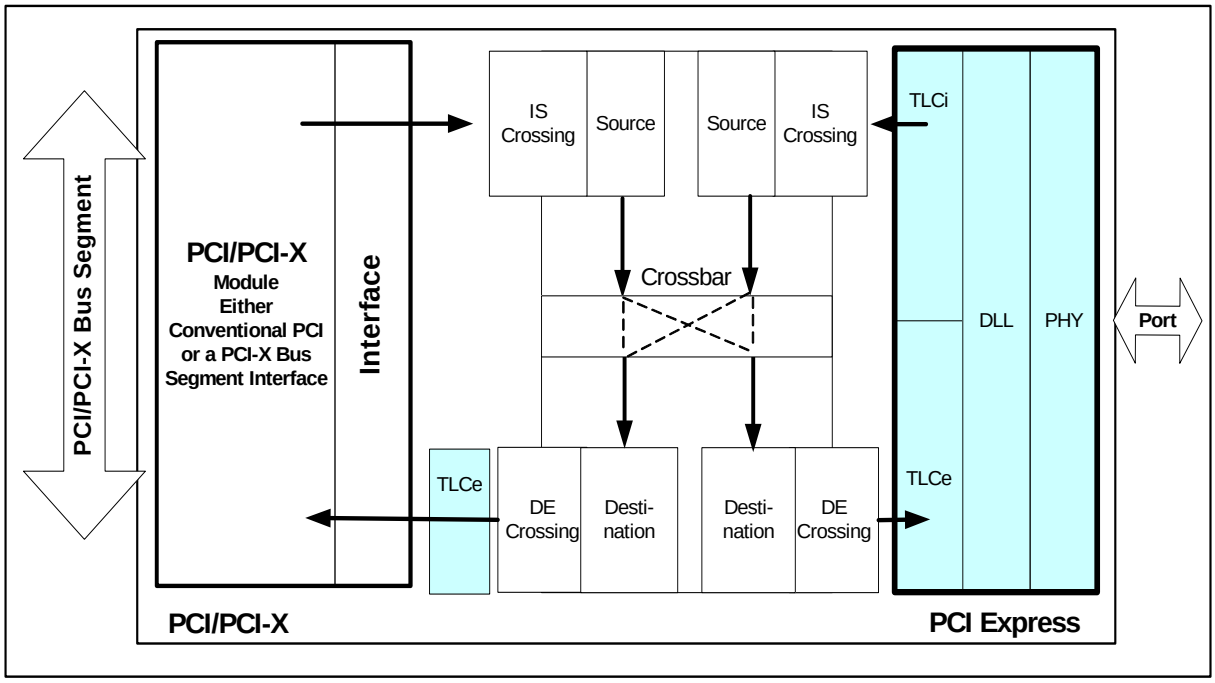
Figure 1-2. PEX 8114 Top-Level Block Diagram



1.3 Detailed Block Diagram

Figure 1-3 illustrates PEX 8114 implementation, with the modules at the data transfer core. Other modules, *such as* the PCI-X Arbiter and Power Management, are not included in Figure 1-3.

Figure 1-3. PEX 8114 Top-Level Detailed Block Diagram



1.3.1 Physical Layer – Layer 1

Layer 1 – Physical Layer (PHY) – defines the PCI Express electrical characteristics. The basic transmission unit consists of two pairs of wires, called a *lane*. Each pair is equipped with unidirectional data transmission at 2.5 Gbps, allowing the two wire pairs, when combined, to provide 2.5 Gbps full-duplex communication, without the risk of transmission collision.

1.3.2 Data Link Layer – Layer 2

Layer 2 – Data Link Layer (DLL) – defines the PCI Express data control. The Data Link Layer provides link management and data integrity, including error detection and correction. This layer calculates and appends a Cyclic Redundancy Check (CRC) and Sequence Number to the information transmitted from the Data packet. The CRC verifies that data from link to link is correctly transmitted[1]. The Sequence Number allows proper Data Packet ordering.

1.3.3 Transaction Layer – Layer 3

Layer 3 – Transaction Layer (TL) – connects the lower protocols to the upper layers. This layer appears to the upper layers as *PCI*.

The Transaction Layer packetizes and prepends a header to the Payload Data. Write and Read commands, as well as prior sideband signals, *such as* Interrupts and Power Management requests, are also included in this layer.

To achieve code compatibility with PCI, PCI Express does not modify the transaction layer. This is significant because it allows vendors to leverage their existing PCI code to achieve not only a faster time to market, using their proven design, it also provides a more stable and mature platform.

1. *To ensure end-to-end data integrity, there is an optional feature in the PCI Express r1.0a. This feature is called* TLP Digest *and is defined in Layer 3.*

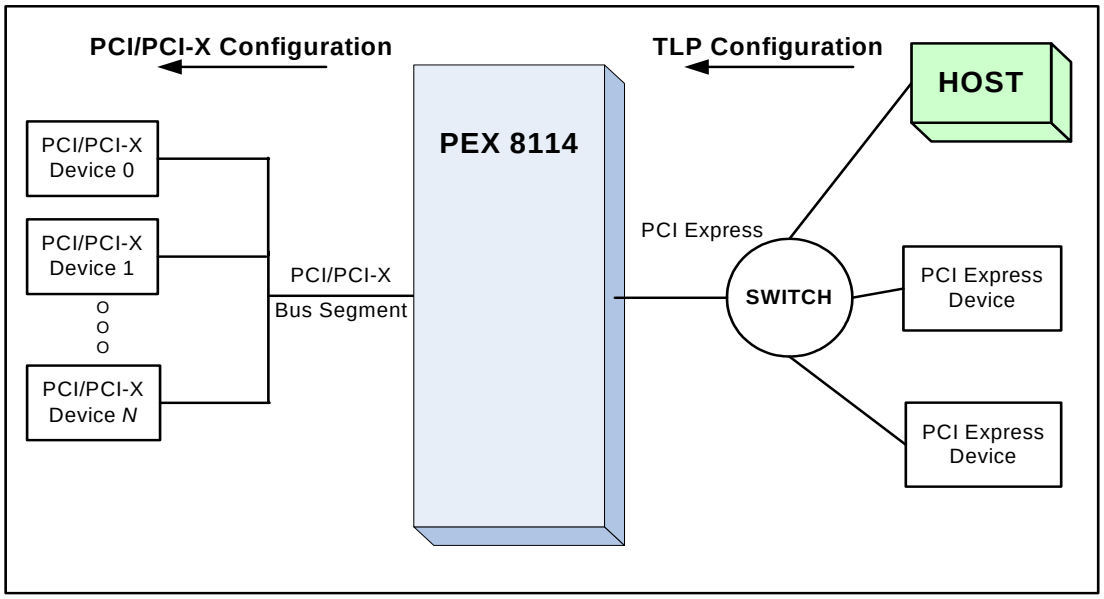
1.3.4 Sample Paths

1.3.4.1 Forward Transparent Bridge Mode

In ***Forward Transparent Bridge mode***, the Configuration cycles originate from the PCI Express link, by way of the PEX 8114 bridge and out to the PCI/PCI-X Bus segment (Conventional PCI or PCI-X).

As a Forward bridge, all Configuration accesses are transmitted from the PCI Express Root Complex.

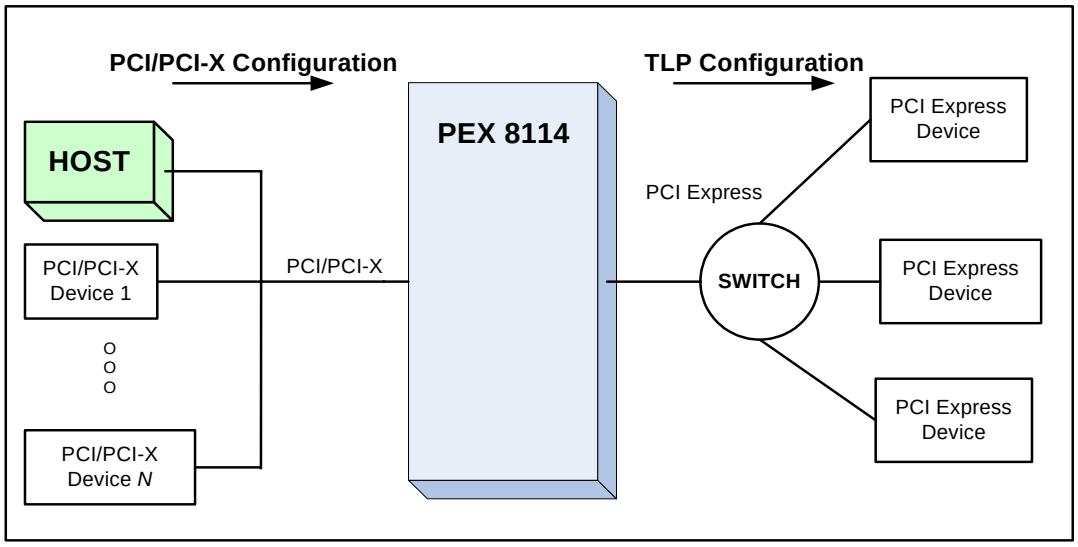
Figure 1-4. PEX 8114 as a Forward Bridge



1.3.4.2 Reverse Transparent Bridge Mode

In ***Reverse Transparent Bridge mode***, the Configuration cycles originate from the PCI/PCI-X Bus segment (Conventional PCI or PCI-X), by way of the PEX 8114 bridge and out to the PCI Express link. As a Reverse bridge, all Configuration accesses originate from the PCI/PCI-X Bus.

Figure 1-5. PEX 8114 as a Reverse Bridge



1.4 PEX 8114 Applications

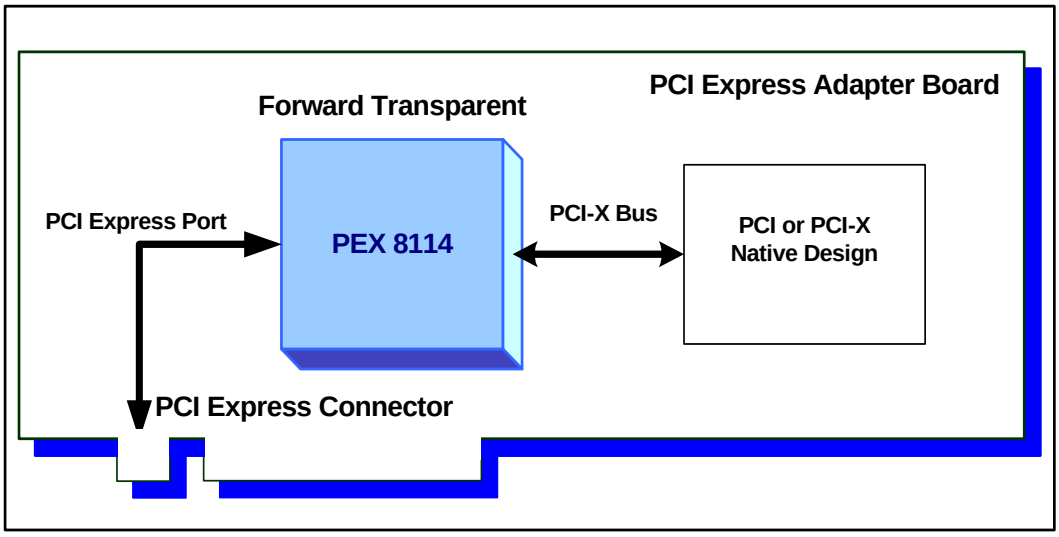
Various PEX 8114 applications are as follows:

- PCI Express Adapter Board
- PCI Express Motherboard to PCI-X Expansion Slot
- PCI-X Host Supporting a PCI Express Expansion Slot
- PCI-X Add-In Board Created from PCI Express Native Silicon
- PCI-X Extender Board

1.4.1 PCI Express Adapter Board

In a PCI Express Adapter Board application, the PEX 8114 is installed on a PCI Express adapter board, allowing a Conventional PCI or PCI-X device to create a PCI Express board. This configuration is illustrated in Figure 1-6, wherein the PEX 8114 is a *Forward Transparent bridge*.

Figure 1-6. PCI Express Board Created from PCI/PCI-X Native Silicon

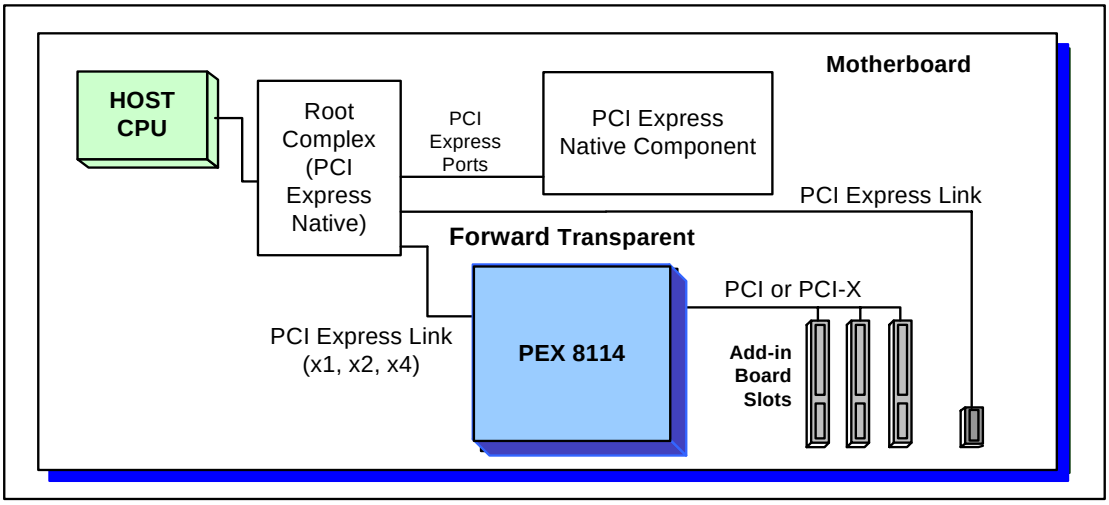


1.4.2 PCI Express Motherboard to PCI-X Expansion Slot

In a PCI Express Motherboard to PCI-X Expansion Slot application, the PEX 8114 is used on the motherboard to support standard PCI-X add-in board slots. It is similar to the PCI Express Adapter Board mode, as it allows a PCI Express root-based processor system to accept Conventional PCI or PCI-X silicon. The configuration is illustrated in Figure 1-7, wherein the PEX 8114 is a *Forward Transparent bridge.* An entire PCI-X Bus segment with standard PCI-X add-in boards can be supported in this mode.

The PEX 8114's simple design and small footprint make it an ideal bridge solution for the motherboard, providing for *PCI r3.0* or *PCI-X r1.0b* slot connectivity or interface to native PCI or PCI-X silicon I/O components on the motherboard.

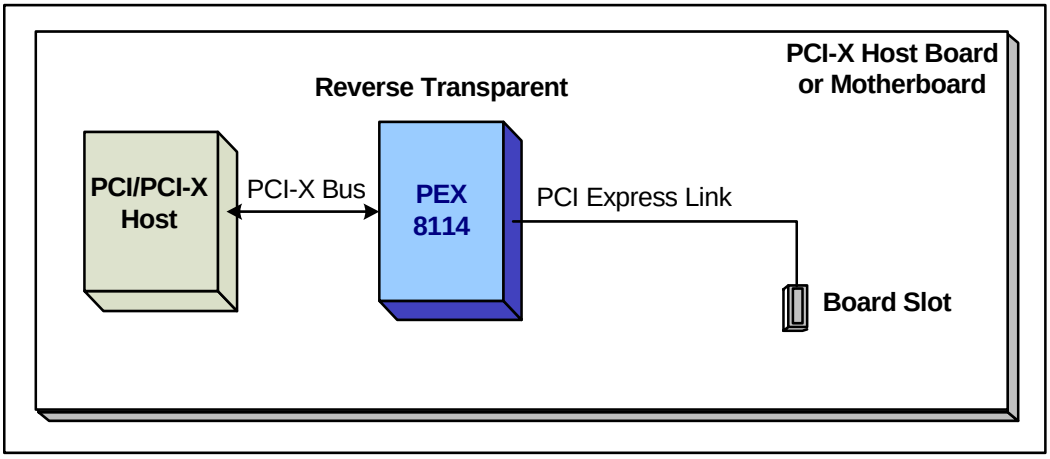
Figure 1-7. PEX 8114 on Motherboard Provides PCI/PCI-X Slots



1.4.3 PCI-X Host Supporting a PCI Express Expansion Slot

In a PCI-X Host supporting a PCI Express Expansion Slot application, the PEX 8114 is used as a *Reverse Transparent bridge* on a PCI-X motherboard to create PCI Express links. The configuration is illustrated in Figure 1-8, wherein the PEX 8114 is a *Reverse Transparent bridge*.

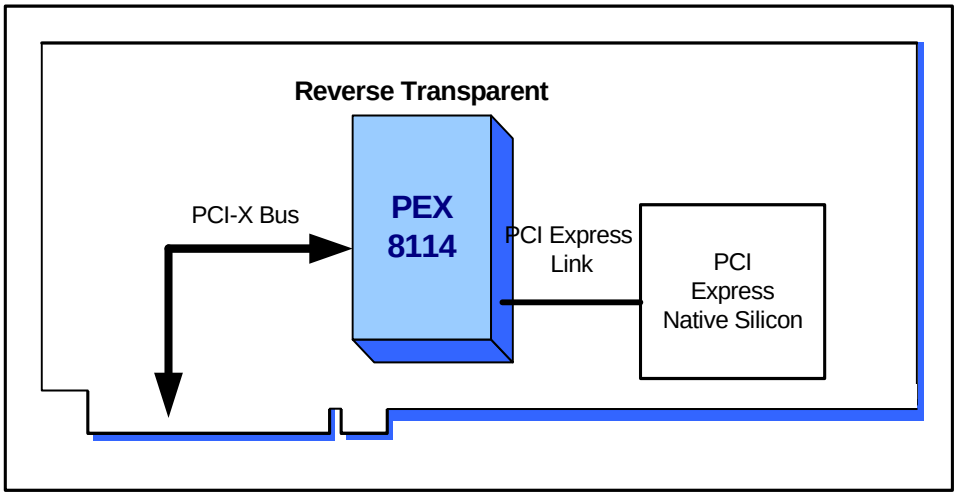
Figure 1-8. PCI-X Host Using PEX 8114 to Create PCI Express Board Slot



1.4.4 PCI-X Add-In Board Created from PCI Express Native Silicon

A PCI-X add-in board created from PCI Express native silicon application enables adapter boards based on state-of-the-art PCI Express silicon to plug into PCI/PCI-X motherboard expansion slots. The configuration is illustrated in Figure 1-9, wherein the PEX 8114 is a *Reverse Transparent bridge*.

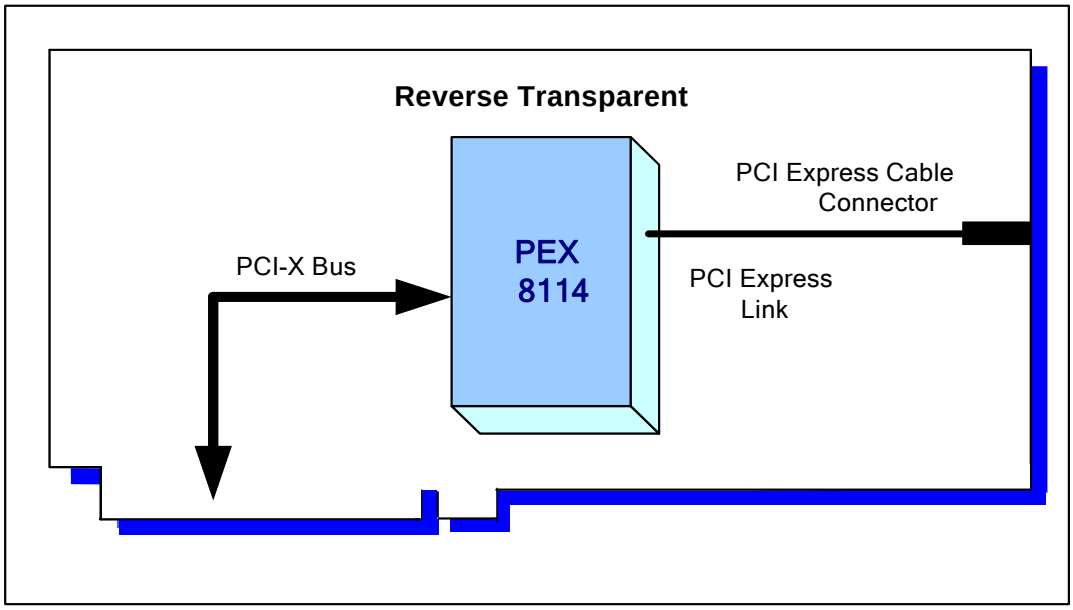
Figure 1-9. PCI-X Adapter Board Created Using PEX 8114 and PCI Express Native Silicon



1.4.5 PCI-X Extender Board

A PCI-X Extender Board application uses the PEX 8114 to create a bridge board, enabling PCI or PCI-X Bus expansion over standardized PCI Express cabling. The configuration is illustrated in Figure 1-10, wherein the PEX 8114 is a *Reverse Transparent bridge*.

Figure 1-10. PCI-X Adapter Board Acting as Bridge Board for Bus Expansion



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Chapter 2 Signal Ball Description

2.1 Introduction

This chapter provides descriptions of the 256 PEX 8114 signal balls. The signals are divided into the following groups:

- PCI/PCI-X Bus Interface Signals
- PCI Express Interface Signals
- Hot Plug Signals
- Strapping Signals
- JTAG Interface Signals
- Serial EEPROM Interface Signals
- Power and Ground Signals

The signal name, type, location, and a brief description are provided for each signal ball.

2.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 2-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
APWR	1.0V Power (VDD10A) balls for SerDes Analog circuits
CPWR	1.0V Power (VDD10) balls for low-voltage Core circuits
DPWR	1.0V Power (VDD10S) balls for SerDes Digital circuits
GND	Ground
I	CMOS Input
I/O	CMOS Bi-Directional Input/Output
I/OPWR	3.3V Power (VDD33) balls for Input and Output interfaces
LVDSRn	Differential low-voltage, high-speed, LVDS negative Receiver Inputs
LVDSRp	Differential low-voltage, high-speed, LVDS positive Receiver Inputs
LVDSTn	Differential low-voltage, high-speed, LVDS negative Transmitter Outputs
LVDSTp	Differential low-voltage, high-speed, LVDS positive Transmitter Outputs
O	CMOS Output
OD	Open Drain Output
PCI	PCI/PCI-X Compliant
PLLPWR	3.3V Power (VDD33A) balls for PLL circuits
PU	Signal is internally pulled up
STRAP	Strapping balls must be tied to High to VDD33 or Low to VSS on the board
STS	PCI/PCI-X Sustained Three-State Output, driven High for one CLK before Float
TP	Totem Pole
TS	Three-State Bi-Directional

Note: *Depending on the strapping configuration, certain balls change type. This is indicated in the* ***Type*** *column and descriptive field for the associated balls.*

2.2.1 Pull-Up Resistors

The balls defined in Table 2-2 have weak internal pull-up resistor values. Therefore, it is strongly advised that an external pull-up resistor to VDD33 (3K to 10K Ohms is recommended) be used on those signal balls when implemented in a design. For the remaining balls listed in this section, depending upon the application, certain balls are driven, pulled or tied, High or Low.

When the PCI_PME# ball is not used, it requires an external pull-up resistor.

When the Internal PCI Arbiter is not used (disabled), the PCI_REQ[3:1]# inputs require external pull-up resistors. If the internal PCI Arbiter is used (enabled), the PCI_REQ[3:0]# balls must be driven, pulled, or tied to a known state. Because the PCI_GNT[3:0]# outputs are driven, regardless of whether the PCI Arbiter is enabled, they do not require external pull-up resistors, and can be connected or remain unconnected (floating).

For information on Hot Plug systems, refer to the *PCI Express-to-PCI/PCI-X Bridge r1.0* for ball connection and usage.

For non-Hot Plug systems, the Hot Plug Input balls defined in Table 2-5 can remain unconnected, as each has its own internal pull-up resistor.

Serial EEPROM interface balls EE_CS#, EE_DI, and EE_SK are outputs that are driven by the PEX 8114, and can be connected or remain unconnected (floating). Serial EEPROM interface balls, EE_DO is an input with an internal pull-up resistor. Drive, pull, or tie this input to a known state.

For designs that do not implement JTAG, ground the JTAG_TRST# ball and drive, pull, or tie the JTAG_TCK input to a known value. JTAG_TDI, JTAG_TMS, and JTAG_TDO can remain unconnected.

Table 2-2. Balls with Internal Pull-Up Resistors

Ball Name	
EE_DO	JTAG_TCK
HP_BUTTON#	JTAG_TDI
HP_MRL#	JTAG_TMS
HP_PRSNT#	JTAG_TRST#
HP_PWRFLT#	

2.3 PCI/PCI-X Bus Interface Signals

The PCI balls defined in Table 2-3 do not contain internal resistors and are generic primary and secondary PCI/PCI-X interface balls. When producing motherboards, system slot boards, adapter boards, backplanes, and so forth, the termination of these balls must follow the guidelines detailed in the *PCI r3.0* and *PCI-X r1.0b*. The following guidelines are not exhaustive; therefore, read in conjunction with the appropriate *PCI r3.0* and *PCI-X r1.0b* sections.

PCI Control signals require a pull-up resistor on the motherboard to ensure that these signals are at valid values when a PCI Bus agent is not driving the bus. These Control signals include PCI_ACK64#, PCI_DEVSEL#, PCI_FRAME#, PCI_INT[D:A]#, PCI_IRDY#, PCI_PERR#, PCI_REQ64#, PCI_SERR#, PCI_STOP#, and PCI_TRDY#.

The 32-bit point-to-point and shared bus signals do ***not*** require pull-up resistors, as bus parking ensures that these signals remain stable. The other 64-bit signals – PCI_AD[63:32], PCI_C/BE[7:4]#, and PCI_PAR64 – also require pull-up resistors, as these signals are not driven during 32-bit transactions.

The PCI_INT[D:A]# balls require pull-up resistors, regardless of whether they are used. In Forward Transparent Bridge mode, PCI_IDSEL is not used and requires a pull-up resistor. Depending on the application, PCI_M66EN can also require a pull-up resistor. The value of these pull-up resistors depends on the bus loading. The *PCI r3.0* provides formulas for calculating the resistor values. When making adapter board devices where the PEX 8114 port is wired to the PCI connector, pull-up resistors are not required because they are pre-installed on the motherboard.

Based on the above, in an embedded design, pull-up resistors can be required for PCI Control signals on the bus.

The PEX 8114 includes 108 PCI/PCI-X signals, which are defined in Table 2-3. The categories included in the **Type** columns of certain of these signals are from the *PCI Express-to-PCI/PCI-X Bridge r1.0*, Tables 6-3 and 6-4.

By convention, multiple balls are listed in high-to-low order (*that is*, PCI_AD63, PCI_AD62, …, PCI_AD0).

Table 2-3. PCI/PCI-X Bus Interface Signals (108 Balls)

Symbol	Type	Location	Description
PCI_ACK64#	I/O STS PCI	A13	**64-Bit Transfer Acknowledge** Asserted by the PCI Slave in response to PCI_REQ64#, to acknowledge a 64-bit Data transfer. 0 = Acknowledges a 64-bit transfer 1 = No acknowledge
PCI_AD[63:0]	I/O TS PCI	A15, C15, A16, D14, B16, D15, C16, E13, D16, E14, E15, F13, E16, F14, F16, G13, G16, G14, H15, H13, H16, H14, J15, J13, J16, J14, K15, K13, K16, K14, L16, L14, F1, F3, E1, F4, D1, E3, D2, D3, B1, C2, A1, C3, A2, D4, B3, C4, C7, A7, D8, A8, C8, A9, D9, B10, A10, C10, B11, D11, A11, C11, A12, C12	**Address and Data (64 Balls)** PCI Multiplexed Address/Data Bus.
PCI_C/BE[7:0]#	I/O TS PCI	C13, A14, D13, B14, C1, A3, B7, D10	**Bus Command and Byte Enables (8 Balls)** During the PCI and/or PCI-X Address phase, PCI_C/BE[3:0]# provide the command type. During the Data phase of PCI and/or PCI-X Memory Write transactions, PCI_C/BE[7:0]# provide Byte Enables. During the PCI-X Attribute phase, PCI_C/BE[7:0]# provide a portion of the attribute information.
PCI_CLK	I PCI	J1	**PCI/PCI-X Bus Clock Input** Clock reference when STRAP_CLK_MST=0. Not the clock reference when STRAP_CLK_MST=1. (Refer to Chapter 3, "Clock and Reset," for further details.)
PCI_CLKO[3:0]	O PCI	L1, L2, K1, K3	**Clock Outputs (4 Balls)** PCI/PCI-X Bus clocks for up to four devices. Derived from PEX_REFCLKn/p. (Refer to Chapter 3, "Clock and Reset," for further details.)
PCI_CLKO_DLY_FBK	O PCI	N3	**PCI Clock Delayed Feedback** PCI/PCI-X clock intended to be fed back to the PEX 8114 PCI_CLK input ball when STRAP_CLK_MST and STRAP_EXT_CLK_SEL are High. The trace length provides a time phase delay on the PCI clock that drives the internal PCI circuitry, thereby aligning the internal PCI_CLK rising edge with the clock edges of other PCI devices on the PCI Bus that can be sufficiently separated physically, such that Clock-phase alignment becomes necessary.
PCI_DEVSEL#	I/O STS PCI	A4	**Device Select** When actively driven, indicates the driving device decoded its address as the Target of the current access.
PCI_FRAME#	I/O STS PCI	D5	**Frame** Driven by the transaction Initiator to indicate an access start and duration. While PCI_FRAME# is asserted, Data transfers continue.

Table 2-3. PCI/PCI-X Bus Interface Signals (108 Balls) *(Cont.)*

Symbol	Type	Location	Description
PCI_GNT# or PCI_GNT0#	I/O TS PCI	G3	**Grant or Internal PCI Arbiter Grant 0** **PCI_GNT# (Input):** When the PEX 8114 Internal PCI Arbiter is disabled, this is a PCI/PCI-X Bus grant from the External Arbiter. **PCI_GNT0# (Output):** When the PEX 8114 Internal PCI Arbiter is enabled, PCI_GNT0# is an output to an arbitrating Master. The PEX 8114 Arbiter asserts PCI_GNT0# to grant the PCI/PCI-X Bus to the Master.
PCI_GNT[3:1]#	O TP PCI	J3, J4, H3	**Internal PCI Arbiter Grants 3 to 1 (3 Balls)** When the PEX 8114 Internal PCI Arbiter is enabled, PCI_GNT[3:1]# are outputs (one each) to an arbitrating Master. The Internal PCI Arbiter asserts PCI_GNT[3:1]# to grant the PCI/PCI-X Bus to the corresponding Master.
PCI_IDSEL	I PCI	E4	**Device Select** **Forward Transparent Bridge mode:** PCI_IDSEL is not used and requires a pull-up resistor. **Reverse Transparent Bridge mode:** Used as a Chip Select during Configuration Write and Read transactions.
PCI_INT[D:A]#	I/O OD PCI	M2, K4, M1, L3	**Interrupts D, C, B, and A (4 Balls)** **Forward Transparent Bridge mode:** PCI/PCI-X Bus interrupt inputs. **Reverse Transparent Bridge mode:** PCI/PCI-X Bus interrupt outputs.
PCI_IRDY#	I/O OD PCI	B4	**Initiator Ready** PCI/PCI-X Bus Initiator ready. Indicates initiating agent's (Bus Master) ability to complete the current Data phase of the transaction.
PCI_M66EN	I PCI	B9	**PCI Bus Clock Speed Capability Indicator** Refer to Table 3-3.
PCI_PAR	I/O TS PCI	D7	**Parity** Even parity across PCI_AD[31:0] and PCI_C/BE[3:0]#. PCI_PAR is stable and valid one clock after the Address phase. For Data phases, PCI_PAR is stable and valid one clock after PCI_IRDY# is asserted on a Write transaction or PCI_TRDY# is asserted on a Read transaction. After PCI_PAR is valid, it remains valid until one clock after the current Data phase completes.
PCI_PAR64	I/O TS PCI	C14	**Upper 32 Bits Parity** Even parity across PCI_AD[63:32] and PCI_C/BE[7:4]#. PCI_PAR64 is stable and valid one clock after the Address phase. For Data phases, PCI_PAR64 is stable and valid one clock after PCI_IRDY# is asserted on a Write transaction or PCI_TRDY# is asserted on a Read transaction. After PCI_PAR64 is valid, it remains valid until one clock after the current Data phase completes.

Table 2-3. PCI/PCI-X Bus Interface Signals (108 Balls) *(Cont.)*

Symbol	Type	Location	Description
PCI_PCIXCAP	I	A5	**PCI-X Capability** Used with PCI_PCIXCAP_PU to determine whether all devices running on the PCI/PCI-X Bus are capable of running PCI-X cycles and at which frequency. **Clock Master mode:** Connect the PCI_PCIXCAP_PU ball to the PCI_PCIXCAP ball through a 1K-Ohm resistor when operating at PCI 66, and PCI-X 66 and 133. A 56K-Ohm resistor between VDD33 and the PCI_PCIXCAP ball is also required.
PCI_PCIXCAP_PU	O	C5	**PCI/PCI-X Bus PCI_PCIXCAP Pull-Up Driver** Used with PCI_PCIXCAP to determine whether all agents on the PCI/PCI-X Bus are PCI-X-compatible in Clock Master mode. **Clock Master mode:** Connect the PCI_PCIXCAP_PU ball to the PCI_PCIXCAP ball through a 1K-Ohm resistor when operating at PCI 66, and PCI-X 66 and 133.
PCI_PERR#	I/O STS PCI	B6	**Parity Error** PCI/PCI-X Bus parity error indicator. Reports and records Data Parity errors during all PCI transactions, except during a special cycle.
PCI_PME#	I/O TS PCI	G4	**Power Management Event** **Forward Transparent Bridge mode:** PCI/PCI-X Bus Power Management Event (PME) indicator input. **Reverse Transparent Bridge mode:** PCI/PCI-X Bus Power Management Event indicator output.
PCI_REQ# or PCI_REQ0#	I/O PCI	G2	**Request or Internal PCI Arbiter Request 0** **PCI_REQ# (Output):** When the PEX 8114 Internal PCI Arbiter is disabled, this is a PCI/PCI-X Bus request to the External Arbiter. **PCI_REQ0# (Input):** When the PEX 8114 Internal PCI Arbiter is enabled, PCI_REQ0# is an input from an arbitrating Master. The Internal PCI Arbiter asserts PCI_GNT0# to grant the PCI/PCI-X Bus to the Master.
PCI_REQ[3:1]#	I PCI	H1, H2, G1	**Internal PCI Arbiter Requests 3 to 1 (3 Balls)** When the PEX 8114 Internal PCI Arbiter is enabled, PCI_REQ[3:1]# are inputs (one each) from an arbitrating Master. The Internal PCI Arbiter asserts a PCI_GNT[3:1]# signal to grant the PCI/PCI-X Bus to the corresponding Master.
PCI_REQ64#	I/O STS PCI	D12	**64-Bit Transfer Request** Asserted (0) with PCI_FRAME# by a PCI Bus Master to request a 64-bit Data transfer. **Forward Transparent Bridge or Clock Master mode:** The PEX 8114 asserts PCI_REQ64# during PCI_RST# to configure a 64-bit backplane. **Reverse Transparent Bridge mode and not Clock Master:** The PEX 8114 samples PCI_REQ64# at PCI_RST# de-assertion to configure a 32- or 64-bit PCI backplane.

Table 2-3. PCI/PCI-X Bus Interface Signals (108 Balls) *(Cont.)*

Symbol	Type	Location	Description
PCI_RST#	I/O PCI	H4	**Reset** **Forward Transparent Bridge mode, Output:** Provides the PCI/PCI-X Bus reset. The PEX 8114 drives PCI_RST# and asserts PCI_RST# during the initialization period. **Reverse Transparent Bridge mode, Input:** Receives the external Reset signal from the bus. (Refer to Chapter 3, "Clock and Reset," for further details.) Input that receives reset from an upstream Host and is the equivalent of Hot Reset internally and causes the propagation of Hot Reset across the PCI Express link.
PCI_SEL100	I	M4	**Bus 100-MHz Indicator** When the PCI/PCI-X Bus is operating in PCI-X Clock Master mode in Forward or Reverse Transparent Bridge mode, or Clock Slave mode in Forward Transparent Bridge mode: 0 = 133-MHz PCI-X Bus capability 1 = 100-MHz PCI-X Bus capability In Clock Slave mode, pull PCI_SEL100 High or Low.
PCI_SERR#	I/O OD PCI	A6	**Bus System Error Indicator** **Input:** Assertion detected by the Host, indicates a PCI System error occurred. **Output:** Asserted by a Target, indicates a Fatal or Non-Fatal PCI Express Parity error occurred.
PCI_STOP#	I/O STS PCI	C6	**Stop** Asserted by the Target to signal to end the transaction on the current Data phase.
PCI_TRDY#	I/O STS PCI	D6	**Target Ready** Driven by the Transaction Target to indicate its ability to complete the current Data phase.

2.4 PCI Express Interface Signals

The PEX 8114 includes 23 PCI Express port interface signals, which are defined in Table 2-4. The port signals are Low-Voltage Differential Signal format that requires two balls for each lane, in each direction. The four PEX_LANE_GOOD*x*# signals are used to drive LEDs to indicate the status of each lane.

Table 2-4. PCI Express Interface Signals (23 Balls)

Symbol	Type	Location	Description
PEX_LANE_GOOD[3:0]#	O	R16, T16, R15, T15	**PCI Express Lane Status Indicators (4 Balls)** 0 = Lane active (LED is On) 1 = Lane inactive (LED is Off)
PEX_PERn[3:0]	I(-) LVDSRn	M11, M9, M7, M5	**Negative Half of PCI Express Receiver Differential Signal Pairs (4 Balls)**
PEX_PERp[3:0]	I(+) LVDSRp	N11, N9, N7, N5	**Positive Half of PCI Express Receiver Differential Signal Pairs (4 Balls)**
PEX_PETn[3:0]	O(-) LVDSTn	T11, T9, T7, T5	**Negative Half of PCI Express Transmitter Differential Signal Pairs (4 Balls)**
PEX_PETp[3:0]	O(+) LVDSTp	R11, R9, R7, R5	**Positive Half of PCI Express Transmitter Differential Signal Pairs (4 Balls)**
PEX_PERST#	I	T1	**PCI Express Reset** Used to cause a Fundamental Reset. In Forward Transparent Bridge mode, PEX_PERST# is a 3.3V input with a weak internal pull-up resistor. (Refer to Chapter 3, "Clock and Reset," for further details.)
PEX_REFCLKn	I(-) LVDSn	R3	**Negative Half of 100-MHz PCI Express Reference Clock Signal Pair** (Refer to Chapter 3, "Clock and Reset," for details.)
PEX_REFCLKp	I(+) LVDSp	T3	**Positive Half of 100-MHz PCI Express Reference Clock Signal Pair** (Refer to Chapter 3, "Clock and Reset," for details.)

2.5 Hot Plug Signals

The PEX 8114 includes nine Hot Plug signals for the PCI Express port, defined in Table 2-5.

Table 2-5. Hot Plug Signals (9 Balls)

Symbol	Type	Location	Description
HP_ATNLED#	O	T14	**Hot Plug Attention LED** Slot Control Logic output used to drive the Attention Indicator. Set Low to turn On the LED. High/Off = Standard Operation Low/On = Operational problem at this slot Blinking = Slot is identified at the user's request Blinking Frequency = 2.0 Hz, 50% duty cycle
HP_BUTTON#	I PU	T13	**Hot Plug Attention Button** Slot Control Logic input directly connected to the Attention Button, which is pressed to request Hot Plug operations. Can be implemented on the bridge or downstream device.
HP_CLKEN#	O	R14	**Clock Enable** Reference Clock enable output. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN# (and HP_PWRLED#) output assertion to HP_CLKEN# output assertion is programmable from 16 ms (default) to 128 ms, in the *HPC* T_{pepv} *Delay* field (offset 1E0h[4:3]).
HP_MRL#	I PU	R13	**Manually Operated Retention Latch Sensor** Slot Control Logic and Power Controller input directly connected to the MRL Sensor. Manually operated Retention Latch switch signal for inserting and extracting Hot Plug-capable boards. High = Board is not available or properly seated in slot Low = Board not properly seated in slot
HP_PERST#	O	P14	**Reset** Hot Plug Reset for downstream link. Enabled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]).
HP_PRSNT#	I PU	P13	**PCI Present** Input connected to external logic that directly outputs PRSNT# from the external combination of PRSNT1# and PRSNT2#.
HP_PWREN#	O	N14	**Power Enable** Slot Control Logic output that controls the slot power state. When HP_PWREN# is Low, power is enabled to the slot.
HP_PWRFLT#	I PU	N13	**Power Fault Input** Indicates that the Slot Power Controller detected a power fault on one or more supply rails.
HP_PWRLED#	O	M13	**Power LED** Slot Control Logic output used to drive the Power Indicator. This output is set Low to turn On the LED.

2.6 Strapping Signals

The eight PEX 8114 Strapping signals, defined in Table 2-6, set the configuration of Forward and Reverse Transparent Bridge mode, Clock Master and Arbiter Master selection, as well as various Setup and Test modes. These balls must be tied High to VDD33 or Low to VSS.

Table 2-6. Strapping Signals (8 Balls)

Symbol	Type	Location	Description
STRAP_ARB	I STRAP	L5	**Arbiter Select** Internal or external PCI/PCI-X Arbiter select. Strapping signal that enables and disables the PEX 8114 PCI/PCI-X Internal PCI Arbiter. 1 = Enables the Arbiter 0 = Disables the Arbiter (refer to Chapter 11, "PCI/PCI-X Arbiter")
STRAP_CLK_MST	I STRAP	L4	**Clock Master Select** In Clock Master mode, the 100-MHz PEX_REFCLKn/p signals are used to generate a clock of 25, 33, 50, 66, 100, or 133 MHz on the PCI_CLKO[3:0] balls. The clock frequency is determined by the PCI_PCIXCAP, PCI_M66EN clock, and PCI_SEL100 ball states. (Refer to Table 3-3.) 1 = PEX 8114 is the PCI_CLK Generator (Clock Master mode) 0 = PEX 8114 is the PCI_CLK Receiver (Clock Slave mode)
STRAP_EXT_CLK_SEL	I STRAP	N6	**External PCI Clock Select** When the PEX 8114 is in Clock Master mode and this ball is Low, the PCI clock is driven from the internal PCI clock frequency generator to the internal PCI module by way of a fed back Clock signal. In this case, the PCI_CLK ball need not be driven by a Clock signal, but pulled to a known level by external circuitry. When the STRAP_EXT_CLK_SEL and STRAP_CLK_MST balls are High, the PCI clock must be driven externally from the PCI_CLKO_DLY_FBK output to the PCI_CLK input. The trace length and delay from PCI_CLK must match the length of other PCB trace driven from PCI_CLKO[3:0] to external PCI devices.
STRAP_FWD	I STRAP	P16	**Forward Transparent Bridge Mode Select** Strapping signal that selects between Forward and Reverse Transparent Bridge modes. 1 = Forward Transparent Bridge mode 0 = Reverse Transparent Bridge mode
STRAP_PLL_BYPASS#	I STRAP	P3	**PLL Bypass** ***Factory Test Only*** Tied High for standard operation.
STRAP_TESTMODE[1:0]	I STRAP	T2, R2	**Test Mode Select (2 Balls)** ***Factory Test Only*** Tied High for standard operation.
STRAP_TRAN	I STRAP	P15	**Transparent Mode Select** Strapping signal that selects Transparent mode. *Note: Value is always 1.* 1 = Transparent mode 0 = ***Reserved***

2.7 JTAG Interface Signals

The PEX 8114 includes five signals for performing JTAG boundary scan, defined in Table 2-7. For further details, refer to Chapter 15, "Test and Debug."

Table 2-7. JTAG Interface Signals (5 Balls)

Symbol	Type	Location	Description
JTAG_TCK	I PU	P1	**Test Clock Input** Clock source for the PEX 8114 Test Access Port (TAP). JTAG_TCK can be any frequency from 0 to 10 MHz.
JTAG_TDI	I PU	N2	**Test Data Input** Used to input data into the TAP. When the TAP enables this ball, it is sampled on the rising edge of JTAG_TCK and the sampled value is input to the selected TAP shift register.
JTAG_TDO	O	N1	**Test Data Output** Used to transmit serial data from the PEX 8114 TAP. Data from the selected shift register is shifted out of JTAG_TDO.
JTAG_TMS	I PU	P2	**Test Mode Select** Sampled by the TAP on the rising edge of JTAG_TCK. The TAP state machine uses the JTAG_TMS ball to determine the TAP mode.
JTAG_TRST#	I PU	R1	**Test Reset** Resets JTAG. Toggle or hold at 0 for the PEX 8114 to properly function. Resets the TAP.

2.8 Serial EEPROM Interface Signals

The PEX 8114 includes five signals for interfacing to a serial EEPROM, defined in Table 2-8. EE_DO requires a weak internal pull-up resistor.

Table 2-8. Serial EEPROM Interface Signals (5 Balls)

Symbol	Type	Location	Description
EE_CS#	O	N15	**Serial EEPROM Active-Low Chip Select Output** Weakly pulled up. Can remain floating if not used or use a stronger pull-up resistor (5K to 10K Ohms).
EE_DI	O	M16	**Serial EEPROM Data In** PEX 8114 output to the serial EEPROM Data input. Weakly pulled up. Can remain floating if not used or use a stronger pull-up resistor (5K to 10K Ohms).
EE_DO	I PU	N16	**Serial EEPROM Data Out** PEX 8114 input from the serial EEPROM Data output. Weakly pulled up. Can remain floating if not used or use a stronger pull-up resistor (5K to 10K Ohms).
EE_PR#	I	L13	**Serial EEPROM Active-Low Present Input** When a serial EEPROM is not used, must be pulled up to VDD33. 5K- to 10K-Ohm pull-up resistor recommended. Must be connected to VSS if a serial EEPROM is present and used.
EE_SK	O	M14	**7.8-MHz Serial EEPROM Clock** For a PCI-X clock greater than 66 MHz, a 10-MHz serial EEPROM is needed. For clock rates of 66 MHz and lower, a 5-MHz serial EEPROM is sufficient. Weakly pulled up. Can remain floating if not used or use a stronger pull-up resistor (5K to 10K Ohms).

2.9 Power and Ground Signals

Table 2-9. Power and Ground Signals (98 Balls)

Symbol	Type	Location	Description
VDD10	CPWR	E6, E8, E9, E11, F5, F12, G5, G12, J5, J12, K5, K12, M6, M10, M12	**Core Supply Voltage (15 Balls)** 1.0V Power for Core Logic V_{CORE}.
VDD10A	APWR	M8	**SerDes Analog Supply Voltage** 1.0V Power for SerDes Analog Circuits.
VDD10S	DPWR	P8, R4, R6, R8, R10, R12	**SerDes Digital Supply Voltage (6 Balls)** 1.0V Power for SerDes Digital Circuits.
VDD33	I/OPWR	B2, B8, B12, B15, E5, E7, E10, E12, F2, G15, H5, H12, J2, L12, M3, M15, P12	**I/O Supply Voltage (17 Balls)** 3.3V Power for I/O logic functions V_{RING}.
VDD33A	PLLPWR	P4	**PLL Analog Supply Voltage** 3.3V Power for PLL Circuits.
VSS	GND	B5, B13, C9, E2, F6, F7, F8, F9, F10, F11, F15, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K2, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, L15, N8, N10, N12, P5, P6, P7, P9, P10, P11, T4, T8, T12	**Digital Ground Connections (55 Balls)**
VSSA	GND	N4	**Analog Ground Connection**
VTT_PEX[1:0]	Supply	T10, T6	**SerDes Termination Supply (2 Balls)** Tied to SerDes termination supply voltage (typically 1.5V).[a]

a. PEX_PETn/p[x] SerDes termination supply voltage controls the transmitter Common mode voltage (V_{TX-CM}) value and output voltage swing ($V_{TX-DIFFp}$), per the following formula:

$$V_{TX-CM} = V_{TT} - V_{TX-DIFFp}$$

2.10 Ball Assignments by Location

Table 2-10. Ball Assignments by Location

Location	Signal Name
A1	PCI_AD21
A2	PCI_AD19
A3	PCI_C/BE2#
A4	PCI_DEVSEL#
A5	PCI_PCIXCAP
A6	PCI_SERR#
A7	PCI_AD14
A8	PCI_AD12
A9	PCI_AD10
A10	PCI_AD7
A11	PCI_AD3
A12	PCI_AD1
A13	PCI_ACK64#
A14	PCI_C/BE6#
A15	PCI_AD63
A16	PCI_AD61
B1	PCI_AD23
B2	VDD33
B3	PCI_AD17
B4	PCI_IRDY#
B5	VSS
B6	PCI_PERR#
B7	PCI_C/BE1#
B8	VDD33
B9	PCI_M66EN
B10	PCI_AD8
B11	PCI_AD5
B12	VDD33
B13	VSS
B14	PCI_C/BE4#
B15	VDD33
B16	PCI_AD59
C1	PCI_C/BE3#
C2	PCI_AD22
C3	PCI_AD20
C4	PCI_AD16

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
C5	PCI_PCIXCAP_PU
C6	PCI_STOP#
C7	PCI_AD15
C8	PCI_AD11
C9	VSS
C10	PCI_AD6
C11	PCI_AD2
C12	PCI_AD0
C13	PCI_C/BE7#
C14	PCI_PAR64
C15	PCI_AD62
C16	PCI_AD57
D1	PCI_AD27
D2	PCI_AD25
D3	PCI_AD24
D4	PCI_AD18
D5	PCI_FRAME#
D6	PCI_TRDY#
D7	PCI_PAR
D8	PCI_AD13
D9	PCI_AD9
D10	PCI_C/BE0#
D11	PCI_AD4
D12	PCI_REQ64#
D13	PCI_C/BE5#
D14	PCI_AD60
D15	PCI_AD58
D16	PCI_AD55
E1	PCI_AD29
E2	VSS
E3	PCI_AD26
E4	PCI_IDSEL
E5	VDD33
E6	VDD10
E7	VDD33
E8	VDD10
E9	VDD10
E10	VDD33

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
E11	VDD10
E12	VDD33
E13	PCI_AD56
E14	PCI_AD54
E15	PCI_AD53
E16	PCI_AD51
F1	PCI_AD31
F2	VDD33
F3	PCI_AD30
F4	PCI_AD28
F5	VDD10
F6	VSS
F7	VSS
F8	VSS
F9	VSS
F10	VSS
F11	VSS
F12	VDD10
F13	PCI_AD52
F14	PCI_AD50
F15	VSS
F16	PCI_AD49
G1	PCI_REQ1#
G2	PCI_REQ# or PCI_REQ0#
G3	PCI_GNT# or PCI_GNT0#
G4	PCI_PME#
G5	VDD10
G6	VSS
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	VDD10
G13	PCI_AD48
G14	PCI_AD46
G15	VDD33
G16	PCI_AD47

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
H1	PCI_REQ3#
H2	PCI_REQ2#
H3	PCI_GNT1#
H4	PCI_RST#
H5	VDD33
H6	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VDD33
H13	PCI_AD44
H14	PCI_AD42
H15	PCI_AD45
H16	PCI_AD43
J1	PCI_CLK
J2	VDD33
J3	PCI_GNT3#
J4	PCI_GNT2#
J5	VDD10
J6	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VDD10
J13	PCI_AD40
J14	PCI_AD38
J15	PCI_AD41
J16	PCI_AD39
K1	PCI_CLKO1
K2	VSS
K3	PCI_CLKO0
K4	PCI_INTC#
K5	VDD10
K6	VSS

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VDD10
K13	PCI_AD36
K14	PCI_AD34
K15	PCI_AD37
K16	PCI_AD35
L1	PCI_CLKO3
L2	PCI_CLKO2
L3	PCI_INTA#
L4	STRAP_CLK_MST
L5	STRAP_ARB
L6	VSS
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VDD33
L13	EE_PR#
L14	PCI_AD32
L15	VSS
L16	PCI_AD33
M1	PCI_INTB#
M2	PCI_INTD#
M3	VDD33
M4	PCI_SEL100
M5	PEX_PERn0
M6	VDD10
M7	PEX_PERn1
M8	VDD10A
M9	PEX_PERn2
M10	VDD10
M11	PEX_PERn3
M12	VDD10

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
M13	HP_PWRLED#
M14	EE_SK
M15	VDD33
M16	EE_DI
N1	JTAG_TDO
N2	JTAG_TDI
N3	PCI_CLKO_DLY_FBK
N4	VSSA
N5	PEX_PERp0
N6	STRAP_EXT_CLK_SEL
N7	PEX_PERp1
N8	VSS
N9	PEX_PERp2
N10	VSS
N11	PEX_PERp3
N12	VSS
N13	HP_PWRFLT#
N14	HP_PWREN#
N15	EE_CS#
N16	EE_DO
P1	JTAG_TCK
P2	JTAG_TMS
P3	STRAP_PLL_BYPASS#
P4	VDD33A
P5	VSS
P6	VSS
P7	VSS
P8	VDD10S
P9	VSS
P10	VSS
P11	VSS
P12	VDD33
P13	HP_PRSNT#
P14	HP_PERST#
P15	STRAP_TRAN
P16	STRAP_FWD
R1	JTAG_TRST#
R2	STRAP_TESTMODE0

Table 2-10. Ball Assignments by Location *(Cont.)*

Location	Signal Name
R3	PEX_REFCLKn
R4	VDD10S
R5	PEX_PETp0
R6	VDD10S
R7	PEX_PETp1
R8	VDD10S
R9	PEX_PETp2
R10	VDD10S
R11	PEX_PETp3
R12	VDD10S
R13	HP_MRL#
R14	HP_CLKEN#
R15	PEX_LANE_GOOD1#
R16	PEX_LANE_GOOD3#
T1	PEX_PERST#
T2	STRAP_TESTMODE1
T3	PEX_REFCLKp
T4	VSS
T5	PEX_PETn0
T6	VTT_PEX0
T7	PEX_PETn1
T8	VSS
T9	PEX_PETn2
T10	VTT_PEX1
T11	PEX_PETn3
T12	VSS
T13	HP_BUTTON#
T14	HP_ATNLED#
T15	PEX_LANE_GOOD0#
T16	PEX_LANE_GOOD2#

2.11 Ball Assignments by Signal Name

Table 2-11. Ball Assignments by Signal Name

Location	Signal Name
N15	EE_CS#
M16	EE_DI
N16	EE_DO
L13	EE_PR#
M14	EE_SK
T14	HP_ATNLED#
T13	HP_BUTTON#
R14	HP_CLKEN#
R13	HP_MRL#
P14	HP_PERST#
P13	HP_PRSNT#
N14	HP_PWREN#
N13	HP_PWRFLT#
M13	HP_PWRLED#
P1	JTAG_TCK
N2	JTAG_TDI
N1	JTAG_TDO
P2	JTAG_TMS
R1	JTAG_TRST#
A13	PCI_ACK64#
C12	PCI_AD0
A12	PCI_AD1
C11	PCI_AD2
A11	PCI_AD3
D11	PCI_AD4
B11	PCI_AD5
C10	PCI_AD6
A10	PCI_AD7
B10	PCI_AD8
D9	PCI_AD9
A9	PCI_AD10
C8	PCI_AD11
A8	PCI_AD12
D8	PCI_AD13
A7	PCI_AD14
C7	PCI_AD15

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
C4	PCI_AD16
B3	PCI_AD17
D4	PCI_AD18
A2	PCI_AD19
C3	PCI_AD20
A1	PCI_AD21
C2	PCI_AD22
B1	PCI_AD23
D3	PCI_AD24
D2	PCI_AD25
E3	PCI_AD26
D1	PCI_AD27
F4	PCI_AD28
E1	PCI_AD29
F3	PCI_AD30
F1	PCI_AD31
L14	PCI_AD32
L16	PCI_AD33
K14	PCI_AD34
K16	PCI_AD35
K13	PCI_AD36
K15	PCI_AD37
J14	PCI_AD38
J16	PCI_AD39
J13	PCI_AD40
J15	PCI_AD41
H14	PCI_AD42
H16	PCI_AD43
H13	PCI_AD44
H15	PCI_AD45
G14	PCI_AD46
G16	PCI_AD47
G13	PCI_AD48
F16	PCI_AD49
F14	PCI_AD50
E16	PCI_AD51
F13	PCI_AD52
E15	PCI_AD53

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
E14	PCI_AD54
D16	PCI_AD55
E13	PCI_AD56
C16	PCI_AD57
D15	PCI_AD58
B16	PCI_AD59
D14	PCI_AD60
A16	PCI_AD61
C15	PCI_AD62
A15	PCI_AD63
D10	PCI_C/BE0#
B7	PCI_C/BE1#
A3	PCI_C/BE2#
C1	PCI_C/BE3#
B14	PCI_C/BE4#
D13	PCI_C/BE5#
A14	PCI_C/BE6#
C13	PCI_C/BE7#
J1	PCI_CLK
K3	PCI_CLKO0
K1	PCI_CLKO1
L2	PCI_CLKO2
L1	PCI_CLKO3
N3	PCI_CLKO_DLY_FBK
A4	PCI_DEVSEL#
D5	PCI_FRAME#
G3	PCI_GNT# or PCI_GNT0#
H3	PCI_GNT1#
J4	PCI_GNT2#
J3	PCI_GNT3#
E4	PCI_IDSEL
L3	PCI_INTA#
M1	PCI_INTB#
K4	PCI_INTC#
M2	PCI_INTD#
B4	PCI_IRDY#
B9	PCI_M66EN
D7	PCI_PAR

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
C14	PCI_PAR64
A5	PCI_PCIXCAP
C5	PCI_PCIXCAP_PU
B6	PCI_PERR#
G4	PCI_PME#
G2	PCI_REQ# or PCI_REQ0#
G1	PCI_REQ1#
H2	PCI_REQ2#
H1	PCI_REQ3#
D12	PCI_REQ64#
H4	PCI_RST#
M4	PCI_SEL100
A6	PCI_SERR#
C6	PCI_STOP#
D6	PCI_TRDY#
T15	PEX_LANE_GOOD0#
R15	PEX_LANE_GOOD1#
T16	PEX_LANE_GOOD2#
R16	PEX_LANE_GOOD3#
M5	PEX_PERn0
M7	PEX_PERn1
M9	PEX_PERn2
M11	PEX_PERn3
N5	PEX_PERp0
N7	PEX_PERp1
N9	PEX_PERp2
N11	PEX_PERp3
T1	PEX_PERST#
T5	PEX_PETn0
T7	PEX_PETn1
T9	PEX_PETn2
T11	PEX_PETn3
R5	PEX_PETp0
R7	PEX_PETp1
R9	PEX_PETp2
R11	PEX_PETp3
R3	PEX_REFCLKn
T3	PEX_REFCLKp

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
L5	STRAP_ARB
L4	STRAP_CLK_MST
N6	STRAP_EXT_CLK_SEL
P16	STRAP_FWD
P3	STRAP_PLL_BYPASS#
R2	STRAP_TESTMODE0
T2	STRAP_TESTMODE1
P15	STRAP_TRAN
E6	VDD10
E8	VDD10
E9	VDD10
E11	VDD10
F5	VDD10
F12	VDD10
G5	VDD10
G12	VDD10
J5	VDD10
J12	VDD10
K5	VDD10
K12	VDD10
M6	VDD10
M10	VDD10
M12	VDD10
M8	VDD10A
P8	VDD10S
R4	VDD10S
R6	VDD10S
R8	VDD10S
R10	VDD10S
R12	VDD10S
B2	VDD33
B8	VDD33
B12	VDD33
B15	VDD33
E5	VDD33
E7	VDD33
E10	VDD33
E12	VDD33

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
F2	VDD33
G15	VDD33
H5	VDD33
H12	VDD33
J2	VDD33
L12	VDD33
M3	VDD33
M15	VDD33
P12	VDD33
P4	VDD33A
B5	VSS
B13	VSS
C9	VSS
E2	VSS
F6	VSS
F7	VSS
F8	VSS
F9	VSS
F10	VSS
F11	VSS
F15	VSS
G6	VSS
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
H6	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
J6	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS

Table 2-11. Ball Assignments by Signal Name *(Cont.)*

Location	Signal Name
J11	VSS
K2	VSS
K6	VSS
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
L6	VSS
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L15	VSS
N8	VSS
N10	VSS
N12	VSS
P5	VSS
P6	VSS
P7	VSS
P9	VSS
P10	VSS
P11	VSS
T4	VSS
T8	VSS
T12	VSS
N4	VSSA
T6	VTT_PEX0
T10	VTT_PEX1

2.12 Physical Ball Assignment

Figure 2-1. PEX 8114 256-Ball PBGA Package Physical Ball Assignment (Underside View)

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	PCI_AD61	PCI_AD63	PCI_C/BE6#	PCI_ACK64#	PCI_AD1	PCI_AD3	PCI_AD7	PCI_AD10	PCI_AD12	PCI_AD14	PCI_SERR#	PCI_PCIXCAP	PCI_DEVSEL#	PCI_C/BE2#	PCI_AD19	PCI_AD21	A
B	PCI_AD59	VDD33	PCI_C/BE4#	VSS	VDD33	PCI_AD5	PCI_AD8	PCI_M66EN	VDD33	PCI_C/BE1#	PCI_PERR#	VSS	PCI_IRDY#	PCI_AD17	VDD33	PCI_AD23	B
C	PCI_AD57	PCI_AD62	PCI_PAR64	PCI_C/BE7#	PCI_AD0	PCI_AD2	PCI_AD6	VSS	PCI_AD11	PCI_AD15	PCI_STOP#	PCI_PCIXCAP_PU	PCI_AD16	PCI_AD20	PCI_AD22	PCI_C/BE3#	C
D	PCI_AD55	PCI_AD58	PCI_AD60	PCI_C/BE5#	PCI_REQ64#	PCI_AD4	PCI_C/BE0#	PCI_AD9	PCI_AD13	PCI_PAR	PCI_TRDY#	PCI_FRAME#	PCI_AD18	PCI_AD24	PCI_AD25	PCI_AD27	D
E	PCI_AD51	PCI_AD53	PCI_AD54	PCI_AD56	VDD33	VDD10	VDD33	VDD10	VDD10	VDD33	VDD10	VDD33	PCI_IDSEL	PCI_AD26	VSS	PCI_AD29	E
F	PCI_AD49	VSS	PCI_AD50	PCI_AD52	VDD10	VSS	VSS	VSS	VSS	VSS	VSS	VDD10	PCI_AD28	PCI_AD30	VDD33	PCI_AD31	F
G	PCI_AD47	VDD33	PCI_AD46	PCI_AD48	VDD10	VSS	VSS	VSS	VSS	VSS	VSS	VDD10	PCI_PME#	PCI_GNT# or PCI_GNT0#	PCI_REQ# or PCI_REQ0#	PCI_REQ1#	G
H	PCI_AD43	PCI_AD45	PCI_AD42	PCI_AD44	VDD33	VSS	VSS	VSS	VSS	VSS	VSS	VDD33	PCI_RST#	PCI_GNT1#	PCI_REQ2#	PCI_REQ3#	H
J	PCI_AD39	PCI_AD41	PCI_AD38	PCI_AD40	VDD10	VSS	VSS	VSS	VSS	VSS	VSS	VDD10	PCI_GNT2#	PCI_GNT3#	VDD33	PCI_CLK	J
K	PCI_AD35	PCI_AD37	PCI_AD34	PCI_AD36	VDD10	VSS	VSS	VSS	VSS	VSS	VSS	VDD10	PCI_INTC#	PCI_CLKO0	VSS	PCI_CLKO1	K
L	PCI_AD33	VSS	PCI_AD32	EE_PR#	VDD33	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_ARB	STRAP_CLK_MST	PCI_INTA#	PCI_CLKO2	PCI_CLKO3	L
M	EE_DI	VDD33	EE_SK	HP_PWRLED#	VDD10	PEX_PERn3	VDD10	PEX_PERn2	VDD10A	PEX_PERn1	VDD10	PEX_PERn0	PCI_SEL100	VDD33	PCI_INTD#	PCI_INTB#	M
N	EE_DO	EE_CS#	HP_PWREN#	HP_PWRFLT#	VSS	PEX_PERp3	VSS	PEX_PERp2	VSS	PEX_PERp1	STRAP_EXT_CLK_SEL	PEX_PERp0	VSSA	PCI_CLKO_DLY_FBK	JTAG_TDI	JTAG_TDO	N
P	STRAP_FWD	STRAP_TRAN	HP_PERST#	HP_PRSNT#	VDD33	VSS	VSS	VSS	VDD10S	VSS	VSS	VSS	VDD33A	STRAP_PLL_BYPASS#	JTAG_TMS	JTAG_TCK	P
R	PEX_LANE_GOOD3#	PEX_LANE_GOOD1#	HP_CLKEN#	HP_MRL#	VDD10S	PEX_PETp3	VDD10S	PEX_PETp2	VDD10S	PEX_PETp1	VDD10S	PEX_PETp0	VDD10S	PEX_REFCLKn	STRAP_TESTMODE0	JTAG_TRST#	R
T	PEX_LANE_GOOD2#	PEX_LANE_GOOD0#	HP_ATNLED#	HP_BUTTON#	VSS	PEX_PETn3	VTT_PEX1	PEX_PETn2	VSS	PEX_PETn1	VTT_PEX0	PEX_PETn0	VSS	PEX_REFCLKp	STRAP_TESTMODE1	PEX_PERST#	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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Chapter 3 Clock and Reset

3.1 PEX 8114 Clocking Introduction

Note: *The PEX 8114 is compliant with the PCI-X Addendum to PCI Local Bus Specification, Revisions 1.0b and 2.0a.*

The PCI/PCI-X clock domain PLL is driven by the 100-MHz PEX_REFCLKn/p input, as well as PCI_CLK input. When the PCI/PCI-X clock domain PLL is driven by PEX_REFCLKn/p, the PLL is used to synthesize the PCI system clock and is referred to as *operating in Clock Master mode*. When the PCI/PCI-X clock domain PLL is driven by PCI_CLK, it is referred to as *operating in Clock Slave mode*.

The PEX 8114 includes a PCI-X Bus Clock Generator and two internal clock domains – one each for PCI-X and PCI Express. The Clock Generator is capable of synthesizing common PCI Clock frequencies and driving four Clock Output balls, PCI_CLKO[3:0]. The PCI Express clock domain runs at a frequency that is compatible with 2.5 Gbps PCI Express data transmission rates, and is a Slave to the PEX_REFCLKn/p inputs. The PCI-X clock domain is driven by the PCI_CLK input system clock, and runs at the PCI-X Bus clock frequency.

3.1.1 PCI-X Clock Generator

The PEX 8114 PCI/PCI-X (PCI-X) Clock Generator is used to synthesize PCI-X Bus clocks. The PCI-X Clock Generator is driven by PEX_REFCLKn/p, and can generate four externally usable PCI-X Bus system clocks. These clocks are driven out of the PEX 8114 onto the PCI_CLKO[3:0] balls. PCI_CLKO[3:0] are designed to drive four external PCI devices.

In addition to PCI_CLKO[3:0], the Clock Master circuitry also provides a PCI_CLKO_DLY_FBK Clock Output ball. The PCI_CLKO_DLY_FBK output can optionally drive the PCI_CLK input to the PEX 8114, by way of a trace on the Printed Circuit Board (PCB). This ensures that the PCI-X System Clock-phase alignment requirements are satisfied when other devices are located requiring long clock lines on the PCB.

The PCI/PCI-X Clock Generator is enabled when the STRAP_CLK_MST input ball is High. The synthesized PCI/PCI-X clock frequency is determined by the PCI_M66EN, PCI_PCIXCAP, PCI_PCIXCAP_PU, and PCI_SEL100 balls. (Refer to Section 3.3.) The Clock Generator is capable of synthesizing frequencies at 25. 33. 50, 66, 100, and 133 MHz. When the Clock Generator is disabled, the PCI_CLKO[3:0] and PCI_CLKO_DLY_FBK signals are driven Low. Additionally, the PCI_CLKO[3:0] signals can be individually disabled by writing 0 to the register bit associated with that specific output (offset FA0h, *PCI_CLKO_EN[3:0]* field). When the PEX 8114 exits reset with STRAP_CLK_MST Low, the PCI_CLKO[3:0] and PCI_CLKO_DLY_FBK outputs are driven Low. When STRAP_CLK_MST is High at PEX 8114 reset, the PCI_CLKO[3:0] and PCI_CLKO_DLY_FBK outputs drive active clocks.

When the PEX 8114 is the Clock Master, it sets the mode (PCI or PCI-X) and the clock frequency when Reset de-asserts.

3.1.2 PCI-X Clocking of PCI-X Module

The PEX 8114 PCI-X module must be supplied a clock from the PEX 8114's internal Clock Generator or a system-level Clock Generator. The PCI clocks, at the Input ball of each device on the PCI Bus segment, must be frequency- and phase-aligned.

3.1.2.1 Clocking the PCI Module when PEX 8114 Clock Generator Is Not Used

When the PEX 8114 is not used as the PCI System Clock Generator, the PEX 8114 receives the PCI Bus System clock from its PCI_CLK input signal. The External Clock Generator is required to supply the clocks to the various PCI devices, allowing the devices to meet the phase-alignment requirements. The PCI-X module can be driven at PCI-X clock frequencies up to 133 MHz, as well as PCI clock frequencies down to DC. The PCI-X module determines to which mode (PCI or PCI-X) and frequency it is be driven at reset, by reading the initialization pattern on the PCI Bus, as described in the *PCI-X r1.0b* and *PCI-X r2.0a*.

3.1.2.2 Clocking the PCI Module when PEX 8114 Clock Generator Is Used

When the PEX 8114's clock generation circuitry is used (by setting STRAP_CLK_MST=1), the PCI clock can be driven to the PCI circuitry, internally or externally across the PCB:

- When the PCI clock must be internally driven from the PEX 8114's Clock Generator to the PEX 8114 PCI device, drive the STRAP_EXT_CLK_SEL ball Low.
- When the PCI clock must be externally driven on the PCB, run a clock trace from the PEX 8114's PCI_CLKO_DLY_FBK output to the PCI_CLK input, then drive the STRAP_EXT_CLK_SEL ball High. The ability to drive an external PCI_CLK PCB trace back to the PCI Express interface allows for delay, and the ability to align the PEX 8114's PCI_CLK input with the other device's PCI_CLK inputs, although the other device's clocks are driven across a long PCB trace. Typically, the PCB trace length from the PCI_CLKO_DLY_FBK output to the PCI_CLK input is equal to the length of the clock traces from the PEX 8114's PCI_CLKO[3:0] balls to the other external device's clock inputs.

3.2 Determining PCI Bus and Internal Clock Initialization

The STRAP_FWD and STRAP_CLK_MST Strapping balls are used to configure the PEX 8114 as a Forward or Reverse Transparent bridge and as a Clock Slave or Master. The PEX 8114 is capable of operating as a Forward or Reverse PCI Express bridge, using its internal PLL to synthesize a PCI clock for the PCI Bus, or it can become a Slave to an incoming PCI Clock:

- **PCI mode** – PEX 8114 is capable of operating as a Clock Master at 25, 33, 50, or 66 MHz, or Clock Slave, at frequencies from 66 MHz down to DC
- **PCI-X mode** – PEX 8114 is capable of operating as a Clock Master at 50, 66, 100, or 133 MHz, or Clock Slave, at frequencies from 133 MHz down to DC

To determine configuration of its internal resources and the PCI Bus when appropriate (because it is assuming the role of a central resource that performs bus initialization), the PEX 8114 can read the maximum bus capability and initialize the PCI Bus, accordingly.

This section defines actions the PEX 8114 takes to perform the following:

1. Determine the PCI Bus maximum capability.
2. Initialize its internal PCI PLL to Clock Master or Slave configuration.
3. Drive the initialization pattern at PCI_RST# de-assertion.
4. Drive or receive the PCI_RST# signal.

Table 3-1 defines the PEX 8114 operation when configured to run as a Forward or Reverse PCI Express bridge, as a Clock Master or Slave.

Table 3-1. PEX 8114 PCI Clock Configurations and Functions

Mode	Bus Capability	Internal Clock Configuration	Bus Initialization Pattern	PCI_RST#
Forward Transparent bridge as PCI Clock Master	Detects	Synthesize PCI clock and PCI_CLKO[3:0] balls	Drive	Drive
Forward Transparent bridge as PCI Clock Slave		Slave to PCI clock		
Reverse Transparent bridge as PCI Clock Master	Detects	Synthesize PCI clock and PCI_CLKO[3:0] balls	Drive	Receive
Reverse Transparent bridge as PCI Clock Slave	Does not detect	Slave to PCI clock	Receive	

3.2.1 Determining Bus Mode Capability and Maximum Frequency

The PEX 8114, as a Clock Master or Forward PCI Express bridge in Clock Slave mode, must determine the system's bus mode capabilities and maximum frequency, using the PCI_PCIXCAP and PCI_PCIXCAP_PU balls.

Table 3-2 defines the maximum clock frequency and PCI_PCIXCAP ball circuitry. For the three clock frequencies listed in the table, connect the PCI_PCIXCAP_PU ball to the PCI_PCIXCAP ball through a 1K-Ohm resistor. A 56K-Ohm resistor between 3.3V and the PCI_PCIXCAP ball is also required. The PEX 8114 detects this circuitry to determine the bus mode and maximum clock frequency, at power-up.

Table 3-2. Bus Mode, Maximum Clock Frequency, and PCI_PCIXCAP Ball Circuitry

Bus Mode	Maximum Clock Frequency	PCI_PCIXCAP Ball
PCI	66 MHz	Grounded
PCI-X	66 MHz	Grounded through an RC network
	133 MHz	Connected to a capacitor

3.3 PCI Clock Master Mode

When the PEX 8114 is strapped as the Clock Master (STRAP_CLK_MST=1), the PEX 8114 uses the 100 MHz Reference Clock (PEX_REFCLKn/p) to synthesize the PCI_CLKO clock(s). It determines the frequency to synthesize by sampling the PCI_M66EN, PCI_PCIXCAP, and PCI_SEL100 balls (refer to Table 3-3) during the clock initialization period. The clock initialization period is the time following PCI Express Power Good Reset input (PEX_PERST#) de-assertion, prior to PCI Reset (PCI_RST#) de-assertion.

During the clock initialization period, the PEX 8114 runs a simple state machine to determine the frequency generated by the clock synthesizer. The state machine samples the PCI_M66EN, PCI_PCIXCAP, and PCI_SEL100 balls to determine the correct PCI_CLKO frequency, initializes the clock synthesizer, drives the correct bus initialization values on the PCI_DEVSEL#, PCI_STOP#, and PCI_TRDY# signals and, when the PLL locks, de-asserts PCI_RST# (Forward Transparent Bridge mode) or waits for PCI_RST# de-assertion (Reverse Transparent Bridge mode).

When STRAP_FWD=1 (Forward Transparent Bridge mode), the PEX 8114 drives PCI_RST# and asserts PCI_RST# during the initialization period.

When STRAP_FWD=0 (Reverse Transparent Bridge mode), PCI_RST# is an input. The PEX 8114 drives initialization values on the PCI_DEVSEL#, PCI_STOP#, and PCI_TRDY# balls during the initialization period. In this configuration, the PEX 8114 requires external logic to drive PCI_RST#.

Table 3-3 defines the PLL divider frequency. Figure 3-1 through Figure 3-3 illustrate the pertinent signals and the clock initialization and reset sequence that the PEX 8114 follows when strapped in Clock Master mode.

Table 3-3. Clock Master Mode PLL Divider Frequency

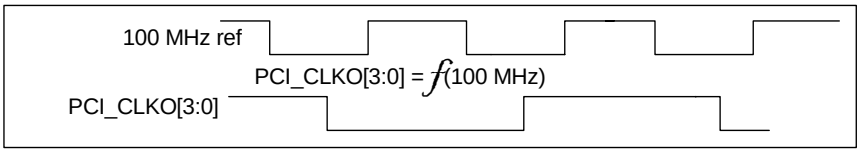
Mode	Clock Frequency	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
PCI	25 MHz	GND	1	0
	33 MHz		0	
	50 MHz		1	1
	66 MHz		0	
PCI-X	50 MHz	10K to GND	1	X
	66 MHz		0	
	100 MHz	High	1	
	133 MHz		0	

Note: *"X" indicates "Don't Care."*

3.3.1 Clock Master Mode Signals

Figure 3-1 illustrates the Clock signal for Clock Master mode.

Figure 3-1. Clock Signal for Clock Master Mode



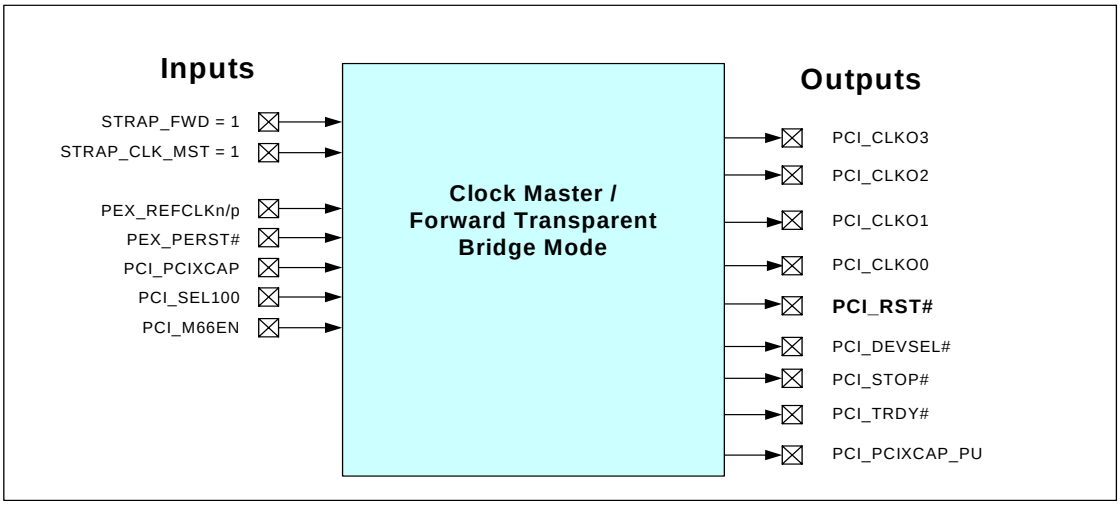
Notes:

1. PLL is driven by the 100-MHz PEX_REFCLKn/p.
2. PLL is used to generate 25, 33, 50, or 66 (PCI), or 66, 100, or 133 (PCI-X) MHz.
3. PCI_CLKO[3:0] frequency is synthesized from the 100-MHz signal.
4. PCI_CLKO[3:0] must drive the PCI Bus, and PCI_CLK is unused, unless the PEX 8114 is configured in Clock Feedback mode by strapping STRAP_EXT_CLK_SEL input High.
5. STRAP_CLK_MST=1.

Figure 3-2 illustrates the PEX 8114 configured as a Clock Master in Forward Transparent Bridge mode. This configuration uses the 100 MHz reference clock (PEX_REFCLKn/p) to generate 25-, 33-, 50-, 66-, 100-, or 133-MHz PCI_CLKO[3:0] signals and a phase-advanced internal clock. The diagram notes explain the clock's functions and limitations.

PCI_RST# is an output in Forward Transparent Bridge mode.

Figure 3-2. Clock Master Mode – Forward Transparent Bridge Mode



Step 1 PEX_PERST# is de-asserted, and STRAP_CLK_MST and STRAP_FWD are High.

Step 2 PEX 8114 reads PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100 to determine clock frequency.

Step 3 PEX 8114 loads its internal PLL values.

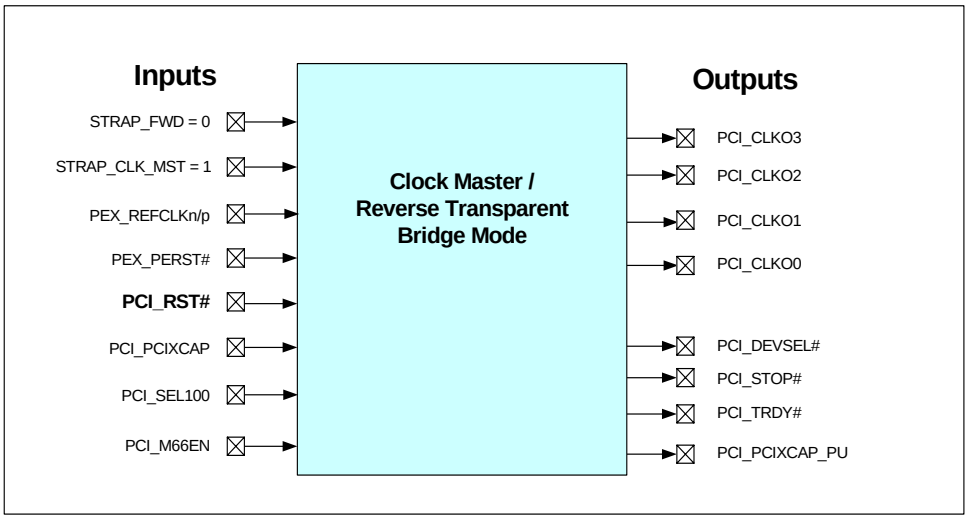
Step 4 PEX 8114 internal PLL reports lock up.

Step 5 PEX 8114 drives PCI_DEVSEL#, PCI_STOP#, and PCI_TRDY# initial values.

Step 6 PEX 8114 de-asserts PCI_RST#.

Figure 3-3 illustrates the Clock Master in Reverse Transparent Bridge mode. Reverse Transparent Bridge mode differs from Forward Transparent Bridge mode, in that the STRAP_FWD input ball is strapped Low and PCI_RST# becomes an input in Reverse Clock Master mode.

Figure 3-3. Clock Master Mode – Reverse Transparent Bridge Mode



Step 1 PEX_PERST# is de-asserted, STRAP_CLK_MST is High, and STRAP_FWD is Low.

Step 2 PEX 8114 reads PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100 to determine clock frequency.

Step 3 PEX 8114 loads its internal PLL values.

Step 4 PEX 8114 PLL reports lock up internally.

Step 5 PEX 8114 drives PCI_DEVSEL#, PCI_STOP#, and PCI_TRDY# initial values.

Step 6 PCI_RST# is de-asserted by external (system) logic. The external system logic must allow PCI_RST# to remain Low for 1 ms. Trst, as required by the *PCI r3.0*. Internal PLLs lock up during this 1 ms period.

3.4 PCI Clock Slave Mode

When the PEX 8114 is strapped as a Clock Slave (STRAP_CLK_MST=0), a PLL is used to cancel the internal Clock Fan-Out delay for PCI clock frequencies above 33 MHz. When a PCI_CLK frequency is 33 MHz or lower, the PLL is bypassed and PCI_CLK directly drives the PCI internal circuitry.

3.4.1 Clock Slave – Forward Transparent Bridge Mode

When the Clock Slave state machine is run in Forward Transparent Bridge mode, the PEX 8114 receives a clock, but takes responsibility to drive the PCI-X initialization pattern at reset. Because the PEX 8114 drives the initialization pattern, it detects the circuit connected to the PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100 ball states to determine the PCI Bus maximum clock frequency and which PCI-X initialization pattern to drive.

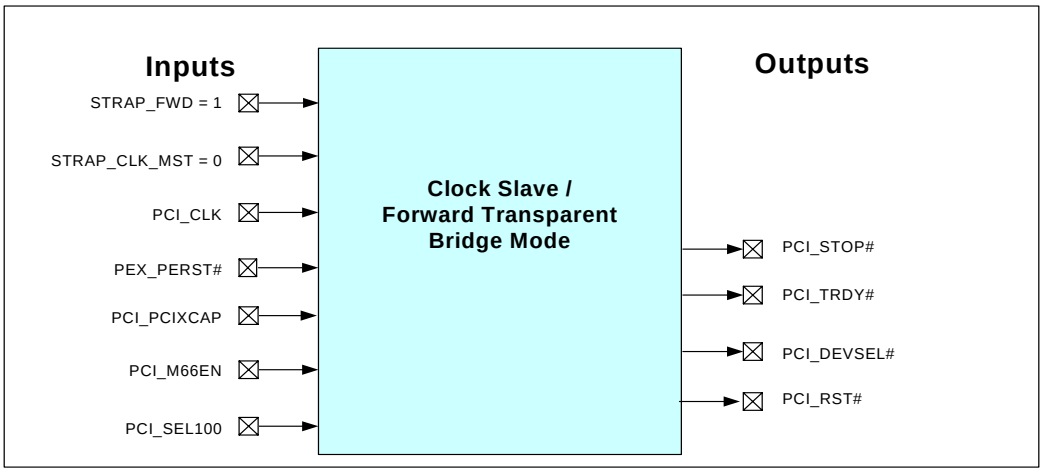
External clock generation circuitry must:

- Determine and set the clock frequency, according to the values on PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100, or
- Limit the system maximum clock frequency by driving values on PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100

This requires coordination of the Clock Generator frequency and the values that the PEX 8114 reads on the PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100 balls.

Figure 3-4 illustrates the pertinent signals and reset sequence that the PEX 8114 follows when strapped in Clock Slave mode. The PEX 8114 supplies the bus initialization in Forward Transparent Bridge mode.

Figure 3-4. Clock Slave Mode – Forward Transparent Bridge Mode



Step 1 PEX_PERST# is de-asserted, STRAP_CLK_MST is Low, and STRAP_FWD is High.

Step 2 PEX 8114 reads PCI_PCIXCAP, PCI_M66EN, and PCI_SEL100 to determine clock frequency at which PCI_CLK is driven into PEX 8114 by an external Clock Generator.

Step 3 PEX 8114 sets up to use its internal PLL and waits until lock if the clock frequency is greater than 33 MHz. If the clock frequency is 33 MHz or lower, the internal PLL is bypassed.

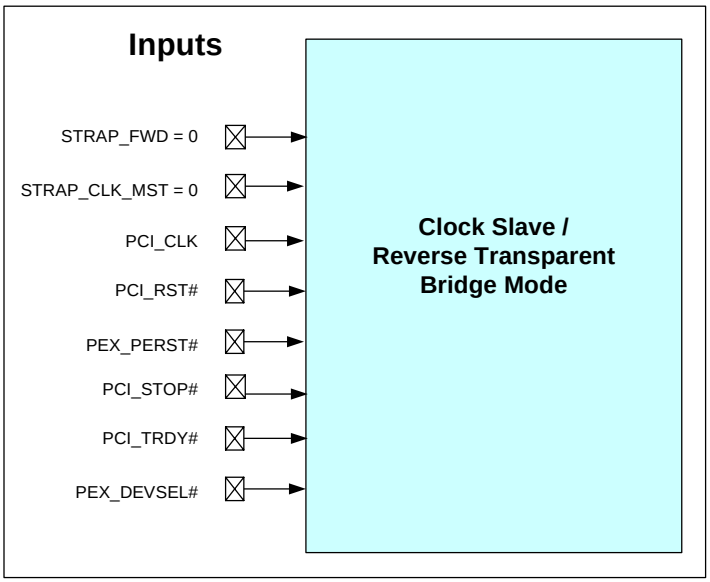
Step 4 PEX 8114 drives PCI_DEVSEL#, PCI_STOP#, and PCI_TRDY# during the initialization period prior to de-asserting PCI_RST#. An external source provides PCI_CLK.

3.4.2 Clock Slave – Reverse Transparent Bridge Mode

The PEX 8114 in Reverse Clock Slave mode, reads the initialization pattern at PCI_RST# de-assertion, to determine bus mode and clock frequency, then loads the internal PLL.

When the PEX 8114 is a Reverse Clock Slave, it is not the central resource and as such, it must detect the PCI-X initialization pattern to determine protocol and frequency. For this mode, PCI_PCIXCAP, PCI_PCIXCAP_PU, and PCI_SEL100 can be pulled High or Low.

Figure 3-5. Clock Slave Mode – Reverse Transparent Bridge Mode



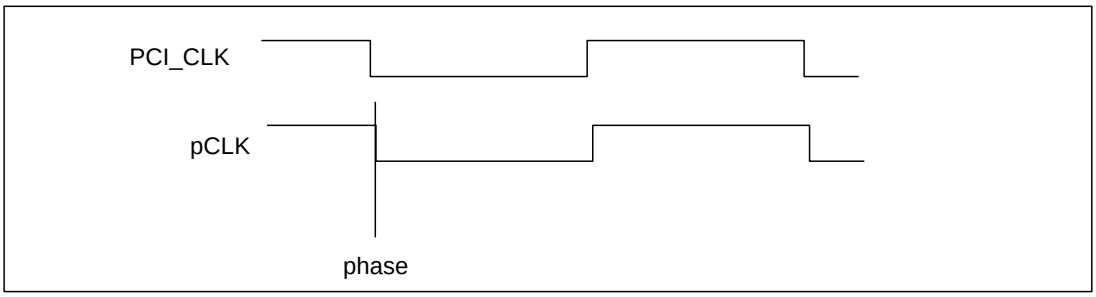
Step 1 PEX_PERST# is de-asserted, and STRAP_CLK_MST and STRAP_FWD are Low.

Step 2 PEX 8114 waits for PCI_RST# de-assertion and the initialization pattern (driven by a device other than PEX 8114).

Step 3 System PCI clock rate is indicated to the PEX 8114 by the initialization pattern at PCI_RST# de-assertion. If the PCI clock rate indicated by the initialization pattern is 33 MHz, bypass the internal PLL. If the initialization pattern indicates a clock rate greater than 33 MHz, load the internal PLL with appropriate settings.

3.4.3 Timing Diagrams – Forward or Reverse Transparent Bridge Mode

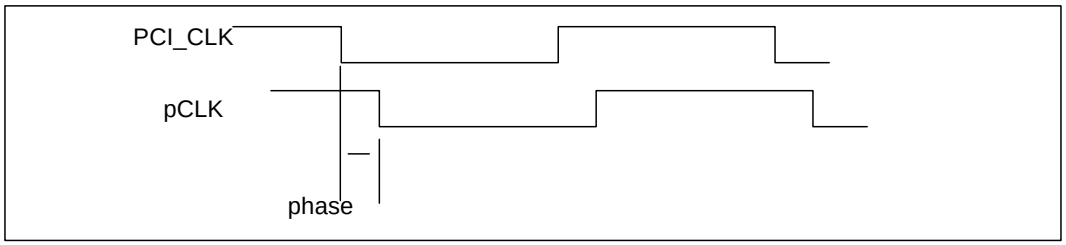
Figure 3-6. Phase Offset in Clock Slave Mode – Frequency > 33 MHz



Notes:

1. PLL is driven by the PCI_CLK input.
2. The PLL input and output frequencies are equal to one another. The PLL is used to provide phase advance to compensate for clock tree delay within the PEX 8114.
3. pCLK is equal to the PCI_CLK input, in frequency and phase.
4. STRAP_CLK_MST=0

Figure 3-7. Phase Offset in Clock Slave Mode – Frequencies ≤ 33 MHz



Notes:

1. PLL is bypassed. This is applicable to Clock Slave mode at PCI clock rates ≤ 33 MHz.
2. The internal pCLK is phase-delayed with respect to the PCI_CLK input.
3. PCI_CLK must drive the PCI/PCI-X Bus and PEX 8114. Do not use PCI_CLKO[3:0] to drive the PCI/PCI-X Bus PCI_CLK traces.
4. STRAP_CLK_MST=0.

The PCI Express and PCI-X PLLs contain a signal that indicates to the PEX 8114 whether the PLL lost the PLL lock. It is considered a serious error condition if the PCI Express or PCI-X PLL, when the PCI-X PLL is in Phase-Locked mode (*that is*, when not in PLL Bypass mode), indicates a loss of PLL lock and potential Data errors. Loss of PLL lock can be caused by one of the following:

- Serious out-of-specification noise
- Voltages on the PLL power inputs
- Out-of-specification jitter on the input reference clocks

Table 3-4 defines the options for handling loss of PLL lock. The options are selected by the *PLL Lock Control 1* and PLL Lock Control 0 bits (offset FA0h[11:10]). By default, this field is cleared to 00b, which configures the PEX 8114 to ignore loss of PLL lock.

Sticky bits are set when the PCI Express or PCI-X PLL loses PLL lock:

- When the PCI Express PLL loses PLL lock, the *Sticky PCI Express PLL Loss Lock* bit is set (offset FA0h[15]=1)
- When the PCI-X PLL loses PLL lock, the *Sticky PCI-X PLL Loss Lock* bit is set (offset FA0h[14]=1)

Table 3-4. Methods for Handling Loss of PLL Lock

Offset FA0h[11:10]	Description
00b	Default. Ignores loss of PLL lock.
01b	Loss of PLL lock immediately causes the PEX 8114 to reset.
10b	The PEX 8114 attempts to tolerate loss of PLL lock: • When lock is re-acquired in less than 200 µs, the PEX 8114 is not reset • When lock is not re-acquired within 200 µs, the PEX 8114 is reset
11b	The PEX 8114 is not reset if loss of PLL lock occurs.

3.5 Resets

This section explains the PEX 8114 Reset mechanism and how the differences between PCI Express and PCI-X resets are incorporated in Forward and Reverse Transparent Bridge modes. The *PCI Express r1.0a* and *PCI-X r1.0b* define two common levels or reset types, Level-1 and Level-2. The *PCI Express r1.0a* defines an additional third level, Level-0. Table 3-5 defines resets.

Table 3-5. Reset Table

Reset Type	PCI Express Definition	Reset Source	Impact to Various Internal Components (Upon De-assertion)	Impact to Internal Registers (No AUX and PME Enabled)
Level-0	Fundamental Reset • Cold Reset • Warm Reset	PEX_PERST# Reset input assertion	• Initialize entire bridge, including Sticky registers • Serial EEPROM contents are loaded • HwInit types evaluated	All registers initialized
Level-1	**Forward Transparent Bridge mode:** Hot Reset	• Reset bit of the TS Ordered-Set is set, at upstream port • Upstream port entering DL_Down state	• Initialize ports • Initialize entire bridge except the Sticky registers • Serial EEPROM contents re-loaded (selectively)	All registers initialized, with following exceptions: • Port Configuration registers • All Sticky bits not affected by Hot Reset (HwInit, R/WS, R/W1CS, ROS)
	Reverse Transparent Bridge mode: PCI_RST#	PCI_RST# is asserted on PCI/PCI-X Bus		
Level-2	Secondary Bus Reset	**Forward Transparent Bridge mode**	• Assert PCI_RST# on PCI-X Bus • Drain traffic • Drop request TLPs • Redefine Bus mode and clock frequency in Clock Master mode	No effect to CSRs
		Reverse Transparent Bridge mode	• PCI Express PL propagates Hot Reset • PCI Express DLL down • TLP layer initialized and exhibits DL_Down behavior • Drops request TLPs • Drain traffic corresponding to DL_Down behavior and initialize credits • Redefine Bus mode and clock frequency in Clock Master mode	No effect to CSRs (other than to initialize credits)

3.5.1 Level-0, Fundamental Reset (Power-On, Hard, Cold, Warm)

The *PCI Express r1.0a* defines the *Fundamental Reset* or *Level-0 Reset*. Level-0 Reset is a Fundamental Reset. It is equivalent to Traditional Power-On Reset.

For this type of reset, PEX_PERST# is *always an input to the* PEX 8114*, regardless of whether the bridge is operating in Forward or Reverse Transparent Bridge mode*. Reset assertion by the system, external to the PEX 8114, causes a reset of all internal PEX 8114 registers, including Sticky bits, and drives all state machines to known states.

3.5.1.1 PEX_PERST#

In PCI Express, Fundamental Reset can be provided by the system Host or central resource. The sideband PCI Express Reset signal (PEX_PERST#) is routed in parallel to all system PCI Express devices in conjunction with a Power Good signal from the system power supply. For the PEX 8114, the PEX_PERST# signal is always an input in Forward and Reverse Transparent Bridge modes, which indicates that the power is within specified tolerances and that the PEX 8114 performs internal Warm or Cold Reset.

In Forward Transparent Bridge mode, the PCI Express Root Complex feeds the PEX_PERST# signal to all devices. PEX_PERST# is driven in parallel to all PCI Express devices, following the PCI Express Power Good reset standard practice.

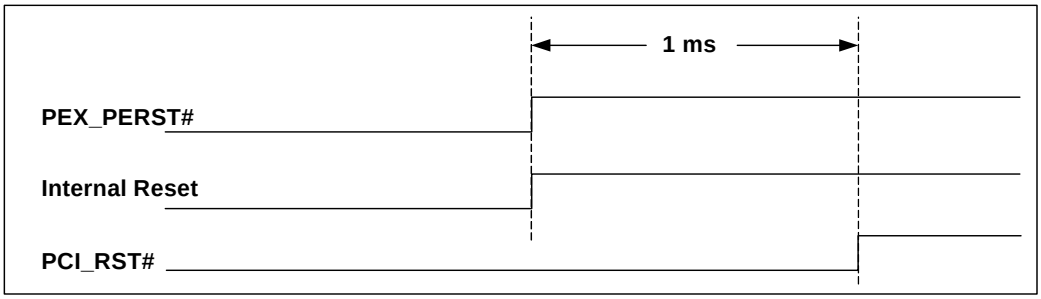
In Reverse Transparent Bridge mode, the PCI central resource, including power supply monitors, feeds the PEX_PERST# signal to all PCI Express devices. The mechanism traditionally used to reset PCI Bus segments is preserved in Reverse Transparent Bridge mode, by transmitting protocol Hot Resets to reset bridges and bus segments.

When the PEX 8114 is operating in Reverse Transparent Bridge mode, the PEX_PERST# signal is expected to function similar to the pwr_good signal in the *PCI r3.0*, Figure 4.11, and to follow the timing and functionality defined in the *PCI r3.0*, Section 4.3.2.

3.5.1.2 Level-0 Reset – Forward Transparent Bridge Mode

In Forward Transparent Bridge mode, when the system asserts PEX_PERST# to the PEX 8114, PCI_RST# is asserted on the PCI/PCI-X Bus. Figure 3-8 illustrates the timing relationship between PEX_PERST#, PCI_RST#, and the PEX 8114 internal reset in Forward Transparent Bridge mode.

Figure 3-8. PEX_PERST# Input, PCI_RST# Output, and Internal Reset Timing in Forward Transparent Bridge Mode



Timing Requirement

The *PCI r3.0* places a power-up timing requirement on the PCI_RST# bus reset signal (*that is*, PCI_RST# must remain asserted for 1 ms after power becomes stable). This applies to the PEX 8114 in Forward Transparent Bridge mode because the PEX 8114 asserts PCI_RST# in this mode.

When power is first applied, PEX_PERST# is asserted by the central resource and remains asserted until power is stable. PCI_RST# is asserted for 1 ms after PEX_PERST# de-assertion, to guarantee that PCI_RST# is asserted for 1 ms after power stabilizes.

Manual Switches – Defining a Warm Reset in Forward Transparent Bridge Mode

The PCI Express Reset, from the PEX_PERST# input ball, is a Level-0 Reset asserted on power-up until board power stabilizes.

On-board manual switches for Hard Resets to the PEX 8114 also control PEX_PERST# when an on-board Reset switch or similar mechanism is used to assert Reset by way of PEX_PERST# without cycling the power supply (Warm Reset).

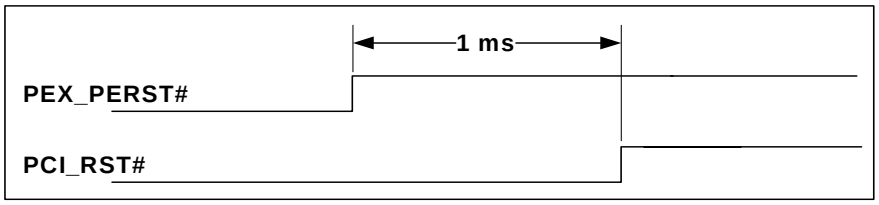
Note: *Perform Warm Resets only in Forward Transparent Bridge mode.*

3.5.1.3 Level-0 Reset – Reverse Transparent Bridge Mode

In Reverse Transparent Bridge mode, PCI_RST# is an input. The PEX 8114 requires that PCI_RST# be asserted during PEX_PERST# assertion and for an additional 1 ms after PEX_PERST# de-assertion.

Figure 3-9 illustrates the PEX_PERST# and PCI_RST# timing waveforms during Fundamental Reset in Reverse Transparent Bridge mode.

Figure 3-9. PEX_PERST# and PCI_RST# Timing in Reverse Transparent Bridge Mode



Timing Requirement

In Reverse Transparent Bridge mode, after power-on, PEX_PERST# (by the central resource) and PCI_RST# (by the upstream bridge) are asserted. PEX_PERST# and PCI_RST# must remain asserted until power becomes stable.

When power is stable, PEX_PERST# must de-assert first and, a minimum of 1 ms later, PCI_RST# can de-assert. There is no limit on the maximum PEX_PERST# assertion time; however, PCI_RST# must continue 1 ms longer or the PEX 8114 might not function correctly. This requirement is associated with initialization pattern capture.

Manual Switches – Defining a Warm Reset in Reverse Transparent Bridge Mode

In Reverse Transparent Bridge mode, when PEX_PERST# is asserted, PCI_RST# must also be asserted. When PCI_RST# is asserted, the initialization pattern is driven on the PCI/PCI-X Bus and the pattern is captured when PCI_RST# is de-asserted.

When the PEX 8114 is strapped as the Clock Master in Reverse Transparent Bridge mode, it drives the initialization pattern on the PCI/PCI-X Bus, but not the PEX 8114 PCI_RST# signal.

3.5.2 Level-1, Hot Reset

The *Level-1 Reset* defined by *PCI Express r1.0a* is carried on the PCI_RST# ball. This reset level is defined by the *PCI Express r1.0a* as an in-band message communicated across a link and is referred to as a *Hot Reset*. Level-1 Reset causes the reset of internal registers and state machines, but not register Sticky bits. This reset also propagates across the bridge and to the downstream devices.

3.5.2.1 Level-1 Reset – Forward Transparent Bridge Mode

When the PEX 8114 is reset during standard operation in Forward Transparent Bridge mode, it is achieved by receiving the in-band messaging reset or Hot Reset.

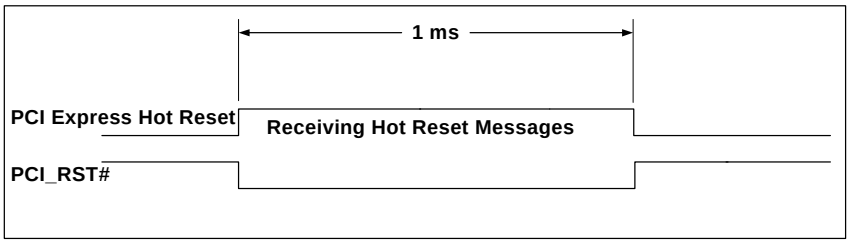
Level-1 Reset is received by the PEX 8114 on the PCI Express link as an in-band message and propagated downstream, through PCI_RST# assertion as an output signal.

Level-1 Reset is propagated to the PEX 8114 by way of an in-band reset message through the PCI Express link, using the physical layer mechanism (the Reset bit in the Training Ordered-Set from the upstream device is asserted).

In addition to the in-band reset, if the PEX 8114 upstream PCI Express port proceeds to a DL_Down state, for any reason, this is also treated as a Hot Reset or Level-1 Reset. This reset is propagated downstream from the PEX 8114, by asserting a reset on PCI_RST#. PCI_RST# is asserted if the in-band Hot Reset is received by the PCI Express interface.

The *PCI r3.0* requires that PCI_RST# reset, applied during standard operation, must retain a minimum assertion time of 1 ms. In the case of a Hot Reset, the Host software must provide the 1 ms PCI_RST# duration, by transmitting the in-band Hot Reset for 1 ms. Figure 3-10 illustrates the timing of propagating PCI_RST# when a Hot Reset is received by the PCI Express interface.

Figure 3-10. In-Band Hot Reset, PCI_RST#, and Internal Reset Timing in Forward Transparent Bridge Mode



3.5.2.2 Level-1 Reset – Reverse Transparent Bridge Mode

In Reverse Transparent Bridge mode, Level-1 Reset is received by the PEX 8114 on the PCI-X interface PCI_RST# ball as an input, and propagated downstream as an in-band message on the PCI Express link (using the Physical Layer mechanism).

Level-1 Reset is the equivalent to Hot Reset in Forward Transparent Bridge mode received on the PCI Express interface. It causes the reset of internal registers and state machines, but not register Sticky bits.

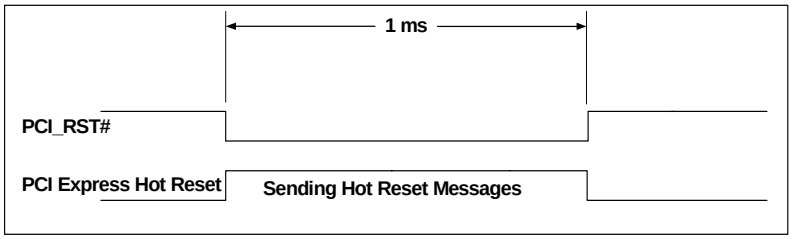
The *PCI r3.0* requires that PCI_RST# be asserted for a minimum of 1 ms.

Level-1 Reset also causes the serial EEPROM reload, bus mode recheck, and clock frequency recheck.

When PCI_RST# is asserted, it is propagated across the bridge and downstream on the PCI Express link as a Hot Reset. During the time that PCI_RST# is asserted in-band, Hot Reset messages are continuously transmitted across the PCI Express link.

Figure 3-11 illustrates the timing relationship between PCI_RST# and transmitting in-band Hot Reset messages.

Figure 3-11. PCI_RST# and Hot Reset Message Timing in Reverse Transparent Bridge Mode



3.5.3 Secondary Bus Reset, Level-2 Reset

Level-2 Reset is provided by the internal **Bridge Control** register *Secondary Bus Reset* bit (bit 6). This reset drives the bridge state machines to a known state, but not internal register resets. This reset also propagates a reset to downstream devices in the same manner as Level-1 Reset.

Level-2 Resets are sustained until the *Secondary Bus Reset* bit is cleared. This bit is set and cleared by software, using Configuration Write accesses.

The Secondary Bus Reset is used to reset all downstream devices, without resetting the bridge.

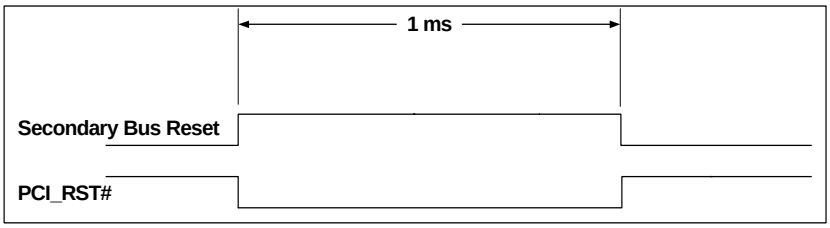
3.5.3.1 Level-2 Reset – Forward Transparent Bridge Mode

Level-2 Reset, when the *Secondary Bus Reset* bit is set to 1, is propagated downstream in Forward Transparent Bridge mode, through PCI_RST# assertion.

In Forward Transparent Bridge mode, PCI_RST# is asserted on the PCI/PCI-X Bus when this bit is set. The minimum duration for PCI_RST# is 1 ms. The PEX 8114 internal state machines are forced to initial states and internal transaction queues are flushed.

Figure 3-12 illustrates the timing relationship between Secondary Bus Reset and PCI_RST# in Forward Transparent Bridge mode.

Figure 3-12. Secondary Bus Reset and PCI_RST# Timing in Forward Transparent Bridge Mode



3.5.3.2 Level-2 Reset – Reverse Transparent Bridge Mode

Level-2 Reset, when the *Secondary Bus Reset* bit is set to 1, is propagated downstream through an in-band message on the PCI Express link.

When this bit is set in Reverse Transparent Bridge mode, in-band message reset is communicated through the PCI Express link from the PEX 8114 to the downstream devices. The PEX 8114 internal state machines are forced to initial states and internal transaction queues are flushed.

Figure 3-13 illustrates the relationship between the Secondary Bus Reset bit and transmitting in-band Hot Reset messages.

Figure 3-13. Secondary Bus Reset and Hot Reset Message Timing in Reverse Transparent Bridge Mode

3.6 Serial EEPROM Load Sequence

Serial EEPROM data is loaded when a Level-1 Reset is de-asserted. Level-1 Reset is asserted during the following:

- Power-on reset
- PEX_PERST# assertion
- Hot Reset (Forward Transparent Bridge mode)
- PCI_RST# assertion (Reverse Transparent Bridge mode)

The serial EEPROM data is read from the serial EEPROM and written into the Configuration registers. This process takes approximately 8,000 PCI Bus Clock cycles. Figure 3-14 illustrates the timing of Level-1 Reset and serial EEPROM data loading.

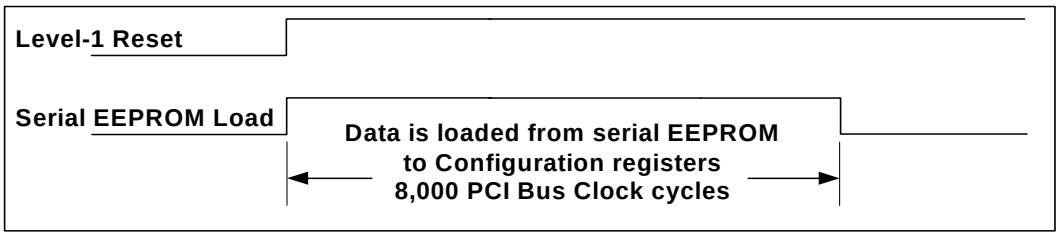
When a serial EEPROM is present, as indicated by the EE_PR# ball, the Serial EEPROM Controller is triggered to perform a serial EEPROM load under the following conditions:

- Upon Level-0 Reset de-assertion
- Upon Level-1 Reset de-assertion

The purpose of loading from serial EEPROM on a Level-1 Reset is to restore registers to customized values, stored in the serial EEPROM, after a Level-1 (Hot) Reset initializes registers to default values.

Consider the typical usage model wherein the serial EEPROM contents are modified after a Level-0 Reset. It is possible for a system to change the serial EEPROM contents through the Serial EEPROM Controller after a Level-0 Reset and restore the values, as modified, with a load upon a Level-1 Reset.

Figure 3-14. Level-1 Reset and Loading of Serial EEPROM Data Timing



Chapter 4 Data Path

4.1 Internal Data Path Description

The PEX 8114 bridge supports Data transfers from the PCI-X port to the PCI Express port. The PCI-X port operates in PCI or PCI-X mode, at clock rates up to 133 MHz and 32- or 64-bit bus widths. The PCI Express port is four lanes wide and can be configured as a 4-, 2-, or 1-lane port.

The PEX 8114 internal data path is based on a central RAM. which holds and orders all data transferred through the bridge in three separate linked lists including Posted, Non-Posted and Completion data. There is a separate, central 8-KB RAM for data flowing in each direction. All transactions are held within the RAM in a double store-and-forward method. Separate link lists for Posted and Non-Posted transactions, as well as Completions, share space within the RAM and all link list accesses to the internal RAM output are governed, according to PCI Express Ordering rules.

At least 2 KB of the 8-KB RAM are dedicated to Completions. Completions can optionally require as much as 6 KB of memory, according to demand. The remainder of the RAM is used for Posted and Non-Posted requests, or remains empty. In addition to the central RAM, there are eight, 256-byte buffers in the PCI modules that track and combine the data (for up to eight concurrent Non-Posted PCI requests) with their Completion data when the Completion returns from the PCI Express link. (Refer to Chapter 7, "Bridge Operations," for further details.)

Additionally, the PCI interface modules include eight data-holding register sets that are dedicated to tracking the Completion progress of eight PCI Express requests on the PCI Bus. These registers hold information that uniquely identifies the Target location and data quantity requested, for up to eight PCI Express requests. As the PCI module's state machines supply the data requested by the PCI Express device, these registers track progress toward Completion. After a transaction completes, the internal resources dedicated to that transaction are recovered and readied to service a new transaction.

4.2 PCI Express Credits

PCI Express credits are issued according to the PCI Express requirements to manage the internal 8-KB central RAM and ensure that no internal memory linked list is overrun.

4.3 Latency and Bandwidth

The PEX 8114 can be configured as a PCI or PCI-X device at up to 133 MHz and 64-bit data bus on the PCI-X side, transacting data with the PCI Express port configured as a 1-, 2-, or 4-lane port. It is anticipated that from a bandwidth-balancing perspective, the PCI Express port configured as a 4-lane device matches well with the PCI-X side operating at 133 MHz and 64 bits. In this matched configuration, expect full bandwidth utilization on the PCI Express lanes and PCI-X Bus, with throughput limitations being the external PCI Express and PCI-X ports' bandwidth capability and not the PEX 8114's internal bandwidth. A 66-MHz, 64-bit PCI-X port should match a x2 PCI Express port. It is anticipated that the PEX 8114 does not limit the bandwidth of those transactions. Bandwidth is affected by many parameters, including but not limited to arbitration latency, cycle startup latency, Retries, packet sizes, and external endpoint latency. Adjust the parameters within the PEX 8114, based on the *PCI Express-to-PCI/PCI-X Bridge r1.0*.

4.3.1 Data Flow-Through Latency

When the PEX 8114 is configured as a PCI-X device, operating at 133-MHz clock frequency with a 64-bit wide data bus, and the PCI Express port is configured as a 4-lane link, expect approximately 300 ns latency through the PEX 8114 for Header-only packets and approximately 850 ns for Headers with 256-byte Data packets. This is the latency of data driven from PCI-X to PCI Express. This latency is measured from the frame drop on the PCI-X Bus, when data is driven into the PEX 8114, until the starting symbol of data TLP appears on the PCI Express lanes. Internal latency of data driven from PCI Express to PCI-X is similar.

4.3.2 PCI Transaction Initial Latency and Cycle Recovery Time

In PCI mode, when the PEX 8114 is a Read Cycle Target, the PEX 8114 supplies data or Retries the Master Read request. There are eight Clock cycles from when the Master asserts PCI_FRAME# until the PEX 8114 signals a Retry or is ready to supply data. This equates to an initial target latency of eight clocks.

When the PEX 8114 is the Write Cycle Master, there is one Clock cycle from when the Master drives PCI_FRAME# until the PEX 8114 drives PCI_IRDY# ready to supply data. This cycle is the Address phase, required by the *PCI r3.0*. There are no initial wait states added by the PEX 8114. The PEX 8114 is a slow-decode device and supports fast back-to-back addressing.

The PEX 8114 requires certain Clock cycles after completion of a previous transaction before it can participate in another transaction. This period is comprised of the Clock cycles from the last Data phase of the preceding transaction until PCI_FRAME# is asserted on a new transaction, and is referred to as *transaction cycle recovery time*. The cycle recover time from mastering a PCI-X transaction is 10 Clock cycles.

4.3.3 PCI-X Transaction Initial Latency and Cycle Recovery Time

In PCI-X mode, when the PEX 8114 is a Read Transaction Target, there are seven Clock cycles from when the Master asserts PCI_FRAME# until the PEX 8114 drives a Split Response to the PCI-X Read request. When the PEX 8114 is a PCI-X Write Cycle Target, there are seven Clock cycles from when the Master asserts PCI_FRAME# until the PEX 8114 drives PCI_IRDY# ready to accept data. This equates to an initial Target latency of two clocks.

When the PEX 8114 is a Write or Read Completion Master, there are three Clock cycles from when the PEX 8114 asserts PCI_FRAME# until the PEX 8114 asserts PCI_IRDY# indicating that it is ready to drive data. These three Clocks cycles are the Address, Attribute, and Turnaround cycles required by the *PCI-X r2.0a*. There are no initial wait states added by the PEX 8114. The PEX 8114 is a slow-decode device and supports fast back-to-back addressing.

The PEX 8114 requires certain Clock cycles after the completion of a previous transaction, before it can participate in another transaction. This period is comprised of the Clock cycles from the last Data phase of the preceding transaction until PCI_FRAME# is asserted on a new transaction, and is referred to as *transaction cycle recovery time*. The cycle recover time for mastering a PCI cycle is seven Clock cycles.

4.3.4 Arbitration Latency

Arbitration latency is the number of PCI Clock cycles required for the bridge to be granted the bus when it is waiting to make a transfer. This time can vary and is a function of the number of devices on the PCI Bus and each device's demand for bus control. At a minimum, the bus can be parked on the bridge and in that case, the arbitration latency is 0 clocks. If the bus is not parked on the bridge and not being used by another device, the latency is 1 clock after the request. If the bus is being used by another Master and hidden arbitration is enabled, the arbitration latency is 1 clock after the other users relinquish the bus. If the bus is being used by another Master and hidden arbitration is not enabled, the arbitration latency is 2 clocks after the other users relinquish the bus.

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Chapter 5 Address Spaces

5.1 Introduction

This chapter discusses the PEX 8114 Address spaces.

5.2 Supported Address Spaces

The PEX 8114 supports the following Address spaces:

- PCI-compatible Configuration (00h to FFh; 256 bytes)
- PCI Express Extended Configuration (100h to FFFh)
- I/O (32-bit; includes ISA and VGA modes)
- Memory-Mapped I/O (32-bit non-prefetchable)
- Prefetchable memory (64-bit)
- Base Address register (BAR) access to internal registers

The first two spaces, used for accessing Configuration registers, are described in Chapter 6, "Configuration." The PCI Express Extended Configuration space (100h to FFFh) is supported only in Forward Transparent Bridge mode, and BARs are used to access Extended Configuration space in Reverse Transparent Bridge mode.

Configuration registers set up for I/O, Memory-Mapped and Prefetchable Memory Address spaces determine which transactions are forwarded from the primary bus to the secondary bus and from the secondary bus to the primary bus. The I/O and Memory ranges are defined by a set of **Base** and **Limit** registers in the Configuration Header. Transactions falling within the ranges defined by the **Base** and **Limit** registers are forwarded from the primary bus to the secondary bus. Transactions falling outside these ranges are forwarded from the secondary bus to the primary bus.

Table 5-1 defines which interfaces are primary and secondary, for the two PEX 8114 bridge modes.

Table 5-1. Bridge Mode Primary and Secondary Interfaces

Bridge Mode	Primary Interface/Bus	Secondary Interface/Bus
Forward Transparent Bridge	PCI Express	PCI
Reverse Transparent Bridge	PCI	PCI Express

5.2.1 I/O Space

The I/O Address space determines whether to forward I/O Read or I/O Write transactions across the bridge. PCI Express uses the 32-bit Short Address Format (DWord-aligned) for I/O transactions.

5.2.1.1 Enable Bits

The following Configuration register bits control the bridge response to I/O transactions:

- **Command** register *I/O Access Enable* bit
- **Command** register *Bus Master Enable* bit
- **Bridge Control** register *ISA Enable* bit
- **Bridge Control** register *VGA Enable* bit

Set the *I/O Access Enable* bit to allow I/O transactions to be forwarded downstream. When this bit is not set, all I/O transactions on the secondary bus are forwarded to the primary bus. If this bit is not set in Forward Transparent Bridge mode, all primary interface I/O requests are completed with Unsupported Request status. If this bit is not set in Reverse Transparent Bridge mode, all I/O transactions are ignored (no PCI_DEVSEL# assertion) on the primary (PCI) bus.

Set the *Bus Master Enable* bit to allow I/O transactions to forward upstream. If this bit is not set in Forward Transparent Bridge mode, all I/O transactions on the secondary (PCI) bus are ignored. If this bit is not set in Reverse Transparent Bridge mode, all I/O requests on the secondary (PCI Express) bus are completed with Unsupported Request status.

Setting the *ISA Enable* bit affects I/O transactions. (Refer to Section 5.2.1.3, "ISA Mode," for details.) Setting the *VGA Enable* bit also affects I/O transactions. (Refer to Section 5.2.1.4, "VGA Mode," for details.)

5.2.1.2 I/O Base and Limit Registers

The PEX 8114 supports the *optional* 32-bit I/O Addressed access. The following **I/O Base** and **Limit** Configuration registers are used to determine whether I/O transactions can be forwarded across the bridge:

- **I/O Base** (upper four bits of the 8-bit register correspond to Address bits [15:12])
- **I/O Base Upper 16 Bits** (16-bit register corresponds to Address bits [31:16])
- **I/O Limit** (upper four bits of the 8-bit register correspond to Address bits [15:12])
- **I/O Limit Upper 16 Bits** (16-bit register corresponds to Address bits [31:16])

The I/O Base address consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O Base address. The lower four bits of the 8-bit register determine the I/O address capability of this device. The **I/O Base Upper 16 Bits** register define bits [31:16] of the I/O Base address.

The I/O Limit address consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O limit. The lower four bits of the 8-bit register determine the I/O address capability of this device, and reflect the value of the same field in the **I/O Base** register. The **I/O Limit Upper 16 Bits** register defines bits [31:16] of the I/O Limit address.

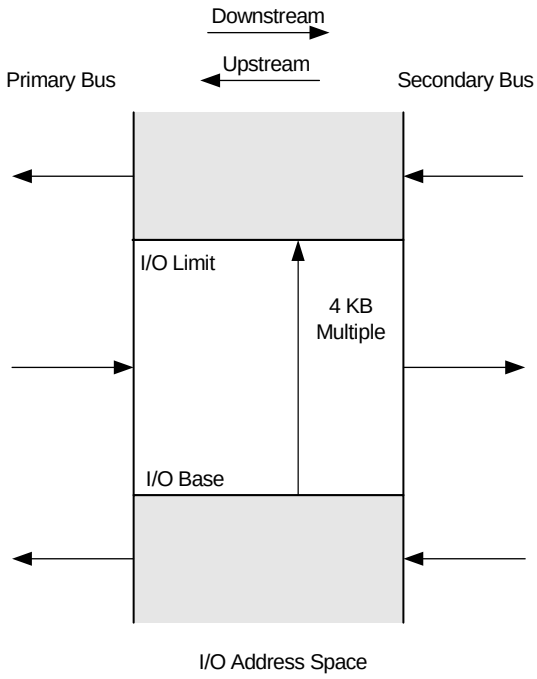
Because Address bits [11:0] are not included in Address Space decoding, the I/O Address range has a granularity of 4 KB, and is always aligned to a 4-KB Address Boundary space. The maximum I/O range is 4 GB.

I/O transactions on the primary bus that fall within the range defined by the Base and Limit addresses are forwarded downstream to the secondary bus. I/O transactions on the secondary bus that are within the range are ignored.

I/O transactions on the primary bus that do not fall within the range defined by the Base and Limit addresses are ignored. I/O transactions on the secondary bus that do not fall within the range are forwarded upstream to the primary bus. Figure 5-1 illustrates I/O forwarding.

When the I/O Base address specified by the **I/O Base** and **I/O Base Upper 16 Bits** registers have a value greater than the I/O Limit address specified by the **I/O Limit** and **I/O Limit Upper 16 Bits** registers, the I/O range is disabled. In this case, all I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

Figure 5-1. I/O Forwarding



5.2.1.3 ISA Mode

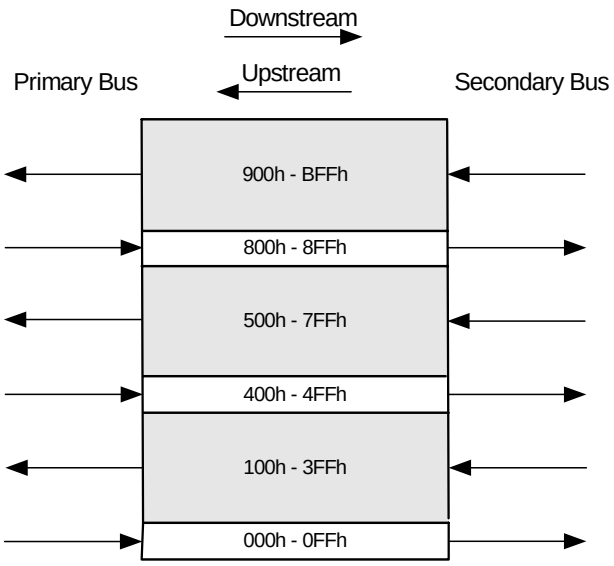
The **Bridge Control** register *ISA Enable* bit supports I/O forwarding in systems that include an ISA Bus. The *ISA Enable* bit affects I/O addresses within the range defined by the **I/O Base** and **I/O Limit** registers, located within the first 64 KB of the I/O Address space.

When the *ISA Enable* bit is set, the bridge does not forward I/O transactions downstream on the primary bus, located within the top 768 bytes of each 1-KB block within the first 64 KB of Address space. Transactions in the lower 256 bytes of each 1-KB block are forwarded downstream. If the *ISA Enable* bit is clear, all addresses within the range defined by the **I/O Base** and **I/O Limit** registers are forwarded downstream. I/O transactions with addresses located above 64 KB are forwarded, according to the range defined by the **I/O Base** and **I/O Limit** registers.

When the *ISA Enable* bit is set, the bridge forwards I/O transactions upstream on the secondary bus, located within the top 768 bytes of each 1-KB block within the first 64 KB of Address space, when the address is within the range defined by the **I/O Base** and **I/O Limit** registers. All other transactions on the secondary bus are forwarded upstream if they fall outside the range defined by the **I/O Base** and **I/O Limit** registers. If the *ISA Enable* bit is clear, all secondary bus I/O addresses outside the range defined by the **I/O Base** and **I/O Limit** registers are forwarded upstream.

As with all upstream I/O transactions, the **Command** register *Bus Master Enable* bit must be set to enable upstream forwarding. Figure 5-2 illustrates I/O forwarding with the *ISA Enable* bit set.

Figure 5-2. I/O Forwarding with ISA Enable Bit Set



ISA I/O Address Space Example

5.2.1.4 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Register accesses to forward downstream from the primary to secondary bus, independent of the **I/O Base** and **I/O Limit** registers.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O address decoding, and is applicable when the *VGA Enable* bit is set.

The *VGA Enable* and *VGA 16-Bit Decode* bits control the following VGA I/O addresses:

- **10-bit VGA I/O addressing** – Address bits [9:0] = 3B0h through 3BBh, and 3C0h through 3DFh
- **16-bit VGA I/O addressing** – Address bits [15:0] = 3B0h through 3BBh, and 3C0h through 3DFh

These ranges only apply to the first 64 KB of I/O Address space.

VGA Palette Snooping

VGA Palette snooping is not supported by PCI Express-to-PCI bridges; however, the PEX 8114 supports VGA Palette snooping in Reverse Transparent Bridge mode. In Forward Transparent Bridge mode, the **Bridge Control** register *VGA Enable* bit determines whether VGA Palette accesses are forwarded from PCI Express-to-PCI. The **Command** register *VGA Palette Snoop* bit is forced to 0 in Forward Transparent Bridge mode.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O Palette Snooping Address decoding, and is applicable when the *VGA Palette Snoop* bit is set.

The *VGA Palette Snoop* and *VGA 16-Bit Decode* bits control the following VGA I/O Palette Snoop addresses:

- **10-bit VGA I/O addressing** – Address bits [9:0] = 3C6h, 3C8h, and 3C9h
- **16-bit VGA I/O addressing** – Address bits [15:0] = 3C6h, 3C8h, and 3C9h

The PEX 8114 supports the following three modes of VGA Palette snooping:

- Ignore VGA Palette accesses when there are no graphic agents downstream that must snoop or respond to VGA Palette Access cycles (Writes or Reads)
- Positively decode and forward VGA Palette Writes when there are graphic agents downstream from the PEX 8114 that must snoop VGA Palette Writes (Reads are ignored)
- Positively decode and forward VGA Palette Writes and Reads when there are graphic agents downstream that must snoop or respond to VGA Palette Access cycles (Writes or Reads)

The **Bridge Control** register *VGA Enable* bit and **Command** register *VGA Palette Snoop* bit select the bridge response to VGA Palette accesses, as defined in Table 5-2.

Table 5-2. Bridge Response to VGA Palette Accesses

VGA Enable Bit (Offset 3Ch[19])	VGA Palette Snoop Bit (Offset 04h[5])	Bridge Response to VGA Palette Accesses
0	0	Ignore all VGA Palette accesses
0	1	Positively decode VGA Palette Writes (ignore Reads)
1	X	Positively decode VGA Palette Writes and Reads

Note: *X is "Don't Care."*

5.2.2 Memory-Mapped I/O Space

The Memory-Mapped I/O Address space determines whether to forward Non-Prefetchable Memory Write or Read transactions across the bridge. Map devices with side effects during Reads, *such as* FIFOs, into this space. For PCI-to-PCI Express Reads, prefetching occurs in this space when Memory Read Line or Memory Read Line Multiple commands are issued on the PCI Bus. When the Memory Read Line command is used, the data quantity prefetched is determined by the *Cache Line Size* value. When a Memory Read Line Multiple is used, the data quantity prefetched is determined by the Cache Line Size field (offset 0Ch[7:0]) and *Cache Line Prefetch Line Count* bit (offset FA0h[4]). For PCI-to-PCI Express transactions, the Prefetched data is flushed after the PCI device reading the data terminates its first successful Read transaction during which it receives data. For PCI-X-to-PCI Express Reads, the number of bytes to read is determined by the transaction size requested in the PCI-X attributes. For PCI Express-to-PCI or PCI-X Reads, the number of bytes to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this Address space are limited to a 32-bit range.

5.2.2.1 Enable Bits

The following Configuration register bits control the bridge response to Memory-Mapped I/O transactions:

- **Command** register *Memory Access Enable* bit
- **Command** register *Bus Master Enable* bit

Set the *Memory Access Enable* bit to allow Memory transactions to forward downstream. If this bit is not set, all Memory request transactions on the secondary bus are forwarded to the primary bus. If this bit is not set in Forward Transparent Bridge mode, all Non-Posted Memory requests are completed with an Unsupported Request status. Posted Write data is discarded. If this bit is not set in Reverse Transparent Bridge mode, all Memory transactions are ignored on the primary (PCI) bus.

Set the *Bus Master Enable* bit to allow Memory transactions to forward upstream. If this bit is not set in Forward Transparent Bridge mode, all Memory Request transactions on the secondary (PCI) bus are ignored. If this bit is not set in Reverse Transparent Bridge mode, all Non-Posted Memory requests on the secondary (PCI Express) bus are completed with an Unsupported Request (UR) status. Posted Write data is discarded.

5.2.2.2 Memory-Mapped I/O Base and Limit Registers

The following Memory Base and Limit Configuration registers are used to determine whether to forward Memory-Mapped I/O transactions across the bridge:

- **Memory Base** (bits [15:4] of the 16-bit register correspond to Address bits [31:20])
- **Memory Limit** (bits [31:20] of the 16-bit register correspond to Address bits [31:20])

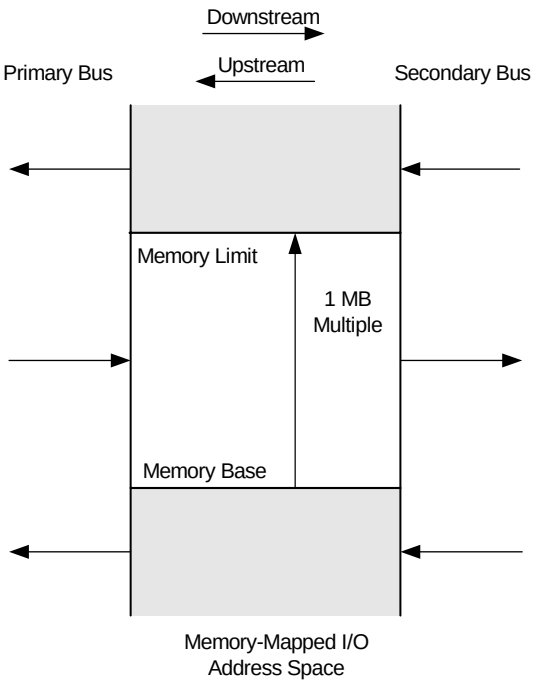
Memory Base register bits [15:4] define Memory-Mapped I/O Base Address bits [31:20]. **Memory Limit** register bits [31:20] define Memory-Mapped I/O Limit bits [31:20]. Bits [3:0] of both registers are hardwired to 0.

Because Address bits [19:0] are not included in the Address Space decoding, the Memory-Mapped I/O Address range has a granularity of 1 MB, and is always aligned to a 1-MB Address Boundary space. The maximum Memory-Mapped I/O range is 4 GB.

Memory transactions that fall within the range defined by the **Memory Base** and **Memory Limit** are forwarded downstream from the primary to secondary bus, and Memory transactions on the secondary bus that are within the range are ignored. Memory transactions that do not fall within the range defined by the **Memory Base** and **Limit** registers are ignored on the primary bus, and forwarded upstream from the secondary bus. Figure 5-3 illustrates Memory-Mapped I/O forwarding.

When the Memory Base is programmed with a value greater than the Memory Limit, the Memory-Mapped I/O range is disabled. In this case, all Memory transaction forwarding is determined by the **Prefetchable Base and Limit** registers, described in the following section.

Figure 5-3. Memory-Mapped I/O Forwarding



5.2.3 Prefetchable Space

The Prefetchable Address space determines whether to forward Prefetchable Memory Write or Read transactions across the bridge. Map devices, without side effects during Reads, into this space. For PCI-to-PCI Express Reads, prefetching occurs in this space for all Memory Read commands issued on the PCI Bus, as defined in Table 5-3. For PCI Express-to-PCI, PCI-X, or PCI-X-to-PCI Express Reads, the number of bytes to read is determined by the Memory Read request. Therefore, prefetching does not occur.

Table 5-3. PCI-to-PCI Express Read Prefetching

Command	Prefetch
Memory Read (MemRd)	The PEX 8114 prefetches the number of bytes indicated in the **Prefetch** register *Prefetch Space Count* field (offset FA4h[13:8]).
Memory Read Line (MemRdLine)	The PEX 8114 prefetches the number of bytes indicated in the Cache Line Size (offset 0Ch[7:0]).
Memory Read Line Multiple (MemRdLineMult)	The PEX 8114 prefetches 1 or 2 Cache Lines, as indicated in the *Cache Line Prefetch Line Count* bit (offset FA0h[4]). Each line contains the number of bytes indicated in the Cache Line Size, up to a maximum of 128 bytes.

5.2.3.1 Enable Bits

The Prefetchable space responds to the Enable bits, as described in Section 5.2.2.1, "Enable Bits."

5.2.3.2 Prefetchable Base and Limit Registers

The following Prefetchable Memory Base and Limit Configuration registers are used to determine whether Prefetchable Memory transactions can be forwarded across the bridge:

- **Prefetchable Memory Base** (bits [15:4] of the 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Base Upper** (32-bit register corresponds to Address bits [63:32])
- **Prefetchable Memory Limit** (bits [31:20] of the 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Limit Upper** (32-bit register corresponds to Address bits [63:32])

Prefetchable Memory Base register bits [15:4] define Prefetchable Memory Base Address bits [31:20]. **Prefetchable Memory Limit** register bits [31:20] define Prefetchable Memory Limit bits [31:20]. Bits [3:0] of both registers are hardwired to 1h, indicating 64-bit addressing. The default 64-bit addressing bit can be cleared to 0h during serial EEPROM load for systems that must run in 32-Bit Addressing mode. For 64-bit addressing, the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are also used to define the space.

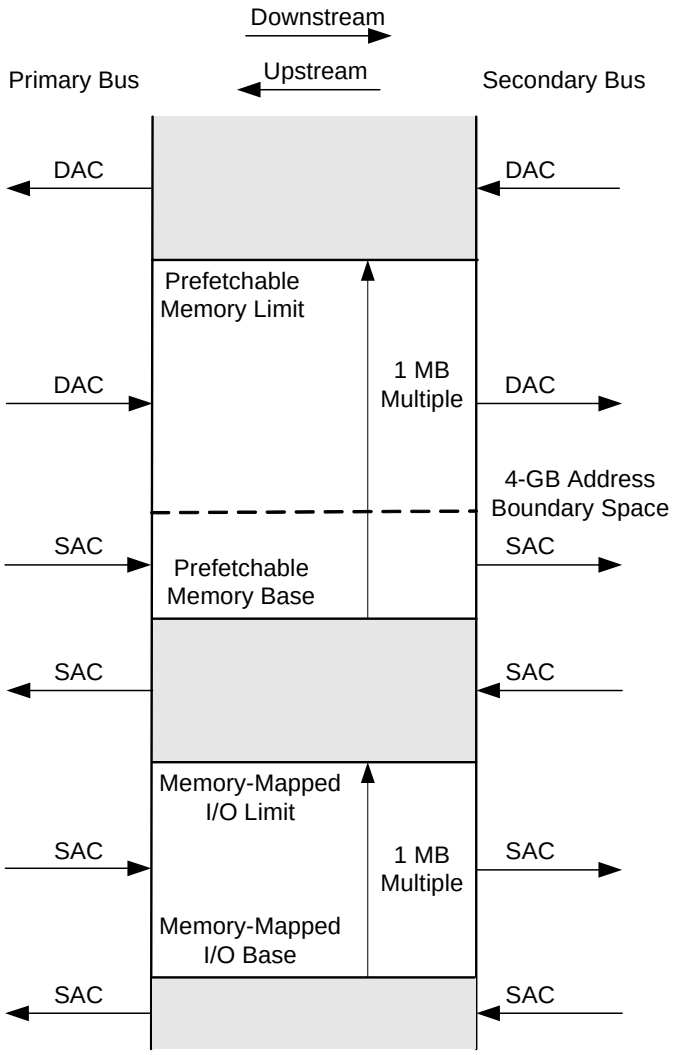
Because Address bits [19:0] are not included in the Address Space decoding, the Prefetchable Memory Address range has a granularity of 1 MB, and is always aligned to a 1-MB Address Boundary space. The maximum Prefetchable Memory range is 4 GB with 32-bit addressing, and 2^{64} with 64-bit addressing.

Memory transactions that fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are forwarded downstream from the primary to secondary bus, and Memory transactions on the secondary bus that are within the range are ignored. Memory transactions that do not fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are ignored on the primary bus and forwarded upstream from the secondary bus (provided they are not in the Address range defined by the Memory-Mapped I/O Address register set). Figure 5-4 illustrates Memory-Mapped I/O and Prefetchable Memory forwarding.

When the **Prefetchable Memory Base** is programmed with a value greater than the **Prefetchable Memory Limit**, the Prefetchable Memory range is disabled. In this case, all Memory transaction forwarding is determined by the **Memory-Mapped I/O Base** and **Limit** registers. All four Prefetchable Base and Limit registers must be considered when disabling the Prefetchable Memory range.

In Figure 5-4, reworded “Prefetchable and Memory-Mapped I/O Memory Space” to “Prefetchable Memory and Memory-Mapped I/O Space.”

Figure 5-4. Memory-Mapped I/O and Prefetchable Memory Forwarding



5.2.3.3 64-Bit Addressing

Unlike Memory-Mapped I/O memory that must reside below the 4-GB Address Boundary space, Prefetchable memory can reside below, above, or span the 4-GB Address Boundary space. Memory locations above the 4-GB Address Boundary space must be accessed using 64-bit addressing. PCI Express Memory transactions that use the Short Address (32-bit) format can target the Non-Prefetchable Memory space, or a Prefetchable Memory window located below the 4-GB Address Boundary space. PCI Express Memory transactions that use the Long Address (64 bit) format can target locations anywhere in 64-bit Memory space.

PCI Memory transactions that use Single Address cycles can only target locations below the 4-GB Address Boundary space. PCI Memory transactions that use Dual Address cycles can target locations anywhere in 64-bit Memory space. The first Address phase of a Dual Address transaction contains the lower 32 bits of the address, and the second Address phase contains the upper 32 bits of the address. If the upper 32 bits of the address are 0, a Single Address transaction is performed.

Forward Transparent Bridge Mode

When the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are both cleared to 0, addresses located above the 4-GB Address Boundary space are ***not supported***. In Forward Transparent Bridge mode, if a PCI Express Memory transaction is detected with an address located above 4 GB, the transaction is completed with Unsupported Request status. All Dual Address transactions on the PCI Bus are forwarded upstream to the PCI Express interface.

When the Prefetchable memory is located entirely above the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are both set to non-zero values. If a PCI Express Memory transaction is detected with an address located below the 4-GB Address Boundary space, the transaction is completed with Unsupported Request status, and all Single Address transactions on the PCI Bus are forwarded upstream to the PCI Express interface (unless they fall within the Memory-Mapped I/O range). A PCI Express Memory transaction located above 4 GB, that falls within the range defined by the **Prefetchable Base**, **Prefetchable Memory Base Upper**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper** registers, is forwarded downstream and becomes a Dual Address cycle on the PCI Bus. If a Dual Address cycle is detected on the PCI Bus located outside the range defined by these registers, it is forwarded upstream to the PCI Express interface. If a PCI Express Memory transaction located above the 4-GB Address Boundary space does not fall within the range defined by these registers, it is completed with Unsupported Request status. If a PCI Dual Address cycle falls within the range determined by these registers, it is ignored.

When the Prefetchable memory spans the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper** register is cleared to 0, and the **Prefetchable Memory Limit Upper** register is set to a non-zero value. If a PCI Express Memory transaction is detected with an address located below 4 GB, and is greater than or equal to the Prefetchable Memory Base Address, the transaction is forwarded downstream. A Single Address transaction on the PCI Bus is forwarded upstream to the PCI Express interface if the address is less than the Prefetchable Memory Base Address. If a PCI Express Memory transaction located above 4 GB is less than or equal to the **Prefetchable Memory Limit** register, it is forwarded downstream to the PCI Bus as a Dual Address cycle. If a Dual Address cycle on the PCI Bus is less than or equal to the **Prefetchable Memory Limit** register, it is ignored. If a PCI Express Memory transaction located above 4 GB is greater than the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status. If a Dual Address cycle on the PCI Bus is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Express interface.

Reverse Transparent Bridge Mode

When the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are both cleared to 0, addresses located above the 4-GB Address Boundary space are ***not supported***. In Reverse Transparent Bridge mode, if a Dual Address transaction on the PCI Bus is detected, the transaction is ignored. If a PCI Express Memory transaction is detected with an address located above the 4-GB Address Boundary space, it is forwarded upstream to the PCI Bus as a Dual Address cycle.

When the Prefetchable memory is located entirely above the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are both set to non-zero values. The PEX 8114 ignores all single address Memory transactions on the PCI Bus, and forwards all PCI Express Memory transactions with addresses located below the 4-GB Address Boundary space upstream to the PCI Bus (unless they fall within the Memory-Mapped I/O range).

A Dual Address transaction on the PCI Bus that falls within the range defined by the **Prefetchable Base**, **Prefetchable Memory Base Upper**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper** registers is forwarded downstream to the PCI Express interface. If a PCI Express Memory transaction is located above the 4-GB Address Boundary space and falls outside the range defined by these registers, it is forwarded upstream to the PCI Bus as a Dual Address cycle. If a Dual Address transaction on the PCI Bus does not fall within the range defined by these registers, it is ignored. If a PCI Express Memory transaction located above 4 GB falls within the range defined by these registers, it is completed with Unsupported Request status.

When the Prefetchable memory spans the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper** register is cleared to 0, and the **Prefetchable Memory Limit Upper** register is set to a non-zero value. If a PCI Single Address cycle is greater than or equal to the Prefetchable Memory Base Address, the transaction is forwarded downstream to the PCI Express interface. If a PCI Express Memory transaction is detected with an address located below the 4-GB Address Boundary space, and is less than the Prefetchable Memory Base Address, the transaction is forwarded upstream to the PCI Bus. If a Dual Address PCI transaction is less than or equal to the **Prefetchable Memory Limit** register, it is forwarded downstream to the PCI Express interface. If a PCI Express Memory transaction located above the 4-GB Address Boundary space is less than or equal to the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status. If a Dual Address PCI transaction is greater than the **Prefetchable Memory Limit** register, it is ignored. If a PCI Express Memory transaction located above the 4-GB Address Boundary space is greater than the **Prefetchable Memory Limit** register, it is forwarded upstream to the PCI Bus as a Dual Address cycle.

5.2.4 Base Address Register Addressing

The Base Address Registers (BARs) provide Memory-Mapped access to internal Configuration registers. This method of accessing internal registers is used exclusively to access the PCI Express Extended register set when operating as a Reverse PCI bridge, which has no other method of accessing without access to the higher Configuration addresses. All accesses using the BARs return 1 DWord of data. The BARs do not affect data forwarding through the bridge that uses Memory I/O, Memory-Mapped, or Prefetchable Memory.

The PEX 8114 defaults to a non-prefetchable 32-bit BAR access, using BAR0 and leaving BAR1 unused. The PEX 8114 can be configured by serial EEPROM to support 64-bit non-prefetchable BAR access, using both BAR0 and BAR1 to create a 64-bit BAR, by setting the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1] to 10b.

Addresses transmitted to the BAR window are linearly translated into register address accesses. The *N*th location of the BAR maps to the *N*th Configuration register. Access to BAR locations that do not contain registers corresponding to that address return UR in Forward Transparent Bridge mode and 0 in Reverse Transparent Bridge mode.

For further details, refer to Chapter 6, "Configuration."

Chapter 6 Configuration

6.1 Introduction

Configuration requests are initiated by the Root Complex in a PCI Express system and by the PCI or PCI-X Host or Central Resource Function in a PCI system. All devices located within a PCI Express or PCI system include a Configuration space accessed using Configuration transactions to configure operational characteristics of the device.

When the PEX 8114 operates as a Forward bridge, all configurations originate at the PCI Express Root Complex. The PEX 8114 is configured by the Root Complex. The PEX 8114 register set appears as a Type 1 PCI Express Bridge register set with a Device ID of 8114h and additional Device-Specific registers. The PCI Express Bridge register set is enumerated and configured by the BIOS according to PCI Express conventions. Configuration or changes to the additional Device-Specific registers is optional, as changes to the Device-Specific registers are not required to allow the PEX 8114 to function. PCI devices located downstream from the PEX 8114 are configured by the Root Complex through the PEX 8114.

When the PEX 8114 operates as a Reverse bridge, all configurations originate at the PCI-X or PCI Host. The PCI-X Host configures the PEX 8114, using PCI transactions. The PCI-X Host also configures PCI Express devices, located downstream from the PEX 8114, by transmitting PCI transactions to the PEX 8114, which the bridge converts into PCI Express Configuration transactions and then forwards to the PCI Express devices downstream.

In Reverse Transparent Bridge mode, the PEX 8114 register set appears as a Type 1 PCI Bridge register set with a Device ID of 8114h and additional Device-Specific registers. The PCI Bridge register set is enumerated and configured by the BIOS according to PCI Bridge conventions. Configuration or changes to the additional Device-Specific registers is optional, as changes to the Device-Specific registers are not required to allow the PEX 8114 to function.

Type 0 Configuration transactions are used to access the internal PEX 8114 Configuration registers. When the PEX 8114 is configured as a Forward or Reverse bridge, Type 1 Configuration transactions are transmitted into the PEX 8114 to access devices downstream from the PEX 8114. These Type 1 configurations are converted to Type 0 transactions, if they are targeted to the device on the bus directly below the PEX 8114. If the transaction is a Target for a bus downstream from the bus located directly below the PEX 8114, the transaction is passed through the PEX 8114 as a Type 1 configuration. If the transaction is not targeted for the PEX 8114, or devices located downstream from the PEX 8114, the transaction is rejected.

The Configuration address is formatted as follows:

PCI Express

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	***Reserved***	Extended Register Address	Register Address	***Reserved***

PCI Type 0 (At Initiator)

31 16	15 11	10 8	7 2	1 0
Single bit decoding of Device Number	***Reserved***	Function Number	Register Number	0 0

PCI Type 0 (At Target)

31 11	10 8	7 2	1 0
Reserved	Function Number	Register Number	0 0

PCI Type 1

31 24	23 16	15 11	10 8	7 2	1 0
Reserved	Bus Number	Device Number	Function Number	Register Number	0 1

6.2 Type 0 Configuration Transactions

The PEX 8114 responds to Type 0 Configuration transactions on its primary bus that address the PEX 8114 Configuration space. A Type 0 Configuration transaction is used to configure the PEX 8114, and is not forwarded downstream to the secondary bus. The PEX 8114 ignores Type 0 Configuration transactions on its secondary bus. Type 0 Configuration transactions result in the transfer of 1 DWord. If Configuration Write data is poisoned, the data is discarded and a Non-Fatal Error message is generated, if enabled.

6.3 Type 1 Configuration Transactions

Type 1 Configuration transactions are used for device configuration in a hierarchical bus system. Transparent bridges and switches are the only devices that respond to Type 1 Configuration transactions.

Type 1 conversion to special cycles are ***not supported***. When the PEX 8114 operates as a Type 1 Transparent bridge, Configuration transactions are used when the transaction is intended for a device residing on a bus other than the one that issued the Type 1 request. The *Bus Number* field in a Configuration transaction request specifies a unique bus in the hierarchy, on which the Transaction Target resides. The bridge compares the specified bus number with two PEX 8114 Configuration registers – **Secondary Bus Number** and **Subordinate Bus Number** – to determine whether to forward a Type 1 Configuration transaction across the bridge.

When the primary interface receives a Type 1 Configuration transaction, the following tests are applied, in sequence, to the *Bus Number* field to determine how to handle the transaction:

1. When the *Bus Number* field is equal to the **Secondary Bus Number** register value, the PEX 8114 forwards the Configuration request to the secondary bus as a Type 0 Configuration transaction.
2. When the *Bus Number* field is not equal to the **Secondary Bus Number** register value, but is within the range of the **Secondary Bus Number** and **Subordinate Bus Number** (inclusive) registers, the Type 1 Configuration request is specifying a bus located behind the bridge. In this case, the PEX 8114 forwards the Configuration request to the secondary bus as a Type 1 Configuration transaction.
3. When the *Bus Number* field does not satisfy the above criteria, the Type 1 Configuration request is specifying a bus that is not located behind the bridge. In this case, the Configuration request is invalid. If the primary interface is PCI Express, a Completion with Unsupported Request (UR) status is returned. If the primary interface is PCI, the Configuration request is ignored, resulting in resulting in delivery of FFFF_FFFFh or a Target Abort. If the **Bridge Control** register *Master Abort Mode* bit (offset 3Ch[21]) is set, the PEX 8114 replies to the PCI requester's follow-on Non-Posted requests with a Target Abort. If the *Master Abort Mode* bit is not set, the PEX 8114 replies to the PCI requester's follow-on Non-Posted requests with FFFF_FFFFh.

6.4 Type 1-to-Type 0 Conversion

The PEX 8114 performs a Type 1-to-Type 0 conversion when the Type 1 transaction is generated on the primary bus and is intended for a device attached directly to the secondary bus. The PEX 8114 must convert the Type 1 Configuration transaction to Type 0, to allow the downstream device to respond to it. Type 1-to-Type 0 conversions are performed only in the downstream direction. The PEX 8114 generates Type 0 Configuration transactions only on the secondary interface.

6.4.1 Forward Transparent Bridge Mode

The PEX 8114 forwards a Type 1 transaction on the PCI Express interface to a Type 0 transaction on the PCI Bus, if the Type 1 Configuration request *Bus Number* field is equal to the **Secondary Bus Number** register value.

The PEX 8114 then performs the following steps on the secondary interface:

1. Clears Address bits AD[1:0] to 00b.
2. Derives Address bits AD[7:2] directly from the Configuration request *Register Address* field.
3. Derives Address bits AD[10:8] directly from the Configuration request *Function Number* field.
4. Clears Address bits AD[15:11] to 00h.
5. Decodes the *Device Number* field and sets a single Address bit within the range AD[31:16] during the Address phase.
6. Verifies that the *Extended Register Address* field in the Configuration request is 0h. If the value is non-zero, the PEX 8114 does not forward the transaction, and treats it as an Unsupported Request on the PCI Express interface, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

6.4.2 Reverse Transparent Bridge Mode

The PEX 8114 forwards a Type 1 transaction on the PCI Bus to a Type 0 transaction on the PCI Express interface, if the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- The Type 1 Configuration request *Bus Number* field (AD[23:16]) is equal to the **Secondary Bus Number** register value.
- The Bus command on PCI_C/BE[3:0]# (32-bit bus) or PCI_C/BE[7:0]# (64-bit bus) is a Configuration Write or Read.
- The Type 1 Configuration request *Device Number* field (AD[15:11]) is 0h. If it is non-zero, the PEX 8114 ignores the transaction, resulting in a Master Abort.

The PEX 8114 then creates a PCI Express Configuration request, according to the following:

1. Sets the request *Type* field to Configuration Type 0.
2. Derives the *Register Address* field [7:2] directly from the Configuration request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derives the *Function Number* field [18:16] directly from the Configuration request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration request *Device Number* field (forced to 0h).
6. Derives the *Bus Number* field [31:24] directly from the Configuration request *Bus Number* field.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

6.5 Type 1-to-Type 1 Forwarding

Type 1-to-Type 1 transaction forwarding provides a hierarchical configuration mechanism when two or more levels of bridges are used. When the PEX 8114 detects a Type 1 Configuration transaction intended for a PCI Bus downstream from the secondary bus, it forwards the transaction, unchanged, to the secondary bus.

In this case, the Transaction Target does not reside on the PEX 8114's secondary interface, but is located on a bus segment farther downstream. Ultimately, this transaction is converted to a Type 0 transaction by a downstream bridge.

6.5.1 Forward Transparent Bridge Mode

The PEX 8114 forwards a Type 1 transaction on the PCI Express interface to a Type 1 transaction on the PCI Bus, if the following are true:

- A Type 1 Configuration transaction is detected on the PCI Express interface
- The value specified by the *Bus Number* field is within the range of Bus Numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive)

The PEX 8114 then performs the following steps on the secondary interface:

1. Generates Address bits AD[1:0] as 01b.
2. Generates PCI Register Number, Function Number, Device Number, and Bus Number directly from the PCI Express Configuration Request register *Address*, *Function Number*, *Device Number*, and *Bus Number* fields, respectively.
3. Generates Address bits AD[31:24] as 00h.
4. Verifies that the *Extended Register Address* field in the Configuration request is 0h. If the value is non-zero, the PEX 8114 does not forward the transaction, and returns a Completion with Unsupported Request status on the PCI Express interface, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 1 forwarding transactions are performed as Non-Posted transactions.

6.5.2 Reverse Transparent Bridge Mode

The PEX 8114 forwards a Type 1 transaction on the PCI Bus to a Type 1 transaction on the PCI Express interface, if the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- The value specified by the *Bus Number* field is within the range of Bus Numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive).
- The Bus command on PCI_C/BE[3:0]# (32-bit bus) or PCI_C/BE[7:0]# (64-bit bus) is a Configuration Write or Read.

The PEX 8114 then creates a PCI Express Configuration request, according to the following:

1. Sets the request *Type* field to Configuration Type 1.
2. Derives the *Register Address* field [7:2] directly from the Configuration request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derives the *Function Number* field [18:16] directly from the Configuration request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration request *Device Number* field.
6. Derives the *Bus Number* field [31:24] directly from the Configuration request *Bus Number* field.

Type 1-to-Type 1 forwarding transactions are performed as Non-Posted transactions.

6.6 PCI Express Enhanced Configuration Mechanism

The PCI Express Enhanced Configuration Mechanism adds four additional bits to the *Register Address* field, thereby expanding the space to 4,096 bytes. The PEX 8114 forwards Configuration transactions only when the *Extended Register Address* bits are all 0. This prevents address aliasing on the PCI Bus that does not support Extended Register Addressing.

When a Configuration transaction targets the PCI Bus and contains a non-zero value in the *Extended Register Address* field, the PEX 8114 treats the transaction as if it received a Master Abort on the PCI Bus. The PEX 8114 then performs the following steps:

1. Sets the appropriate status bits for the destination bus, as if the transaction executed and resulted in a Master Abort.
2. Generates a PCI Express Completion with Unsupported Request status.

6.7 Configuration Retry Mechanism

6.7.1 Forward Transparent Bridge Mode

Bridges must return a Completion for all Configuration requests that traverse the bridge from PCI Express-to-PCI prior to expiration of the Completion Timeout Timer in the Root Complex. This requires that bridges take ownership of all Configuration requests forwarded across the bridge. If the Configuration request to PCI successfully completes prior to the bridge Timer expiration, the bridge returns a Completion with Successful Status to PCI Express. If the Configuration request to PCI encounters an error condition prior to the bridge Timer expiration, the bridge returns an appropriate error Completion to PCI Express. If the Configuration request to PCI does not successfully complete or with an error prior to Timer expiration, the bridge returns a Completion with Configuration Retry Status (CRS) to the PCI Express interface.

After the PEX 8114 returns a Completion with CRS to PCI Express, the PEX 8114 continues to allow the Configuration transaction to remain alive on the PCI Bus. The *PCI r3.0* states that once a PCI Master detects a Target Retry, it must continue to Retry the transaction until at least 1 DWord is transferred. The PEX 8114 Retries the transaction until the transaction completes on the PCI Bus or until the PCI Express to PCI Retry Timer expires.

When the Configuration transaction completes on the PCI Bus after the return of a Completion with CRS on the PCI Express interface, the PEX 8114 discards the Completion information. Bridges that implement this option are also required to implement the **Device Control** register *Bridge Configuration Retry Enable* bit [15]. If this bit is cleared, the bridge does not return a Completion with CRS on behalf of Configuration requests forwarded across the bridge. The lack of a Completion results in eventual Completion Timeout at the Root Complex.

Bridges, by default, do not return CRS for Configuration requests to a PCI device located behind the bridge. This can result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

6.7.2 Reverse Transparent Bridge Mode

In Reverse Transparent Bridge mode, when the PEX 8114 detects a CRS, it resends the Configuration request to the PCI Express device to allow the configuration request to remain alive, and reset its Internal Timer. If the PEX 8114 is in PCI mode and the Internal Timer times out before receiving a CRS or Error message from the PCI Express device, the PEX 8114 replies with FFFF_FFFFh if the **Bridge Control** register *Master Abort Mode* bit (offset 3Ch[21]) is not set. Otherwise, it causes a Target Abort if the *Master Abort Mode* bit is set. If the PEX 8114 is in PCI-X mode, it transmits a Split Completion with a Target Abort Error message.

6.8 Configuration Methods

The PEX 8114 supports the Standard Configuration methods and maintains several Device-Specific Configuration methods. The PEX 8114 supports Forward and Reverse Transparent Bridge modes. Each mode is slightly different from a configuration perspective.

The basic configuration methods include:

- PCI Express Extended Configuration cycles
- PCI Configuration cycles
- BAR0/1 Memory-Mapped configuration of Device-Specific registers
- Address and Data Pointer method for register access

The PCI Express Extended Configuration method provides a *PCI Express r1.0a*-compliant method for configuring PCI Express registers. The PCI Configuration method provides a *PCI r3.0*-compliant method for accessing PCI registers. The BAR0 and BAR1 configuration method provides 32- or 64-bit Memory-Mapped access to registers. This is typically used to access registers that cannot be accessed by PCI Express Extended or Conventional PCI configurations. In general, BAR0 and BAR1 point to 8 KB of Memory Cycle-Accessible Address space. This 8 KB of space is used to Write and Read registers within, or downstream from, the PEX 8114. The 8 KB of Memory-Mapped space accesses registers in a slightly different manner in Forward and Reverse Transparent modes. The differences are explained in the next section. The Address and Data Pointer method provides two registers within the Configuration space for Reverse Transparent mode. One register represents an address in the PCI/PCI Express hierarchy, the other is a data value register. By loading the Address register with a Target address, then writing or reading the Data register, a location in the Address space can be written or read.

6.8.1 Configuration Methods Intent and Variations

Configuration register accesses must be supported in all primary operation modes. These modes include Forward and Reverse Transparent. Each supported Configuration method provides access to at least some of the Configuration registers. Certain Configuration methods provide access to Conventional PCI registers, while others provide easy access to Device-Specific registers. By providing a combination of configuration methods, the PEX 8114 allows Conventional PCI access to many registers and logical simple access to Device-Specific registers, as well as downstream device registers. Operation modes slightly vary; therefore, certain Configuration methods also vary. The following sections explain the basic capability differences.

6.8.2 PCI Express Extended Configuration Method

The PCI Express Extended Configuration method provides Forward Transparent bridges with access to the standard set of PCI Express registers. This configuration method provides PCI-SIG-compliant access to the PEX 8114 PCI-SIG-defined registers. It also provides access to PCI-SIG-compliant access to registers in downstream devices when the PEX 8114 is used in Forward Transparent Bridge mode. This method is, however, confined to accessing the PCI Express-defined registers and is not used to access the PEX 8114 Device-Specific registers.

In Forward Transparent Bridge mode, Memory-Mapped access is supported to access Device-Specific PEX 8114 registers. Address and Data Pointer register access is ***not supported*** in Forward Transparent Bridge mode. Therefore, the PEX 8114 Device-Specific registers can only be accessed by Memory-Mapped access.

6.8.3 PCI Configuration Cycles

PCI Configuration cycles are used in Reverse Transparent Bridge mode to access the standard 256-byte PCI-defined register space. This method provides Conventional PCI register access that functions with Conventional PCI BIOS; however, it does not provide access in the following:

- Reverse Transparent Bridge mode to downstream devices' PCI Express Extended registers
- Reverse Transparent Bridge mode to downstream devices' Device-Specific registers

In Reverse Transparent Bridge mode, use the Memory-Mapped or Address and Data Pointer method to access the downstream devices' PCI Express Extended registers or the Device-Specific registers.

6.8.4 BAR0/1 Device-Specific Register Memory-Mapped Configuration

BAR0 and **BAR1** are used to provide 32- or 64-bit Memory-Mapped access to the Device-Specific registers. The use of Memory-Mapped access is slightly different in Forward Transparent Bridge mode than it is in Reverse Transparent Bridge mode.

- **Forward Transparent Bridge mode** – Memory-Mapped access provides access to PEX 8114 internal Device-Specific registers.
- **Reverse Transparent Bridge mode** – Memory-Mapped access provides access to all PEX 8114 internal registers, as well as to downstream PCI Express device registers. This Memory-Mapped method allows PCI Hosts (which support only Conventional PCI Configuration registers) to access devices on the downstream PCI Express side of the bridge, using PCI Express Extended Configuration space.

BAR0 and **BAR1** Device-Specific Register Memory-Mapped configuration can be disabled by setting the Disable BAR0 bit (offset FA0h[7]). By default, this bit is cleared; however, it can be set by way of serial EEPROM load. When this bit is set, BAR0 is loaded with all zeros (0) at reset, and appears to the operating system as disabled.

6.8.5 Address and Data Pointer Configuration Method

In Reverse Transparent Bridge mode, the Address and Data Pointer Configuration method provides the PCI Host with access to all PEX 8114 extended registers, as well as all registers of PCI Express devices on links located downstream from the PEX 8114.

Access to the Configuration registers through the Memory-Mapped or Address and Data Pointer Configuration method is intended; however, both methods cannot be used concurrently. Access to the Configuration registers by way of the Address and Data pointers, which were accessed by the BAR0/1 Memory-Map access (Double-Indirect access) results in undefined data.

6.8.6 Configuration Specifics

This section details how Configuration cycles function in Forward and Reverse Transparent Bridge modes and defines the register Address ranges accessed by each cycle type. The three operational modes are described separately, and in each description a table is provided that defines the recommended method for accessing the register ranges, located within and downstream from the PEX 8114. Following the table of recommended access methods, the methods are described as they function in that mode.

6.8.6.1 Forward Transparent Bridge Mode

In Forward Transparent Bridge mode, access to all registers located within and downstream from the PEX 8114 is provided according to Table 6-1.

Table 6-1. Access to Registers during Forward Transparent Bridge Mode

Target Register Type	Register Location	Intended Configuration Method
PEX 8114 PCI Express-defined registers	PEX 8114 registers 00h through 1C7h, FB4h through FFFh	PCI Express Extended configuration
PEX 8114 Device-Specific registers	PEX 8114 registers FFFh to FB3h	BAR0/1 Memory-Mapped configuration
Downstream device PCI registers	Downstream bus with register addresses 00h through FFh	PCI Express Extended Configuration Accessing of PCI-defined registers – first 256 bytes
Downstream device Device-Specific registers	Downstream Device-Specific	***Not supported***

PCI Express Extended Configuration Access in Forward Transparent Bridge Mode

In Forward Transparent Bridge mode (as in all other modes), the PCI Express Extended Configuration method functions, as described in the *PCI Express r1.0a*, and as previously described. The PEX 8114 makes no non-standard modifications to the standard PCI Express Extended Configuration method.

Forward Transparent Memory-Mapped BAR0/1 Access to Internal Registers

In Forward Transparent Bridge mode, BAR0 and BAR1 are used to provide 32- or 64-bit Memory-Mapped access to internal Configuration registers. When BAR0 and BAR1 are enumerated according to PCI convention and the bridge operation description herein, access to a 4-KB Memory-Mapped window into the Configuration registers is provided. The 4-KB window provides access to all PCI Express Extended register addresses. The Memory-Mapped window locations are linearly mapped to Configuration register space, according to the following equation:

for $N = 0$ through 4 KB-1; Memory-Mapped address BASE+N access register N

All internal registers can be accessed through Memory-Mapped access in Forward Transparent Bridge mode.

6.8.6.2 Reverse Transparent Bridge Mode

In Reverse Transparent Bridge mode, access to all registers located within and downstream from the PEX 8114 is provided according to Table 6-2.

Table 6-2. Access to Registers during Reverse Transparent Bridge Mode

Target Register Type	Register Location	Intended Configuration Method
PEX 8114 PCI-defined registers	PEX 8114 registers 00h through FFh	Conventional PCI configuration
PEX 8114 PCI and Device-Specific registers	PEX 8114 registers 100h through FFFh	BAR0/1 Memory-Mapped configuration Address and Data Pointer configuration
Downstream device PCI Type 0 Bridge register set from register 00h through FFh for enumeration	Downstream bus with register addresses 00h through FFh	Conventional PCI configuration
Downstream device PCI Express Extended registers	PCI Express Extended registers (includes registers 100h through FFFh)	BAR0/1 Memory-Mapped configuration Address and Data Pointer configuration
Downstream device Device-Specific registers	Downstream Device-Specific	BAR0/1 Memory-Mapped configuration Address and Data Pointer configuration

Conventional PCI Configuration Access

In Reverse Transparent Bridge mode, the Conventional PCI configuration method functions, as described in the *PCI r3.0*, and as previously described. The PEX 8114 makes no non-standard modifications to the PCI Configuration method. Using the PCI Configuration method, accesses can be made to the PEX 8114 standard 256 bytes of PCI register space and the first 256 bytes of any downstream PCI Express device located on links downstream from the PEX 8114. Because of the limitation of having access to only the first 256-byte offsets of the 4-KB Extended Register space of the downstream PCI Express device, an extended Memory-Mapped method is used to access the additional PCI Express registers of the downstream devices. The extended Memory-Mapped access method is described in the next section.

Reverse Transparent Memory-Mapped BAR0/1 Access to Internal Extended Registers and Downstream Device Registers

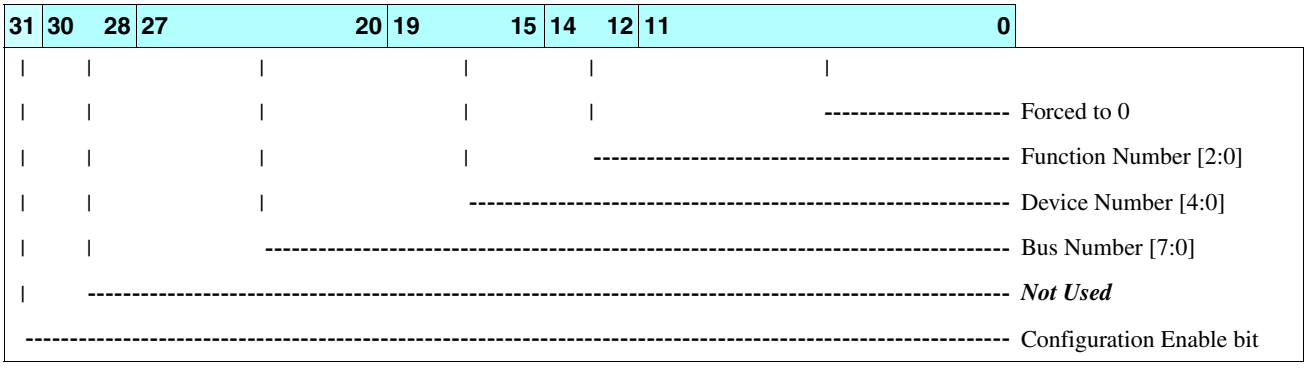
In Reverse Transparent Bridge mode, **BAR0** and **BAR1** are used to provide 32- or 64-bit Memory-Mapped access to the PEX 8114 internal Configuration registers and 4-KB PCI Express Extended Configuration register space of PCI Express devices on link(s) located downstream from the PEX 8114. When **BAR0** and **BAR1** are enumerated, according to PCI convention and according to the bridge operation description herein, access is allowed to an 8-KB Memory-Mapped window into the Configuration registers of a device in the hierarchy that originates at the PEX 8114. The 8-KB window provides access to all PEX 8114 PCI Express Extended register addresses and the PCI Express Extended Address space of all downstream PCI Express devices. The lower 4 KB of Memory-Mapped space, locations 0 through 4 KB-1 (FFFh), is a 4-KB access window into Configuration space that allows writing and reading of registers. The Memory-Mapped location at 4 KB (1000h) is a pointer to a register set on the bus hierarchy, which indicates the start location in the access window. The pointer's contents create an address, defined in Table 6-3.

When a PEX 8114 internal register is accessed, the Memory-Mapped Access cycle causes an internal register Read. When the register accessed is in a device located downstream from the PEX 8114, the Memory-Mapped Access cycle is converted to a Configuration access, which is transmitted down the link. The Memory-Mapped window is linearly mapped to the Configuration Register space of the register set pointed to by the pointer, according to the following equation:

for N = 0: 4 KB-1; Memory-Mapped address BASE+N access register N

Set the *Configuration Enable* bit to 1, to enable downstream Memory-Mapped accesses. All PEX 8114 internal registers and downstream PCI Express devices can be accessed through the Memory-Mapped method.

Table 6-3. Reverse Transparent Configuration Address Pointer at Memory-Mapped Location 1000h



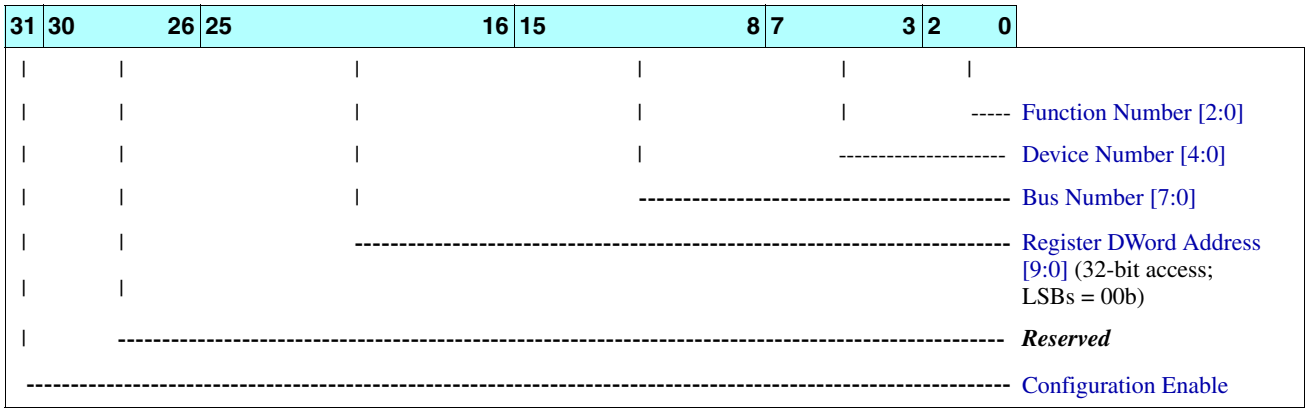
Reverse Transparent Address and Data Pointer Register Access to Internal and Extended Registers and Downstream Device Registers

In Reverse Transparent Bridge mode, two registers in PEX 8114 Configuration space provide indirect access into any Configuration register in the PEX 8114 or any PCI Express device located downstream from the PEX 8114. The Address pointer register is a 32-bit register, located at offset F8h. This register points to the address of a unique register located within or downstream from the PEX 8114. The Address pointer bits are defined in Table 6-4.

The **Data** register is a 32-bit register located at offset FCh. When this register is written or read, the 32-bit register value pointed to by the address pointer is written or read.

Set the *Configuration Enable* bit to 1 to enable Address and Data Pointer accesses. When a PEX 8114 internal register is accessed using the Address and Data Pointer Access cycle, the PEX 8114 executes an internal register access. When the register accessed is in a device located downstream from the PEX 8114, the Address and Data Pointer Access cycle is converted to a Configuration access, which is transmitted down the link. All internal PEX 8114 registers and downstream PCI Express devices can be accessed through the Address and Data Pointer method in Reverse Transparent Bridge mode.

Table 6-4. Reverse Transparent Configuration Address Pointer at Offset F8h



Chapter 7 Bridge Operations

7.1 Introduction

The PEX 8114 supports PCI Express transaction bridging to a PCI Bus operating in PCI or PCI-X mode. To simplify the descriptions, the PEX 8114 operational description is divided into the following types:

- PCI-to-PCI Express Transactions
- PCI-X-to-PCI Express Transactions
- PCI Express-to-PCI Transactions
- PCI Express-to-PCI-X Transactions

The following sections discuss these transactions. Transaction transfer failures and general compliance are also discussed.

7.2 General Compliance

The PEX 8114 complies with the following specifications for the listed processes and modes:

- *PCI r3.0* – PCI mode
- *PCI-X r1.0b* or *PCI-X r2.0a* – PCI-X mode
- *PCI Express r1.0a* – PCI Express port
- *PCI Express-to-PCI/PCI-X Bridge r1.0* – PCI and PCI Express Transaction Ordering rules

7.3 PCI-to-PCI Express Transactions

When a PCI device attempts a Write from the PCI Bus to the PCI Express interface, the PEX 8114 translates PCI Burst Write transactions into PCI Express data TLPs. In the most basic transaction, the PEX 8114 receives a Data burst on the PCI Bus and transfers the data into a PCI Express TLP.

7.3.1 PCI-to-PCI Express Flow Control

The PEX 8114 ensures that the internal resources for storing data are not overrun. If an internal data storage resource is full, or approaching full in certain cases, the PEX 8114 issues Retries to all new Request transactions and only accepts Completions or requests of types without depleted resources.

7.3.2 PCI-to-PCI Express – PCI Posted Write Requests

When servicing Posted Writes, no Completion information is returned to the PCI device that originated the transaction, and when the TLP is transmitted to the PCI Express link, the transaction is considered complete. Table 7-1 defines PCI Posted Write requests and the resultant PCI Express transactions created in response to the Posted Write.

Table 7-1. PCI Posted Write Requests

Initial Posted PCI Transactions	Resultant PCI Express Transaction
Interrupt ACK	***Not supported***
Special Cycle	***Not supported***
Dual Address Cycle	MWr TLP, up to Maximum Packet Size; type=00000b, fmt=11b
Memory Write	MWr TLP, up to Maximum Packet Size; type=00000b, fmt=1Xb
Memory Write and Invalidate	MWr TLP, up to Maximum Packet Size; type=00000b, fmt=1Xb

7.3.3 PCI-to-PCI Express – PCI Non-Posted Requests

On Non-Posted PCI transactions, the PEX 8114 issues a Retry to the PCI originator when it receives the first request. The Retry indicates that the Non-Posted transaction was not completed on the PCI Express port. In addition to transmitting the Retry in response to the first Non-Posted PCI request, the PEX 8114 also creates and issues a Non-Posted TLP on the PCI Express link. Table 7-2 defines all Non-Posted requests and their resultant PCI Express requests. Direct Non-Posted transactions to Prefetchable or Non-Prefetchable Memory space.

Table 7-2. PCI Non-Posted Requests

Initial Non-Posted PCI Transactions	Resultant PCI Express Transaction
I/O Write	IOwr TLP; length=1; type=0010b, fmt=10b
I/O Read	IOrd TLP; length=1; type=0010b, fmt=00b
Memory Read	MemRd TLP, up to Prefetch Size; type=0000b, fmt=0Xb
Configuration Write	CfgWr0/1 TLP; length=1; type=00100b, fmt=10b
Configuration Read	CfgRd0/1 TLP; length=1; type=00100b, fmt=00b
Configuration Type 1 Write	CfgWr1 TLP; length=1; type=00100b, fmt=10b
Configuration Type 1 Read	CfgRd1 TLP; length=1; type=00100b, fmt=00b
Dual Address Cycle	fmt=01b for Memory Reads and Memory Writes
Memory Read Line	MemRd TLP, up to Cache Line Size; type=00000b, fmt=1Xb
Memory Read Line Multiple	One or more MemRd TLP, up to Cache Line Size; type=0000b, fmt=1Xb

Note: *"X" indicates "Don't Care."*

7.3.4 PCI-to-PCI Express – PCI Non-Posted Transactions until PCI Express Completion Returns

After the initial Non-Posted request that caused the resultant transaction is issued on the PCI Express interface, subsequent requests from the PCI device are Retried until the PEX 8114 detects that the PCI Express link transmitted a Completion TLP matching the request. The PEX 8114 supports up to eight parallel Non-Posted requests. If the internal state machines indicate that the link is down, and the **Bridge Control** register *Master Abort Mode* bit (offset 3Ch[21]) is set, the PEX 8114 replies to the PCI requester's follow-on Non-Posted requests with a Target Abort. If the *Master Abort Mode* bit is not set, the PEX 8114 replies to the PCI requester's follow-on Non-Posted requests with FFFF_FFFFh.

7.3.5 PCI-to-PCI Express – PCI Requests Do Not Contain Predetermined Lengths

PCI Read requests do not contain an indication of the quantity of data they require; however, the TLPs that the PEX 8114 issues to the PCI Express device must indicate Data request quantities. The PEX 8114 treats Memory Reads to Prefetchable space differently than it treats Memory Reads to Non-Prefetchable space, and differently than it treats Memory Read Lines and Memory Read Line Multiples. The PEX 8114 resolves the Data request quantity ambiguity, as discussed in the following sections.

7.3.5.1 Memory Read Requests to Non-Prefetchable Space

When the PEX 8114 receives a Memory Read request to Non-Prefetchable Memory space, it generates a PCI Express Read request for 1 DWord, if the system is running a 32-bit bus, and 2 DWords, if the system is running a 64-bit bus.

7.3.5.2 Memory Read Requests to Prefetchable Space

When the PEX 8114 receives a Memory Read Request to Prefetchable Memory space in PCI mode, it issues a Read request on the PCI Express interface for an amount of data that is determined by the **Prefetch** register *Prefetch Space Count* field (offset FA4h[13:8]) and the starting address of the request. The *Prefetch Space Count* field is not used in PCI-X mode because the Request size is provided in the PCI-X Read request. Use of the *Prefetch Space Count* field to determine Prefetch Size pertains only to PCI mode.

The *Prefetch Space Count* field specifies the number of DWords to prefetch for Memory Reads originating on the PCI Bus that are forwarded to the PCI Express interface. Only Even values between 0 and 32 are allowed.

When the PEX 8114 is configured as a Forward bridge, prefetching occurs for all Memory Reads of Prefetchable and Non-Prefetchable Memory space. This occurs because the BARs are not used for Memory Reads, making it impossible to determine whether the space is prefetchable. In Reverse Transparent Bridge mode, prefetching occurs only for Memory Reads that address Prefetchable Memory space. Prefetching is Quad-word aligned, in that data is prefetched to the end of a Quad-word boundary. The number of DWords prefetched is as follows:

- PEX 8114 prefetches 2 DWords when the following conditions are met:
  - *Prefetch Space Count* field is cleared to 00h, and
  - PCI_AD0 or PCI_AD1 is High
  - PCI_REQ64# is asserted (Low)
- PEX 8114 prefetches 1 DWord when the following conditions are met:
  - *Prefetch Space Count* field is cleared to 00h, and
  - PCI_AD0 or PCI_AD1 is High
  - PCI_REQ64# is de-asserted (High)
- When the *Prefetch Space Count* field contains an Even value greater than 0 and PCI_AD2 is High, the number of Prefetched DWords is 1 DWord less than the value in the *Prefetch Space Count* field; otherwise, the number of DWords prefetched is equal to the value in the *Prefetch Space Count* field.

  Only Even values between 0 and 32 are allowed. Odd values provide unexpected results.

7.3.5.3 Memory Read Line or Memory Read Line Multiple

When the Read request is a Memory Read Line or Memory Read Line Multiple, the TLP Read Request Size is determined by the Cache Line Prefetch Line Count and Cache Line Size. When a Memory Read Line command is issued, a single Cache Line of data is prefetched. The number of lines prefetched for a Memory Read Line Multiple command is one or two Cache Lines, and is controlled by the *Cache Line Prefetch Line Count* bit (offset FA0h[4]). The Cache Line Size is determined by the **Miscellaneous Control** register *Cache Line Size* field (offset 0Ch[7:0]), and can be 1, 2, 4, 8, 16, or 32 DWords. Regardless of the Cache Line Prefetch Line Count and Cache Line Size, the prefetched TLP can never be larger than 128 bytes. The PEX 8114 allows the *Cache Line Size* field to be written with any value; however, if they are written to with a value other than 1, 2, 4, 8, 16, or 32 DWords, they are treated as if the value was cleared to 0 during the calculation. When the *Cache Line Size* field is cleared to 0, 1 DWord (if the system is running a 32-bit bus) or 2 DWords (if the system is running a 64-bit bus) are prefetched.

When prefetching for a given Cache Line Size, the prefetching is done to the end of the Cache Line. This means that if the starting address of the Memory Read Line or Memory Read Line Multiple request is at the beginning of the Cache Line, then a full Cache Line of data is prefetched. If the starting address of the Memory Read Line or Memory Read Line Multiple request is not at the beginning of the Cache Line, some amount of data less than a full Cache Line is prefetched, such that data is prefetched up to the end of a Cache Line.

When the Read request is a Memory Read Line Multiple and the *Cache Line Prefetch Line Count* bit is set, the bridge issues a PCI Express Memory Read TLP with a size such that data is prefetched up to the end of the next Cache Line, if the Cache Line Size is less than or equal to 16 DWords (64 bytes). This operation is executed in an attempt to prefetch data from the PCI Express endpoint. If the additional data (the data requested in an attempt to prefetch) remains unused, the bridge drops the data.

7.3.5.4 Credits

The PEX 8114 power-on default settings in register offsets A00h, A04h, and A08h are values that advertise finite credits.

7.3.6 PCI-to-PCI Express Disposition of Unused Prefetched Data

After the PCI Express device completes the request to the PEX 8114, the PEX 8114 completes one of the PCI device's subsequent attempts to Read by supplying data until the PCI device:

- Terminates the transaction normally, satisfying its need for data, –OR–
- Depletes the data that it transmitted from the PCI Express device

If the PCI device terminates the Read, the PEX 8114 flushes the remaining data it prefetched from the PCI Express device. If the data is depleted by the PCI device's Read, the PEX 8114 terminates the PCI transaction with a Disconnect-with-Data on the Data phase in which the last available data is read. The PEX 8114 does not store and combine data from TLPs in an attempt to support lengthening the PCI burst.

7.3.7 PCI-to-PCI Express Pending Transaction Count Limits

The PEX 8114 is capable of accepting multiple Posted PCI Writes. Each Write is stored in the central RAM until it can be transmitted on the PCI Express link. Non-Posted transactions require Completion on the PCI Express side of the bridge, prior to completing the transaction on the PCI side of the bridge. When a Non-Posted transaction enters the PEX 8114, its context is saved until a PCI Express Completion with a matching Requester ID is received. Upon receipt of the Completion from the PCI Express interface, the Completion is relayed to the PCI Initiator, which completes the transaction. The transaction is defined as outstanding from the time that the bridge receives the initial PCI request until the bridge completes the transaction and returns it to the PCI requester. Up to eight Non-Posted transactions can be outstanding at any given time.

7.3.8 PCI-to-PCI Express – PCI Write Transaction with Discontiguous Byte Enables

PCI Express requires that all packet data beats, except the first and last, have all Byte Enables enabled. PCI has no such requirement. If the PCI data written to the PCI Express port disabled Byte Enables in the middle of a burst, the PEX 8114 continues to accept the PCI data and creates two or more TLPs, as necessary, to support long PCI bursts, while also honoring the PCI Express requirement for contiguously asserted bytes.

7.3.9 PCI-to-PCI Express – PCI Write Transactions Larger than Maximum Packet Size

When a PCI Burst Write transaction is longer than the PCI Express Maximum Packet Size, the PEX 8114 creates two or more PCI Express TLPs, as necessary, to support long bursts, while also honoring the PCI Express Maximum Packet Size requirements. When a PCI Data burst is completed, the TLP is transmitted and no attempt is made to combine multiple PCI Burst Writes into a single TLP transaction. When the PEX 8114 PCI Express lanes cannot transmit PCI Express TLPs across the PCI Express interface because of posted credit depletion, which would result in the filling of 6-KB central memory within the PEX 8114, the PEX 8114 starts issuing Retries on the PCI Bus to hold-off the PCI Bus initiator from sending additional data to the PEX 8114.

7.4 PCI-X-to-PCI Express Transactions

When a PCI-X device attempts a Write from the PCI-X Bus to the PCI Express lanes, the PEX 8114 translates PCI-X Burst transactions into PCI Express TLPs. In the most basic transaction, the PEX 8114 receives a Data burst on the PCI-X Bus and translates the data into a PCI Express TLP. The PCI-X protocol is more similar to PCI Express protocol than to PCI protocol. (*That is*, the PCI-X transaction size is included in the request and the PCI-X Bus supports Split Responses.) These two factors allow transactions from PCI-X-to-PCI Express to flow more efficiently than transactions from PCI-to-PCI Express. The following description of PCI-X transactions is similar to PCI transactions; however, it contains a few significant differences, as described in the following sections.

7.4.1 PCI-X-to-PCI Express Flow Control

The PEX 8114 ensures that the internal resources for storing data are not overrun. If an internal data storage resource is full or approaching full in certain cases, the PEX 8114 issues Retries to all new request transactions and only accepts Completions or requests to types without depleted resources. There are several data buffers that must be managed and not allowed to overflow, including the eight PCI Completion buffers and internal 8-KB RAM.

In general, the bridge tracks the outstanding data it requested and does not transmit more requests than it has space to receive Completions. There are two exceptions – Oversubscribe and Flood modes. In Oversubscribe mode, the PEX 8114 tracks the number of outstanding bytes requested and ensures that it limits the number to that allowed in the **Upstream** and **Downstream Split Transaction Control** register *Split Transaction Commitment Limit* fields (offsets 60h[31;16] and 64h[31;16], respectively). In Flood mode, the PEX 8114 accepts and forwards all Read requests.

7.4.2 PCI-X-to-PCI Express – PCI-X Posted Requests

For Posted PCI-X Writes, no Completion information is returned to the PCI-X device that originated the transaction, and when the TLP is transmitted on the PCI Express link, the transaction is considered complete. Table 7-3 defines PCI-X Posted transactions and the resultant PCI Express transactions created in response to the Posted Write.

Table 7-3. PCI-X Posted Requests

Initial Posted PCI Transactions	Resultant PCI Express Transaction
Interrupt ACK	***Not supported***
Special Cycle	***Not supported***
Dual Address Cycle	fmt=01b for Reads and 10b for Writes
Memory Write	MWr TLP, up to Maximum Packet Size; type=00000b, fmt=1Xb
Memory Write Block	MWr TLP, up to Maximum Packet Size; type=00000b, fmt=1Xb

7.4.3 PCI-X-to-PCI Express – PCI-X Non-Posted Requests

When the initial PCI-X request is a Non-Posted Write, the PEX 8114 completes the PCI-X transaction with a Completion message, indicating a successful or unsuccessful Completion following the Completion from PCI Express. If the Non-Posted request is a Read and the transaction data is successfully gathered, the Split Completion is accompanied by data.

When servicing Non-Posted PCI-X transactions, the PEX 8114 issues a Split Response to the PCI-X originator when it receives the first request and creates and issues a Non-Posted TLP on the PCI Express link. When the PCI Express endpoint responds to the Non-Posted request with a Completion, a Split Completion is returned to the PCI-X Initiator. Non-Posted Reads return data along with the Completion status. Non-Posted Writes return a Completion with status only. There are no Retries and no subsequent attempts. Table 7-4 defines possible PCI-X Non-Posted transactions and the resultant PCI Express transaction.

Table 7-4. PCI-X Non-Posted Requests

Initial Non-Posted PCI-X Transactions	Resultant PCI Express Transaction
I/O Write	IOwr TLP length=1; type=00000b fmt=10b
I/O Read	IOrd TLP length=1; type=00000b fmt=00b
Memory Read DWord	MemRd TLP length=1; type=00000b fmt=0Xb
Configuration Write	CfgWr0/1 TLP length=1; type=0010b fmt=10b
Configuration Read	CfgRd0/1 TLP length=1; type=0010b fmt=00b
Configuration Type 1 Write	CfgWr1 TLP; length=1; type=00100b, fmt=10b
Configuration Type 1 Read	CfgRd1 TLP; length=1; type=00100b, fmt=00b
Dual Address Cycle	fmt=01b
Memory Read Block	MemRd TLP length=up to maximum Read request; type=00000b fmt=0Xb

Note: *"X" indicates "Don't Care."*

7.4.4 PCI-X-to-PCI Express – PCI-X Read Requests Larger than Maximum Read Request Size

During a PCI-X-to-PCI Express Read request, the PCI-X Read request Byte Count is loaded into the PCI Express TLP Read request quantity, if the PCI-X Read request is less than the Maximum Read Request Size. If the Read request is larger than the PCI Express Maximum Read Request Size, the PEX 8114 issues multiple Read requests of Maximum Read Request Size or smaller, in the case of the last TLP to complete the total Request Size. Generation of multiple Read request TLPs is performed to honor the PCI Express Maximum Read Request Size and contiguous Byte Enable requirements, while supplying the entire data quantity requested by the PCI-X requester. When the data is returned from the PCI Express device, it is returned in TLPs that are no larger than the Maximum Packet Size, nor larger than the maximum Read Completion Size. As TLPs arrive, they are aligned to the PCI-X Allowable Disconnect Boundary (ADB), and Writes with discontiguous Byte Enables are transmitted as Completions on the PCI-X Bus, followed by disconnects on the ADB until the original PCI-X requester's data request quantity is supplied.

During long Data bursts, if the PCI Express Read Completion Boundary (RCB) is set to 64 bytes, the bridge must combine two 64-byte PCI Express packets into a single 128-byte PCI-X burst, to ensure that the PCI-X transfer ends on the PCI-X ADB boundary. The combining of the two 64-byte TLPs into a single 128-byte ADB is performed in parallel with transmission of the previous 128-byte burst, and is transmitted as a single 128-byte PCI-X burst, thereby maximizing the PCI-X Bus bandwidth. The PEX 8114 does not store and combine data from TLPs in an attempt to support lengthening the PCI burst length.

7.4.5 PCI-X-to-PCI Express – PCI-X Transfer Special Case

This section documents the PCI-X transfer special case that exists when PCI-X Write requests are larger than the Maximum Packet Size, cross 4-KB Address Boundary spaces, or have discontiguous Byte Enables. When a PCI-X device issues Write requests that are larger than the Maximum Packet Size, if the Write Request burst crosses a 4-KB Address Boundary space or the data has internal discontiguous Byte Enables, the PEX 8114 must break up the transaction into two or more transactions, assign unique Transaction IDs, and store details about each transaction generated, to facilitate accounting for the transaction Completion.

7.4.6 PCI-X-to-PCI Express – PCI-X Transactions that Require Bridge to Take Ownership

When the PCI-X transaction is broken into multiple PCI Express transactions, the PEX 8114 must ensure that all requested data is read. To track data from large requests that require multiple TLPs to generate, the PEX 8114 must track all transactions to completion. The PEX 8114 allows eight PCI-X Read Request transactions to be outstanding at any time. PCI-X Non-Posted Read transactions that are smaller than the Maximum Read Request Size, as well as PCI-X Read requests that do not cross a 4-KB Address Boundary space, without discontiguous Byte Enables, are not limited to eight outstanding transactions. Limiting the Read Request Size, as less than or equal to the Maximum Read Request Size, allows for higher performance.

7.4.7 PCI-X-to-PCI Express – PCI-X Writes with Discontiguous Byte Enables

The PEX 8114 is capable of accepting multiple Posted PCI-X Writes. Each Write is stored in the central RAM until it can be transmitted on the PCI Express link. PCI Express requires that all packet data beats, except the first and last, have all Byte Enables enabled. PCI-X has no such requirement. If the PCI-X data has disabled Byte Enables in the middle of a burst, the PEX 8114 continues to accept the PCI-X data and creates two or more TLPs, as necessary, to support long PCI bursts, while also honoring the PCI Express requirement for contiguously asserted bytes.

7.4.8 PCI-X-to-PCI Express – PCI-X Writes Longer than Maximum Packet Size

When a PCI-X Burst transaction is longer than the PCI Express Maximum Packet Size, the PEX 8114 creates two or more PCI Express TLPs, as necessary, to support long bursts, while also honoring the PCI Express Maximum Packet Size requirements. When a PCI-X Data burst is completed, the TLP is transmitted and no attempt is made to combine multiple small PCI-X Burst Writes into a single TLP transaction. When the PEX 8114 PCI Express lanes cannot transmit PCI Express TLPs across the PCI Express interface because of posted credit depletion, which would result in the filling of 6-KB central memory within the PEX 8114, the PEX 8114 starts issuing Retries on the PCI Bus to hold-off the PCI Bus initiator from sending additional data to the PEX 8114.

7.5 PCI Express-to-PCI Transactions

In PCI mode, when a PCI Express device transmits a transaction from the PCI Express interface to the PEX 8114 PCI-X bus, the transaction is translated from a PCI Express TLP into a PCI Burst transaction. In the most basic transaction, the PEX 8114 receives a TLP on the PCI Express lanes and translates the data into one or more PCI bursts.

7.5.1 PCI Express-to-PCI Flow Control

Credits for up to 6 KB of PCI Express Posted and Non-Posted transactions are issued. These transactions are queued, according to PCI Ordering Transaction rules in central memory, and are transmitted to the PCI-X modules as bandwidth allows, limited by the eight outstanding PCI transactions. Transmitting packets into the PCI Express side of the bridge is throttled by space remaining in the central RAM. The process of transmitting transactions onto the PCI Bus is throttled by the number of outstanding transactions transmitted to the PCI endpoints that did not complete. The PEX 8114 supports up to eight outstanding transactions on the PCI Bus. All transactions are driven through the bridge as quickly as possible, limited only by the PCI Express and PCI Bus bandwidths.

7.5.2 PCI Express-to-PCI – PCI Express Posted Transactions

When servicing Posted transactions, no Completion information is returned to the PCI Express device that originated the transaction, and when the transaction is transmitted on the PCI Bus, the transaction is considered complete. Table 7-5 defines which PCI Express Posted transactions are supported and to which PCI transaction they are translated.

Table 7-5. PCI Express Posted Transactions

Initial PCI Express Posted Transaction Type	Resultant PCI Transaction
Memory Write	PCI Memory Write.
Message Request	Messages that cause changes on the PCI side of the bridge are Interrupt messages, which are translated to INTA#. Internally, Power Management and error conditions can cause Error messages to generate to the PCI Express side of the bridge.
Message Request with Payload	***Not supported.***

7.5.3 PCI Express-to-PCI – PCI Express Non-Posted Transactions

When servicing Non-Posted PCI Express transactions, the PEX 8114 accepts the PCI Express TLP and creates and issues a PCI request on the PCI Bus. The necessary data quantity is indicated in the TLP and the PEX 8114 executes as many transactions as required on the PCI Bus to Write or Read the requested data. After the PEX 8114 successfully transmits or receives all data, it issues a Completion TLP to the PCI Express original requester. The PEX 8114 supports up to eight concurrent Non-Posted PCI requests. Table 7-6 defines the PCI Express Non-Posted requests and the resulting PCI transactions when the Non-Posted PCI Express request is received.

Table 7-6. PCI Express Non-Posted Transactions

Initial PCI Express Non-Posted Transaction Type	Resultant PCI Transaction
I/O Write Request	I/O Write
I/O Read Request	I/O Read
Configuration Write Type 0	Configuration Write Type 0
Configuration Read Type 0	Configuration Read Type 0
Configuration Write Type 1	Configuration Write Type 1
Configuration Read Type 1	Configuration Read Type 1
Memory Read – Locked	***Not supported*** – returns a UR
Memory Read Request	PCI Memory Read, PCI Memory Read Line, or PCI Memory Read Line Multiple

7.5.4 PCI Express-to-PCI – PCI Bus Retry

Writes are serially processed on a first-come, first-served basis. Reads are attempted in parallel, *that is*, if one request receives a disconnect, the PEX 8114 attempts to gather data for another outstanding request, moving from request to request in an effort to complete as many transactions as possible, as soon as possible. If the *Force Strong Ordering* bit (offset FA0h[8]) is set, after data is returned in response to a Read request, the PEX 8114 concentrates all requests on gathering the remaining data for that transaction until the transaction completes. By default, the bit is cleared at power-on reset. If the bit is set, only one outstanding Read is allowed at a time. All Posted and Non-Posted Write bursts on the PCI Bus cannot be longer than the PCI Express Maximum Packet Size. There is no internal combining of Write TLPs in an effort to increase the PCI Burst Size.

7.5.5 PCI Express-to-PCI Transaction Request Size

The PEX 8114 determines which type of PCI Read request to issue on the PCI Bus, based on the size of the PCI Express Read request that the bridge receives. If a PCI Express Memory Read request enters the PEX 8114 Prefetchable Memory space, with a TLP length and starting address such that all requested data is within a single Cache Line and is less than an entire Cache Line, a Memory Read request is issued on the PCI Bus. If a PCI Express Memory Read request enters PEX 8114 Prefetchable Memory space, with a TLP length greater than or equal to the Cache Line Size, but less than two Cache Lines in size, the PEX 8114 issues a Memory Read Line request on the PCI Bus.

When a PCI Express Memory Read request enters the PEX 8114's Prefetchable Memory space, with a TLP length greater than or equal to two Cache Lines in size, the PEX 8114 issues a Memory Read Line Multiple request. Issuing of Memory Read Line Multiple requests can be disabled by clearing the *Memory Read Line Multiple Enable* bit. This method of determining whether to issue a Memory Read Line or Memory Read Line Multiple request applies only to PCI mode. In PCI-X mode, the Transaction Size is stated in the transaction and it is unnecessary to indicate the Transaction Size.

7.5.6 PCI Express-to-PCI Transaction Completion Size

Read Completions are arranged according to the following description. If the data quantity requested in the initial PCI Express Read request is less than or equal to the size of the maximum Read Completion Size, the data is returned to the PCI Express requester in a single TLP. If the data quantity requested in the initial PCI Express Read request is more than the maximum Read Completion Size, or if the Read crosses a 4-KB Address Boundary space, the Completion is constructed into more than one TLP. The TLPs are sized at the maximum Read Completion Size, except for the final TLP, which is sized to complete the remainder of the transaction.

7.6 PCI Express-to-PCI-X Transactions

In PCI-X mode, when a PCI Express device attempts a transaction from the PCI Express interface to the PCI-X Bus, the PEX 8114 translates the PCI Express transaction TLP into a PCI-X Burst transaction. In the most basic transaction, the PEX 8114 receives a TLP on the PCI Express lanes and translates the data into one or more PCI-X bursts. Credits for up to 6 KB of PCI Express Posted and Non-Posted transactions are issued. These transactions are queued according to the PCI Ordering Transaction rules in central memory, and transmitted to the PCI-X modules, as bandwidth allows.

7.6.1 PCI Express-to-PCI-X Posted Writes

For Posted Writes, typically including Memory Writes, no Completion information is returned to the PCI Express device that originated the transaction, and when the transaction is transmitted on the PCI-X Bus, the transaction is considered complete. If the PCI-X Bus is busy, the PEX 8114 can receive and retain many Posted PCI Express Write TLPs, limited only by the 6-KB central RAM's capacity. These transactions are processed as quickly as possible, in the order received. Table 7-7 defines this process.

Table 7-7. Posted Writes

Initial PCI Express Posted Transaction Type	Resultant PCI Transaction
Memory Write	PCI Memory Write.
Message Request	Interrupt messages cause changes on the PCI side of the bridge, which are translated to IntA to IntD. Internally, Power Management and error conditions can cause Error messages to generate to PCI Express side of the bridge.
Message Request with Payload	***Not supported.***

7.6.2 PCI Express-to-PCI-X Non-Posted Transactions

In the case of Non-Posted PCI Express transactions (which typically include Memory Reads and Configuration and I/O Writes and Reads), the PEX 8114 accepts the PCI Express TLP and creates and issues a PCI-X I/O or Configuration Write or Read request on the PCI-X Bus.

7.6.2.1 Non-Posted Writes

When the transaction is a Write, the PEX 8114 is prepared to transfer the entire burst as a single transaction on the PCI-X Bus.

7.6.2.2 Non-Posted Writes and Reads

When the Non-Posted PCI Express transaction is a Read request, the PEX 8114 issues a Read request on the PCI-X Bus, in an effort to fulfill the PCI Express Data request. The PCI-X Target of the request has the option of responding with a Split Completion or Immediate data – the PEX 8114 accepts either response:

- If the PCI-X Target responds with a Split Response, the Target must complete the Split Response with a Split Completion, at least to the next ADB, at a later time.
- If the PCI-X device replies to the PCI-X Read request with Immediate data, the PCI-X Target must continue supplying Immediate data, up to the next ADB.

The PEX 8114 does not allow a device to respond with a single data disconnect, unless the device is prepared to respond with single data disconnects up to the next ADB or to the end of the transaction, whichever comes first. This requirement is supported by the *PCI-X r1.0b* and *PCI-X r2.0a*. After the PEX 8114 successfully transmits or receives all data, the PEX 8114 issues a Completion TLP to the PCI Express requester.

Table 7-8 defines PCI Express Non-Posted requests and the resultant PCI transactions when the Non-Posted PCI Express request is received.

Table 7-8. Non-Posted Writes and Reads

Initial PCI Express Non-Posted Transaction Type	Resultant PCI Transaction
Memory Read Request	PCI-X Memory Read or Memory Read Line Multiple
Memory Read – Locked	***Not supported*** – returns a UR
I/O Write Request	I/O Write
I/O Read Request	I/O Read
Configuration Write Type 0	Configuration Write Type 0
Configuration Read Type 0	Configuration Read Type 0
Configuration Write Type 1	Configuration Write Type 1 or 0
Configuration Read Type 1	Configuration Read Type 1 or 0

7.6.2.3 Transaction Concurrency

The PEX 8114 supports up to eight Non-Posted PCI Express requests. Writes are serially processed on a first-come, first-served basis. Reads are attempted in parallel, *that is*, if one request receives a disconnect, the PEX 8114 attempts to gather data for another of the outstanding requests, moving from request to request in an effort to complete as many transactions as possible, as soon as possible. If the *Force Strong Ordering* bit (offset FA0h[8]) is set, after data is returned in response to a Read request, the PEX 8114 concentrates all requests on gathering data to complete that transaction until the transaction completes. This is performed only if the *Force Strong Ordering* bit is not set. If the bit is set, only one outstanding Read is allowed at a time.

All Posted and Non-Posted Write bursts on the PCI Bus can be no longer than the PCI Express Maximum Packet Size. There is no internal combining of Write TLPs in an effort to increase the PCI Burst Size. Read Completions are gathered from the PCI-X Bus as a single DWord Disconnect, Completions to the next ADB, or Completion of the entire requested data size. The Completion data is collected within the PEX 8114, then delivered to the PCI Express requesters as TLP packets that are no larger than the Maximum Packet Size, until all data requested by the PCI Express device is satisfied.

7.7 Transaction Transfer Failures

The previously described transactions are the set of legal and expected transactions. Successful Data transfer is dependent upon the PCI-X and PCI Express devices connected to the PEX 8114 performing, as described in the *PCI r3.0*, *PCI-X r2.0a*, and *PCI Express r1.0a*. When a device fails to correctly perform, the transaction is likely to fail. These failures typically result in transaction timeouts and the setting of internal register bits. The *PCI Express-to-PCI/PCI-X Bridge r1.0* anticipates most of the typical failures and specifies error handling procedures for error condition recovery. The PEX 8114 supports these error handling routines, recovers internal resources, and logs errors according to the specifications. For further details on error handling and recovery, refer to Chapter 8, "Error Handling," and the *PCI Express-to-PCI/PCI-X Bridge r1.0*.

The other side of this failure to flush a pending transaction from the bridge is that it is assumed that a transaction will not complete and quickly reclaim its internal buffers. To accommodate heavy traffic densities, the bridge has several selectable transaction timeout periods. These timeout periods are based on PCI_CLK cycles and in PCI mode, can be selected as 2^{10}, 2^{15}, or 2^{20} Clock cycles, or the timeout can be disabled. The following register bits are used to select these timeouts:

- *Primary Discard Timer* (**Bridge Control** register, offset 3Ch[24])
- *Secondary Discard Timer* (**Bridge Control** register, offset 3Ch[25]) (discussed further in Section 7.7.1)
- *Disable Completion Timeout Timer* (offset FA0h[5]) (discussed further in Section 7.7.2 and Section 7.7.4)
- *Enable Long Completion Timeout Timer* (offset FA0h[6]) (discussed further in Section 7.7.2 and Section 7.7.4)

Table 7-9 defines register bit Timer values as they apply to available timeouts.

When Completions are not returned to the PEX 8114, or when the endpoint does not accept returned Completions held within the PEX 8114, the PEX 8114 internal resources remain ***reserved*** to those uncompleted transactions and cannot be used for future transactions. The following sections describe how the PEX 8114 controls slow or stalled transactions:

- PCI Endpoint Fails to Retry Read Request
- PCI-X Endpoint Fails to Transmit Split Completion
- PCI-X Endpoint Allows Infinite Retries
- PCI Express Endpoint Fails to Return Completion Data

Table 7-9. Clock Cycle Timeout Period Selection

Clock Cycle Timeout	Bridge Control Register		Disable Completion Timeout Timer (Offset FA0h[5])	Enable Long Completion Timeout Timer (Offset FA0h[6])
	Primary Discard Timer (Offset 3Ch[24])	Secondary Discard Timer (Offset 3Ch[25])		
Default	0	0	0	1
2^{10}	0	0	0	0
2^{15}	1	1	0	0
2^{20}	X	X	0	1
No Timer (Disabled)	X	X	1	X

Note: *"X" indicates "Don't Care."*

7.7.1 PCI Endpoint Fails to Retry Read Request

The Secondary Discard Timer monitors Completions located within the PEX 8114, waiting to return to the initial PCI requester. This Timer applies in PCI mode, and only when the PCI device initiated the initial Read request. After the Completion returns from the PCI Express endpoint to the PEX 8114, if the original PCI requester fails to Retry for the Read Completion, the data remains in the PEX 8114 and results in wasted resources.

The Timer times Completions within the PEX 8114. If a Completion is not requested by the initial PCI requester before the Secondary Discard Timer times out, the Completion is dropped and the PEX 8114 reclaims the internal resources. The Timer can be configured by the **Bridge Control** register *Secondary Discard Timer* bit (offset 3Ch[25]) to time out at 2^{10} PCI_CLK clock periods when set, or 2^{15} PCI_CLK clock periods when cleared.

7.7.2 PCI-X Endpoint Fails to Transmit Split Completion

When the PEX 8114 receives and takes ownership of a PCI Express Read request, and successfully forwards that request to a PCI-X device and receives a Split Response, the PEX 8114 waits a specified length of time for a Split Completion from the PCI-X device. If that Split Completion fails to return within the specified time, the PEX 8114 reclaims its internal resources.

Table 7-10 defines the three available Timer settings, selectable by way of the *Enable Long Completion Timeout Timer* and *Disable Completion Timeout Timer* bits (offset FA0h[6:5], respectively).

Table 7-10. Timer Settings for Transmitting Split Completions

Offset FA0h[6:5]	Timer Setting
00b	2^{15} PCI_CLK cycles timeout
10b	2^{20} PCI_CLK cycles timeout
X1b	No timeout

7.7.3 PCI-X Endpoint Allows Infinite Retries

When the PEX 8114 attempts to master a PCI or PCI-X Read Request transaction onto the PCI-X Bus in response to a PCI Express endpoint Read request, it is expected that the PCI-X endpoint might not contain data that is immediately ready and can respond to the PEX 8114's Read request with a Retry. In response to the Retry, the PEX 8114 re-attempts the Read request, and it is expected that a future Read attempt will be completed with data. If the endpoint infinitely replies to the PEX 8114 Read request with a Retry, the PEX 8114 terminates the transaction. To facilitate this, the number of Retries received for each Read request are counted. At which time, the PEX 8114 compares the value stored in the *Maximum Read Cycle Value* field (offset FA0h[26:16]). If the number of Retries received matches the number stored in the *Maximum Read Cycle Value* field, the Read request is dropped and the *Retry Failure Status* bit (offset FA0h[27]) is set. If the *Force Strong Ordering* bit (offset FA0h[8]) is not set, the PEX 8114 attempts up to eight Read requests in a Round-Robin scheme. A Retry Count for each of the eight Read requests is maintained, and compared, as it takes its turn at the PCI Bus.

7.7.4 PCI Express Endpoint Fails to Return Completion Data

The PEX 8114 holds internal resources ***reserved*** to receive Completions. If the PCI Express endpoint responsible for a Completion fails to transmit a Completion, the PEX 8114's internal resources are at risk of remaining ***reserved***, waiting for a Completion that might never occur. The PEX 8114 contains an Internal Timer used to trigger the bridge to reclaim internal resources reserved for Completions that might never occur. Table 7-11 defines the three available Timer settings, selectable by way of the *Enable Long Completion Timeout Timer* and *Disable Completion Timeout Timer* bits (offset FA0h[6:5], respectively).

When PCI Non-Posted requests and Completions from PCI Express-to-PCI are executed and no timeout is selected (offset FA0h[6:5]=X1b), the buffer holding Completions for the PCI requests are not automatically reclaimed. However, after 2^{20} clocks transpire without a Completion, the Completion Buffer Timeout status bit for that buffer (offset F88h) is set to indicate that the buffer is ***reserved*** for an extremely late Completion. When the timeout setting is set to 2^{15} or 2^{20} (offset FA0h[6:5]=00b or 10b, respectively) and the Completion fails to return before the timeout, the buffer is reclaimed after the timeout and reused. If after a transaction times out, and the buffer is scheduled for reuse, and the PCI endpoint Retries the Read request for the transaction that timed out, the PEX 8114 returns a Target Abort or FFFF_FFFFh, as selected by the **Bridge Control** register *Master Abort Mode* bit (offset 3Ch[21]) to indicate that a timeout occurred to the PCI endpoint. Each buffer can timeout and be reclaimed three times. After three reclaims and four timeouts, the *Completion Buffer Timeout Status* bit for that buffer is set, to indicate that the buffer can no longer be reclaimed. When a buffer times out, if a user or operating system confirms that no stale Completions are pending, the buffer can be re-initialized by writing 1 to the offset F88h bit representing that buffer.

There is a degree of risk involved in re-initializing buffers. If a stale Completion is pending, and the software is not aware of this, and the associated *Completion Buffer Timeout Status* bit is mistakenly cleared, the stale Completion can be mistaken for a Completion to a more-recent request, resulting in incorrect data being used for the Completion. If 32 PCI Read requests fail to complete by the PCI Express endpoint, all eight buffers timeout four times and all resources are consumed.

To prevent a lockup condition, the PEX 8114 automatically clears the *Completion Buffer Timeout Status* bits for all eight registers, allowing it to continue to accept Non-Posted requests. If a lockup condition occurs, the PEX 8114 can no longer accept Non-Posted PCI-X requests, which precludes Configuration Writes. It therefore becomes impossible to clear the buffer timeouts after all buffers time out.

Table 7-11. Timer Settings for Receiving Completions

Offset FA0h[6:5]	Timer Setting
00b	2^{15} PCI_CLK cycles timeout
10b	2^{20} PCI_CLK cycles timeout
X1b	No timeout

Note: *"X" indicates "Don't Care."*

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Chapter 8 Error Handling

8.1 Forward Transparent Bridge Error Handling

For all errors detected by the bridge, the bridge sets the appropriate error status bit [both Conventional PCI/PCI-X Error bit(s) and PCI Express error status bit(s)], and generates an Error message on the PCI Express interface, if enabled. Each error condition has an error severity level programmable by software, and a corresponding Error message generated on the PCI Express interface.

Four bits control PCI Express interface Error message generation:

- **PCI/PCI-X Command** register *SERR# Enable* bit
- **PCI Express Device Control** register *Correctable Error Reporting Enable* bit
- **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Fatal Error Reporting Enable* bit

ERR_COR messages are enabled for transmission if the *Correctable Error Reporting Enable* bit is set. ERR_NONFATAL messages are enabled for transmission if the *SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. ERR_FATAL messages are enabled for transmission if the *SERR# Enable* or *Fatal Error Reporting Enable* bit is set. The **Device Status** register *Correctable Error Detected, Non-Fatal Error Detected*, and *Fatal Error Detected* status bits are set for the corresponding errors on the PCI Express interface, regardless of the *Error Reporting Enable* bit values.

8.1.1 Forward Transparent Bridge PCI Express Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI Express interface, and the destination interface is operating in Conventional PCI/PCI-X modes. If a Write Request or Read Completion is received with a Poisoned TLP, consider the entire Data Payload of the PCI Express transaction as *corrupt*. Parity is inverted for all Data phases when completing the transaction on the PCI/PCI-X Bus. If a TLP is received and an ECRC error is detected, consider the entire TLP as *corrupt* and not forwarded, but dropped by the bridge.

Table 8-1 defines the translation a bridge must perform when forwarding a Non-Posted PCI Express request (Write or Read) to the PCI/PCI-X Bus, and the request is immediately completed on the PCI/PCI-X Bus, normally or with an error condition.

Table 8-1. Translation Bridge Action when Forwarding Non-Posted PCI Express Request to PCI/PCI-X Bus

Immediate PCI/PCI-X Termination	PCI Express Completion Status
Data Transfer with Parity error (Non-Posted Writes)	Unsupported Request
Data Transfer with Parity error (Reads)	Successful (Poisoned TLP)
Master Abort	Unsupported Request
Target Abort	Completer Abort

8.1.1.1 Received Poisoned TLP

When the PCI Express interface receives a Write Request or Read Completion with poisoned data, the following occurs:

1. **PCI Status** register *Detected Parity Error* bit is set.
2. **PCI Status** register *Master Data Parity Error* bit is set if the Poisoned TLP is a Read Completion and the **PCI Command** register *Parity Error Response Enable* bit is set.
3. **Uncorrectable Error Status** register *Poisoned TLP Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared and the *First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Poisoned TLP Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared and the *SERR# Enable* bit is set.
8. Parity bit associated with each DWord of data on the PCI/PCI-X Bus is inverted.
9. When a Poisoned TLP Write Request is forwarded to the PCI/PCI-X Bus and the bridge detects PCI_PERR# asserted, the following occurs:
   - **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
   - **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set
   - Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear and the *First Error Pointer* is inactive
10. No Error message is generated when a Poisoned TLP is forwarded to the PCI/PCI-X Bus with inverted parity and PCI_PERR# is detected asserted by the PCI/PCI-X Target device.

8.1.1.2 Received ECRC Error

When a TLP is received and the bridge detects an ECRC error, the following occurs:

1. Transaction is dropped.
2. **PCI Status** register *Detected Parity Error* bit is set.
3. **Uncorrectable Error Status** register *ECRC Error Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared and the *First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *ECRC Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.3 PCI/PCI-X Uncorrectable Data Errors

The following sections describe error handling when forwarding Non-Poisoned PCI Express transactions to the PCI/PCI-X Bus, and an Uncorrectable PCI/PCI-X error is detected.

Posted Writes

When the PEX 8114 detects PCI_PERR# asserted on the PCI/PCI-X secondary interface while forwarding a Non-Poisoned Posted Write transaction from the PCI Express interface, the following occurs:

1. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register *Secondary Uncorrectable First Error Pointer* is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *SERR# Enable* bit is set.
7. After the error is detected, the remainder of the data is forwarded.

Non-Posted Writes

When the PEX 8114 detects PCI_PERR# asserted on the PCI/PCI-X secondary interface while forwarding a Non-Poisoned Non-Posted Write transaction from the PCI Express interface, the following occurs:

1. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. PCI Express Completion with Unsupported Request status is generated.
3. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *SERR# Enable* bit is set.

When the Target signals Split Response, the bridge terminates the transaction as it would for a Split Request that does not contain an error and takes no further action. If the returned Split Completion is a Split Completion Error message, the bridge returns a PCI Express Completion with Unsupported Request status to the requester.

Immediate Reads

When the PEX 8114 forwards a Read request (I/O, Memory, or Configuration) from the PCI Express interface and detects an Uncorrectable Data error on the secondary bus while receiving an Immediate or Split Response from the completer, the following occurs:

1. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
3. PCI_PERR# is asserted on the secondary interface if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

After detecting an Uncorrectable data error on the destination bus for an Immediate Read transaction, the PEX 8114 continues to fetch data until the Byte Count is satisfied or the Target ends the transaction. When the bridge creates the PCI Express Completion, it forwards the Completion with Successful Completion and poisons the TLP. For PCI-X, an Uncorrectable Data error on a Split Response does not affect handling of subsequent Split Completions.

PCI-X Split Read Completions

When the bridge forwards a Non-Poisoned Read Completion from PCI Express to PCI-X and detects PCI_PERR# asserted by the PCI-X Target, the following occurs:

1. Bridge continues to forward the remainder of the Split Completion.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.4 PCI/PCI-X Address/Attribute Errors

When the PEX 8114 forwards transactions from PCI Express to PCI/PCI-X, PCI Address errors are reported by SERR# Target assertion. When the PEX 8114 detects SERR# asserted, the following occurs:

1. **Secondary Status** register *Secondary Received System Error* bit is set.
2. **Secondary Uncorrectable Error Status** register *SERR# Assertion Detected* bit is set.
3. **FECh** register Secondary Uncorrectable Error Pointer is updated if the *Secondary Uncorrectable First Error Pointer* is inactive and the **Secondary Uncorrectable Error Mask** register *SERR# Assertion Detected Mask* bit is clear. No Header is logged.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *SERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *SERR# Assertion Detected Mask* bit is clear OR the **Bridge Control** register *SERR# Enable* bit is set AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the **PCI Command** and **Bridge Control** register *SERR# Enable* bits are set.

8.1.1.5 PCI/PCI-X Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express to PCI/PCI-X results in a Master Abort on the PCI/PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **Secondary Status** register *Secondary Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared OR the **Bridge Control** register *Master Abort Mode* bit is set AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Master Abort Mode* bit is set or the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.6 PCI/PCI-X Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express to PCI/PCI-X results in a Master Abort on the PCI/PCI-X Bus, the following occurs:

1. Completion with Unsupported Request status is returned on the PCI Express interface.
2. **Secondary Status** register *Secondary Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.7 PCI-X Master Abort on Split Completion

When a Split Completion forwarded from PCI Express to PCI-X results in a Master Abort on the PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **Secondary Status** register *Secondary Received Master Abort* bit is set.
3. **PCI-X Secondary Status** register *Split Completion Discarded* bit is set.
4. **Secondary Uncorrectable Error Status** register *Master Abort on Split Completion Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Master Abort on Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Master Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Master Abort on Split Completion Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Master Abort on Split Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.8 PCI/PCI-X Target Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express to PCI/PCI-X results in a Target Abort on the PCI/PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **Secondary Status** register *Secondary Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.9 PCI/PCI-X Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express to PCI/PCI-X results in a Target Abort on the PCI/PCI-X Bus, the following occurs:

1. Completion with Completer Abort status is returned on the PCI Express interface.
2. **Secondary Status** register *Secondary Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.10 PCI-X Target Abort on Split Completion

When a Split Completion forwarded from PCI Express to PCI-X results in a Target Abort on the PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **Secondary Status** register *Secondary Received Target Abort* bit is set.
3. **PCI-X Secondary Status** register *Split Completion Discarded* bit is set.
4. **Secondary Uncorrectable Error Status** register *Target Abort on Split Completion Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Target Abort on Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Target Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Target Abort on Split Completion Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Target Abort on Split Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.11 Completer Abort

CSR registers internal to the PEX 8114 can be accessed through BAR0 Memory-Mapped accesses. These Read/Write accesses are limited to single DWord transactions. If a Memory-Mapped CSR access is received with a TLP length field greater than 1 DWord, the following occurs:

1. When the transaction is a Write Request, the transaction is dropped.

   When the transaction is a Read request, a Completion with Completer Abort status is returned to the requester and the **PCI Status** register *Signaled Target Abort* bit is set.
2. **Uncorrectable Error Status** register *Completer Abort Status* bit is set.
3. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared and the *First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Completer Abort Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Completer Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the **Uncorrectable Error Mask** register *Completer Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.12 Unexpected Completion

When a Completion, targeted at the bridge, is received on the PCI Express interface that does not contain a corresponding outstanding request, the following occurs:

1. Entire transaction is discarded.
2. **PCI-X Bridge Status** register *Unexpected Split Completion* bit is set.
3. **Uncorrectable Error Status** register *Unexpected Completion Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared and the *First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Unexpected Completion Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.13 Receive Non-Posted Request Unsupported

When a Non-Posted request, targeted to the PEX 8114, is received on the PCI Express interface and the bridge cannot complete the request, the following occurs:

1. Completion with Unsupported Request Completion status is returned to the requester.
2. **Uncorrectable Error Status** register *Unsupported Request Error Status* bit is set.
3. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *Uncorrectable First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Unsupported Request Error Mask* bit is cleared and the *Uncorrectable First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Unsupported Request Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Unsupported Request Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the *Unsupported Request Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.1.1.14 Link Training Error

When a PCI Express Link Training error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Training Error Status* bit is set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Training Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Training Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *Training Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.15 Data Link Protocol Error

When a PCI Express Data Link Protocol error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Data Link Protocol Error Status* bit is set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Data Link Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Data Link Protocol Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *Data Link Protocol Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.1.1.16 Flow Control Protocol Error

When a PCI Express Flow Control Protocol error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Flow Control Protocol Error Status* bit is set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Flow Control Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Flow Control Protocol Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *Flow Control Protocol Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.1.1.17 Receiver Overflow

When a PCI Express Receiver Overflow is detected, the following occurs:

1. **Uncorrectable Error Status** register *Receiver Overflow Status* bit is set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Receiver Overflow Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Receiver Overflow Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *Receiver Overflow Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.1.18 Malformed TLP

When a PCI Express Malformed TLP is received, the following occurs:

1. **Uncorrectable Error Status** register *Malformed TLP Status* bit is set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Malformed TLP Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Malformed TLP Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *Malformed TLP Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.2 Forward Transparent Bridge PCI/PCI-X Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI/PCI-X Bus, and the destination side is PCI Express. The PEX 8114 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on the PCI/PCI-X interface. Posted Write data received on the PCI/PCI-X interface with bad parity is forwarded to the PCI Express interface as Poisoned TLPs.

Table 8-2 defines the error forwarding requirements for Uncorrectable Data errors that the PEX 8114 detects when a transaction targets the PCI Express interface.

Table 8-3 defines the bridge behavior on a PCI/PCI-X Delayed transaction forwarded by a bridge to the PCI Express interface as a Memory Read or I/O Read/Write Request, and the PCI Express interface returns a Completion with UR or CA status for the request.

Table 8-2. Error Forwarding Requirements for Uncorrectable Data Errors

Received PCI/PCI-X Error	Forwarded PCI Express Error
Write with Parity error	Write Request with Poisoned TLP
Read Completion or Split Read Completion with Parity error in Data phase	Read Completion with Poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write Completion with Completer Abort Status
Split Completion message with Uncorrectable Data error in Data phase	

Table 8-3. Bridge Behavior on PCI/PCI-X Delayed Transaction Forwarded by Bridge

PCI Express Completion Status	PCI/PCI-X Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory or I/O Read)	Target Abort	Normal Completion, returns FFFF_FFFFh
Unsupported Request (on I/O Write)		Normal Completion
Completer Abort	Target Abort	

8.1.2.1 Received PCI/PCI-X Errors

Uncorrectable Data Error on Posted Write

When the PEX 8114 detects an Uncorrectable Data error on the PCI/PCI-X secondary interface for a Posted Write transaction that crosses the bridge, the following occurs:

1. PCI_PERR# is asserted if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
3. Posted Write transaction is forwarded to PCI Express as a Poisoned TLP.
4. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
5. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
6. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
7. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

Uncorrectable Data Error on Non-Posted Write in Conventional PCI Mode

When a Non-Posted Write is addressed allowing it to cross the bridge, and the PEX 8114 detects an Uncorrectable Data error on the PCI interface, the following occurs:

1. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
2. When the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to the PCI Express interface, and PCI_PERR# is asserted on the PCI Bus.

   When the *Secondary Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a Poisoned TLP. The **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set. PCI_PERR# is not asserted on the PCI Bus.
3. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Data Error on Non-Posted Write in PCI-X Mode

When a Non-Posted Write is addressed allowing it to cross the bridge, and the PEX 8114 detects an Uncorrectable Data error on the PCI-X interface, the following occurs:

1. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
2. PEX 8114 signals Data Transfer for Non-Posted Write transactions, and if there is an Uncorrectable Data error, the transaction is discarded.
3. When the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, PCI_PERR# is asserted on the PCI-X Bus.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8114 forwards a Non-Poisoned Read Completion from PCI Express to PCI, and it detects PCI_PERR# asserted by the PCI Master, the following occurs:

1. Remainder of the Completion is forwarded.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

When the PEX 8114 forwards a Poisoned Read Completion from PCI Express to PCI, the PEX 8114 proceeds with the listed actions when it detects PCI_PERR# asserted by the PCI Master; however, an Error message is not generated on the PCI Express interface.

Uncorrectable Data Error on PCI-X Split Read Completions

When the PEX 8114 detects an Uncorrectable Data error on the PCI-X secondary interface while receiving a Split Read Completion that crosses the bridge, the following occurs:

1. PCI_PERR# is asserted if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
3. Split Read Completion transaction is forwarded to PCI Express as a Poisoned TLP.
4. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
5. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
6. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
7. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

Uncorrectable Address Error

When the PEX 8114 detects an Uncorrectable Address error, and Parity error detection is enabled by way of the **Bridge Control** register *Secondary Parity Error Response Enable* bit, the following occurs:

1. Transaction is terminated with a Target Abort and discarded.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set, independent of the **Bridge Control** register *Secondary Parity Error Response Enable* bit value.
3. **Secondary Status** register *Secondary Signaled Target Abort* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Address Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Address Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Address Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Address Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Address Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Attribute Error

When the PEX 8114 detects an Uncorrectable Attribute error, and Parity error detection is enabled by way of the **Bridge Control** register *Secondary Parity Error Response Enable* bit, the following occurs:

1. Transaction is terminated with a Target Abort and discarded.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set, independent of the **Bridge Control** register *Secondary Parity Error Response Enable* bit value.
3. **Secondary Status** register *Secondary Signaled Target Abort* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Attribute Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Attribute Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Attribute Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Attribute Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Attribute Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.1.2.2 Unsupported Request (UR) Completion Status

The PEX 8114 provides two methods for handling a PCI Express Completion received with Unsupported Request (UR) status in response to requests originated by the PCI/PCI-X interface. The **Bridge Control** register *Master Abort Mode* bit controls the response. In either case, the **PCI Status** register *Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and an Unsupported Request is not considered an error. When a Read transaction initiated on the PCI/PCI-X Bus results in the return of a Completion with Unsupported Request status, the PEX 8114 returns FFFF_FFFFh to the originating Master and asserts PCI_TRDY# to terminate the Read transaction normally on the originating interface.

When a Non-Posted Write transaction results in a Completion with Unsupported Request status, the PEX 8114 asserts PCI_TRDY# to complete the Write transaction normally on the originating bus, and discards the Write data.

Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8114 signals a Target Abort to the originating Master of an upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a Completion with UR Status. Additionally, the **Secondary Status** register *Secondary Signaled Target Abort* bit is set.

8.1.2.3 Completer Abort (CA) Completion Status

When the PEX 8114 receives a Completion with Completer Abort status on the PCI Express primary interface in response to a forwarded Non-Posted PCI/PCI-X transaction, the **PCI Status** register *Received Target Abort* bit is set. A CA response results in a Delayed Transaction Target Abort or a Split Completion Target Abort Error message on the PCI/PCI-X Bus. The PEX 8114 provides data to the requesting PCI/PCI-X agent, up to the point where data was successfully returned from the PCI Express interface, then signals Target Abort. The **Secondary Status** register *Secondary Signaled Target Abort* bit is set when signaling Target Abort to a PCI/PCI-X agent.

8.1.2.4 Split Completion Errors

Split Completion Message with Completer Errors

A transaction originating from the PCI Express interface and requiring a Completion can be forwarded to the PCI-X interface, where the Target (completer) responds with Split Response. If the completer encounters a condition that prevents the successful execution of a Split transaction, the completer must notify the requester of the abnormal condition, by returning a Split Completion message with the Completer Error class. If the bridge responds with Completer Abort status, it sets the **PCI Status** register *Signaled Target Abort* bit.

Table 8-4 defines the abnormal conditions and the bridge's response to the Split Completion message. Each is described in the sections that follow.

Table 8-4. Abnormal Conditions and Bridge Response to Split Completion Messages

PCI-X Split Completion Message	Completer Error Code		Bit Set in Secondary Status Register	Bit Set in Secondary Uncorrectable Error Status Register	PCI Express Completion Status
	Class	Index			
Master Abort	1h	00h	*Received Master Abort*	*Received Master Abort*	Unsupported Request
Target Abort	1h	01h	*Received Target Abort*	*Received Target Abort*	Completer Abort
Uncorrectable Write Data Error	1h	02h	*Master Data Parity Error*	*PERR# Assertion Detected*	Unsupported Request
Byte Count Out of Range	2h	00h	***None***	***None***	Unsupported Request
Uncorrectable Split Write Data Error	2h	01h	*Master Data Parity Error*	*PERR# Assertion Detected*	Unsupported Request
Device-Specific Error	2h	8Xh	***None***	***None***	Completer Abort

Split Completion Message with Master Abort

When a bridge receives a Split Completion message indicating Master Abort, the following occurs:

1. Completion with Unsupported Request status is returned to the requester.
2. **Secondary Status** register *Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is clear and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

Split Completion Message with Target Abort

When a bridge receives a Split Completion message indicating Target Abort, the following occurs:

1. Completion with Completer Abort status is returned to the requester.
2. **Secondary Status** register *Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort Status* bit is set.
4. **PCI Status** register *Signaled Target Abort* bit is set.
5. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is clear and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

Split Completion Message with Uncorrectable Write Data Error or Uncorrectable Split Write Data Error

When a bridge receives a Split Completion message indicating an Uncorrectable Write Data error or Uncorrectable Split Write Data error, the following occurs:

1. Completion with Unsupported Request status is returned to the requester.
2. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
3. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set.
4. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

Split Completion Message with Byte Count Out of Range

When a bridge receives a Split Completion message indicating a Byte Count Out of Range error, a Completion with Unsupported Request status is returned to the requester.

Split Completion Message with Device-Specific Error

When a bridge receives a Split Completion message indicating a Device-Specific error, a Completion with Completer Abort status is returned to the requester.

Corrupted or Unexpected Split Completion

When a bridge receives a corrupted or unexpected Split Completion, the following occurs:

1. **PCI-X Secondary Status** register *Unexpected Split Completion Status* bit is set.
2. **Secondary Uncorrectable Error Status** register *Unexpected Split Completion Error Status* bit is set.
3. TLP Header of the corrupt or unexpected Split Completion is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Unexpected Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Unexpected Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Unexpected Split Completion Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the *Unexpected Split Completion Mask* bit is clear and the *SERR# Enable* bit is set.

Data Parity Error on Split Completion Messages

When a bridge detects a Data error during the Data phase of a Split Completion message, the following occurs:

1. **Secondary Uncorrectable Error Status** register *Uncorrectable Split Completion Message Data Error Status* bit is set.
2. TLP Header of the Split Completion is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Split Completion Message Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
3. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Split Completion Message Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Split Completion Message Data Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Split Completion Message Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.1.3 Forward Transparent Bridge Timeout Errors

8.1.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted Request if a Completion does not arrive within a reasonable time. Bridges, when acting as Initiators on the PCI Express interface on behalf of internally generated requests, or when forwarding requests from a secondary interface, behave as endpoints for requests of which they assume ownership. If a Completion timeout is detected and the link is up, the PEX 8114 responds as if a Completion with Unsupported Request status was received, and the following occurs:

1. **Uncorrectable Error Status** register *Completion Timeout Status* bit is set.
2. TLP Header of the original request is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Completion Timeout Mask* bit is cleared and the *First Error Pointer* is inactive.
3. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Uncorrectable Error Severity** register *Completion Timeout Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Completion Timeout Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *SERR# Enable* bit is set.

8.1.3.2 PCI Delayed Transaction Timeout Errors

The PEX 8114 contains Delayed Transaction Discard Timers for each queued Delayed transaction. If a Delayed Transaction timeout is detected, the following occurs:

1. **Bridge Control** register *Discard Timer Status* bit and **Secondary Uncorrectable Error Status** register *Delayed Transaction Discard Timer Expired Status* bit are set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the **Secondary Uncorrectable Error Severity** register *Delayed Transaction Discard Timer Expired Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Delayed Transaction Discard Timer Expired Mask* bit is cleared OR **Bridge Control** register *Discard Timer SERR# Enable* bit is set AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the *SERR# Enable* bit is set.

8.1.4 Forward Transparent Bridge SERR# Forwarding

PCI devices can assert SERR# when detecting errors that compromise system integrity. When the PEX 8114 detects SERR# asserted on the secondary PCI/PCI-X Bus, the following occurs:

1. **Secondary Status** register *Received System Error* bit and **Secondary Uncorrectable Error Status** register *SERR# Assertion Detected Status* bit are set.
2. ERR_FATAL/ERR_NONFATAL message is generated on the PCI Express interface, depending on the severity of the **Secondary Uncorrectable Error Severity** register *SERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *SERR# Assertion Detected Mask* bit is clear OR **Bridge Control** register *SERR# Enable* bit is set AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set
3. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
4. **PCI Status** register *Signaled System Error* bit is set if the **PCI Command** and **Bridge Control** register *SERR# Enable* bits are set.

8.2 Reverse Transparent Bridge Error Handling

8.2.1 Reverse Transparent Bridge Forwarding PEX 8114 System Errors and System Error Messages

PCI Express Error Reporting messages are not compatible with PCI/PCI-X interfaces. There are three types of error levels, each reported by a unique Error message:

- Correctable (ERR_COR)
- Non-Fatal (ERR_NONFATAL)
- Fatal (ERR_FATAL)

Error messages received from the PCI Express hierarchy are forwarded upstream, through the PCI_INTA# or PCI_SERR# balls or a Message Signaled interrupt (MSI). To control error reporting and forwarding by the PEX 8114, use one of the following:

- Root Port registers
- Conventional PCI Type 1 register set

For all errors detected by the bridge, the bridge sets the appropriate error status bit [both Conventional PCI/PCI-X error bit(s) and PCI Express error status bit(s)]. If reporting for an error is not masked, the bridge also reports to the Root Port registers. The Root Port registers Forward bridge-detected errors in the same manner as Error messages received from the hierarchy, as if the bridge transmitted an Error message to itself.

8.2.1.1 Root Port Error Forwarding Control

The Root Port registers provide control, to enable forwarding of each error type, independently of the others.

The **Root Control** register enables reporting of error events through Conventional PCI system errors. PCI_SERR# is asserted when the PEX 8114 detects errors that are not masked, or an Error message is received and the corresponding *Reporting Enable* bit is set. Three bits control PCI_SERR# assertion for Correctable, Non-Fatal, and Fatal errors:

- *System Error on Correctable Error Enable*
- *System Error on Non-Fatal Error Enable*
- *System Error on Fatal Error Enable*

The **Root Error Command** register enables forwarding of error events through Interrupt requests:

- PCI_INTA# is asserted when the PEX 8114 detects errors that are not masked, the corresponding *Reporting Enable* bit is set, and the **Command** register *Interrupt Disable* bit is cleared
- An MSI is transmitted, and PCI_INTA# is not asserted, when the PEX 8114 detects errors that are not masked, the corresponding *Reporting Enable* bit is set, the **Command** register *Interrupt Disable* bit is cleared, and the **MSI Control** register *MSI Enable* bit is set
- PCI_INTA# is asserted when the PEX 8114 receives an Error message on the PCI Express interface, and the corresponding *Reporting Enable* bit is set
- An MSI is transmitted, and PCI_INTA# is not asserted, when the PEX 8114 receives an Error message on the PCI Express interface, the corresponding *Reporting Enable* bit is set, and the **MSI Control** register *MSI Enable* bit is set

Three **Root Error Command** register bits control PCI_INTA# assertion or MSI signaling for Correctable, Non-Fatal, and Fatal errors:

- *Correctable Error Reporting Enable*
- *Non-Fatal Error Reporting Enable*
- *Fatal Error Reporting Enable*

8.2.1.2 Conventional PCI Type 1 Error Forwarding Control

Two Conventional PCI bits control reporting and forwarding of bridge-detected errors and Error messages received from the PCI Express hierarchy:

- **PCI Command** register *SERR# Enable* bit
- **Bridge Control** register *SERR# Enable* bit

Fatal and Non-Fatal errors detected by the bridge are forwarded to the Host by PCI_SERR# assertion, if the **PCI Command** register *SERR# Enable* bit is set. Fatal and Non-Fatal Error messages received from the PCI Express hierarchy are forwarded to the Host by PCI_SERR# assertion if the **PCI Command** and **Bridge Control** register *SERR# Enable* bits are set.

8.2.1.3 Bridge-Detected Error Reporting

Errors detected by the PEX 8114 that are not masked must be enabled to report to the Root Port registers. The following four bits control error reporting to the Root Port registers:

- **PCI Command** register *SERR# Enable* bit
- **PCI Express Device Control** register *Correctable Error Reporting Enable* bit
- **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Fatal Error Reporting Enable* bit

Additionally, the *SERR# Enable* bit controls the forwarding of errors upstream to the Host.

Correctable errors (ERR_COR) are reported to the Root Port registers if the *Correctable Error Reporting Enable* bit is set. Non-Fatal errors (ERR_NONFATAL) are reported to the Root Port registers if the *SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. Fatal errors (ERR_FATAL) are reported to the Root Port registers if the *SERR# Enable* or *Fatal Error Reporting Enable* bit is set. The **Device Status** register *Correctable*, *Non-Fatal*, and *Fatal Error Detected* status bits are set for the corresponding errors, regardless of the *Error Reporting Enable* settings.

8.2.2 Reverse Transparent Bridge PCI Express Originating Interface (Secondary to Primary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI Express (secondary) interface, and the destination interface is operating in a Conventional PCI/PCI-X (primary) mode. If a Write Request or Read Completion is received with a Poisoned TLP, the entire PCI Express transaction Data Payload must be considered *corrupt*. Parity is inverted for all Data phases when completing PCI/PCI-X Bus transactions. If a TLP is received and an ECRC error is detected, the entire TLP must be considered corrupt and not forwarded, but dropped by the bridge.

Table 8-5 defines the translation the PEX 8114 performs when it forwards a Non-Posted PCI Express Request (Write or Read) to the PCI/PCI-X Bus, and the request is immediately completed normally on the PCI/PCI-X Bus or with an error condition.

Table 8-5. Translation Bridge Action when Forwarding Non-Posted PCI Express Request to PCI/PCI-X Bus

Immediate PCI/PCI-X Termination	PCI Express Completion Status
Data Transfer with Parity error (Reads)	Successful (Poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

8.2.2.1 Received Poisoned TLP

When a Write Request or Read Completion is received by the PCI Express interface, and the data is poisoned, the following occurs:

1. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
2. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the Poisoned TLP is a Read Completion and the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
3. **Uncorrectable Error Status** register *Poisoned TLP Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared and the *First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Poisoned TLP Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Poisoned TLP Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Poisoned TLP Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Poisoned TLP Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Poisoned TLP Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the **Uncorrectable Error Mask** register *Poisoned TLP Error Mask* bit is cleared and the *SERR# Enable* bit is set.
9. Parity bit associated with each DWord of data on the PCI/PCI-X Bus is inverted.
10. When a Poisoned TLP Write Request is forwarded to the PCI/PCI-X Bus and the bridge detects PCI_PERR# asserted, the following occurs:
    - **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set
    - **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set
    - Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *First Error Pointer* is inactive

8.2.2.2 Received ECRC Error

When a TLP is received and the bridge detects an ECRC error, the following occurs:

1. Transaction is dropped.
2. **Secondary Status** register *Secondary Detected Parity Error* bit is set.
3. **Uncorrectable Error Status** register *ECRC Error Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared and the *First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *ECRC Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *ECRC Error Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *ECRC Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *ECRC Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *ECRC Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *ECRC Error Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *ECRC Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.3 PCI/PCI-X Uncorrectable Data Errors

The following sections describe error handling when forwarding Non-Poisoned PCI Express transactions to the PCI/PCI-X Bus, and an Uncorrectable PCI/PCI-X error is detected.

Posted Writes

When the PEX 8114 detects PCI_PERR# asserted on the PCI/PCI-X primary interface while forwarding a Non-Poisoned Posted Write transaction from the PCI Express interface, the following occurs:

1. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *PERR# Assertion Detected Severity*
5. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity*
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.
8. After the error is detected, the remainder of the data is forwarded.

Non-Posted Writes

When the PEX 8114 detects PCI_PERR# asserted on the PCI/PCI-X primary interface while forwarding a Non-Poisoned Non-Posted Write transaction from the PCI Express interface, the following occurs:

1. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
2. PCI Express Completion with Unsupported Request status is generated.
3. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *PERR# Assertion Detected Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

When the Target signals Split Response, the bridge terminates the transaction as it would for a Split Request that does not contain an error and takes no further action. If the returned Split Completion is a Split Completion Error message, the bridge returns a PCI Express Completion with Unsupported Request status to the requester.

Immediate Reads

When the PEX 8114 forwards a Read request (I/O, Memory, or Configuration) from the PCI Express interface and detects an Uncorrectable Data error on the primary bus while receiving an Immediate or Split Response from the completer, the following occurs:

1. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
2. **PCI Status** register *Detected Parity Error* bit is set.
3. PCI_PERR# is asserted on the secondary interface if the **PCI Command** register *Parity Error Response Enable* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Data Error Severity*
7. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8114 continues to fetch data until the Byte Count is satisfied or the Target ends the transaction. When the bridge creates the PCI Express Completion, it forwards the Completion with Successful Completion status and poisons the TLP. For PCI-X, an Uncorrectable Data error on a Split Response does not affect handling of subsequent Split Completions.

PCI-X Split Read Completions

When the bridge forwards a Non-Poisoned Read Completion from PCI Express to PCI-X and detects PCI_PERR# asserted by the PCI-X Target, the following occurs:

1. Bridge continues to forward the remainder of the Split Completion.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected Status* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. PCI_SERR# is asserted on the PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *PERR# Assertion Detected Severity*
5. PCI_INTA# is asserted on the PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity*
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

8.2.2.4 PCI/PCI-X Address/Attribute Errors

When the PEX 8114 forwards transactions from PCI Express to PCI/PCI-X, the Target asserts SERR# to report PCI Address errors. The PEX 8114 ignores the SERR# assertion, and allows the PCI Central Resource to service the error.

8.2.2.5 PCI/PCI-X Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express to PCI/PCI-X results in a Master Abort on the PCI/PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **PCI Status** register *Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Master Abort Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.6 PCI/PCI-X Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express to PCI/PCI-X results in a Master Abort on the PCI/PCI-X Bus, the following occurs:

1. Completion with Unsupported Request status is returned on the PCI Express interface.
2. **PCI Status** register *Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Master Abort Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.7 PCI-X Master Abort on Split Completion

When a Split Completion forwarded from PCI Express to PCI-X results in a Master Abort on the PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **PCI Status** register *Received Master Abort* bit is set.
3. **PCI-X Status** register *Split Completion Discarded* bit is set.
4. **Secondary Uncorrectable Error Status** register *Master Abort on Split Completion Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Master Abort on Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Master Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Master Abort on Split Completion Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Master Abort on Split Completion Severity*
7. PCI_INTA# is asserted on the PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Master Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Master Abort on Split Completion Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Master Abort on Split Completion Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Master Abort on Split Completion Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Master Abort on Split Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.8 PCI/PCI-X Target Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express to PCI/PCI-X results in a Target Abort on the PCI/PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **PCI Status** register *Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Target Abort Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.9 PCI/PCI-X Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express to PCI/PCI-X results in a Target Abort on the PCI/PCI-X Bus, the following occurs:

1. Completion with Completer Abort status is returned on the PCI Express interface.
2. **PCI Status** register *Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Target Abort Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.10 PCI-X Target Abort on Split Completion

When a Split Completion forwarded from PCI Express to PCI-X results in a Target Abort on the PCI-X Bus, the following occurs:

1. Entire transaction is discarded.
2. **PCI Status** register *Received Target Abort* bit is set.
3. **PCI-X Bridge Status** register *Split Completion Discarded* bit is set.
4. **Secondary Uncorrectable Error Status** register *Target Abort on Split Completion Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Target Abort on Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Target Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Target Abort on Split Completion Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Target Abort on Split Completion Severity*
7. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Target Abort on Split Completion Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Target Abort on Split Completion Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Target Abort on Split Completion Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Target Abort on Split Completion Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Target Abort on Split Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.11 Unexpected Completion Received

When a Completion targeted at the bridge is received on the PCI Express interface, without a corresponding outstanding request, the following occurs:

1. Entire transaction is discarded.
2. **PCI-X Secondary Status** register *Unexpected Split Completion* bit is set.
3. **Uncorrectable Error Status** register *Unexpected Completion Status* bit is set.
4. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *Uncorrectable First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared and the *Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Unexpected Completion Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Unexpected Completion Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Unexpected Completion Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Unexpected Completion Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unexpected Completion Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unexpected Completion Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Unexpected Completion Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.12 Received Request Unsupported

When a Non-Posted request, targeted to the PEX 8114, is received on the PCI Express interface and the bridge cannot complete the request, the following occurs:

1. Completion with Unsupported Request Completion status is returned to the requester.
2. **Uncorrectable Error Status** register *Unsupported Request Error Status* bit is set.
3. TLP Header is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *Uncorrectable First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Unsupported Request Error Mask* bit is cleared and the *Uncorrectable First Error Pointer* is inactive.
4. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Unsupported Request Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Unsupported Request Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Unsupported Request Error Severity*
5. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Unsupported Request Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Unsupported Request Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unsupported Request Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unsupported Request Error Severity*
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Unsupported Request Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.2.2.13 Link Training Error

When a PCI Express Link Training error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Training Error Status* bit is set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Training Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Training Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Training Error Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Training Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Training Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Training Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Training Error Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Training Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.14 Data Link Protocol Error

When a PCI Express Data Link Protocol error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Data Link Protocol Error Status* bit is set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Data Link Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Data Link Protocol Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Data Link Protocol Error Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Data Link Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Data Link Protocol Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Data Link Protocol Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Data Link Protocol Error Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Data Link Protocol Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.15 Flow Control Protocol Error

When a PCI Express Flow Control Protocol error is detected, the following occurs:

1. **Uncorrectable Error Status** register *Flow Control Protocol Error Status* bit is set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Flow Control Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Flow Control Protocol Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Flow Control Protocol Error Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Flow Control Protocol Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Flow Control Protocol Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Flow Control Protocol Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Flow Control Protocol Error Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Flow Control Protocol Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.2.2.16 Receiver Overflow

When a PCI Express Receiver Overflow is detected, the following occurs:

1. **Uncorrectable Error Status** register *Receiver Overflow Status* bit is set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Receiver Overflow Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Receiver Overflow Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Receiver Overflow Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Receiver Overflow Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Receiver Overflow Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Receiver Overflow Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Receiver Overflow Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Receiver Overflow Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.2.17 Malformed TLP

When a PCI Express Malformed TLP is received, the following occurs:

1. **Uncorrectable Error Status** register *Malformed TLP Status* bit is set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Malformed TLP Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Malformed TLP Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Malformed TLP Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Malformed TLP Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Malformed TLP Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Malformed TLP Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Malformed TLP Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Malformed TLP Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.3 Reverse Transparent Bridge PCI/PCI-X Originating Interface (Primary to Secondary)

This section describes error support for transactions that cross the bridge if the originating side is the PCI/PCI-X Bus, and the destination side is PCI Express. The PEX 8114 supports TLP poisoning as a transmitter to allow proper forwarding of Parity errors that occur on the PCI/PCI-X interface. Posted Write data received on the PCI/PCI-X interface with bad parity is forwarded to the PCI Express interface as Poisoned TLPs.

Table 8-6 defines the error forwarding requirements for Uncorrectable Data errors that the PEX 8114 detects when a transaction targets the PCI Express interface.

Table 8-7 defines the bridge behavior on a PCI/PCI-X Delayed transaction forwarded by the PEX 8114 to the PCI Express interface as a Memory Read or I/O Read/Write request, and the PCI Express interface returns a Completion with UR or CA status for the request.

Table 8-6. Error Forwarding Requirements for Uncorrectable Data Errors

Received PCI/PCI-X Error	Forwarded PCI Express Error
Write with Parity error	Write request with Poisoned TLP
Read Completion or Split Read Completion with Parity error in Data phase	Read Completion with Poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write Completion with Completer Abort Status
Split Completion message with Uncorrectable Data error in Data phase	

Table 8-7. Bridge Behavior on PCI/PCI-X Delayed Transaction Forwarded by PEX 8114

PCI Express Completion Status	PCI/PCI-X Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory or I/O Read)	Target Abort	Normal Completion, returns FFFF_FFFFh
Unsupported Request (on I/O Write)		Normal Completion
Completer Abort	Target Abort	

8.2.3.1 Received PCI/PCI-X Errors

Uncorrectable Data Error on Posted Write

When the PEX 8114 detects an Uncorrectable Data error on the PCI/PCI-X primary interface for a Posted Write transaction that crosses the bridge, the following occurs:

1. PCI_PERR# is asserted if the **PCI Command** register *Parity Error Response Enable* bit is set.
2. **PCI Status** register *Detected Parity Error* bit is set.
3. Posted Write transaction is forwarded to the PCI Express interface as a Poisoned TLP.
4. **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
5. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
6. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
7. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Data Error Severity*
8. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity*
9. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
10. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Data Error on Non-Posted Write in Conventional PCI Mode

When a Non-Posted Write is addressed allowing it to cross the bridge, and the PEX 8114 detects an Uncorrectable Data error on the PCI interface, the following occurs:

1. **PCI Status** register *Detected Parity Error* bit is set.
2. When the **PCI Command** register *Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to the PCI Express interface. PCI_PERR# is asserted on the PCI Bus.

   When the *Parity Error Response Enable* bit is not set, the data is forwarded to the PCI Express interface as a Poisoned TLP. The **Secondary Status** register *Secondary Master Data Parity Error* bit is set if the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set. PCI_PERR# is not asserted on the PCI Bus.
3. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
4. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Data Error Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Data Error on Non-Posted Write in PCI-X Mode

When a Non-Posted Write is addressed allowing it to cross the bridge, and the PEX 8114 detects an Uncorrectable Data error on the PCI-X interface, the following occurs:

1. **PCI Status** register *Detected Parity Error* bit is set.
2. PEX 8114 signals a Data transfer for Non-Posted Write transactions. If there is an Uncorrectable Data error, the transaction is discarded.
3. When the **PCI Command** register *Parity Error Response Enable* bit is set, PCI_PERR# is asserted on the PCI-X Bus.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Data Error Severity*
7. PCI_INTA# is asserted on the PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8114 forwards a Non-Poisoned or Poisoned Read Completion from PCI Express to PCI, and it detects PCI_PERR# asserted by the PCI Master, the following occurs:

1. Remainder of the Completion is forwarded.
2. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set.
3. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. PCI_SERR# is asserted on the PCI Bus, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *PERR# Assertion Detected Severity*
5. PCI_INTA# is asserted on the PCI Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity*
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

If the PEX 8114 forwards a Poisoned Read Completion from PCI Express to PCI, the PEX 8114 proceeds with the above actions when it detects PCI_PERR# asserted by the PCI Master; however, an Error message is not generated on the PCI Express interface.

Uncorrectable Data Error on PCI-X Split Read Completions

When the PEX 8114 detects an Uncorrectable Data error on the PCI-X interface while receiving a Split Read Completion that crosses the bridge, the following occurs:

1. PCI_PERR# is asserted if the **PCI Command** register *Parity Error Response Enable* bit is set.
2. **PCI Status** register *Detected Parity Error* bit is set.
3. Split Read Completion transaction is forwarded to the PCI Express interface as a Poisoned TLP.
4. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
5. **Secondary Uncorrectable Error Status** register *Uncorrectable Data Error Status* bit is set.
6. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
7. PCI_SERR# is asserted on the PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Data Error Severity*
8. PCI_INTA# is asserted on the PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Data Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Data Error Severity*
9. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
10. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Data Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Address Error

When the PEX 8114 detects an Uncorrectable Address error and Parity error detection is enabled by way of the **PCI Command** register *Parity Error Response Enable* bit, the following occurs:

1. Transaction is terminated with a Target Abort and discarded.
2. **PCI Status** register *Detected Parity Error* bit is set, independent of the **PCI Command** register *Parity Error Response Enable* bit value.
3. **PCI Status** register *Signaled Target Abort* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Address Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Address Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Address Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Address Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Address Error Severity*
7. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Address Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Address Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Address Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Address Error Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Address Error Mask* bit is clear and the *SERR# Enable* bit is set.

Uncorrectable Attribute Error

When the PEX 8114 detects an Uncorrectable Attribute error and Parity error detection is enabled by way of the **PCI Command** register *Parity Error Response Enable* bit, the following occurs:

1. Transaction is terminated with a Target Abort and discarded.
2. **PCI Status** register *Detected Parity Error* bit is set, independent of the **PCI Command** register *Parity Error Response Enable* bit value.
3. **PCI Status** register *Signaled Target Abort* bit is set.
4. **Secondary Uncorrectable Error Status** register *Uncorrectable Attribute Error Status* bit is set.
5. Transaction command, attributes, and address are logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Attribute Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Attribute Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Attribute Error Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Attribute Error Severity*
7. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Attribute Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Attribute Error Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Attribute Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Attribute Error Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Attribute Error Mask* bit is clear and the *SERR# Enable* bit is set.

8.2.3.2 Unsupported Request (UR) Completion Status

The PEX 8114 provides two methods for handling a PCI Express Completion received with Unsupported Request (UR) status in response to a request originated by the PCI/PCI-X interface. The **Bridge Control** register *Master Abort Mode* bit controls the response. In either case, the **Secondary Status** register *Secondary Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI/PCI-X compatibility mode, and a UR is not considered an error. When a Read transaction initiated on the PCI/PCI-X Bus results in the return of a Completion with UR status, the PEX 8114 returns FFFF_FFFFh to the originating Master and asserts PCI_TRDY# to terminate the Read transaction normally on the originating interface. When a Non-Posted Write transaction results in a Completion with UR status, the PEX 8114 asserts PCI_TRDY# to complete the Write transaction normally on the originating bus and discards the Write data.

Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8114 signals a Target Abort to the originating Master of an upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a Completion with UR status. Additionally, the **PCI Status** register *Signaled Target Abort* bit is set.

8.2.3.3 Completer Abort Completion Status

When the PEX 8114 receives a Completion with Completer Abort (CA) status on the PCI Express secondary interface, in response to a forwarded Non-Posted PCI/PCI-X transaction, the **Secondary Status** register *Secondary Received Target Abort* bit is set. A CA response results in a Delayed Transaction Target Abort or Split Completion Target Abort Error message on the PCI/PCI-X Bus. The PEX 8114 provides data to the requesting PCI/PCI-X agent, up to the point where data was successfully returned from the PCI Express interface, then signals Target Abort. The **PCI Status** register *Signaled Target Abort* bit is set when signaling Target Abort to a PCI/PCI-X agent.

8.2.3.4 Split Completion Errors

Split Completion Message with Completer Errors

A transaction originating from the PCI Express interface and requiring a Completion can be forwarded to the PCI-X interface where the Target (completer) responds with Split Response. If the completer encounters a condition that prevents the successful execution of a Split Transaction, the completer must notify the requester of the abnormal condition by returning a Split Completion message with the Completer Error class. If the bridge responds with Completer Abort status, it sets the **Secondary Status** register *Signaled Target Abort* bit.

Table 8-8 defines the abnormal conditions and the bridge's response to the Split Completion message. Each is described in the sections that follow.

Table 8-8. Abnormal Conditions and Bridge Response to Split Completion Messages

PCI-X Split Completion Message	Completer Error Code		Bit Set in PCI Status Register	Bit Set in Secondary Uncorrectable Error Status Register	PCI Express Completion Status
	Class	Index			
Master Abort	1h	00h	*Received Master Abort*	*Received Master Abort*	Unsupported Request
Target Abort	1h	01h	*Received Target Abort*	*Received Target Abort*	Completer Abort
Uncorrectable Write Data Error	1h	02h	*Master Data Parity Error*	*PERR# Assertion Detected*	Unsupported Request
Byte Count Out of Range	2h	00h	***None***	***None***	Unsupported Request
Uncorrectable Split Write Data Error	2h	01h	*Master Data Parity Error*	*PERR# Assertion Detected*	Unsupported Request
Device-Specific Error	2h	8Xh	***None***	***None***	Completer Abort

Split Completion Message with Master Abort

When a bridge receives a Split Completion message indicating Master Abort, the following occurs:

1. Completion with Unsupported Request status is returned to the requester.
2. **PCI Status** register *Received Master Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Master Abort Status* bit is set.
4. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Master Abort Status Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Master Abort Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Master Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Master Abort Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Master Abort Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *Received Master Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

Split Completion Message with Target Abort

When a bridge receives a Split Completion message indicating Target Abort, the following occurs:

1. Completion with Completer Abort status is returned to the requester.
2. **PCI Status** register *Received Target Abort* bit is set.
3. **Secondary Uncorrectable Error Status** register *Received Target Abort* bit is set.
4. **Secondary Status** register *Signaled Target Abort* bit is set.
5. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
6. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Received Target Abort Severity*
7. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Received Target Abort Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Received Target Abort Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Received Target Abort Severity*
8. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
9. **PCI Status** register *Signaled System Error* bit is set if the *Received Target Abort Mask* bit is cleared and the *SERR# Enable* bit is set.

Split Completion Message with Uncorrectable Write Data Error or Uncorrectable Split Write Data Error

When a bridge receives a Split Completion message indicating an Uncorrectable Write Data error or Uncorrectable Split Write Data error, the following occurs:

1. Completion with Unsupported Request status is returned to the requester.
2. **PCI Status** register *Master Data Parity Error* bit is set if the **PCI Command** register *Parity Error Response Enable* bit is set.
3. **Secondary Uncorrectable Error Status** register *PERR# Assertion Detected* bit is set.
4. TLP Header of the original request is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
5. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *PERR# Assertion Detected Severity*
6. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *PERR# Assertion Detected Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *PERR# Assertion Detected Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *PERR# Assertion Detected Severity*
7. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
8. **PCI Status** register *Signaled System Error* bit is set if the *PERR# Assertion Detected Mask* bit is clear and the *SERR# Enable* bit is set.

Split Completion Message with Byte Count Out of Range

When a bridge receives a Split Completion message indicating a Byte Count Out of Range error, a Completion with Unsupported Request status is returned to the requester.

Split Completion Message with Device-Specific Error

When a bridge receives a Split Completion message indicating a Device-Specific error, a Completion with Completer Abort status is returned to the requester.

Corrupted or Unexpected Split Completion

When a bridge receives a corrupted or unexpected Split Completion, the following occurs:

1. **PCI-X Bridge Status** register *Unexpected Split Completion Status* bit is set.
2. **Secondary Uncorrectable Error Status** register *Unexpected Split Completion Error Status* bit is set.
3. TLP Header of the corrupt or unexpected Split Completion is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Unexpected Split Completion Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
4. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Unexpected Split Completion Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Unexpected Split Completion Mask* bit is clear AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Unexpected Split Completion Severity*
5. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Unexpected Split Completion Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Unexpected Split Completion Mask* bit is clear AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unexpected Split Completion Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Unexpected Split Completion Severity*
6. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
7. **PCI Status** register *Signaled System Error* bit is set if the *Unexpected Split Completion Mask* bit is clear and the *SERR# Enable* bit is set.

Data Parity Error on Split Completion Messages

When a bridge detects a Data error during the Data phase of a Split Completion message, the following occurs:

1. **Secondary Uncorrectable Error Status** register *Uncorrectable Split Completion Message Data Error Status* bit is set.
2. TLP Header of the Split Completion is logged in the **Secondary Header Log** register and the **FECh** register Secondary Uncorrectable Error Pointer is updated if the **Secondary Uncorrectable Error Mask** register *Uncorrectable Split Completion Message Data Error Mask* bit is cleared and the *Secondary Uncorrectable First Error Pointer* is inactive.
3. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Split Completion Message Data Error Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Split Completion Message Data Error Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Uncorrectable Split Completion Message Data Error Severity*
4. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Secondary Uncorrectable Error Severity** register *Uncorrectable Split Completion Message Data Error Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Secondary Uncorrectable Error Mask** register *Uncorrectable Split Completion Message Data Error Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Split Completion Message Data Error Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Uncorrectable Split Completion Message Data Error Severity*
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the *Uncorrectable Split Completion Message Data Error Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.4 Reverse Transparent Bridge Timeout Errors

8.2.4.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted request if a Completion does not arrive within a reasonable time. Bridges, when acting as Initiators on the PCI Express interface on behalf of internally generated requests or when forwarding requests from a secondary interface, behave as endpoints for requests of which they assume ownership. If a Completion timeout is detected and the link is up, the PEX 8114 responds as if a Completion with Unsupported Request status was received, and the following occurs:

1. **Uncorrectable Error Status** register *Completion Timeout Status* bit is set.
2. TLP Header of the original request is logged in the **Header Log** register and the **Advanced Error Capabilities and Control** register *First Error Pointer* is updated if the **Uncorrectable Error Mask** register *Completion Timeout Mask* bit is cleared and the *First Error Pointer* is inactive.
3. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Secondary Uncorrectable Error Severity** register *Completion Timeout Severity* bit's severity, if the following conditions are met:
   - **Secondary Uncorrectable Error Mask** register *Completion Timeout Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Completion Timeout Severity*
4. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Completion Timeout Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Completion Timeout Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Completion Timeout Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Completion Timeout Severity*
5. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
6. **PCI Status** register *Signaled System Error* bit is set if the *Completion Timeout Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.4.2 PCI Delayed Transaction Timeout Errors

The PEX 8114 has Delayed Transaction Discard Timers for each queued delayed transaction. If a Delayed Transaction timeout is detected, the following occurs:

1. **Bridge Control** register *Discard Timer Status* bit and **Secondary Uncorrectable Error Status** register *Delayed Transaction Discard Timer Expired Status* bit are set.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus, depending on the **Uncorrectable Error Severity** register *Delayed Transaction Discard Timer Expired Severity* bit's severity, if the following conditions are met:
   - **Uncorrectable Error Mask** register *Delayed Transaction Discard Timer Expired Mask* bit is cleared AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set, the **Root Control** register *System Error on Fatal Error Enable* or *System Error on Non-Fatal Error Enable* bit is set, and both bits match the *Delayed Transaction Discard Timer Expired Severity*
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, depending on the **Uncorrectable Error Severity** register *Delayed Transaction Discard Timer Expired Severity* bit's severity, if the following conditions are met:
   - **Command** register *Interrupt Disable* bit is cleared AND
   - **Uncorrectable Error Mask** register *Delayed Transaction Discard Timer Expired Mask* bit is cleared AND
   - **Root Error Command** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Delayed Transaction Discard Timer Expired Severity* AND EITHER
   - **PCI Command** register *SERR# Enable* bit is set OR
   - **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set and matches the *Delayed Transaction Discard Timer Expired Severity*
4. **Device Status** register *Fatal Error Detected* or *Non-Fatal Error Detected* bit is set.
5. **PCI Status** register *Signaled System Error* bit is set if the *Delayed Transaction Discard Timer Expired Mask* bit is cleared and the *SERR# Enable* bit is set.

8.2.5 Reverse Transparent Bridge PCI Express Error Messages

PCI Express devices can transmit Error messages when detecting errors that compromise system integrity. When the PEX 8114 receives Error messages on the secondary PCI Express interface, the following occurs:

1. **Secondary Status** register *Received System Error* bit is set if a Non-Fatal (ERR_NONFATAL) or Fatal (ERR_FATAL) Error message is received.
2. PCI_SERR# is asserted on the PCI/PCI-X Bus when one of the following conditions occur:
   - **Root Control** register *System Error on Correctable Error Enable* bit is set and a Correctable Error message (ERR_COR) is received
   - **Root Control** register *System Error on Non-Fatal Error Enable* bit is set and a Non-Fatal Error message (ERR_NONFATAL) is received
   - **Root Control** register *System Error on Fatal Error Enable* bit is set and a Fatal Error message (ERR_FATAL) is received
   - **PCI Command** and **Bridge Control** register *SERR# Enable* bits are set and a Non-Fatal Error message (ERR_NONFATAL) is received
   - **PCI Command** and **Bridge Control** register *SERR# Enable* bits are set and a Fatal Error message (ERR_FATAL) is received
3. PCI_INTA# is asserted on the PCI/PCI-X Bus –OR– an MSI is transmitted if the **MSI Control** register *MSI Enable* bit is set, when one of the following conditions occur:
   - **Root Error Command** register *Correctable Error Reporting Enable* bit is set and a Correctable Error message (ERR_COR) is received
   - **Root Error Command** register *Non-Fatal Error Reporting Enable* bit is set and a Non-Fatal Error message (ERR_NONFATAL) is received
   - **Root Error Command** register *Fatal Error Reporting Enable* bit is set and a Fatal Error message (ERR_FATAL) is received

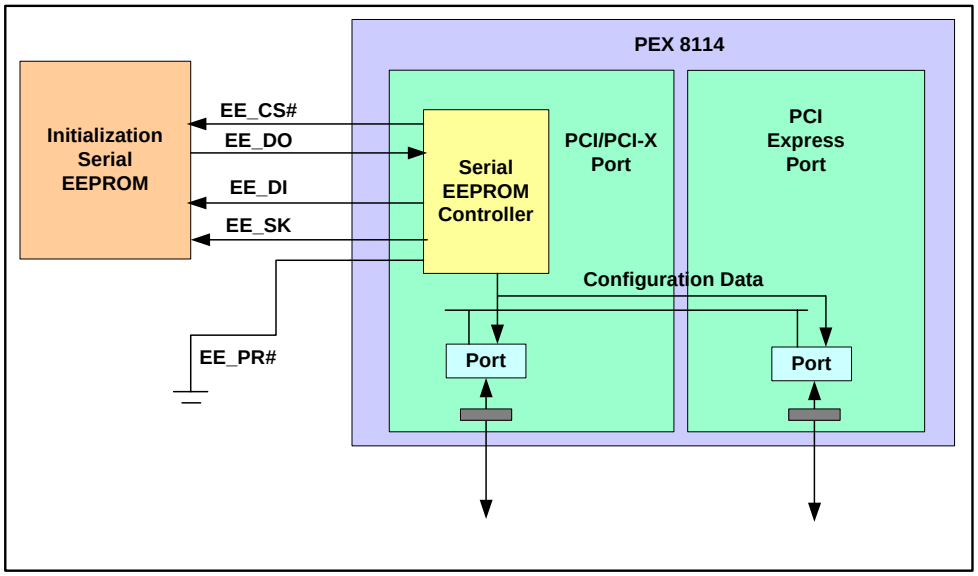
Chapter 9 Serial EEPROM

9.1 Introduction

The on-bridge Serial EEPROM Controller is contained in the PEX 8114 PCI/PCI-X port, as illustrated in Figure 9-1. The controller performs a serial EEPROM download when:

- A serial EEPROM is present, as indicated by the EE_PR# Strap ball = Low, and
- The Configuration registers are reset to their default values.

Figure 9-1. Serial EEPROM Connections to PEX 8114



9.2 Configuration Data Download

The Serial EEPROM Controller generates an EE_SK signal by dividing the PCI_CLK by 16, resulting in a shift clock frequency up to 8.3 MHz. The Serial EEPROM Controller reads a total of 1,004 bytes, from the serial EEPROM, which represents all data necessary to initialize the PEX 8114 registers. The serial EEPROM Memory Map reflects the basic device register map. A detailed description of the serial EEPROM Memory maps is provided in Appendix A, "Serial EEPROM Map."

Note: For a PCI-X clock greater than 66 MHz, a 10-MHz serial EEPROM is needed. For clock rates of 66 MHz and lower, a 5-MHz serial EEPROM is sufficient.

When registers are modified through the serial EEPROM load, the serial EEPROM must retain data for all registers. Registers that must be modified away from their power-on default states can be changed by loading the necessary modified values in the serial EEPROM, at the location that corresponds to that register's value in the serial EEPROM map. Registers that are not intended to be modified from their default values by the serial EEPROM load must be located within the serial EEPROM loaded with the default value.

Serial Peripheral Interface EEPROMs, from 1 KB up to 64 KB sizes, are supported. A minimum of a 1-KB serial EEPROM is required to support the PEX 8114 register load. If a serial EEPROM larger than 1 KB is used, the additional space remains unused by the PEX 8114 register load resources and is used as a general-purpose serial EEPROM. The register load data starts at location 0 in the serial EEPROM and the serial EEPROM data is loaded into the registers, in ascending sequence, and mapped according to the register assignment tables in Appendix A, "Serial EEPROM Map." The table is arranged with the left column listing the Configuration Space register (CSR) addresses and the right column listing the serial EEPROM address to load to modify the CSR.

In a few instances, the value of a single PCI-defined or PLX-specific CSR must be stored in two separate internal registers within the PEX 8114. When writing a CSR using PCI-type Configuration Writes – Memory-Mapped Writes or Pointer Indirect Writes – the internal state machines associated with the Write, place the data in both internal registers, without intervention. When loading a CSR location that contains two internal copies of the register using serial EEPROM loads, the value must be specifically loaded into both internal registers (*that is*, two distinct Writes to two distinct locations are required). Therefore, in certain instances, when creating the serial EEPROM image, the value needed in a CSR must be placed in two address locations in the serial EEPROM, allowing two distinct Writes to occur. The required registers for this procedure are indicated in the register assignment tables in Appendix A, "Serial EEPROM Map," by having two serial EEPROM addresses listed in a row that has only one corresponding CSR address. In cases where two serial EEPROM addresses must be loaded to modify one CSR location, the Data loaded into both serial EEPROM addresses ***must*** be identical or the PEX 8114's operation is undefined.

During the serial EEPROM download, the controller checks for a valid Class Code and terminates the download if a value other than 060400h is used.

While downloading data, the PEX 8114 generates a CRC value from the data read. When the serial EEPROM download is completed, the generated CRC value is compared to a CRC value stored in the last DWord location of the serial EEPROM. For serial EEPROMs, the CRC value is located at serial EEPROM byte offset 03ECh. All CRC are calculated in DWords and the CRC value is also a DWord. The CRC is calculated, starting at location 0, and is calculated through one location below where the CRC is stored. The CRC polynomial is as follows:

$$G(x) = x^{32} + x^{31} + x^{30} + x^{28} + x^{27} + x^{25} + x^{24} + x^{22} + x^{21} + x^{20} + x^{16} + x^{10} + x^{9} + x^{6} + 1$$

A C code sample used to generate the CRC is provided in Appendix B, "Sample C Code Implementation of CRC Generator."

When the CRC values match, the PEX 8114 sets the **Serial EEPROM Status and Control** register *Serial EEPROM Present*[17:16] value to 01b (serial EEPROM download complete and serial EEPROM CRC check is correct).

When the CRC check fails, the PEX 8114 sets all the registers for the port to their default values, and sets the *Serial EEPROM Present*[17:16] bits to 11b to indicate failure.

Disable the CRC check by loading a value of 1 in **Serial EEPROM Status** register *CRC Disable* bit (offset 260h[21]) during the serial EEPROM load.

It is the responsibility of system software to detect that the serial EEPROM download is completed without error.

Serial EEPROM register initialization data, as well as user-accessible, general-purpose space located above the register initialization data, can be modified by Writes to the PEX 8114 PLX-Specific Serial EEPROM registers. The **Serial EEPROM Status and Control** register (offset 260h) contains Status and Control bits that set the Read/Write address and cause status data to be written to or read from the serial EEPROM. There are 14 Address bits – bits [12:0] and *Extended Address* bit 20. The addressing is at a DWord address (rather than a byte offset), which allows 16-KB DWords or 64 KB to be addressed. The **Serial EEPROM Buffer** register (offset 264h) contains data to be written to, or the most recent data read from, the serial EEPROM. (Refer to Register 14-73 and Register 14-74, respectively, for further details.)

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Chapter 10 Interrupt Handler

10.1 Introduction

The PEX 8114 includes two types of interrupts:

- *Conventional PCI Interrupt,* PCI/PCI-X PCI_INT[D:A]#, which are PEX 8114 I/O balls on the PCI/PCI-X Bus and their analogous PCI Express Assert_Int*x* Virtual Interrupt messages
- *Message Signal Interrupt* (MSI), which is conveyed with Memory Write transactions

In Forward Transparent Bridge mode, Conventional PCI interrupts generated external to the bridge and asserted on the bridge INT*x* balls, when enabled, are converted by the PEX 8114 to Virtual Interrupt messages and transmitted upstream on the PCI Express interface. MSI interrupts are passed through the PEX 8114 from PCI/PCI-X to PCI Express. Interrupts generated by sources internal to the bridge can be converted to MSI interrupt messages or Assert_IntA.

In Reverse Transparent Bridge mode, the Virtual Interrupt messages received on the PCI Express interface are converted to Conventional PCI interrupt signals and driven on the PCI_INT[D:A]# balls. MSI interrupts are passed through the PEX 8114, from PCI Express to PCI/PCI-X. Interrupts generated by sources internal to the bridge can be converted to MSI interrupt or Assert_IntA and Deassert_IntA messages.

10.2 Interrupt Handler Features

Interrupt handler features are as follows:

- Senses internal interrupt events
- Generates Virtual Interrupt messages from Conventional PCI PCI_INT[D:A]# balls
- Drives Conventional PCI_INT[D:A]# balls from Virtual Interrupt messages
- Signals interrupts through Virtual INTA# signaling, PCI_INT[D:A]# signal Conventional PCI assertion, or MSI

10.3 Events that Cause Interrupts

Events internal to the PEX 8114 that cause interrupts are as follows:

- Hot Plug events
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Presence Detect Changed
  - Command Completed
- Internal Error FIFO overflow
- Power Management Events
- PCI Express Egress Credit Update Timeout

Interrupts can also be generated if the **Root Error Command** register (offset F94h), is implemented by software in Reverse Transparent Bridge mode. Conditions that cause these interrupts are as follows:

- Correctable error message is received by the PEX 8114 from downstream and the **Root Error Command** register *Correctable Error Reporting Enable* bit is set (offset F94h[0]=1)
- Non-Fatal Error message is received by the PEX 8114 from downstream and the **Root Error Command** register *Non-Fatal Error Reporting Enable* bit is set (offset F94h[1]=1)
- Fatal error message is received by the PEX 8114 from downstream and the **Root Error Command** register *Fatal Error Reporting Enable* bit is set (offset F94h[2]=1)
- Correctable error is detected by the PEX 8114, the **Command** register *Interrupt Disable* bit is ***not*** set, and the **Root Error Command** register *Correctable Error Reporting Enable* bit is set (offset 04h[10]=0 and offset F94h[0]=1, respectively)
- Non-Fatal error is detected by the PEX 8114, the **Command** register *Interrupt Disable* bit is ***not*** set and the **Root Error Command** register *Non-Fatal Error Reporting Enable* bit is set (offset 04h[10]=0 and offset F94h[1]=1, respectively)
- Fatal error is detected by the PEX 8114 the is not set in the **Command** register *Interrupt Disable* bit is ***not*** set and the **Root Error Command** register *Fatal Error Reporting Enable* bit is set (offset 04h[10]=0 and offset F94h[2]=1, respectively)

Interrupt requests proceed to the Interrupt Generator module, which sets the **Status** register *Interrupt Status* bit. Setting the status bit causes an INTA# interrupt or MSI to generate, depending on which interrupt is enabled.

INTA# and MSI interrupt generation are mutually exclusive.

10.4 INT*x*# Signaling

In Forward Transparent Bridge mode, the PEX 8114 converts PCI_INT*x*# ball interrupts to virtual PCI Express INT*x*# signaled interrupts. PCI/PCI-X interrupts appearing on PCI_INT*x*# lines are converted to PCI Express-compatible packets (Assert_INT*x*# and Deassert_INT*x*# signaled interrupts) and transmitted to the upstream port.

In Reverse Transparent Bridge mode, the PEX 8114 converts PCI Express virtual INT*x*# signaled interrupts to PCI_INT*x*# interrupts. Assert_INT*x*# and Deassert_INT*x*# signaled interrupts from the PCI Express port are converted to the PCI_INT*x*# ball interrupts.

The PEX 8114 supports the *PCI r3.0* **Interrupt Pin** and **Interrupt Line** registers (offset 3Ch[15:8 and 7:0], respectively), as well as the *PCI r3.0* **Command** register *Interrupt Disable* and **Status** register *Interrupt Status* bits (offset 04h[10, 19], respectively).

Although the *PCI Express r1.0a* provides INT[D:A]# for PCI_INT[D:A]# interrupt signaling, the PEX 8114 uses only PCI_INTA# for internal Interrupt message generation.

When MSI is disabled (**Message Signaled Interrupt Control** register *MSI Enable* bit is cleared to 0) and INTA#-type interrupts are not disabled (**Command** register *Interrupt Disable* bit value is 0), interrupt requests from a defined event generate INTA#-type interrupts.

When MSI is enabled, the interrupt requests from a defined event generate MSI type interrupts, regardless of the **Command** register *Interrupt Disable* bit state.

When PCI_INTA# interrupts are enabled and there is an interrupt request from interrupt sources internal to the PEX 8114, the **Status** register *Interrupt Status* bit is set.

- In Forward Transparent Bridge mode, when the *Interrupt Status* bit is set by an interrupt source internal to the PEX 8114, an Assert_INTA# message is transmitted on the PCI Express interface. When an external PCI-X device asserts the INT*x*# input to the PEX 8114, the *Interrupt Status* bit is not set; however, the Assert_INT*x*# message is translated. When the external PCI-X device later de-asserts the PCI_INT*x*# input, the Deassert_INT*x*# message is transmitted without action from the host software.
- In Reverse Transparent Bridge mode, when the *IInterrupt Status* bit is set, the PCI_INTA# signal is asserted on the PCI/PCI-X Bus.

When an interrupt source internal to the PEX 8114 causes an interrupt to be transmitted to the PCI Express Root Complex, the Host software reads and clears the event status after servicing the interrupt.

When an interrupt source internal to the PEX 8114 causes an interrupt, the PCI device hardware clears the **Status** register *Interrupt Status* bit when all event status bits are cleared, and transmits a Deassert_INTA# message on the PCI Express interface or de-asserts PCI_INTA# on the PCI/PCI-X Bus.

10.5 Message Signaled Interrupts (MSI)

A scheme supported by PEX 8114 is the MSI, which is optional for *PCI r3.0* devices, but required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSI are edge-triggered interrupts. If MSI is enabled and the interrupt status bit is set, the module generates an MSI.

MSI and INT[D:A]# interrupt generation are mutually exclusive.

10.5.1 MSI Capability Structure

Table 10-1 defines the Message Capability structure required for MSI, and is implemented in the Interrupt Generator module.

The Capability Pointer register (defined in the *PCI r3.0*) contains the pointer to the Capability ID. The **Message Address**, **Message Upper Address**, and **Message Data** registers are located at offsets Capability Pointer + 4h, Capability Pointer + 8h, and Capability Pointer + Ch, respectively.

Table 10-1. Message Signaled Interrupt Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Message Signaled Interrupt Control		Next Capability Pointer (58h if PCI-X; 68h if PCI Express)	Capability ID (05h)	48h
Lower Message Address[31:0]				4Ch
Upper Message Address[63:32]				50h
Reserved		Message Data		54h

10.5.2 MSI Operation

At configuration, system software traverses the capability list of the function. If a Capability ID of 05h is found, the function implements MSI. System software reads the **Message Signaled Interrupt Capability List** register to determine whether the PEX 8114 is set up to support MSI.

Because the PEX 8114 supports only one message for MSI, the *Multiple Message Enable* and *MSI 64-Bit Address Capable* fields are always 000b.

System software initializes the *MSI 64-Bit Address Capable* field.

- When set, the message address field is 64 bits
- When not set, the message address field is 32 bits

System software initializes the **Message Data** register (offset 54h) with a system-specified message.

The *MSI Enable* bit is cleared after reset and software must set the bit if the system supports the MSI scheme. After the bit is enabled, the module performs a DWord Memory Write to the address specified by the Message Address register contents. The two lower bytes of data written are taken from the contents of the two lower bytes of the Message Data register. The upper two bytes of data are zero (0).

Because the *Multiple Message Enable* field is always 000b, the module is not permitted to change the low order bits of message data to indicate a multiple message vector, and all **Message Data** register data bits are directly copied to the data.

After the *Interrupt Status* bit is set and a message generated, the module does not generate another message until the system services the interrupt and clears the *Event Status* bits.

The module hardware clears the *Interrupt Status* bit when all event status bits are cleared.

10.6 Remapping INTA# Interrupts

The PEX 8114 does not perform interrupt remapping, due to its single internal register-set topology.

When the PEX 8114 acts as a Forward bridge, interrupt lines INTA_ INTB_, INTC_, and INTD_ are routed straight through the PEX 8114 and converted into De-assert Interrupt and Assert Interrupt A, B, C, and D packets, respectively, on the PCI Express side of the bridge.

When PEX 8114 acts as a Reverse bridge, each assert A, B, C, and D interrupt and de-assert interrupt packet causes the interrupt A, B, C, and D lines, respectively, to assert and de-assert.

Refer to the *PCI Express-to-PCI/PCI-X Bridge r1.0*, Section 8.2, for an explanation of routing for Option A bridges.

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Chapter 11 PCI/PCI-X Arbiter

11.1 Introduction

The PCI/PCI-X Arbiter efficiently manages accesses to the PCI/PCI-X Bus shared by multiple Masters. It is not required that all systems provide equal bus access to all Masters. In reality, most systems require certain Masters be granted greater access to the bus than others. This is the case for systems with an embedded processor.

It is assumed that the bus access requirements for all Masters in a system are known. It is possible to program the bus access requirements to meet system needs.

11.2 Arbiter Key Features

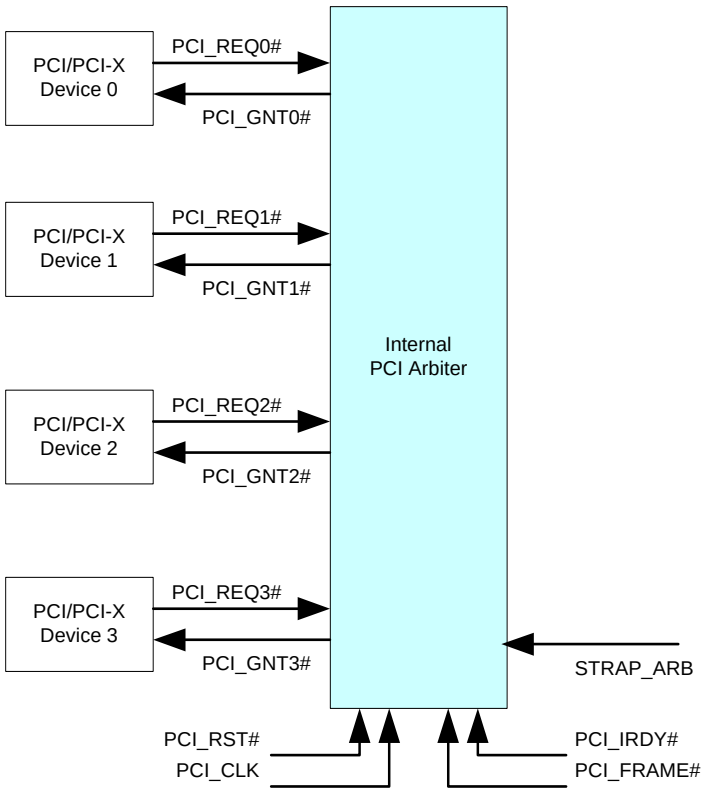
The key features of the PCI/PCI-X Arbiter are as follows:

- Arbiter supports up to five PCI-X or Conventional PCI devices (four external and one internal)
- Bus allocation is programmable in 10% increments
- Park bus on latest Master
- Enable/disable Arbiter (by way of STRAP_ARB ball)
- Address stepping on Configuration cycles
- Asserts grants in two ways:
  - Standard PCI/PCI-X-compliant grants during accesses
  - Wait for idle bus to issue grant

11.3 Functional Block Diagram

At any time, more than one PCI/PCI-X Bus Master can assert its specific PCI_REQ[3:0]# signal and request PCI/PCI-X Bus ownership. The Arbiter determines which PCI/PCI-X devices acquire bus ownership by asserting the specific device PCI_GNT[3:0]# signal. Figure 11-1 illustrates the relationship between the PCI/PCI-X devices and PCI/PCI-X Arbiter.

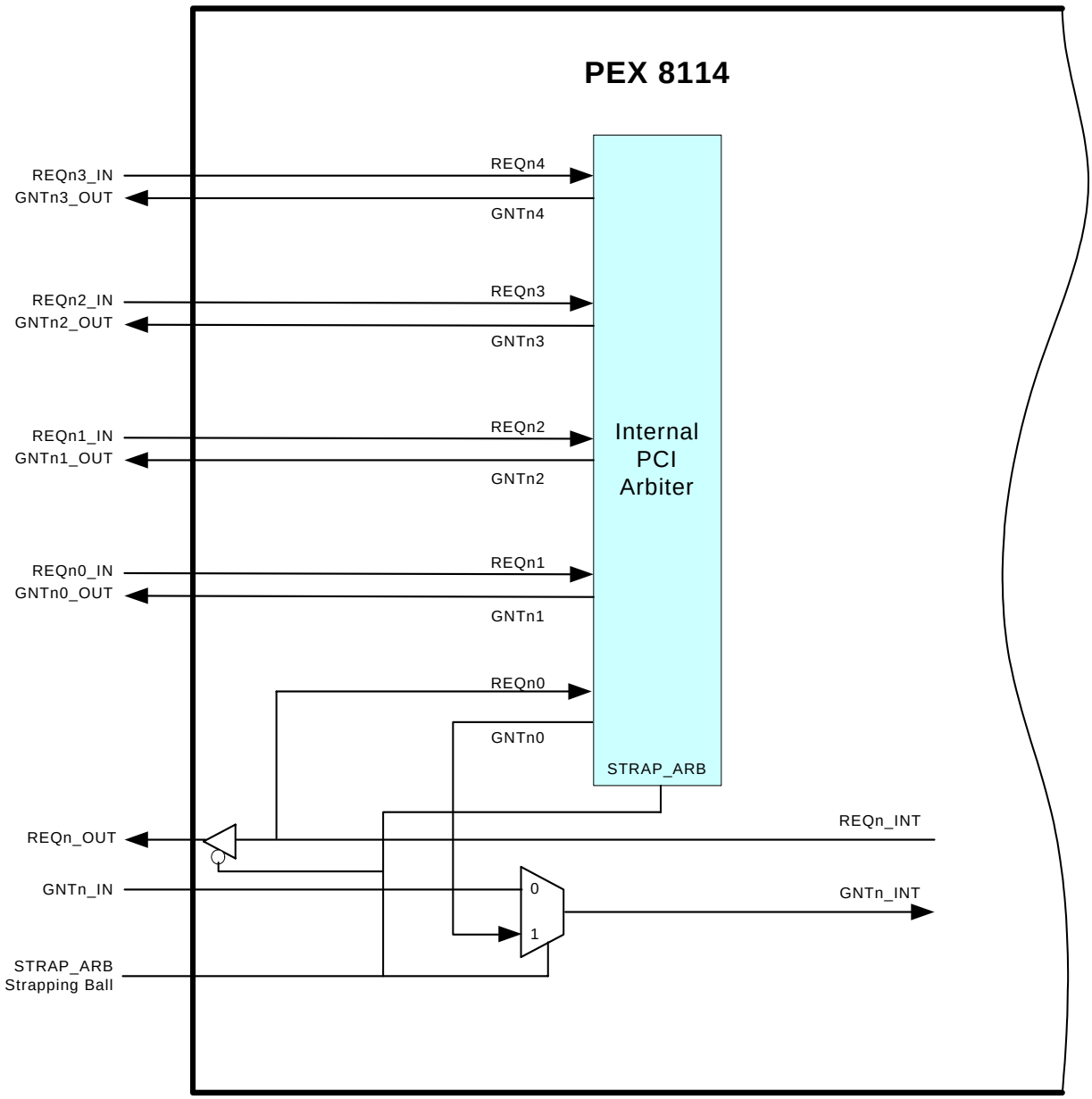
Figure 11-1. Internal PCI Arbiter Top-Level Diagram



11.4 PEX 8114 Arbiter Usage

Figure 11-2 illustrates PCI/PCI-X Arbiter use in a PEX 8114 application. In this illustration, four Request/Grant pairs are used only when the Arbiter is enabled. Another active Request/Grant pair is shown, regardless of whether the Arbiter is enabled. The pair interfaces with the External Arbiter as PCI_REQ# when the Arbiter is disabled. The pair acts as PCI_REQ0# when the Arbiter is enabled.

Figure 11-2. PEX 8114 Internal PCI Arbiter Usage



11.5 External Bus Functional Description

The PCI/PCI-X Arbiter is designed to arbitrate the bus requests of up to four PCI/PCI-X Master devices on the PCI/PCI-X Bus. The PCI-X Bus includes several enhancements that enable faster and more efficient Data transfers than the PCI Local Bus allowed, at PCI-X Bus clock frequencies up to 133 MHz. Because of these higher clock rates, register all inputs and outputs. Registering Request signals by the Arbiter should in no way limit its usage to PCI-X Bus applications. It is backward-compatible with the PCI Bus and functions as an arbiter in the PCI environment.

Note: *Registering of an arbiter signal is performed in compliance to the PCI-X r2.0a. No additional requirements are implied herein.*

11.6 Detailed Functional Description

Arbitration is necessary if more than one Master simultaneously requests the bus. When only one Master is requesting the bus and the bus is idle, the requesting bus receives the grant if it is allowed at least one Configuration register assignment. The PEX 8114 can be configured as a Slave to an external arbiter, or function as the PCI Bus Arbiter supporting up to four external PCI Bus requesters and the PEX 8114's internal request. The **PCI Arbiter** registers (offsets FA8h, FACh, and FB0h), in conjunction with the STRAP_ARB ball, control PEX 8114 arbitration characteristics. When STRAP_ARB is grounded, the PEX 8114 functions as a Slave to the External Arbiter. When functioning as a Slave to the External Arbiter, the PEX 8114 requests access to the PCI Bus by asserting PCI_REQ#, and receives grants from the External Arbiter on the PCI_GNT# ball.

The three **PCI Arbiter** registers are divided into ten, three-bit Arbiter Allocation subregisters. When the Arbiter is enabled, the PCI Bus bandwidth is distributed in 10% increments, by loading the Allocation subregisters with the value that represents an external or internal arbitration contender.

Table 11-1 defines the bandwidth allocations that occur when one of the 10 Arbiter Allocation subregisters are set or cleared to the values listed.

It is not required that the requester values be evenly distributed in the allocation subregisters to achieve the proper bus percentage, or to achieve random bus allocation. The register power-on default values provide equal bandwidth distribution among the requesters. Typically, the Arbiter Allocation subregisters are set at initialization; however, they can be modified at any time. If the value representing a Request ball is not loaded into an arbitration allocation subregister, that requester is not granted access to the PCI Bus. If all arbitration allocation subregisters are loaded with the same Requester ID, all PCI Bus bandwidth is allocated to that requester.

Table 11-1. Arbiter Allocation Subregister Values and Bandwidth Allocation

Arbiter Allocation Subregister Value	Bandwidth Allocation
000b	Allocates 10% of the bus bandwidth to the internal requests.
001b	Allocates 10% of the bus bandwidth to the PCI_REQ0# input.
010b	Allocates 10% of the bus bandwidth to the PCI_REQ1# input.
011b	Allocates 10% of the bus bandwidth to the PCI_REQ2# input.
100b	Allocates 10% of the bus bandwidth to the PCI_REQ3# input.
101b and higher	Effectively removes that Arbiter Allocation subregister from the set of usable registers (*for example*, if five of the Arbiter Allocation subregisters are loaded with 111b, each of the remaining five Allocation subregisters represent 20% of the bus bandwidth).

11.6.1 Bus Parking

The Arbiter is designed to implement bus parking when there are no pending requests (bus idle). In this case, the Arbiter allows the Grant signal for the last Master to remain active. This ensures that if the last Master requested the bus again, it receives an immediate grant; however, if another Master requests the bus, the Arbiter causes all grants to go High before issuing a new grant.

11.6.2 Hidden Bus Arbitration

The *PCI r3.0* allows bus arbitration to occur while the currently granted device is performing a Data transfer. This feature greatly reduces arbitration overhead and improves bus utilization. Hidden arbitration occurs if the control register Grant_mode has a value of 1; otherwise, arbitration occurs when the bus is idle. Idle bus arbitration supports Conventional PCI devices.

11.6.3 Address Stepping

The PEX 8114's Internal PCI Arbiter supports address stepping. To acquire maximum PCI Bus utilization, the Arbiter removes a grant from a device that requests the bus if it fails to start a transaction on the bus within a specified minimum number of PCI_CLK cycles.

In PCI-X mode high-frequency operation, when several devices are connected to the high-order Address lines, the AD bus can be slow to settle when a device is trying to drive a Configuration cycle on the bus. To accommodate these slow transitions during configurations, a Configuring Master can delay PCI_FRAME# assertion one extra cycle, to allow the AD Bus lines sufficient time to settle. The PCI_FRAME# delayed assertion is called *address stepping*. When a Configuring Master delays PCI_FRAME# assertion, if the Master is used with a high-performance Arbiter, the Arbiter can remove the Grant signal when the Configuring Master starts to assert PCI_FRAME#. Address stepping forces the Arbiter to allow one extra Clock cycle for the device that is driving the configuration to assert PCI_FRAME# before removing the grant.

The *Address Stepping Enable* bit (offset FA0h[13]) controls PEX 8114 Address stepping. At reset, the bit is cleared to 0 and address stepping is disabled. Setting the *Address Stepping Enable* bit causes the Arbiter to delay grant removal during PCI-X Configuration cycles.

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Chapter 12 Hot Plug Support

12.1 Hot Plug Purpose and Capabilities

Note: *The PEX 8114's Hot Plug Controller is compliant with the Hot Plug r1.0 and PCI Standard Hot Plug Controller and Subsystem r1.0.*

Hot Plug capabilities allow orderly insertion and extraction of boards from a running system, without adversely affecting the system. Board insertion or extraction, without system down time, is performed when repair of a faulty board or system reconfiguration becomes necessary. Hot Plug capabilities also allow systems to isolate faulty boards in the event of a failure. The PEX 8114 includes a Hot Plug Controller capable of supporting Hot Plugging of a downstream PCI Express link. Therefore, the Hot Plug Controller is used when the PEX 8114 is in Reverse Transparent Bridge mode. ***PCI/PCI-X Hot Plug is not supported. Do not use the PEX 8114 to support Hot Plug in Forward Transparent Bridge mode.***

12.1.1 Hot Plug Controller Capabilities

- Insertion and removal of PCI Express boards, without removing system power
- Hot Plug Controller function
- Board Present and MRL Sensor signal support
- Power Indicator and Attention Indicator Output signal controlled
- Attention Button monitored
- Power fault detection and Faulty board isolation
- Power switch for controlling downstream device power
- Generates PME for a Hot Plug event in a sleeping system (D3hot)
- Presence detect is achieved through an in-band SerDes Receiver Detect mechanism or by the HP_PRSNT# signal

12.1.2 Hot Plug Port External Signals

The PEX 8114 Hot Plug Controller includes nine Hot Plug signals. These signals are detailed in Table 12-1. The signal ball numbers are provided in Table 2-5, "Hot Plug Signals (9 Balls)."

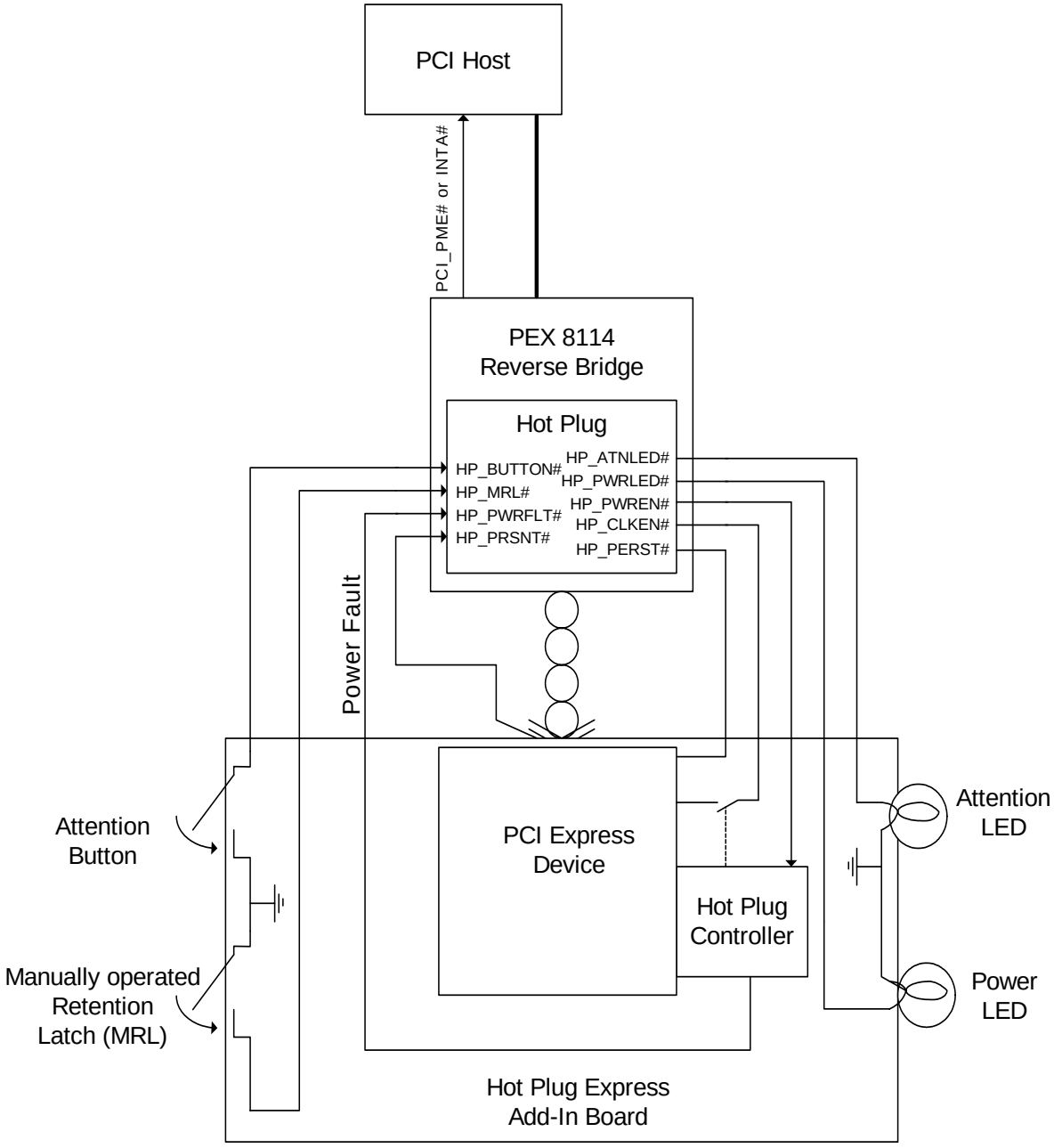
Table 12-1. Hot Plug Signals

Signal Name	Type	Description
HP_ATNLED#	O	**Hot Plug Attention LED** Slot Control Logic output used to drive the Attention Indicator. Set Low to turn On the LED. High/Off = Standard Operation Low/On = Operational problem at this slot Blinking = Slot is identified at the user's request Blinking Frequency = 2.0 Hz, 50% duty cycle
HP_BUTTON#	I PU	**Hot Plug Attention Button** Slot Control Logic input directly connected to the Attention Button, which can be pressed to request Hot Plug operations. Can be implemented on the bridge or on the downstream device.
HP_CLKEN#	O	**Clock Enable** Reference Clock enable output. Enabled when the **Slot Capabilities** register *Power Controller Present* bit is set (offset 7Ch[1]=1), and controlled by the *Slot Control register Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN# (and HP_PWRLED#) output assertion to HP_CLKEN# output assertion is programmable from 16 ms (default) to 128 ms, in the *HPC Tpepv Delay* field (offset 1E0h[4:3]).
HP_MRL#	I PU	**Manually Operated Retention Latch Sensor** Slot Control Logic and Power Controller input directly connected to the MRL Sensor. Manually Operated Retention Latch switch signal for inserting and extracting Hot Plug-capable boards. High = Board is not available or properly seated in slot Low = Board properly seated in slot
HP_PERST#	O	**Reset** Hot Plug Reset for downstream link. Enabled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]).
HP_PRSNT#	I PU	**PCI Present** Input connected to external logic that outputs PRSNT# directly from the external combination of PRSNT1# and PRSNT2#.
HP_PWREN#	O	**Power Enable** Slot Control Logic output that controls the slot power state. When HP_PWREN# is Low, power is enabled to the slot.
HP_PWRFLT#	I PU	**Power Fault Input** Indicates that the power controller for the slot detected a power fault on one or more supply rails.
HP_PWRLED#	O	**Power LED** Slot Control Logic output used to drive the Power Indicator. This output is set Low to turn On the LED.

12.1.3 Hot Plug Typical Hardware Configuration

Figure 12-1 illustrates a typical system-level hardware configuration using the PEX 8114 to provide Hot Plug support in Reverse Transparent Bridge mode.

Figure 12-1. Hot Plug Typical Hardware Configuration for Reverse Transparent Bridge Mode Application



12.1.4 Hot Plug Sequence Illustration

The following scenarios define the Hot Plug sequences for removing and installing boards.

To remove a board:

1. Determine that the board must be removed and notify the PCI Host by pressing the Attention Button or typing a command on the Host console.
2. The Hot Plug portion of the operating system quiesces the appropriate board driver and blinks the Attention LED.
3. The Hot Plug system driver asserts HP_PERST#, powers down the slot by way of HP_PWREN# de-assertion, and turns Off the Power LED, indicating that the board can be removed.
4. Disengages the MRL switch and allows the board to be removed.
5. The Hot Plug driver detects the MRL switch disconnect, and the HP_PRSNT# lines indicate that no board is present.

To insert a board:

1. Insert the board and notify the system console, MRL, or Attention button.
2. The system tells the Hot Plug driver to power-up the slot, de-assert HP_PERST#, and turn On the Power LED.
3. The Hot Plug driver indicates to the system that the board is ready for use.

12.1.5 PCI Express Capabilities Register

The Hot Plug Configuration, Capabilities, Command, Status, and Events are included in the PEX 8114 PCI Express Capabilities register. The applicable register map is provided in Table 12-2.

Table 12-2. PCI Express Capabilities Register Map (Partial)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Slot Capabilities (Reverse Transparent Bridge Mode Only)				7Ch
Slot Status		Slot Control		80h

12.1.6 Hot Plug Interrupts

The Hot Plug Controller supports Hot Plug interrupt generation on the following events:

- Attention Button Pressed
- Power Fault Detected
- MRL Sensor Changed
- Presence Detect Changed
- Command Completed

Depending on the PEX 8114 downstream PCI Express port power state, a Hot Plug event can generate a system interrupt or PME. When the PEX 8114 downstream PCI Express port is in the D0 power state, Hot Plug events generate a system interrupt; when not in the D0 state, a PME interrupt is generated on Hot Plug events. The *Command Completed* bit does not generate a PME interrupt. When the system is in Sleep mode, Hot Plug operation causes a system wakeup using PME logic.

12.1.7 Hot Plug Insertion and Removal Process

Table 12-3 defines the board insertion procedure supported by the PEX 8114. Table 12-4 defines the board removal procedure.

Table 12-3. Hot Plug Insertion Process

Operator	Hot Plug Controller	Software
A. Place board in slot.	**1.** *Presence Detect State* bit is set to 1. **2.** *Presence Detect Change* bit is set to 1. **3.** PCI_INTA# is asserted, if enabled. **4.** PCI_INTA# is de-asserted.	*Presence Detect Change* bit is cleared to 0.
B. Lock the MRL (Manually operated Retention Latch).	**5.** *MRL Sensor Present* bit is cleared to 0. **6.** *MRL Sensor Changed* bit is set to 1. **7.** PCI_INTA# is asserted, if enabled. **8.** PCI_INTA# is de-asserted.	*MRL Sensor Changed* bit is cleared to 0.
C. Press Attention Button.	**9.** *Attention Button Present* bit is set to 1. **10.** PCI_INTA# is asserted, if enabled. **11.** PCI_INTA# is de-asserted.	*Attention Button Present* bit is cleared to 0.
D. Power Indicator blinks.	**12.** *Power Indicator Control* field is set to 10b. **13.** Power Indicator Blink message is transmitted downstream. **14.** *Command Complete* bit is set to 1. **15.** PCI_INTA# is asserted, if enabled. **16.** PCI_INTA# is de-asserted.	Write to *Power Indicator Control* field to blink the power LED, to indicate that the board is being powered up. *Command Complete* bit is cleared to 0.
E. Power Indicator On.	**17.** *Power Indicator Control* field is set to 01b. **18.** After a T_{pepv} delay of 16 ms, *Command Complete* bit is set. **19.** PCI_INTA# is asserted, if enabled. **20.** PCI_INTA# is de-asserted.	Write to the Control register *Power Indicator Control* field, to turn On power to the port. *Command Complete* bit is cleared to 0.

Table 12-4. Hot Plug Removal Process

Operator	Hot Plug Controller	Software
A. Press Attention Button.	**1.** *Attention Button Present* bit is set to 1. **2.** PCI_INTA# is asserted, if enabled. If the Attention Button is present on the downstream device, the "Attention Button" message is received, and the *Attention Button Present* bit is set to 1. **3.** PCI_INTA# is de-asserted.	*Attention Button Present* bit is cleared to 0.
B. Power Indicator blinks.	**4.** *Power Indicator Control* field is set to 10b. **5.** Power Indicator Blink message is transmitted downstream. **6.** *Command Complete* bit is set. **7.** PCI_INTA# is asserted, if enabled. **8.** PCI_INTA# is de-asserted.	Write to *Power Indicator Control* field to blink the power LED, to indicate board is being powered down. *Command Complete* bit is cleared to 0.
C. Power Indicator Off.	**9.** *Power Indicator Control* field is cleared to 0. **10.** After a T_{pepv} delay of 16 ms, *Command Complete* bit is set. **11.** PCI_INTA# is asserted, if enabled. **12.** PCI_INTA# is de-asserted.	Write to the Control register *Power Indicator Control* field, to turn Off power to the port. *Command Complete* bit is cleared to 0.
D. Unlock the MRL (Manually operated Retention Latch).	**13.** *MRL Sensor Present* bit is set to 1. **14.** *MRL Sensor Change* bit is set to 1. **15.** PCI_INTA# is asserted, if enabled. **16.** PCI_INTA# is de-asserted.	*MRL Sensor Change* bit is cleared to 0.
E. Remove board from slot.	**17.** *Presence Detect State* bit is cleared to 0. **18.** *Presence Detect Change* bit is set to 1. **19.** PCI_INTA# is asserted, if enabled. **20.** PCI_INTA# is de-asserted.	*Presence Detect Change* bit is cleared to 0.

Chapter 13 Power Management

13.1 Power Management Capabilities

The PEX 8114 Power Management (PM) module interfaces with different areas of the PEX 8114 to reduce power consumption during idle periods. The PEX 8114 supports hardware autonomous Power Management and software-driven D-State Power Management. It supports L0s and L1 link states in hardware autonomous active state link PM. It also supports L1, L2/L3 Ready, and L3 PCI Express link states in PCI-compatible Power Management states. D0, D3hot, and D3cold device states and B0 PCI Bus states are supported in the PCI-compatible Power Management. Because the PEX 8114 does not support Aux-Power, PME generation in the D3cold state is ***not supported***.

In Forward Transparent Bridge mode, the PM module interfaces with the Physical Layer electrical sub-block, to transition the Link State into low-power states when it receives a power state change request from an upstream PCI Express component, or when an internal event forces the link state entry into low-power states in hardware autonomous PM (Active Link State PM) mode. PCI Express link states are not directly visible to Conventional PCI Bus Driver software, but are derived from the Power Management state of the components residing on those links.

13.2 PEX 8114 Power Management Capabilities Summary

13.2.1 General Power Management Capabilities

- Link Power Management State (L States)
  - PCI Express Power Management – L1, L2/L3 Ready, and L3 (AUX power is ***not supported***)
  - Active State Power Management – L0s and L1
  - PCI Bus B0 state
- Device Power Management State (D States)
  - D0 (uninitialized and active) and D3 (hot and cold) support
- Power Management Event (PCI_PME#) support in D0 and D3hot
- Power Management Data register is supported through serial EEPROM load

13.2.2 Forward Bridge-Specific Power Management Capabilities

- PME message generation on the PCI Express link caused by PCI_PME# assertion on the PCI Bus in Forward Transparent Bridge mode.
- The PEX 8114 has no internal sources that generate PME messages in Forward Transparent Bridge mode. *That is*, there is no Forward Transparent Bridge mode PCI Bus Hot Plug support. Therefore, all PME messages result from downstream devices asserting PCI_PME# input to the PEX 8114.
- Only PCI D0 and D3 Device power states and B0 Bus power state are supported in Forward Transparent Bridge mode.

13.2.3 Reverse Transparent Bridge-Specific Power Management Capabilities

- Power Management events due to Hot Plug events in Reverse Transparent Bridge mode only (PCI Hot Plug is ***not supported***).
- Assert PCI_PME# on the upstream PCI Bus:
  - Upon receiving a PME message from the PCI Express downstream device, if the PME signaling bit in the **Power Management Status and Control** register is enabled. The PCI_PME# signal is de-asserted when the *PME Status* or *Enable* bits are cleared, according to the *PCI Power Mgmt. r1.2*.
  - Caused by a PEX 8114 internal Hot Plug event.
- Generate a PME_Turn_Off message to the PCI Express downstream devices when the bridge is requested to be placed into the D3 state. After generating the PME_Turn_Off message, the PEX 8114 waits for the PME_ACK message to return prior to entering the D3 state.

13.2.4 Device Power States

The PEX 8114 supports the PCI Express PCI-PM D0, D3hot, and D3cold (no VAUX) device Power Management states. The D1 and D2 states, which are optional in the *PCI Express r1.0a*, are ***not supported***.

13.2.4.1 D0 State

D0 is divided into two distinct substates, "uninitialized" and "active." When power is initially applied to the PCI Express bridge, it enters the D0_uninitialized state. The component remains in the D0_initialized state until the serial EEPROM loading and initial link training are complete.

A device enters the D0_active state when:

- Single *Memory Access Enable* occurs
- Combination of the following are set by system software:
  - *I/O Access Enable*
  - *Memory Access Enable*
  - *Bus Master Enable*

13.2.4.2 D3hot State

A device in the D3hot state must be able to respond to Configuration accesses, allowing it to transition by software to the D0_uninitialized state. Once in D3hot state, the device can be transitioned into D3cold by removing power from the device. In the D3hot state, Hot Plug operations cause a PME.

13.2.4.3 D3cold State

The PEX 8114 transitions to the D3cold state when its power is removed. Re-applying power causes the device to transition from the D3cold state into the D0_uninitialized state. D3cold state assumes that all previous context is lost; therefore, software must save the necessary context while the device is in the D3hot state.

13.2.5 Link Power Management State

Link Power Management state is determined by the D-state of its downstream link. The PEX 8114 maintains its PCI Express link in the L0 state when it operates in standard operational mode (PCI PM state in D0_active). Active State Link Power Management defines a protocol for components in the D0 state to reduce link power, by placing their links into a low-power state, and instructs the other end of the link to do likewise. This capability allows hardware autonomous dynamic-link power reduction beyond what is achievable by software-only Power Management. Table 13-1 defines the relationship between the PEX 8114 device power state and its downstream link.

Table 13-1. Connected Link Components Power States

Downstream Component D State	PEX 8114 D State	Permissible Interconnect State	Power Saving Actions
D0	D0	L0	Full power.
		L0s, L1 (optional)	PHY Transmit lanes are operating in high-impedance state.
D1	D0	L1	
D2			
D3hot	D0 or D3hot[a]	L1, L2/L3 Ready	PHY Transmit lanes are operating in high-impedance state. FC and DLL ACK/NAK Timers suspended. PLL can be disabled.
D3cold (no AUX-Pwr)	D0, D3hot, or D3cold	L3 Link-off State	No power to component.

a. The PEX 8114 initiates a Link-state transition of its upstream port to L1 when the port is programmed to D3hot.

13.2.6 PEX 8114 PCI Express Power Management Support

The PEX 8114 supports PCI Express features that are required or important for PCI Express Bridge Power Management. Table 13-2 defines the supported and non-supported features, and the register bits used for activating feature configuration. ***Reserved*** bits are not listed.

Note: *Power Management is not supported in PCI-X mode.*

Table 13-2. Supported PCI Express Power Management Capabilities

Register		Description	Supported	
Offset	Bit(s)		Y	N
40h	**Power Management Capabilities**			
	7:0	**Capabilities ID** Default 11h indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	15:8	**Next Pointer** Default 48h points to the **Message Signaled Interrupt Capability List** register	✔	
	18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	19	**PME Clock** Set to 1, as required by the *PCI Express Base 1.0a.*	✔	
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.		✔
	24:22	**AUX Current** ***Not supported.*** Default 000b indicates that the PEX 8114 does not support Auxiliary Current requirements.		✔
	25	**D1 Support** ***Not supported.*** Default 0 indicates that the PEX 8114 does not support the D1 Power state.		✔
	26	**D2 Support** ***Not supported.*** Default 0 indicates that the PEX 8114 does not support the D2 Power state.		✔
	31:27	**PME Support** Default 11001b indicates that the PEX 8114 forwards PME messages in the D0, D3hot, and D3cold power states.	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
44h		**Power Management Status and Control**		
	1:0	**Power State** Reports the PEX 8114 power state. 00b = D0 11b = D3hot 01b and 10b = ***Not supported***	✔	
	3	**No Soft Reset** When set to 1, indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset.	✔	
	8	**PME Enable** 0 = Disables PME generation by the PEX 8114[a] 1 = Enables PME generation by the PEX 8114	✔	
	12:9	**Data Select** R/W by Serial EEPROM mode[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	✔	
		RO for hardware auto configuration – ***Not supported***		✔
	14:13	**Data Scale** R/W by Serial EEPROM mode[b]. There are four internal **Data Scale** registers. Bits [12:9], *Data Select*, select the **Data Scale** register.	✔	
	15	**PME Status** 0 = PME is not generated by the PEX 8114[a] 1 = PME is generated by the PEX 8114	✔	
		Power Management Control/Status Bridge Extensions		
	22	**B2/B3 Support** Cleared to 0, as required by the *PCI Power Mgmt. r1.2*.		✔
	23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Power Mgmt. r1.2*.		✔
		Power Management Data		
	31:24	**Data** R/W by Serial EEPROM mode[b]. There are four internal Data registers. Bits [12:9], *Data Select*, select the **Data** register.	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
6Ch		**Device Capabilities**		
	8:6	**Endpoint L0s Acceptable Latency** ***Not supported.*** Because the PEX 8114 is a bridge and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** ***Not supported.*** Because the PEX 8114 is a bridge and not an endpoint, it does ***not support*** this feature. 000b = Disables the capability		✔
	12	**Attention Button Present** Valid only in Forward Transparent Bridge mode. For the PCI Express interface, when set to 1, indicates that an Attention Button is implemented on that adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Button is not present on an adapter board for which the PEX 8114 is providing the system interface.	✔	
	13	**Attention Indicator Present** Valid only in Forward Transparent Bridge mode. For the PCI Express interface, when set to 1, indicates that an Attention Indicator is implemented on the adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating an Attention Indicator is not present on an adapter board for which the PEX 8114 is providing the system interface.	✔	
	14	**Power Indicator Present** Valid only in Forward Transparent Bridge mode. For the PCI Express interface, when set to 1, indicates that a Power Indicator is implemented on the adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating that a Power Indicator is not present on an adapter board for which the PEX 8114 is providing the system interface.	✔	
	25:18	**Captured Slot Power Limit Value** Valid only in Forward Transparent Bridge mode. For the PCI Express interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the *Captured Slot Power Limit Scale* field value.	✔	
	27:26	**Captured Slot Power Limit Scale** Valid only in Forward Transparent Bridge mode. For the PCI Express interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the *Captured Slot Power Limit Value* field value. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
		Device Status and Control		
70h	10	**AUX Power PM Enable** ***Not supported.*** Cleared to 0.		✔
	20	**AUX Power Detected** ***Not supported.*** Cleared to 0.		✔
		Link Capabilities		
74h	11:10	**Active-State Power Management Support** 01b = PEX 8114 supports the L0s link power state 11b = PEX 8114 supports the L0s and L1 Link power states	✔	
	14:12	**L0s Exit Latency** 101b = PCI Express interface L0s Exit Latency is between 1 and 2 µs	✔	
	17:15	**L1 Exit Latency** 101b = PCI Express interface L1 Exit Latency is between 16 and 32 µs	✔	
		Link Status and Control		
78h	1:0	**Active-State Power Management Control** 00b = Disables L0s and L1 Entries for the PEX 8114 PCI Express port[c] 01b = Enables only L0s Entry 10b = Enables only L1 Entry 11b = Enables both L0s and L1 Entries	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
7Ch		**Slot Capabilities (Reverse Transparent Bridge Mode Only)**		
	0	**Attention Button Present** 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the PEX 8114 PCI Express interface	✔	
	1	**Power Controller Present** 0 = Power Controller is not implemented 1 = Power Controller is implemented for the slot of the PEX 8114 PCI Express interface	✔	
	2	**MRL Sensor Present** 0 = MRL Sensor is not implemented 1 = MRL Sensor is implemented on the slot chassis of the PEX 8114 PCI Express interface	✔	
	3	**Attention Indicator Present** 0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the PEX 8114 PCI Express interface	✔	
	4	**Power Indicator Present** 0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the PEX 8114 PCI Express interface	✔	
	5	**Hot Plug Surprise** 0 = No device in the PEX 8114 PCI Express interface slot is removed from the system, without prior notification 1 = Device in the PEX 8114 PCI Express interface slot can be removed from the system, without prior notification	✔	
	6	**Hot Plug Capable** 0 = PEX 8114 PCI Express interface slot is not capable of supporting Hot Plug operations 1 = PEX 8114 PCI Express interface slot is capable of supporting Hot Plug operations	✔	
	14:7	**Slot Power Limit Value** The maximum power available from the PEX 8114 PCI Express interface is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the *Slot Power Limit Scale* field value.	✔	
	16:15	**Slot Power Limit Scale** The maximum power available from the PEX 8114 PCI Express port is determined by multiplying the value in this field by the *Slot Power Limit Value* field value. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
80h	**Slot Status and Control (Reverse Transparent Bridge Mode Only)**			
	1	**Power Fault Detected Enable** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event on a Power Fault event on the PEX 8114 PCI Express port	✔	
	9:8	**Power Indicator Control** Controls the Power Indicator on the PEX 8114 PCI Express port slot. 00b = ***Reserved – Do not use*** 01b = Turns On indicator to constant On state 10b = Causes indicator to Blink 11b = Turns Off indicator Writes cause the PEX 8114 PCI Express port to transmit the appropriate Power Indicator message. Reads return the PEX 8114 PCI Express port Power Indicator's current state.	✔	
	10	**Power Controller Control** Controls the PEX 8114 PCI Express port Slot Power Controller: 0 = Turns On Power Controller 1 = Turns Off Power Controller	✔	
	17	**Power Fault Detected** Set to 1 when the PEX 8114 PCI Express port Slot Power Controller detects a Power Fault at the slot.	✔	
138h	**Device Power Budgeting Extended Capabilities**			
	15:0	**Extended Capability ID** Set to 0004h, as required by the *PCI Express Base 1.0a.*	✔	
	19:16	**Capability Version** Set to 1h, as required by the *PCI Express r1.0a*.	✔	
	31:20	**Next Capability Offset** Set to 148h, which addresses the PEX 8114 **Virtual Channel Budgeting Extended Capability** registers.	✔	
13Ch	**Data Select**			
	7:0	**Data Select** Indexes the Power Budgeting Data reported by way of eight **Power Data** registers and selects the DWord of Power Budgeting Data that appears in each **Power Data** register. Index values start at 0, to select the first DWord of Power Budgeting Data; subsequent DWords of Power Budgeting Data are selected by increasing index values 1 to 7.	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
		Power Data		
		Note: *There are eight registers per port that can be programmed through the serial EEPROM. Each register retains a different power configuration for the port. Each configuration is selected by writing to the Data Select register Data Select bits.*[a]		
	7:0	**Base Power** Four registers. Specifies, in watts, the base power value in the operating condition. This value must be multiplied by the Data Scale to produce the actual power consumption value.	✔	
	9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. Defined encodings are: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** 000b = PEX 8114 is in the default Power Management sub-state	✔	
140h	14:13	**PM State** Current power state. 00b = D0 state 01b = ***Not used – D1 state not supported*** 10b = ***Not used – D2 state not supported*** 11b = D3 state	✔	
	17:15	**Type** Type of operating condition. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other values are ***reserved***.	✔	
	20:18	**Power Rail** Power Rail of operating condition. 000b = Power is 12V 001b = Power is 3.3V 010b = Power is 1.8V 111b = Thermal All other values are ***Reserved.***	✔	
		Power Budget Capability		
144h	0	**System Allocated** 1 = Power budget for the device is included within the system power budget	✔	

Table 13-2. Supported PCI Express Power Management Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Y	N
1E0h	**Power Management Hot Plug User Configuration**			
	0	**L0s Entry Idle Count** Time to meet to enter L0s. 0 = Idle condition lasts for 1 µs 1 = Idle condition lasts for 4 µs	✔	
	1	**L1 Upstream Port Receiver Idle Count** For active L1 entry. 0 = Upstream port receiver idle for 2 µs 1 = Upstream port receiver idle for 3 µs	✔	
	2	**HPE PME Turn-Off Enable** 1 = PME Turn-off message is transmitted before the port is turned off on downstream port	✔	
	4:3	**HPC T_{pepv} Delay** Slot power-applied to power-valid delay time. 00b = 16 ms 01b = 32 ms 10b = 64 ms 11b = 128 ms	✔	
	5	**HPC In-band Presence-Detect Enable** 0 = HP_PRSNT# Input ball used to detect a board present in the slot 1 = SerDes receiver detect mechanism is used to detect a board present in the slot	✔	
	6	**HPC T_{pvperl} Delay** Downstream port power-valid to reset signal release time. 0 = 20 ms 1 = 100 ms (default)	✔	

a. Because the PEX 8114 does not support auxiliary power, this bit is not sticky, and is cleared to 0 at power-on reset.
*b. Without serial EEPROM, Reads return 00h for **Data Scale** and **Data** registers (for all Data Selects).*
c. The port receiver must be capable of entering the L0s state, regardless of whether the state is disabled.

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Chapter 14 PEX 8114 Registers

14.1 Introduction

This chapter details the PEX 8114 registers, and presents the PEX 8114 user-programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in Forward and Reverse Transparent Bridge modes.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r2.3*
- *PCI r3.0*
- *PCI-to-PCI Bridge r1.1*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base 1.0a*
- *PCI Express-to-PCI/PCI-X Bridge r1.0*
- *PCI-X r1.0b*
- *PCI-X r2.0a*

14.2 Type 1 PEX 8114 Register Map

Table 14-1. Type 1 PEX 8114 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Type 1 Configuration Space Header Registers	New Capability Pointer (40h)	00h … 34h … 3Ch
Next Capability Pointer (48h)	Capability ID (01h)	40h
Power Management Capability Registers		44h
Next Capability Pointer (58h)	Capability ID (05h)	48h
Message Signaled Interrupt Capability Registers		… 54h
Next Capability Pointer (68h)	Capability ID (07h)	58h
PCI-X Capability Registers		… 64h
Next Capability Pointer (00h)	Capability ID (10h)	68h
PCI Express Capabilities Registers		… 80h
Reserved		84h – F4h
PLX Indirect Configuration Access Mechanism Registers		F8h FCh
Next Capability Offset (FB4h) / 1h	Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers		104h 108h
Reserved		10Ch – 134h
Next Capability Offset (148h) / 1h	Extended Capability ID (0004h)	138h
Device Power Budgeting Extended Capability Registers		… 144h
Next Capability Offset (000h) / 1h	Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers		… 1C4h
PLX-Specific Registers		1C8h … F7Ch

Table 14-1. Type 1 PEX 8114 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
PCI-X PLX-Specific Registers		F80h … F88h
Root Port Registers		F8Ch … F9Ch
PCI-X-Specific Registers		FA0h FA4h
PCI Arbiter Registers		FA8h … FB0h
Next Capability Offset (138h)	1h PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Capability Registers		… FFCh

14.3 Register Descriptions

The remainder of this chapter details the PEX 8114 registers, including:

- Bit/field names
- Register function in Forward and Reverse Transparent Bridge modes
- Type
- Whether the power-on/reset value can be modified by way of the PEX 8114 serial EEPROM initialization feature
- Initial power-on/reset (default) value

The register types are grouped by user accessibility. The types used in this device, and their descriptions, are defined in Table 14-2.

Table 14-2. Register Types

Type	Description
HwInit	**Hardware Initialized Register or Register Bit** The register bits are initialized by the PEX 8114 Hardware Initialization mechanism or PEX 8114 serial EEPROM register initialization feature. The register bits are Read-Only after initialization and can only be reset with "Power Good Reset" (PEX_PERST# assertion).
RC	**Read-Clear – Reading Register Clears Register Value** The register bits generally indicate the tally of event occurrences. These registers are used for performance monitoring and, when read, are cleared to 0.
RO	**Read-Only Register or Register Bit** The register bits are Read-Only and cannot be altered by software. The register bits can be initialized by the PEX 8114 Hardware Initialization mechanism or PEX 8114 serial EEPROM register initialization feature.
R/W	**Read-Write Register or Register Bit** The register bits are Read-Write and can be set or cleared by software to the needed state.
R/W1C	**Read-Only Status – Write 1 to Clear Status Register or Register Bit** The register bits indicate status when read. A status bit set by the system to 1 to indicate status can be cleared by writing 1 to that bit.
R/W1CS	**Read-Only Status – Write 1 to clear Status register or Register Bit** The register bits indicate status when read. A status bit set by the system to 1 to indicate status can be cleared by writing 1 to that bit. Writing 0 has no effect. Bits are not initialized or modified by reset. Devices that consume AUX power preserve register values when AUX power consumption is enabled (by way of AUX power or PME Enable).
R/WS	**Read-Write Register or Bit** The register bits are Read-Write and can be set or cleared by software to the needed state. Bits are not initialized or modified by reset. Devices that consume AUX power preserve register values when AUX power consumption is enabled (by way of AUX power or PME Enable).

14.4 Type 1 Configuration Space Header Registers

Table 14-3. Type 1 Configuration Space Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST *(Not Supported)*	Header Type and Multi-Function	Primary Latency Timer	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit	I/O Base	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Upper Base Address[63:32]				28h
Prefetchable Memory Upper Limit Address[63:32]				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			New Capability Pointer (48h if PCI-X; 40h if PCI Express)	34h
Expansion ROM Base Address *(Not Supported)*				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch

Register 14-1. 00h Product Identification

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Vendor ID** Unless overwritten by the serial EEPROM, returns the PLX PCI-SIG-assigned Vendor ID. The PEX 8114 Serial EEPROM register initialization capability is used to replace the PLX Vendor ID with another Vendor ID.	HwInit	Yes	10B5h
31:16	**Device ID** Unless overwritten by the serial EEPROM, the PEX 8114 returns 8114h, the PLX-assigned Device ID. The PEX 8114 Serial EEPROM register initialization capability is used to replace the PLX-assigned Device ID with another Device ID.	HwInit	Yes	8114h

Register 14-2. 04h Command/Status

Bit(s)	Description	Type	Serial EEPROM	Default
	Command			
0	**I/O Access Enable** 0 = PEX 8114 ignores I/O accesses on the primary interface 1 = PEX 8114 responds to I/O accesses on the primary interface	R/W	Yes	0
1	**Memory Access Enable** 0 = PEX 8114 ignores Memory accesses on the primary interface 1 = PEX 8114 responds to Memory accesses on the primary interface	R/W	Yes	0
2	**Bus Master Enable** Controls the PEX 8114 Memory and I/O request forwarding in the upstream direction. This bit does not affect the forwarding of messages nor Completions in the upstream or downstream direction. **Forward Transparent Bridge mode:** 0 = PEX 8114 does not respond to Memory and I/O requests targeting the bridge on the secondary interface 1 = PEX 8114 forwards Memory and I/O requests **Reverse Transparent Bridge mode:** 0 = PEX 8114 handles Memory and I/O requests received on the secondary interface as Unsupported Requests (UR); for Non-Posted requests, the PEX 8114 returns a Completion with UR Completion status 1 = PEX 8114 forwards Memory and I/O requests	R/W	Yes	0
3	**Special Cycle Enable** ***Not supported.*** Cleared to 0.	RO	No	0

Register 14-2. 04h Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
4	**Memory Write and Invalidate** Used when the PCI-X interface is in PCI mode. Controls bridge ability to convert PCI Express Memory Write requests into Memory Write and Invalidate requests on the PCI Bus.	R/W	Yes	0
5	**VGA Palette Snoop** Valid in Reverse Transparent Bridge mode. PCI Express-to-PCI bridges do ***not support*** VGA Palette snooping. When the bit value is 0, the PEX 8114 treats VGA Palette Write accesses as other accesses. When set to 1, VGA Palette snooping is enabled (*that is*, the PEX 8114 does not respond to VGA Palette register Writes and snoops the data). Refer to Section 5.2.1.4, "VGA Mode," for further details.	R/W	Yes	0
6	**Parity Error Response Enable** Controls the bridge response to Data Parity errors forwarded from its primary interface (*such as* a Poisoned TLP or PCI Bus Parity errors). 0 = Bridge must ignore Data Parity errors that it detects and continue standard operation (however, records status, *such as* setting the *Detected Parity Error* bit) 1 = Bridge must set the proper error bits and report the error when a Data Parity error is detected	R/W	Yes	0
7	**IDSEL Stepping/Write Cycle Control** ***Not supported.*** Cleared to 0.	RO	No	0
8	**SERR# Enable** Controls the *Signaled System Error* bit. **Forward Transparent Bridge mode:** When = 1, enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex. **Reverse Transparent Bridge mode:** When = 1, enables reporting of errors detected by the device by asserting SERR# on the PCI-X Bus.	R/W	Yes	0
9	**Fast Back-to-Back Transaction Enabled** ***Not supported.*** Cleared to 0.	RO	No	0
10	**Interrupt Disable** **Forward Transparent Bridge mode:** 0 = PEX 8114 is enabled to generate INTA# Interrupt messages 1 = PEX 8114 is prevented from generating INTA# Interrupt messages **Reverse Transparent Bridge mode:** 0 = PEX 8114 is enabled to generate INTA# interrupts 1 = PEX 8114 is prevented from generating INTA# interrupts	R/W	Yes	0
15:11	***Reserved***			00h

Register 14-2. 04h Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Status			
18:16	***Reserved***			000b
19	**Interrupt Status** Indicates that an INT*x*# interrupt message is pending on behalf of sources internal to the bridge. This bit does not reflect the PCI_INT*x*# input status associated with the secondary interface. 0 = No INTA# Interrupt message is pending 1 = INTA# Interrupt message is pending internally	RO	No	0
20	**Capabilities List** Required by the *PCI Express Base 1.0a* as 1 at all times.	RO	No	1
21	**66-MHz Capable** **Forward Transparent Bridge mode:** Cleared to 0, as required by the *PCI Express Base 1.0a*. **Reverse Transparent Bridge mode:** PCI-X interface is capable of 66-MHz operation; therefore, this bit is set to 1.	RO/Fwd RO/Rev	No	0 1
22	***Reserved***			0
23	**Fast Back-to-Back Transaction Capable** **Forward Transparent Bridge mode:** Cleared to 0, as required by the *PCI Express Base 1.0a*. **Reverse Transparent Bridge mode:** Set to 1, indicating Fast Back-to-Back Transaction capability.	RO/Fwd RO/Rev	No	0 1

Register 14-2. 04h Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
24	**Master Data Parity Error** Reports Data Parity error detection by the bridge on the primary interface. Set to 1 if the **Command** register *Parity Error Response Enable* bit is set and one of the following conditions occur. **Forward Transparent Bridge mode:** • Bridge receives a Completion marked *poisoned* on the primary interface • Bridge poisons a Write request on the primary interface **Reverse Transparent Bridge mode:** • Bridge, as a bus Master on the primary interface, asserts PCI_PERR# on a Read transaction or detects PCI_PERR# asserted on a Write transaction • Bridge receives a Completion or Split Completion with a Parity error on the secondary interface • Bridge receives a Split Completion message for a Non-Posted Write on the primary interface, indicating an Uncorrectable (Split) Write Data error	R/W1C	Yes	0
26:25	**DEVSEL Timing** **Forward Transparent Bridge mode:** Cleared to 00b, as required by the *PCI Express Base 1.0a*. **Reverse Transparent Bridge mode:** Pertain to PCI and PCI-X modes. Encode PCI_DEVSEL# timing. For the PEX 8114, the field is set to 10b, indicating slow speed.	RO/Fwd RO/Rev	No No	00b 10b
27	**Signaled Target Abort** **Forward Transparent Bridge mode:** When a Memory-Mapped access Payload Length is greater than 1 DWord, the PEX 8114 sets this bit to 1. Also set to 1 when the bridge completes a request as a Transaction Target on its primary interface using Completer Abort Completion status. **Reverse Transparent Bridge mode:** When the PCI-X interface signals Target Abort, the PEX 8114 sets this bit to 1.	R/W1C	Yes	0

Register 14-2. 04h Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Received Target Abort** **Forward Transparent Bridge mode:** Set to 1 when the bridge receives a Completion with Completer Abort Completion status. **Reverse Transparent Bridge mode:** Set to 1 when the bridge is the transaction Master terminated with a Target Abort or PCI-X Split Completion message indicating that a Target Abort was received.	R/W1C	Yes	0
29	**Received Master Abort** **Forward Transparent Bridge mode:** Set to 1 when the bridge receives a Completion with Unsupported Request Completion status. **Reverse Transparent Bridge mode:** Set to 1 when the bridge is the transaction Master terminated by the bridge with Master Abort status.	R/W1C	Yes	0
30	**Signaled System Error** **Forward Transparent Bridge mode:** Set to 1 when the bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex. **Reverse Transparent Bridge mode:** Set to 1 when the bridge asserts SERR# on the PCI-X Bus.	R/W1C	Yes	0
31	**Detected Parity Error** **Forward Transparent Bridge mode:** Set to 1 by the bridge when it receives a Poisoned TLP or TLP with bad ECRC (Read Completion or Write Request) on the primary interface, regardless of the **Command** register *Parity Error Response Enable* bit state. **Reverse Transparent Bridge mode:** Reports detection of an Address or Data Parity error by the bridge on its primary interface. Must be set to 1, regardless of the **Command** register *Parity Error Response Enable* bit state, when any of the following three conditions is true: • Detects an Address or Attribute Parity error as a potential Target • Detects a Data Parity error when the Target of a Write transaction or PCI-X Split Completion • Detects a Data Parity error when the Master of a Read transaction (Immediate Read data or PCI-X Split Response)	R/W1C	Yes	0

Register 14-3. 08h Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns BCh, the PLX-assigned Revision ID for this version of the PEX 8114. The PEX 8114 Serial EEPROM register initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	BCh
Class Code				**060400h**
15:8	**Programming Interface** The PEX 8114 supports the *PCI-to-PCI Bridge r1.1* requirements, but not subtractive decoding, on its upstream interface.	RO	Yes	00h
23:16	**Subclass Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 14-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Cache Line Size** Specifies the system Cache Line Size (in units of DWords). 00h = 1 DWord (32-bit bus); 2 DWords (64-bit bus) 01h = 1 DWord 02h = 2 DWords 04h = 4 DWords 08h = 8 DWords 10h = 16 DWords 20h = 32 DWords	R/W	Yes	00h
15:8	**Primary Latency Timer** **Forward Transparent Bridge mode:** Cleared to 00h, as required by the *PCI Express Base 1.0a.* **Reverse Transparent Bridge mode:** Specifies the Master Latency Timer (in units of PCI Bus clocks) when the primary interface is a Bus Master.	RO/Fwd R/W/Rev R/W/Rev	No Yes Yes	00h 00h (PCI) 40h (PCI-X)
22:16	**Header Type** The PEX 8114 Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.1*.	RO	No	01h
23	**Multi-Function** Always 0, because the PEX 8114 is a single-function device.	RO	No	0
31:24	**BIST** ***Not supported.*** Cleared to 00h.	RO	No	00h

Register 14-5. 10h Base Address 0

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** When enabled, the Base Address register maps the PEX 8114 Configuration registers into Memory space.	RO	No	0
2:1	**Memory Map Type** 00b = PEX 8114 Configuration registers can be mapped anywhere in 32-bit Memory Address space 10b = PEX 8114 Configuration registers can be mapped anywhere in 64-bit Memory Address space 01b, 11b = ***Reserved***	RO	Yes	00b
3	**Prefetchable** Base Address register maps the PEX 8114 Configuration registers into Non-Prefetchable Memory space by default.	RO	No	0
12:4	***Reserved***			000h
31:13	**Base Address** Base Address for PLX-specific Memory-Mapped Configuration Space Access mechanism.	R/W	Yes	0_0000h

Register 14-6. 14h Base Address 1

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address 1** For 64-bit addressing (**Base Address 0** register *Memory Map Type* field = 10b), Base Address 1 extends Base Address 0 to provide the upper 32 Address bits.	R/W	Yes	0000_0000h

Register 14-7. 18h Bus Number

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Record the Bus Number of the PCI Bus segment to which the primary interface of this bridge is connected. Set by Configuration software.	R/W	Yes	00h
15:8	**Secondary Bus Number** Record the Bus Number of the PCI Bus segment that is the secondary interface of this bridge. Set by Configuration software.	R/W	Yes	00h
23:16	**Subordinate Bus Number** Record the Bus Number of the highest numbered PCI Bus segment subordinate to this bridge. Set by Configuration software.	R/W	Yes	00h
31:24	**Secondary Latency Timer** **Forward Transparent Bridge mode:** Specifies the Master Latency Timer (in units of PCI Bus clocks) when the secondary interface is a Bus Master. **Reverse Transparent Bridge mode:** Cleared to 00h, as required by the *PCI Express Base 1.0a.*	R/W/Fwd R/W/Fwd RO/Rev	Yes Yes No	00h (PCI) 40h (PCI-X) 00h

Register 14-8. 1Ch Secondary Status, I/O Limit, and I/O Base

Bit(s)	Description	Type	Serial EEPROM	Default
	I/O Base			
3:0	**I/O Base Addressing Capability** 1h = 32-bit Address decoding is supported Other values are not allowed.	RO	No	1h
7:4	**I/O Base Address[15:12]** The PEX 8114 uses the **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from the primary interface to the secondary interface or vice versa. I/O Base Address[15:12] bits specify the corresponding PEX 8114 I/O Base Address[15:12]. The PEX 8114 assumes I/O Base Address[11:0] = 000h. The PEX 8114 decodes Address bits [31:0], and uses the *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits*.	R/W	Yes	0h
	I/O Limit			
11:8	**I/O Limit Addressing Capability** 1h = 32-bit Address decoding is supported Other values are not allowed.	RO	No	1h
15:12	**I/O Limit Address[15:12]** The PEX 8114 uses the **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from the primary interface to the secondary interface or vice versa. I/O Limit Address[15:12] specify the corresponding PEX 8114 I/O Limit Address[15:12]. The PEX 8114 assumes Address bits [11:0] of the I/O Limit Address are FFFh. The PEX 8114 decodes Address bits [31:0], and uses the *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits*. When the I/O Limit Address is less than the I/O Base Address, the PEX 8114 does not forward I/O transactions from the primary/upstream bus to its secondary/downstream bus. However, the PEX 8114 forwards all I/O transactions from the secondary bus to its primary bus.	R/W	Yes	0h

Register 14-8. 1Ch Secondary Status, I/O Limit, and I/O Base *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Secondary Status			
20:16	***Reserved***			0-0h
21	**66 MHz Enabled** **Forward Transparent Bridge mode:** PCI-X interface is capable of 66-MHz operation; therefore, this bit is set to 1. **Reverse Transparent Bridge mode:** Cleared to 0, as required by the *PCI Express Base 1.0a*.	RO/Fwd RO/Rev	No No	1 0
22	***Reserved***			0
23	**Fast Back-to-Back Transaction Enabled** **Forward Transparent Bridge mode:** Set to 1, indicating Fast Back-to-Back Transactions capable. **Reverse Transparent Bridge mode:** Cleared to 0, as required by the *PCI Express Base 1.0a*.	RO/Fwd RO/Rev	No No	1 0
24	**Master Data Parity Error** Reports Data Parity error detection by the bridge on the secondary interface. Set to 1 if the **Bridge Control** register *Parity Error Response Enable* bit is set and one of the following conditions occur. **Forward Transparent Bridge mode:** • Bridge, as a bus Master on the secondary interface, asserts PCI_PERR# on a Read transaction or detects PCI_PERR# asserted on a Write transaction • Bridge receives a Completion or Split Completion with a Parity error on the secondary interface • Bridge receives a Split Completion message for a Non-Posted Write, indicating an Uncorrectable (Split) Write Data error **Reverse Transparent Bridge mode:** • Bridge receives a Completion marked *poisoned* on the secondary interface • Bridge poisons a Write Request on the secondary interface	R/W1C	Yes	0
26:25	**DEVSEL Timing** **Forward Transparent Bridge mode:** Pertain to PCI and PCI-X modes. Encode PCI_DEVSEL# timing. For the PEX 8114, the field is set to 10b, indicating slow speed. **Reverse Transparent Bridge mode:** Cleared to 00b, as required by the *PCI Express Base 1.0a.*	RO/Fwd RO/Rev	No No	10b 00b
27	**Signaled Target Abort** **Forward Transparent Bridge mode:** When the PCI-X interface signals Target Abort, the PEX 8114 sets this bit to 1. **Reverse Transparent Bridge mode:** Set to 1 when the bridge completes a request as a Transaction Target on its secondary interface using Completer Abort Completion status.	R/W1C	Yes	0

Register 14-8. 1Ch Secondary Status, I/O Limit, and I/O Base *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
28	**Received Target Abort** **Forward Transparent Bridge mode:** Set to 1 when the bridge is the transaction Master terminated with a Target Abort or PCI-X Split Completion message indicating Target Abort was received. **Reverse Transparent Bridge mode:** Set to 1 when the bridge receives a Completion with Completer Abort Completion status.	R/W1C	Yes	0
29	**Received Master Abort** **Forward Transparent Bridge mode:** Set to 1 when the bridge is the transaction Master terminated by the bridge with Master Abort status. **Reverse Transparent Bridge mode:** Set to 1 when the bridge receives a Completion with Unsupported Request Completion status.	R/W1C	Yes	0
30	**Received System Error** **Forward Transparent Bridge mode:** Set to 1 when SERR# is asserted on the secondary interface of the bridge. **Reverse Transparent Bridge mode:** Set to 1 when an ERR_FATAL or ERR_NONFATAL message is received on the secondary interface of the bridge.	R/W1C	Yes	0
31	**Detected Parity Error** **Forward Transparent Bridge mode:** Reports the detection of an Address or Data Parity error by the bridge on its secondary interface. Must be set to 1, regardless of the **Bridge Control** register *Parity Error Response Enable* bit state, when any of the following three conditions is true: • Detects an Address or Attribute Parity error as a potential Target • Detects a Data Parity error when the Target of a Write transaction or PCI-X Split Completion • Detects a Data Parity error when the Master of a Read transaction (Immediate Read data or PCI-X Split Response) **Reverse Transparent Bridge mode:** Set to 1 by the bridge when it receives a Poisoned TLP or a TLP with bad ECRC (Read Completion or Write Request) on the secondary interface, regardless of the **Bridge Control** register *Parity Error Response Enable* bit state.	R/W1C	Yes	0

Note: *The PEX 8114 uses the **Memory Base and Limit Address** registers to determine the Address range of Non-Prefetchable Memory transactions to forward from one of its interfaces to the other.*

Register 14-9. 20h Memory Base and Limit Address

Bit(s)	Description	Type	Serial EEPROM	Default
Memory Base Address				
3:0	***Reserved***			0h
15:4	**Memory Base Address[31:20]** Specifies the PEX 8114 non-prefetchable Memory Base Address[31:20]. The PEX 8114 assumes Memory Base Address[19:0] = 00000h.	R/W	Yes	000h
Memory Limit Address				
19:16	***Reserved***			0h
31:20	**Memory Limit Address[31:20]** Specifies the PEX 8114 non-prefetchable Memory Limit Address[31:20]. The PEX 8114 assumes Memory Limit Address[19:0] = FFFFFh.	R/W	Yes	000h

Note: *The PEX 8114 uses the* ***Prefetchable Memory Base and Limit Address*** *register to determine the Address range of Prefetchable Memory transactions to forward from one of its interfaces to the other.*

Register 14-10. 24h Prefetchable Memory Base and Limit Address

Bit(s)	Description	Type	Serial EEPROM	Default
Prefetchable Memory Base Address				
3:0	**Prefetchable Memory Base Capability** 1h = PEX 8114 defaults to 64-bit Prefetchable Memory Addressing support	RO	Yes	1h
15:4	**Prefetchable Memory Base Address[31:20]** Specifies the PEX 8114 Prefetchable Memory Base Address[31:20]. The PEX 8114 assumes Prefetchable Memory Base Address[19:0] = 00000h. ***Note:*** *When the Prefetchable Memory Limit Address is less than the Prefetchable Memory Base Address, the PEX 8114 does* ***not*** *forward Prefetchable Memory transactions from the upstream bus to its downstream bus. However, the PEX 8114 forwards all Memory transactions from the downstream bus to its upstream bus.*	R/W	Yes	000h
Prefetchable Memory Limit Address				
19:16	**Prefetchable Memory Limit Capability** 1h = PEX 8114 defaults to 64-bit Prefetchable Memory Addressing support	RO	Yes	1h
31:20	**Prefetchable Memory Limit Address[31:20]** Specifies the PEX 8114 Prefetchable Memory Base Address[31:20]. The PEX 8114 assumes Prefetchable Memory Base Address[19:0] = FFFFFh.	R/W	Yes	000h

Register 14-11. 28h Prefetchable Memory Upper Base Address[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base Address[63:32]** The PEX 8114 uses this register for Prefetchable Memory Upper Base Address[63:32].	R/W	Yes	0000_0000h

Register 14-12. 2Ch Prefetchable Memory Upper Limit Address[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit Address[63:32]** The PEX 8114 uses this register for Prefetchable Memory Upper Limit Address[63:32].	R/W	Yes	0000_0000h

Register 14-13. 30h I/O Base Address[31:16] and I/O Limit Address[31:16]

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8114 uses this register for I/O Base Address[31:16].	R/W	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** The PEX 8114 uses this register for I/O Limit Address[31:16].	R/W	Yes	0000h

Register 14-14. 34h New Capability Pointer

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**New Capability Pointer** **PCI-X interface:** Default 48h points to the **Message Signaled Interrupt Capability List** register. **PCI Express interface:** Default 40h points to the **Power Management Capability List** register.	RO	No	48h (PCI-X) 40h (PCI Express)
31:8	***Reserved***			0000_00h

Register 14-15. 38h Expansion ROM Base Address

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Expansion ROM Base Address** ***Not supported.*** Cleared to 0000_0000h.	RO	No	0000_0000h

Register 14-16. 3Ch Bridge Control and Interrupt Signal

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Interrupt Line** The PEX 8114 does ***not*** use this register, but provides it for operating system and device driver use.	R/W	Yes	00h
15:8	**Interrupt Pin** Identifies the Conventional PCI Interrupt message that the PEX 8114 uses. 01h maps to Conventional PCI INTA# Interrupt message.	RO	No	01h
	Bridge Control			
16	**Parity Error Response Enable** Controls bridge response to Address and Data Parity errors on the secondary interface. If this bit is set, the bridge must detect and report Parity errors on the secondary interface. If cleared, the bridge must ignore Parity errors that it detects on the secondary interface and continue standard operation. A bridge must generate parity, although Parity Error reporting is disabled.	R/W	Yes	0
17	**SERR# Enable** **Forward Transparent Bridge mode:** Controls forwarding of secondary interface SERR# assertions to the primary interface. The bridge transmits an ERR_FATAL or ERR_NONFATAL cycle on the primary interface when all of the following conditions are true: • SERR# is asserted on the secondary interface • This bit is set • **Command** register *SERR# Enable* bit is set **Reverse Transparent Bridge mode:** Controls forwarding of ERR_FATAL and ERR_NONFATAL from the secondary interface to the primary interface by asserting SERR# when all the following conditions are true. • ERR_FATAL or ERR_NONFATAL is received on the secondary interface • This bit is set • **Command** register *SERR# Enable* bit is set When set to 1, and the **Command** register *SERR# Enable* bit value is 1, enables the *Signaled System Error* bit.	R/W	Yes	0
18	**ISA Enable** Refer to Section 5.2.1.3, "ISA Mode," for details.	R/W	Yes	0
19	**VGA Enable** Refer to Section 5.2.1.4, "VGA Mode," and the *PCI r3.0* for details.	R/W	Yes	0

Register 14-16. 3Ch Bridge Control and Interrupt Signal *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
20	**VGA 16-Bit Decode** Refer to Section 5.2.1.4, "VGA Mode," and the *PCI r3.0* for details.	R/W	Yes	0
21	**Master Abort Mode** Controls bridge behavior after it receives a Master Abort termination (*such as*, an Unsupported Request on PCI Express) on either interface. This bit does not affect the behavior of the bridge when forwarding a UR Completion from PCI Express to the PCI-X interface, if the PCI-X interface is operating in PCI-X mode. 0 = Do not report Master Aborts. Return FFFF_FFFFh on Reads and discard data on Writes initiated from the PCI-X interface (PCI-to-PCI Express). For Posted transactions initiated from the PCI Express interface (PCI Express-to-PCI), no action is taken (*that is*, all data is discarded). 1 = Report UR Completions from PCI Express by signaling Target Abort on the PCI-X interface operating in Conventional PCI mode (PCI-to-PCI Express). For Posted transactions initiated from the PCI Express interface (PCI Express-to-PCI) that experience a Master Abort on the PCI-X interface, the bridge must return ERR_FATAL or ERR_NONFATAL on the primary interface (provided the **Command** register *SERR# Enable* bit is set).	R/W	Yes	0
22	**Secondary Bus Reset** **Forward Transparent Bridge mode:** Setting this bit causes RST# to assert on the secondary interface. **Reverse Transparent Bridge mode:** Setting this bit causes a Hot Reset to communicate on the PEX 8114 secondary interface.	R/W	Yes	0
23	**Fast Back-to-Back Transaction Enable** ***Not supported.*** Cleared to 0.	RO	No	0

Register 14-16. 3Ch Bridge Control and Interrupt Signal *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
24	**Primary Discard Timer** Pertains to the PCI Bus in Conventional PCI mode and Reverse Transparent Bridge mode. Selects the number of PCI clocks that the bridge waits for a Master on the primary interface to repeat a Delayed Transaction request. The Counter starts after the Delayed Completion (the Delayed Transaction Completion on the secondary interface) reaches the head of the bridge's upstream queue (*that is*, all Ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating Master on the primary bus). If the originating Master does not repeat the transaction before the Counter expires, the bridge deletes the Delayed Transaction from its queue and sets the *Discard Timer Status* bit. 0 = Primary Discard Timer counts 2^{15} PCI Clock cycles 1 = Primary Discard Timer counts 2^{10} PCI Clock cycles	RO/Fwd R/W/Rev	No Yes	0 0
25	**Secondary Discard Timer** Pertains to the PCI Bus in Conventional PCI mode and Forward Transparent Bridge mode. Selects the number of PCI clocks the bridge waits for a Master on the secondary interface to repeat a Delayed Transaction request. The Counter starts after the Completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the bridge's downstream queue (*that is*, all Ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating Master on the secondary bus). If the originating Master does not repeat the transaction before the Counter expires, the bridge deletes the Delayed Transaction from its queue and set the *Discard Timer Status* bit. 0 = Secondary Discard Timer counts 2^{15} PCI Clock cycles 1 = Secondary Discard Timer counts 2^{10} PCI Clock cycles	R/W/Fwd RO/Rev	Yes No	0 0
26	**Discard Timer Status** Pertains to the PCI Bus in Conventional PCI mode. Set to 1 when the *Primary Discard Timer* or *Secondary Discard Timer* expires and a Delayed Completion is discarded from a queue in the bridge. The default state of this bit after reset must be 0. Once set, remains set until it is reset by writing 1 to this bit location.	R/W1C	Yes	0
27	**Discard Timer SERR# Enable** Pertains to the PCI Bus in Conventional PCI mode. When set to 1, enables the bridge to generate an ERR_FATAL or ERR_NONFATAL transaction when the *Secondary Discard Timer* expires and a Delayed Transaction is discarded from a queue in the bridge.	R/W	Yes	0
31:28	***Reserved***			0h

14.5 Power Management Capability Registers

This section details the PEX 8114 **Power Management** registers. Table 14-4 defines the register map.

Table 14-4. Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Power Management Capabilities		Next Capability Pointer (48h)	Capability ID (01h)	40h
Data	Power Management Control/ Status Bridge Extensions	Power Management Status and Control		44h

Register 14-17. 40h Power Management Capability List, Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
Power Management Capability List				
7:0	**Capability ID** Default 01h indicates that the data structure currently pointed to is the PCI Power Management data structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **Message Signaled Interrupt Capability List** register.	RO	Yes	48h
Power Management Capabilities				
18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	RO	Yes	011b
19	**PME Clock** Set to 1, as required by the *PCI Express Base 1.0a.*	RO	No	1
20	***Reserved***			0h
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** ***Not supported.*** Default 000b indicates that the PEX 8114 does ***not support*** Auxiliary Current requirements.	RO	Yes	000b
25	**D1 Support** ***Not supported.*** Default 0 indicates that the PEX 8114 does ***not support*** the D1 Power state.	RO	No	0
26	**D2 Support** ***Not supported.*** Default 0 indicates that the PEX 8114 does ***not support*** the D2 Power state.	RO	No	0
31:27	**PME Support** Default 11001b indicates that the PEX 8114 forwards PME messages in the D0, D3hot, and D3cold power states.	RO	Yes	11001b

Register 14-18. 44h Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
Power Management Status and Control				
1:0	**Power State** Reports the PEX 8114 power state. 00b = D0 11b = D3hot 01b and 10b = ***Not supported***	R/W	Yes	00b
2	***Reserved***			0
3	**No Soft Reset** When set to 1, indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset.	RO	Yes	1
7:4	***Reserved***			0h
8	**PME Enable** 0 = Disables PME generation by the PEX 8114[a] 1 = Enables PME generation by the PEX 8114	R/WS	No	0
12:9	**Data Select** R/W by Serial EEPROM mode[b]. Bits [12:9] select the **Data** and **Data Scale** registers. 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	RO	Yes	0h
	Not supported. RO for hardware auto-configuration.	RO	No	0h
14:13	**Data Scale** R/W by Serial EEPROM mode[b]. There are four internal **Data Scale** registers. Bits [12:9], *Data Select*, select the **Data Scale** register.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the PEX 8114[a] 1 = PME is generated by the PEX 8114	R/W1C	No	0
Power Management Control/Status Bridge Extensions				
21:16	***Reserved***			0-0h
22	**B2/B3 Support** Cleared to 0, as required by the *PCI Power Mgmt. r1.2*.	RO	No	0
23	**Bus Power/Clock Control Enable** Cleared to 0, as required by the *PCI Power Mgmt. r1.2*.	RO	No	0
Power Management Data				
31:24	**Data** R/W by Serial EEPROM mode[b]. There are four internal Data registers. Bits [12:9], *Data Select*, select the **Data** register.	RO	Yes	00h

a. Because the PEX 8114 does not support auxiliary power, this bit is not sticky, and is cleared to 0 at power-on reset.

*b. Without serial EEPROM, Reads return 00h for **Data Scale** and **Data** registers (for all Data Selects).*

14.6 Message Signaled Interrupt Capability Registers

This section details the PEX 8114 **Message Signaled Interrupt (MSI) Capability** registers. Table 14-5 defines the register map.

Table 14-5. Message Signaled Interrupt Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Message Signaled Interrupt Control		Next Capability Pointer (58h if PCI-X; 68h if PCI Express)	Capability ID (05h)	48h
Lower Message Address[31:0]				4Ch
Upper Message Address[63:32]				50h
Reserved		Message Data		54h

Register 14-19. 48h Message Signaled Interrupt Capability List, Control

Bit(s)	Description	Type	Serial EEPROM	Default
Message Signaled Interrupt Capability List				
7:0	**Capability ID** Set to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** **PCI-X interface:** Set to 58h to point to the PEX 8114 PCI-X Capability registers. **PCI Express interface:** Set to 68h to point to the PEX 8114 PCI Express Capabilities registers.	RO	Yes	58h (PCI-X) 68h (PCI Express)
Message Signaled Interrupt Control				
16	**MSI Enable** 0 = Message Signaled Interrupts for the PEX 8114 are disabled 1 = Message Signaled Interrupts for the PEX 8114 are enabled	R/W	Yes	0
19:17	**Multiple Message Capable** 000b = PEX 8114 is requesting one message – only value supported	RO	Yes	000b
22:20	**Multiple Message Enable** 000b = PEX 8114 contains one allocated message – only value supported	R/W	Yes	000b
23	**MSI 64-Bit Address Capable** 1 = PEX 8114 is capable of generating 64-bit Message Signaled Interrupt addresses	RO	Yes	1
31:24	***Reserved***			00h

Register 14-20. 4Ch Lower Message Address[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	***Reserved***			00b
31:2	**Message Address[31:2]** MSI Write transaction lower address[31:2]. ***Note:*** *Refer to offset 50h for Upper Message Address[63:32].*	R/W	Yes	0000_0000h

Register 14-21. 50h Upper Message Address[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Message Address[63:32]** MSI Write transaction upper address[63:32]. ***Note:*** *Refer to offset 4Ch for Lower Message Address[31:2].*	R/W	Yes	0000_0000h

Register 14-22. 54h Message Data

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Message Data** MSI Write Transaction Payload.	R/W	Yes	0000h
31:16	***Reserved***			0000h

14.7 PCI-X Capability Registers

This section details the PEX 8114 **PCI-X Capability** registers. Table 14-6 defines the register map.

Table 14-6. PCI-X Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-X Secondary Status		Next Capability Pointer (68h)	Capability ID (07h)	58h
PCI-X Bridge Status				5Ch
Upstream Split Transaction Control				60h
Downstream Split Transaction Control				64h

Register 14-23. 58h PCI-X Capability List, Secondary Status

Bit(s)	Description	Type	Serial EEPROM	Default
PCI-X Capability List				
7:0	**Capability ID** Set to 07h.	RO	No	07h
15:8	**Next Capability Pointer** Set to 68h to point to PEX 8114 PCI Express Capabilities registers.	RO	No	68h
PCI-X Secondary Status				
16	**64-Bit Device** Pertains to the PCI-X interface in Forward Transparent Bridge mode. When set to 1, indicates that the PCI-X interface has 64 AD lines.	RO/Fwd RO/Rev	Yes No	1 0
17	**133 MHz Capable** Pertains to the PCI-X interface in Reverse Transparent Bridge mode and PCI-X mode. When set to 1, indicates that the PCI-X interface is capable of operating with a clock frequency of 133 MHz. 0 = Maximum operating clock frequency is 66 MHz 1 = Maximum operating clock frequency is 133 MHz	RO/Fwd RO/Rev	No No	1 0
18	**Split Completion Discarded** Pertains to the PCI-X interface in Forward Transparent Bridge mode.This bit is set if the bridge discards a Split Completion propagating downstream toward the secondary bus because the requester does not accept it. 0 = Split Completion is not discarded 1 = Split Completion is not discarded	R/W1C/Fwd RO/Rev	No No	0 0
19	**Unexpected Split Completion** Pertains to the PCI-X interface in Forward Transparent Bridge mode and the PCI Express interface in Reverse Transparent Bridge mode. This bit is set if a Split Completion is received on the PCI-X interface and there is no matching request. 0 = Unexpected Split Completion is not received 1 = Unexpected Split Completion is received	R/W1C	No	0

Register 14-23. 58h PCI-X Capability List, Secondary Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
20	**Split Completion Overrun** Pertains to the PCI-X interface in Forward Transparent Bridge mode. This bit is set if the bridge terminates a Split Completion on the secondary bus with Retry or Disconnect at Next ADB because the bridge buffers are full. Used by algorithms that optimize the downstream *Split Transaction Commitment Limit* field setting. (Refer to the *PCI-X r2.0a*, Appendix D, for further details.) The bridge is also permitted to set this bit in other situations that indicate that the bridge commitment limit is overly high. *For example*, if the bridge stores Immediate Completion data in the same buffer area as Split Completion data, the completer executes the transaction as an Immediate transaction, and the bridge disconnects the transaction because the buffers are full. 0 = Bridge accepted all Split Completions 1 = Bridge terminated a Split Completion with Retry or Disconnect at Next ADB because the bridge buffers are full	R/W1C/Fwd RO/Rev	No No	0 0
21	**Split Request Delayed** Pertains to the PCI-X interface in Forward Transparent Bridge mode and the PCI Express interface in Reverse Transparent Bridge mode. This bit is set when the PCI-X interface cannot forward a transaction due to a lack of space specified in the **Downstream Split Transaction Control** register *Split Transaction Commitment Limit* field. (Refer to the *PCI-X r2.0a*, Appendix D, for further details.) 0 = Bridge does not delayed a Split Request 1 = Bridge does delay a Split Request	R/W1C/Fwd R/W1C/Rev	No No	0 0
25:22	**Secondary Clock Bus Mode and Frequency** Pertains to the PCI-X interface in Forward Transparent Bridge mode. Provides a code that indicates to software the mode and frequency in which the PCI-X interface is operating. **Reg Mode** / **Error Protection** / **Max. Clock Freq. (MHz)** / **Min. Clock Period (ns)** 0h / Conventional PCI parity / N/A / N/A 1h / PCI-X Mode 1 parity / 66 / 15 2h / PCI-X Mode 1 parity / 100 / 10 3h / PCI-X Mode 1 parity / 133 / 7.5	RO/Fwd RO/Rev	No No	0h 0h
27:26	***Reserved***			00b
29:28	**PCI-X Capabilities List Item Version** Pertains to the PCI-X interface in Forward Transparent Bridge mode. Indicates the PCI-X Capabilities List item format, and whether the bridge supports ECC in Mode 1. **Value** / **Version** / **ECC Support Capabilities** / **List Item Size** 00b / 0 / None / 16 bytes 01b / 1 / Mode 2, not Mode 1 / 32 bytes 10b / 2 / Mode 1 or Modes 1 and 2 / 32 bytes 11b / ***Reserved***	RO/Fwd RO/Rev	No No	00b 00b
30	**PCI-X 266 Capable** ***Not supported.*** Cleared to 0.	RO	No	0
31	**PCI-X 533 Capable** ***Not supported.*** Cleared to 0.	RO	No	0

Register 14-24. 5Ch PCI-X Bridge Status

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Function Number** Contains the PEX 8114 Function Number. This number is used in the Completer ID.	RO	No	000b
7:3	**Device Number** Contains the PEX 8114 Device Number. **Forward Transparent Bridge mode:** This number is assigned by the number in the Device Number field of the Type 0 Configuration Write Request targeted to this device on the PCI Express interface. **Reverse Transparent Bridge mode:** The Device Number is assigned by the Device Number field in the Type 0 Configuration Transaction targeted to the device on the PCI-X interface. This number is used in the Completer ID.	RO/Fwd RO/Rev	No No	00h 1Fh
15:8	**Bus Number** This number is a second register for software to read the value of the Bus Number written into the *Primary Bus Number* at offset 18h. This number is used in the Completer ID.	RO	No	00h
16	**64-Bit Device** Pertains to the PCI-X interface in Reverse Transparent Bridge mode. When set to 1, indicates that the PCI-X interface has 64 AD lines.	RO/Fwd RO/Rev	No Yes	0 1
17	**133 MHz Capable** Pertains to the PCI-X interface in Forward Transparent Bridge mode and PCI-X mode. When set to 1, indicates that the PCI-X interface is capable of operating with a clock frequency of 133 MHz. 0 = Maximum operating clock frequency is 66 MHz 1 = Maximum operating clock frequency is 133 MHz	RO/Fwd RO/Rev	No No	0 1
18	**Split Completion Discarded** Pertains to the PCI-X interface in Reverse Transparent Bridge mode. This bit is set if the bridge discards a Split Completion propagating downstream toward the secondary bus because the requester would not accept it. 0 = Split Completion is not discarded 1 = Split Completion is discarded	RO/Fwd R/W1C/Rev	No No	0 0
19	**Unexpected Split Completion** Pertains to the PCI-X interface in Reverse Transparent Bridge mode and the PCI Express interface in Forward Transparent Bridge mode. This bit is set if a Split Completion is received on the PCI-X interface and there is no matching request. 0 = Unexpected Split Completion is not received 1 = Unexpected Split Completion was received	R/W1C/Fwd R/W1C/Rev	No No	0 0

Register 14-24. 5Ch PCI-X Bridge Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
20	**Split Completion Overrun** Pertains to the PCI-X interface in Reverse Transparent Bridge mode. This bit is set if the bridge terminates a Split Completion on the secondary bus with Retry or Disconnect at Next ADB because the bridge buffers are full. Used by algorithms that optimize the downstream *Split Transaction Commitment Limit* field setting. (Refer to the *PCI-X r2.0a*, Appendix D, for further details.) The bridge is also permitted to set this bit in other situations that indicate that the bridge commitment limit is overly high. *For example*, if the bridge stores immediate Completion data in the same buffer area as Split Completion data, the completer executes the transaction as an Immediate transaction, and the bridge disconnects the transaction because the buffers became full. 0 = Bridge accepted all Split Completions 1 = Bridge terminated a Split Completion with Retry or Disconnect at Next ADB because the bridge buffers are full	RO/Fwd R/W1C/Rev	No No	0 0
21	**Split Request Delayed** Pertains to the PCI-X interface in Reverse Transparent Bridge mode and the PCI Express interface in Forward Transparent Bridge mode. This bit is set when the PCI-X interface cannot forward a transaction due to a lack of space specified in the **Downstream Split Transaction Control** register *Split Transaction Commitment Limit* field. (Refer to the *PCI-X r2.0a*, Appendix D, for further details.) 0 = Bridge is not delayed a Split Request 1 = Bridge delayed a Split Request	R/W1C/Fwd R/W1C/Rev	No No	0 0
28:22	***Reserved***			00h
29	**Device ID Messaging Capable** ***Not supported.*** Cleared to 0.	RO	No	0
30	**PCI-X 266 Capable** ***Not supported.*** Cleared to 0.	RO	No	0
31	**PCI-X 533 Capable** ***Not supported.*** Cleared to 0.	RO	No	0

Register 14-25. 60h Upstream Split Transaction Control

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Split Transaction Capacity** Indicates the Buffer Size (in ADQs) available for storage of Completions for requests on the secondary interface that are addressing completers on the primary interface.	RO	No	0010h
31:16	**Split Transaction Commitment Limit** Indicates the Sequence Size (in units of ADQs) for Read transactions forwarded by the bridge from requesters on the secondary interface, to completers on the primary interface. (Refer to the *PCI-X r2.0a*, Appendix D, for a detailed discussion of Split Transaction commitment.) When the bridge stores Split Read Completions in the same buffer as other Split Completions, this register indicates the size of all upstream Split Transactions of these types that the bridge is permitted to commit to at one time. Software is permitted to program this register to a value greater than or equal to the contents of the Split Transaction Capacity register. A value less than the contents of the Split Transaction Capacity register causes unspecified results. When this register is set to FFFFh, the bridge is permitted to forward all Split Requests of any size, regardless of available buffer space (an exception is described in Section 2.6, "Strapping Signals"). Software is permitted to change this register at any time. The most recent value of the register is used each time the bridge forwards a Split Transaction. If the register value is set to FFFFh, the bridge does not track the outstanding commitment. If the register is later set to another value, the bridge does not accurately track outstanding commitments until all outstanding commitments complete. Systems that require accurate limitation of Split Transactions must never set this register to FFFFh. They must quiesce all devices that initiate traffic that crosses the bridge in this direction after the register setting is changed from FFFFh. An algorithm for setting this register is not specified. System software is permitted to use any method for selecting the value for this register. Individual devices and device drivers are not permitted to change the value of this register except under control of a system-level configuration routine. (Refer to the *PCI-X r2.0a*, Appendix D, for details and setting recommendations.) Default value of this field equals the value stored in the *Split Transaction Capacity* field.	R/W	Yes	0010h

Register 14-26. 64h Downstream Split Transaction Control

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Split Transaction Capacity** Indicates the Buffer Size (in ADQs) available for storage of Completions for requests on the primary interface that are addressing completers on the secondary interface.	RO	No	0010h
31:16	**Split Transaction Commitment Limit** Indicates the Sequence Size (in units of ADQs) for Read transactions forwarded by the bridge from requesters on the primary interface, to completers on the secondary interface. (Refer to the *PCI-X r2.0a*, Appendix D, for a detailed discussion of Split Transaction commitment.) If the bridge stores Split Read Completions in the same buffer as other Split Completions, this register indicates the size of all downstream Split Transactions of these types that the bridge is permitted to commit to at one time. Software is permitted to program this register to a value greater than or equal to the contents of the Split Transaction Capacity register. A value less than the contents of the Split Transaction Capacity register causes unspecified results. If this register is set to FFFFh, the bridge is permitted to forward all Split Request of any size, regardless of available buffer space. Software is permitted to change this register at any time. The most recent value of the register is used each time the bridge forwards a Split Transaction. When the register value is set to FFFFh, the bridge does not track the outstanding commitment. If the register is later set to another value, the bridge does not accurately track outstanding commitments until all outstanding commitments complete. Systems that require accurate limitation of Split Transactions must never set this register to FFFFh. They must quiesce all devices that initiate traffic that crosses the bridge in this direction after the register setting is changed from FFFFh. An algorithm for setting this register is not specified. System software is permitted to use any method for selecting the value for this register. Individual devices and device drivers are not permitted to change the value of this register except under control of a system-level configuration routine. (Refer to the *PCI-X r2.0a* for details and setting recommendations.) Default value of this field equals the value stored in the *Split Transaction Capacity* field.	R/W	Yes	0010h

14.8 PCI Express Capabilities Registers

This section details the PEX 8114 **PCI Express Capabilities** registers. Hot Plug capability, command, status, and events are included in these registers. Table 14-7 defines the register map.

Table 14-7. PCI Express Capabilities Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capabilities		Next Capability Pointer (00h)	Capability ID (10h)	68h
Device Capabilities				6Ch
Device Status		Device Control		70h
Link Capabilities				74h
Link Status		***Reserved***	Link Control	78h
Slot Capabilities (Reverse Transparent Bridge Mode Only)				7Ch
Slot Status (Reverse Transparent Bridge Mode Only)		Slot Control (Reverse Transparent Bridge Mode Only)		80h

Register 14-27. 68h PCI Express Capability List, Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
PCI Express Capability List				
7:0	**Capability ID** Set to 10h, as required by the *PCI Express Base 1.0a.*	RO	Yes	10h
15:8	**Next Capability Pointer** 00h = PCI Express Capabilities is the last capability in the PEX 8114 Capabilities list The PEX 8114 Extended Capabilities list starts at 100h.	RO	Yes	00h
PCI Express Capabilities				
19:16	**Capability Version** The PEX 8114 sets this field to 1h, as required by the *PCI Express Base 1.0a.*	RO	Yes	1h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base 1.0a.*	RO/Fwd RO/Rev	Yes Yes	7h 8h
24	**Slot Implemented** **Forward Transparent Bridge mode:** 0 = Disables or connects to an upstream port **Reverse Transparent Bridge mode:** 0 = Disables or connects to an integrated component[a] 1 = Indicates that the downstream port connects to a slot, as opposed to connected to an integrated component or disabled	RO/Fwd RO/Rev	No Yes	0 1
29:25	**Interrupt Message Number** The Serial EEPROM writes 0000_0b, because the Base message and MSI messages are the same.	RO	Yes	0000_0b
31:30	***Reserved***			00b

a. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0h, indicating that the PEX 8114 downstream port connects to an integrated component or is disabled.

Register 14-28. 6Ch Device Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Maximum Payload Size Supported** 000b = PEX 8114 supports 128-byte maximum Payload 001b = PEX 8114 supports 256-byte maximum Payload No other values are supported.	RO	Yes	001b
4:3	**Phantom Functions** ***Not supported.*** Cleared to 00b.	RO	Yes	00b
5	**Extended Tag Field** 0 = Maximum Tag field is 5 bits 1 = Maximum Tag field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported.*** Because the PEX 8114 is a bridge and not an endpoint, it does not support this feature. 000b = Disables the capability	RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported.*** Because the PEX 8114 is a bridge and not an endpoint, it does not support this feature. 000b = Disables the capability	RO	Yes	000b

Register 14-28. 6Ch Device Capabilities *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
12	**Attention Button Present** **Forward Transparent Bridge mode:** For the PEX 8114 PCI Express interface, value of 1 indicates that an Attention Button is implemented on that adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Button is ***not*** present on an adapter board for which the PEX 8114 provides the system interface. **Reverse Transparent Bridge mode:** Not valid for Reverse Transparent Bridge mode.	HwInit/Fwd RO/Rev	Yes No	1 0
13	**Attention Indicator Present** **Forward Transparent Bridge mode:** For the PEX 8114 PCI Express interface, value of 1 indicates that an Attention Indicator is implemented on the adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating that an Attention Indicator is ***not*** present on an adapter board for which the PEX 8114 provides the system interface. **Reverse Transparent Bridge mode:** Not valid for Reverse Transparent Bridge mode.	HwInit/Fwd RO/Rev	Yes No	1 0
14	**Power Indicator Present** **Forward Transparent Bridge mode:** For the PEX 8114 PCI Express interface, value of 1 indicates that a Power Indicator is implemented on the adapter board. The PEX 8114 Serial EEPROM register initialization capability is used to change this value to 0, indicating that a Power Indicator is ***not*** present on an adapter board for which the PEX 8114 provides the system interface. **Reverse Transparent Bridge mode:** Not valid for Reverse Transparent Bridge mode.	HwInit/Fwd RO/Rev	Yes No	1 0
17:15	***Reserved***			000b
25:18	**Captured Slot Power Limit Value** **Forward Transparent Bridge mode:** The upper limit on power supplied by the slot to the PEX 8114 is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Scale* field. **Reverse Transparent Bridge mode:** Not valid for Reverse Transparent Bridge mode.	RO/Fwd RO/Rev	Yes No	00h 00h
27:26	**Captured Slot Power Limit Scale** **Forward Transparent Bridge mode:** The upper limit on power supplied by the slot to the PEX 8114 is determined by multiplying the value in this field by the value in the *Captured Slot Power Limit Value* field. 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001 **Reverse Transparent Bridge mode:** Not valid for Reverse Transparent Bridge mode.	RO/Fwd RO/Rev	Yes No	00b 00b
31:28	***Reserved***			0h

Register 14-29. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Control			
0	**Correctable Error Reporting Enabled** 0 = Disables 1 = Enables PEX 8114 to report Correctable errors	R/W	Yes	0
1	**Non-Fatal Error Reporting Enabled** 0 = Disables 1 = Enables PEX 8114 to report Non-Fatal errors	R/W	Yes	0
2	**Fatal Error Reporting Enabled** 0 = Disables 1 = Enables PEX 8114 to report Fatal errors	R/W	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables PEX 8114 to report Unsupported Request errors	R/W	Yes	0
4	**Relaxed Ordering Enabled** ***Not supported.*** Cleared to 0.	RO	No	0
7:5	**Maximum Payload Size** Power-on/reset value is 000b, indicating that initially the PEX 8114 is configured to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the PEX 8114 to support Payload Sizes of 256 or 128. Software must not change this field to values other than those indicated by the **Device Capabilities** register *Maximum Payload Size Supported* field.	R/W	Yes	000b
8	**Extended Tag Field Enabled** ***Not supported.*** Cleared to 0.	RO	No	0
9	**Phantom Functions Enable** ***Not supported.*** Cleared to 0.	RO	No	0
10	**AUX Power PM Enable** ***Not supported.*** Cleared to 0.	RO	No	0
11	**No Snoop Enable** ***Not supported.*** Cleared to 0.	RO	No	0
14:12	**Maximum Read Request Size** Specifies the maximum size (in bytes) of a Read request generated by the PEX 8114. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes (default) 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = ***Reserved***	R/W	Yes	010b
15	**Bridge Configuration Retry Enable**	R/W	Yes	0

Register 14-29. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Device Status			
16	**Correctable Error Detected** 1 = PEX 8114 detected a Correctable error Set when the PEX 8114 detects a Correctable error, regardless of the *Correctable Error Reporting Enabled* bit state.	R/W1C	Yes	0
17	**Non-Fatal Error Detected** 1 = PEX 8114 detected a Non-Fatal error Set when the PEX 8114 detects a Non-Fatal error, regardless of the *Non-Fatal Error Reporting Enabled* bit state.	R/W1C	Yes	0
18	**Fatal Error Detected** 1 = PEX 8114 detected a Fatal error Set when the PEX 8114 detects a Fatal error, regardless of the *Fatal Error Reporting Enabled* bit state.	R/W1C	Yes	0
19	**Unsupported Request Detected** 1 = PEX 8114 detected an Unsupported Request Set when the PEX 8114 detects an Unsupported Request, regardless of the *Unsupported Request Reporting Enable* bit state.	R/W1C	Yes	0
20	**AUX Power Detected** ***Not supported.*** Cleared to 0.	RO	No	0
21	**Transactions Pending** When set to 1, indicates that the bridge is waiting for a Completion from an outstanding transaction.	RO	No	0
31:22	***Reserved***			000h

Register 14-30. 74h Link Capabilities

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Maximum Link Speed** Set to 0001b, as required by the *PCI Express Base 1.0a* for 2.5 Gbps PCI Express link.	RO	Yes	0001b
9:4	**Maximum Link Width** Maximum link width is x4 = 00_0100b.	RO	No	00_0100b
11:10	**Active-State Power Management Support** 01b = PEX 8114 supports the L0s Link power state 11b = PEX 8114 supports the L0s and L1 Link power states All other values are ***reserved***.	RO	Yes	11b
14:12	**L0s Exit Latency** 101b = PEX 8114 L0s Exit Latency is between 1 and 2 µs	RO	No	101b
17:15	**L1 Exit Latency** 101b = PEX 8114 L1 Exit Latency is between 16 and 32 µs	RO	Yes	101b
23:18	***Reserved***			0-0h
31:24	**Port Number** Port number is 0.	RO	No	00h

Register 14-31. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Link Control			
1:0	**Active-State Power Management Control** 00b = Disables L0s and L1 Entries for the PEX 8114 PCI Express port[a] 01b = Enables only L0s Entry 10b = Enables only L1 Entry 11b = Enables both L0s and L1 Entries	R/W	Yes	00b
2	***Reserved***			0
3	**Read Completion Boundary** Specifies the naturally occurring boundary on which a Read request can be broken up into smaller Completions than the original size of the request. Defined encodings are: 0 = 64 bytes 1 = 128 bytes	R/W	Yes	0
4	**Link Disable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** When set to 1, disables the PEX 8114 downstream PCI Express link.	RO/Fwd R/W/Rev	No Yes	0 0
5	**Retrain Link** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Writing 1 to this bit causes the PEX 8114 to initiate retraining of its PCI Express link. When read, always returns 0.	RO/Fwd RO/Rev	No Yes	0 0
6	**Common Clock Configuration** 0 = PEX 8114 and the device at the other end of the PCI Express link are operating with an **asynchronous** reference clock 1 = PEX 8114 and the device at the other end of the PCI Express link are operating with a **distributed** common reference clock	R/W	Yes	0
7	**Extended Sync** When set to 1, causes the PEX 8114 to transmit: • 4,096 FTS Ordered-Sets in the L0s state • Followed by a single SKIP Ordered-Set prior to entering the L0 state • Finally, transmission of 1,024 TS1 Ordered-Sets in the Recovery state	R/W	Yes	0
15:8	***Reserved***			00h

Register 14-31. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Link Status			
19:16	**Link Speed** Set to 1h, as required by the *PCI Express Base 1.0a* for 2.5 Gbps PCI Express link.	RO	Yes	1h
25:20	**Negotiated Link Width** Link width is determined by negotiated value with attached port/lane. 00_0001b = x1 00_0010b = x2 00_0100b = x4 (default) All other values are ***not supported***.	RO	Yes	00_0100b
26	**Training Error** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** When set to 1, indicates that the PEX 8114 detected a Link Training error.	RO/Fwd RO/Rev	No Yes	0 0
27	**Link Training** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** When set to 1, indicates that the PEX 8114 PCI Express interface requested link training and the link training is in progress or about to start.	RO/Fwd RO/Rev	No No	0 0
28	**Slot Clock Configuration** 0 = Indicates PEX 8114 uses an independent clock 1 = Indicates PEX 8114 uses the same physical reference clock that the platform provides on the connector	HwInit	Yes	0
31:29	***Reserved***			000b

a. The port receiver must be capable of entering the L0s state, regardless of whether the state is disabled.

Register 14-32. 7Ch Slot Capabilities *(Reverse Transparent Bridge Mode Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Attention Button Present** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the PEX 8114 PCI Express interface	RO/Fwd HwInit/Rev	No Yes	0 1
1	**Power Controller Present** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Power Controller is not implemented 1 = Power Controller is implemented for the slot of the PEX 8114 PCI Express interface	RO/Fwd HwInit/Rev	No Yes	0 1
2	**MRL Sensor Present** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = MRL Sensor is not implemented 1 = MRL Sensor is implemented on the slot chassis of the PEX 8114 PCI Express interface	RO/Fwd HwInit/Rev	No Yes	0 1
3	**Attention Indicator Present** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Attention Indicator is not implemented 1 = Attention Indicator is implemented on the slot chassis of the PEX 8114 PCI Express interface	RO/Fwd HwInit/Rev	No Yes	0 1

Register 14-32. 7Ch Slot Capabilities *(Reverse Transparent Bridge Mode Only) (Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
4	**Power Indicator Present** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Power Indicator is not implemented 1 = Power Indicator is implemented on the slot chassis of the PEX 8114 PCI Express interface	RO/Fwd HwInit/Rev	No Yes	0 1
5	**Hot Plug Surprise** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = No device in the PEX 8114 PCI Express interface slot is removed from the system, without prior notification 1 = Device in the PEX 8114 PCI Express interface slot can be removed from the system, without prior notification	RO/Fwd HwInit/Rev	No Yes	0 0
6	**Hot Plug Capable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = PEX 8114 PCI Express interface slot is not capable of supporting Hot Plug operations 1 = PEX 8114 PCI Express interface slot is capable of supporting Hot Plug operations	RO/Fwd HwInit/Rev	No Yes	0 1
14:7	**Slot Power Limit Value** **Forward Transparent Bridge mode:** Do not change in Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** The maximum power available from the PEX 8114 PCI Express interface is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the value specified by the *Slot Power Limit Scale* field.	RO/Fwd HwInit/Rev	No Yes	00h 19h
16:15	**Slot Power Limit Scale** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** The maximum power available from the PEX 8114 PCI Express interface is determined by multiplying the value in this field by the *Slot Power Limit Value* field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO/Fwd HwInit/Rev	No Yes	00b 00b
18:17	***Reserved***			00b
31:19	**Physical Slot Number** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Specifies a non-zero identification number for the PEX 8114 PCI Express port slot.	RO/Fwd HwInit/Rev	No Yes	0-0h 0-0h

Register 14-33. 80h Slot Status and Control *(Reverse Transparent Bridge Mode Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Slot Control			
0	**Attention Button Pressed Enabled** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event on an Attention Button Pressed event on the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0
1	**Power Fault Detected Enable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event on a Power Fault event on the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0
2	**MRL Sensor Change Enable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event on an MRL Sensor Change event on the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0
3	**Presence Detect Change Enable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event on a Presence Detect Change event on the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0

Register 14-33. 80h Slot Status and Control *(Reverse Transparent Bridge Mode Only) (Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
4	**Command Completed Interrupt Enable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt or Wakeup event when a command is completed by the Hot Plug Controller on the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0
5	**Hot Plug Interrupt Enable** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** 0 = Function disabled 1 = Enables a Hot Plug Interrupt on any enabled Hot Plug events for the PEX 8114 PCI Express port	RO/Fwd R/W/Rev	No Yes	0 0
7:6	**Attention Indicator Control** **Forward Transparent Bridge mode:** Do not change for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Controls the Attention Indicator on the PEX 8114 PCI Express port slot. 00b = ***Reserved – Do not use*** 01b = Turns On indicator to constant On state 10b = Causes indicator to Blink 11b = Turns Off indicator Writes cause the PEX 8114 PCI Express port to transmit the appropriate Attention Indicator messages. Reads return the PEX 8114 PCI Express port Attention Indicator's current state.	RO/Fwd R/W/Rev	No Yes	00b 11b
9:8	**Power Indicator Control** **Forward Transparent Bridge mode:** Do not change for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Controls the Power Indicator on the PEX 8114 PCI Express port slot. 00b = ***Reserved – Do not use*** 01b = Turns On indicator to constant On state 10b = Causes indicator to Blink 11b = Turns Off indicator Writes cause the PEX 8114 PCI Express port to transmit the appropriate Power Indicator message. Reads return the PEX 8114 PCI Express port Power Indicator's current state.	RO/Fwd R/W/Rev	No Yes	00b 11b
10	**Power Controller Control** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Controls the PEX 8114 PCI Express port Slot Power Controller: 0 = Turns On Power Controller 1 = Turns Off Power Controller	RO/Fwd R/W/Rev	No Yes	0 1
15:11	***Reserved***			0-0h

Register 14-33. 80h Slot Status and Control *(Reverse Transparent Bridge Mode Only) (Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
	Slot Status			
16	**Attention Button Pressed** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Set to 1 when the PEX 8114 PCI Express port slot Attention Button is pressed.	RO/Fwd R/W1C/Rev	No Yes	0 0
17	**Power Fault Detected** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Set to 1 when the PEX 8114 PCI Express port Slot Power Controller detects a Power Fault at the slot.	RO/Fwd R/W1C/Rev	No Yes	0 0
18	**MRL Sensor Changed** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Set to 1 when an MRL state change is detected on the PEX 8114 PCI Express port slot.	RO/Fwd R/W1C/Rev	No Yes	0 0
19	**Presence Detect Changed** **Forward Transparent Bridge mode:** Not valid for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Set to 1 when a Presence Detect Change is detected on the PEX 8114 PCI Express port slot.	RO/Fwd R/W1C/Rev	No Yes	0 0
20	**Command Completed** **Forward Transparent Bridge mode:** Do not change for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Set to 1 when the PEX 8114 PCI Express port slot Hot Plug Controller completes an issued command.	RO/Fwd R/W1C/Rev	No Yes	0 0
21	**MRL Sensor State** **Forward Transparent Bridge mode:** Do not change for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Reveals the PEX 8114 PCI Express port MRL sensor's current state. 0 = MRL sensor closed 1 = MRL sensor open	RO/Fwd RO/Rev	No Yes	0 0
22	**Presence Detect State** **Forward Transparent Bridge mode:** Do not use for Forward Transparent Bridge mode. **Reverse Transparent Bridge mode:** Reveals the PEX 8114 PCI Express port slot's current state. 0 = Slot empty 1 = Slot occupied	RO/Fwd RO/Rev	No Yes	0 0
31:23	***Reserved***			0-0h

14.9 PLX Indirect Configuration Access Mechanism Registers

Table 14-8. PLX Indirect Configuration Access Mechanism Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Configuration Address Window				F8h
Configuration Data Window				FCh

Register 14-34. F8h Configuration Address Window

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Function Number [2:0]**	RO/Fwd R/W/Rev	No No	000b 000b
7:3	**Device Number [4:0]**	RO/Fwd R/W/Rev	No No	0000_0b 0000_0b
15:8	**Bus Number [7:0]**	RO/Fwd R/W/Rev	No No	00h 00h
25:16	**Register DWord Address [9:0]**	RO/Fwd R/W/Rev	No No	000h 000h
30:26	***Reserved***			0h
31	**Configuration Enable**	RO/Fwd R/W/Rev	No No	0 0

Register 14-35. FCh Configuration Data Window

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	Software selects a register by writing into the Register Address Window, write or read that register using Data Window.	RO/Fwd R/W/Rev	No No	0000_0000h 0000_0000h

14.10 Device Serial Number Extended Capability Registers

This section details the PEX 8114 **Device Serial Number Extended Capability** registers. Table 14-9 defines the register map.

Table 14-9. PEX 8114 Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h) / Capability Version (1h)	Extended Capability ID (0003h)	100h
Serial Number (Low)		104h
Serial Number (High)		108h

Register 14-36. 100h Device Serial Number Extended Capability

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0003h, as required by the *PCI Express Base 1.0a.*	RO	Yes	0003h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base 1.0a.*	RO	Yes	1h
31:20	**Next Capability Offset** Set to FB4h, which is the **PCI Express Enhanced Capability Header** registers.	RO	Yes	FB4h

Register 14-37. 104h Serial Number (Low)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial Number[31:0]** Lower half of a 64-bit register. Value set by Serial EEPROM register initialization.	RO	Yes	0000_0EDFh

Register 14-38. 108h Serial Number (High)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial Number[63:32]** Upper half of a 64-bit register. Value set by Serial EEPROM register initialization.	RO	Yes	0000_0001h

14.11 Device Power Budgeting Extended Capability Registers

This section details the PEX 8114 **Device Power Budgeting Extended Capability** registers. Table 14-10 defines the register map.

Table 14-10. PEX 8114 Device Power Budgeting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
(148h)	Capability Version (1h)	(0004h)	138h
Reserved	Data Select	13Ch
Power Data		140h
Reserved	Power Budget Capability	144h

Register 14-39. 138h Device Power Budgeting Extended Capability

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0004h, as required by the *PCI Express Base 1.0a.*	RO	Yes	0004h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base 1.0a.*	RO	Yes	1h
31:20	**Next Capability Offset** Set to 148h, which addresses the PEX 8114 **Virtual Channel Budgeting Extended Capability** registers.	RO	Yes	148h

Register 14-40. 13Ch Data Select

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Data Select** Indexes the Power Budgeting Data reported by way of eight **Power Data** registers and selects the DWord of Power Budgeting Data that appears in each **Power Data** register. Index values start at 0, to select the first DWord of Power Budgeting Data; subsequent DWords of Power Budgeting Data are selected by increasing index values 1 to 7.	R/W	Yes	00h
31:8	***Reserved***			0000_00h

Note: *There are eight registers that can be programmed by way of the serial EEPROM. Each register has a different power configuration for the port. Each configuration is selected by writing to the* ***Data Select*** *register Data Select bits.*

Register 14-41. 140h Power Data

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Base Power** Four registers. Specifies, in watts, the base power value in the operating condition. This value must be multiplied by the Data Scale to produce the actual power consumption value.	RO	Yes	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The power consumption of the device is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. Defined encodings are: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	Yes	00b
12:10	**PM Sub-State** 000b = PEX 8114 is in the default Power Management sub-state	RO	Yes	000b
14:13	**PM State** Current power state. 00b = D0 state 01b = ***Not used – D1 state not supported*** 10b = ***Not used – D2 state not supported*** 11b = D3 state	RO	Yes	00b
17:15	**Type** Type of operating condition. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other values are ***reserved***.	RO	Yes	000b
20:18	**Power Rail** Power Rail of operating condition. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other values are ***reserved***.	RO	Yes	000b
31:21	***Reserved***			0-0h

Register 14-42. 144h Power Budget Capability

Bit(s)	Description	Type	Serial EEPROM	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	HwInit	Yes	1
31:1	***Reserved***			0-0h

14.12 Virtual Channel Extended Capability Registers

This section details the PEX 8114 PCI Express **Virtual Channel Extended Capability** registers. Table 14-11 defines the register map.

Table 14-11. PEX 8114 Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (000h) / Capability Version (1h)	Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2 ***(Not Supported)***		150h
Port VC Status ***(Not Supported)***	Port VC Control ***(Not Supported)***	154h
VC0 Resource Capability ***(Not Supported)***		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
Reserved		164h – 1C4h

Register 14-43. 148h Virtual Channel Budgeting Extended Capability

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Extended Capability ID** Set to 0002h, as required by the *PCI Express Base 1.0a*.	RO	Yes	0002h
19:16	**Capability Version** Set to 1h, as required by the *PCI Express Base 1.0a*.	RO	Yes	1h
31:20	**Next Capability Offset** Set to 000h, indicating that the Virtual Channel Extended Capability is the last extended capability in the Extended Capability list.	RO	Yes	000h

Register 14-44. 14Ch Port VC Capability 1

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Extended VC Count** 0 = PEX 8114 supports only the default Virtual Channel 0	RO	No	0
3:1	***Reserved***			000b
4	**Low-Priority Extended VC Count** For strict priority arbitration, indicates the number of extended virtual channels (those in addition to the default Virtual Channel 0) that belong to the Low-Priority Virtual Channel group for the PEX 8114. 0 = For the PEX 8114, only the default Virtual Channel 0 belongs to the Low-Priority Virtual Channel group	RO	No	0
7:5	***Reserved***			000b
9:8	**Reference Clocks** ***Not supported.*** Cleared to 00b.	RO	No	00b
11:10	**Port Arbitration Table-Entry Size** ***Not supported.*** Cleared to 00b.	RO	No	00b
31:12	***Reserved***			0-0h

Register 14-45. 150h Port VC Capability 2

Bit(s)	Description	Type	Serial EEPROM	Default
1:0	**VC Arbitration Capabilities** ***Not supported.*** Cleared to 00b.	RO	No	00b
23:2	***Reserved***			0-0h
31:24	**VC Arbitration Table Offset** ***Not supported.*** Cleared to 00h.	RO	No	00h

Register 14-46. 154h Port VC Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
	Port VC Control			
0	**Load VC Arbitration Table** ***Not supported.*** Cleared to 0.	RO	No	0
1	**VC Arbitration Select** ***Not supported.*** Cleared to 0.	RO	No	0
15:2	***Reserved***			0-0h
	Port VC Status			
16	**VC Arbitration Table Status** ***Not supported.*** Cleared to 0.	RO	No	0
31:17	***Reserved***			0-0h

Register 14-47. 158h VC0 Resource Capability

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Port Arbitration Capability** ***Not supported.*** Cleared to 0.	RO	No	0
13:1	***Reserved***			0-0h
14	**Advanced Packet Switching** ***Not supported.*** Cleared to 0.	RO	No	0
15	**Reject Snoop Transactions** ***Not supported.*** Cleared to 0.	RO	No	0
22:16	**Maximum Time Slots** ***Not supported.*** Cleared to 000_0000b.	RO	No	000_0000b
23	***Reserved***			0
31:24	**Port Arbitration Table Offset** ***Not supported.*** Cleared to 00h.	RO	No	00h

Register 14-48. 15Ch VC0 Resource Control

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TC/VC0 Map** The PEX 8114 supports only VC0. Traffic Class 0 (TC0) must be mapped to Virtual Channel 0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	Yes	FFh
7:1		R/W	Yes	
15:8	***Reserved***			00h
16	**Load Port Arbitration Table** ***Not supported.*** Cleared to 0.	RO	No	0
19:17	**Port Arbitration Select** ***Not supported.*** Cleared to 000b.	RO	No	000b
23:20	***Reserved***			0-0h
26:24	**VC0 ID** Defines the PEX 8114 PCI Express Virtual Channel 0 ID code. Because this is the default VC0, it is cleared to 000b.	RO	Yes	000b
30:27	***Reserved***			0-0h
31	**VC0 Enable** 0 = Not allowed 1 = Enables PEX 8114 PCI Express default Virtual Channel 0	RO	Yes	1

Register 14-49. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	***Reserved***			0000h
16	**Port Arbitration Table Status** ***Not supported.*** Cleared to 0.	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed 1 = VC0 initialization is not complete for the PEX 8114 PCI Express link	RO	Yes	1
31:18	***Reserved***			0-0h

14.13 PLX-Specific Registers

The registers described in this section are unique to the PEX 8114 device, are not referenced in the *PCI Express Base 1.0a*, and pertain to the PCI Express interface. Table 14-12 defines the register map.

Table 14-12. PLX-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Error Checking and Debug Registers	1C8h … 1F8h
Physical Layer Registers	210h … 2C4h
CAM Routing Registers	2C8h … 6BCh
Base Address Registers (BARs)	6C0h … 73Ch
Ingress Credit Handler (INCH) Registers	9F4h B7Ch
Internal Credit Handler (ITCH) VC&T Threshold Registers	C00h … C10h F70h … F7Ch

Note: *In Reverse Transparent Bridge mode, this register group is accessed using a Memory-Mapped cycle or the PLX Indirect Configuration Access mechanism. It is recommended that these register values* ***not*** *be changed.*

14.13.1 Error Checking and Debug Registers

Table 14-13. PLX-Specific Error Checking and Debug Register Map (PCI Express Interface)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
ECC Check Disable				1C8h
Reserved		Device-Specific Error 32-Bit Error Status (Factory Test Only)		1CCh
Reserved		Device-Specific Error 32-Bit Error Mask (Factory Test Only)		1D0h
Reserved				1D4h – 1DCh
Power Management Hot Plug User Configuration				1E0h
Egress Control and Status				1E4h
Reserved			Bad TLP Count	1E8h
Reserved			Bad DLLP Count	1ECh
TLP Payload Length Count				1F0h
Reserved				1F4h
Reserved		ACK Transmission Latency Limit		1F8h

a. Certain registers are station-specific, while others are device-specific.

Register 14-50. 1C8h ECC Check Disable

Bit(s)	Description	Type	Serial EEPROM	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	R/W	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	R/W	Yes	0
31:2	***Reserved***			0-0h

Note: *All errors in register offset 1CCh generate MSI/INTA# interrupts, if enabled.*

Register 14-51. 1CCh Device-Specific Error 32-Bit Error Status *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Device-Specific Error Completion FIFO Overflow Status** 0 = No overflow detected 1 = Completion FIFO Overflow detected when 4-deep Completion FIFO for ingress, or 2-deep Completion FIFO for egress, overflows	R/W1CS	Yes	0
1	**Egress PRAM Soft Error Overflow** Egress Packet RAM 1-bit Soft Error Counter overflow. 0 = No error detected 1 = Egress PRAM 1-bit Soft Error (8-bit Counter) overflow when destination packet RAM 1-bit soft error count is greater than or equal to 256, it generates an MSI/INTA# interrupt, if enabled	R/W1CS	Yes	0
2	**Egress LLIST Soft Error Overflow** Egress Link-List RAM 1-bit Soft Error Counter overflow. 0 = No error detected 1 = Egress Link-List 1-bit Soft Error (8-bit Counter) overflow when destination module link lists RAM 1-bit soft error count is greater than or equal to 256, it generates an MSI/INTA# interrupt, if enabled	R/W1CS	Yes	0
3	**Egress PRAM ECC Error** Egress Packet RAM 2-bit error detection. 0 = No error detected 1 = Egress PRAM 2-bit ECC error detected	R/W1CS	Yes	0
4	**Egress LLIST ECC Error** Egress Link-List RAM 2-bit error detection. 0 = No error detected 1 = Egress Link-List 2-bit ECC error detected	R/W1CS	Yes	0
5	**Ingress RAM 1-Bit ECC Error** Source Packet RAM 1-bit soft error detection. 0 = No error detected 1 = Ingress RAM 1-BIT ECC error detected	R/W1CS	Yes	0
6	**Egress Memory Allocation Unit (MAU) 1-Bit Soft Error Counter Overflow** Egress Memory Allocation/De-allocation RAM 1-bit soft error count is greater than or equal to 8. 0 = No error detected 1 = Egress MAU 1-bit Soft Error overflow	R/W1CS	Yes	0
7	**Egress Memory Allocation Unit (MAU) 2-Bit Soft Error** Egress Packet Memory Allocation/De-allocation RAM 2-bit error detection. 0 = No 2-bit error detected 1 = Egress MAU 2-bit soft error detected	R/W1CS	Yes	0

Register 14-51. 1CCh Device-Specific Error 32-Bit Error Status *(Factory Test Only) (Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
8	**Ingress RAM Uncorrectable ECC Error** Ingress Packet RAM 2-bit Error detection. 0 = No 2-bit error detected 1 = Packet RAM Uncorrectable ECC error detected	R/W1CS	Yes	0
9	**Ingress LLIST 1-Bit ECC Error** Ingress Link-List RAM 1-bit soft error detection. 0 = No error detected 1 = 1-bit ECC error detected	R/W1CS	Yes	0
10	**Ingress LLIST Uncorrectable ECC Error** Ingress packet Link-List RAM 2-bit error detection. 0 = No 2-bit error detected 1 = Ingress Link-List Uncorrectable ECC Error detected	R/W1CS	Yes	0
11	**Credit Update Timeout Status** No useful credit update to make forward progress for 512 ms or 1s (disabled by default). 0 = No Credit Update Timeout detected 1 = Credit Update Timeout completed	R/W1CS	Yes	0
12	**INCH Underrun Error** Ingress Credit Underrun. 0 = No error detected 1 = Credit underrun error detected	R/W1CS	Yes	0
13	**Ingress Memory Allocation Unit 1-Bit Soft Error Counter Overflow** Ingress Memory Allocation/De-allocation RAM 1-bit Soft Error count greater than or equal to 8. 0 = No error detected 1 = 1-bit Soft Error Counter is ≥ 8	R/W1CS	Yes	0
14	**Ingress Memory Allocation Unit 2-Bit Soft Error** Ingress Memory Allocation/De-allocation RAM 2-bit error detection for Transaction Layer Ingress Memory Allocation/De-allocation unit. 0 = No error detected 1 = 2-bit soft error detected	R/W1CS	Yes	0
31:15	***Reserved***			0-0h

Register 14-52. 1D0h Device-Specific Error 32-Bit Error Mask *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Device-Specific Error Completion FIFO Overflow Status Mask** 0 = When enabled, error generates MSI/INTA# interrupt 1 = *Device-Specific Error Completion FIFO Overflow Status* bit is masked/disabled	R/WS	Yes	1
1	**Egress PRAM Soft Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress PRAM Soft Error Overflow* bit is masked/disabled	R/WS	Yes	1
2	**Egress LLIST Soft Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress LLIST Soft Error Overflow* bit is masked/disabled	R/WS	Yes	1
3	**Egress PRAM ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress PRAM ECC Error* bit is masked/disabled	R/WS	Yes	1
4	**Egress LLIST ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress LLIST ECC Error* bit is masked/disabled	R/WS	Yes	1
5	**Ingress RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM 1-Bit ECC Error* bit is masked/disabled	R/WS	Yes	1
6	**Egress Memory Allocation Unit 1-Bit Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Egress Memory Allocation Unit (MAU) 1-Bit Soft Error Counter Overflow* bit is masked/disabled	R/WS	Yes	1
7	**Egress Memory Allocation Unit 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Egress Memory Allocation Unit (MAU) 2-Bit Soft Error* bit is masked/disabled	R/WS	Yes	1
8	**Ingress RAM Uncorrectable ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM Uncorrectable ECC Error* bit is masked/disabled	R/WS	Yes	1
9	**Ingress LLIST 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM 1-Bit ECC Error* bit is masked/disabled	R/WS	Yes	1
10	**Ingress LLIST Uncorrectable ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress LLIST Uncorrectable ECC Error* bit is masked/disabled	R/WS	Yes	1
11	**Credit Update Timeout Status Mask** 0 = No effect on reporting activity 1 = *Credit Update Timeout Status* bit is masked/disabled	R/WS	Yes	1

Register 14-52. 1D0h Device-Specific Error 32-Bit Error Mask *(Factory Test Only) (Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
12	**INCH Underrun Error Mask** 0 = No effect on reporting activity 1 = *INCH Underrun Error* bit is masked/disabled	R/WS	Yes	1
13	**Ingress Memory Allocation Unit 1-Bit Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = TIC_MAU 1-bit Soft Error Counter-overflow is masked/disabled	R/WS	Yes	1
14	**Ingress Memory Allocation Unit 2-Bit Soft Error Mask** 0 = Error reporting enabled using interrupts 1 = 2-Bit soft error reporting is masked/disabled	R/WS	Yes	1
31:15	***Reserved***			0-0h

Register 14-53. 1E0h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM	Default
0	**L0s Entry Idle Count** Time to meet to enter L0s. 0 = Idle condition lasts for 1 µs 1 = Idle condition lasts for 4 µs	R/W	Yes	0
1	**L1 Upstream Port Receiver Idle Count** For active L1 entry. 0 = Upstream port receiver idle for 2 µs 1 = Upstream port receiver idle for 3 µs	R/W	Yes	0
2	**HPC PME Turn-Off Enable** 1 = PME Turn-off message is transmitted before the port is turned off on downstream port	R/W	Yes	0
4:3	**HPC T_{pepv} Delay** Slot power-applied to power-valid delay time. 00b = 16 ms 01b = 32 ms 10b = 64 ms 11b = 128 ms	RO	Yes	00b
5	**HPC Inband Presence Detect Enable** 0 = HP_PRSNT# Input ball used to detect a board present in the slot 1 = SerDes receiver detect mechanism is used to detect a board present in the slot	RO	Yes	0
6	**HPC T_{pvperl} Delay** Downstream port power-valid to reset signal release time. 0 = 20 ms 1 = 100 ms	RO	Yes	1
12:7	**HPC Test Bits** ***Factory Test Only.*** Testing bits – must be 0_0000_0b.	R/W	Yes	0_0000_0b
31:13	***Reserved***			0-0h

Register 14-54. 1E4h Egress Control and Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Egress Credit Update Timer Enable** In this mode, when the port is not receiving credits to make forward progress and the Egress Timeout timer times out, the downstream link is brought down. 0 = Egress Credit update timer disabled 1 = Egress Credit update timer enabled	R/W	Yes	0
1	**Egress Timeout Value** 0 = Minimum 512 ms (Maximum 768 ms) 1 = Minimum 1,024 ms (Maximum 1,280 ms)	R/W	Yes	0
2	**DL_Down Handling** 0 = Reports unsupported request error for all TLP requests received in DL_Down state 1 = Reports unsupported request for first Posted/Non-Posted TLP request in DL_Down state – silently drops subsequent TLP requests	R/W	Yes	0
7:3	***Reserved***			0-0h
15:8	**Link-List RAM Soft Error Count** Link-List RAM 8-bit Soft Error Counter value. Counter shared by: • Packet Link-List RAM • Packet Link-List De-allocation RAM • Scheduler Data RAM Counter increments for 1-bit soft errors detected in any of these RAM.	RO	Yes	00h
19:16	**VC&T Encountered Timeout** 0h = VC0 Posted 1h = VC0 Non-Posted 2h = VC0 Completion All other values are ***not supported***.	RO	Yes	0h
23:20	***Reserved***			0h
31:24	**Packet RAM Soft Error Count** Counter increments for each 1-bit soft error detected in RAM.	RO	No	00h

Register 14-55. 1E8h Bad TLP Count

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Bad TLP Count** Counts number of TLPs with bad LCRC, or number of TLPs with a Sequence Number mismatch error. The maximum value is FFh.	R/W	Yes	00h
31:8	***Reserved***			0000_00h

Register 14-56. 1ECh Bad DLLP Count

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Bad DLLP Count** Counts number of DLLPs with bad LCRC, or number of DLLPs with a Sequence Number mismatch error. The maximum value is FFh.	R/W	Yes	00h
31:8	***Reserved***			0000_00h

Register 14-57. 1F0h TLP Payload Length Count

Bit(s)	Description	Type	Serial EEPROM	Default
20:0	**TLP Payload Length Count** Defines the TLP Payload Size transferred over the link in 1-ms period.	R/W	Yes	00_0000h
31:21	***Reserved***			000h

Register 14-58. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**ACK Transmission Latency Limit** Value based on the negotiated link width encoding: Link Width / Register Value (Decimal / Hex): x1: 255 / FFh x2: 217 / D9h x4: 118 / 76h	R/W	Yes	FFh
15:8	**HPC Test Bits** ***Factory Test Only.*** Testing bits – must be 00h.	R/W	Yes	00h
31:16	***Reserved***			0000h

14.13.2 Physical Layer Registers

Table 14-14. PLX-Specific Physical Layer Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Test Pattern_0		210h
Test Pattern_1		214h
Test Pattern_2		218h
Test Pattern_3		21Ch
Physical Layer Status	Physical Layer Control	220h
Port Configuration		224h
Physical Layer Test		228h
Physical Layer (Factory Test Only)		22Ch
Physical Layer Port Command		230h
SKIP Ordered-Set Interval		234h
Quad SerDes[0-3] Diagnostics Data		238h
Reserved		23Ch – 244h
Reserved	SerDes Nominal Drive Current Select	248h
Reserved	SerDes Drive Current Level_1	24Ch
Reserved		250h
Reserved	SerDes Drive Equalization Level Select_1	254h
Reserved		258h – 25Ch
Status Data from Serial EEPROM	Serial EEPROM Status / Serial EEPROM Control	260h
Serial EEPROM Buffer		264h
Reserved		268h – 2C4h

Note: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes lanes into a group of four contiguous lanes for testing purposes. The quad is defined as SerDes[0-3].*

Register 14-59. 210h Test Pattern_0

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern_0** Used for Digital Far-End Loop-Back testing.	R/W	Yes	0-0h

Register 14-60. 214h Test Pattern_1

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern_1** Used for Digital Far-End Loop-Back testing.	R/W	Yes	0-0h

Register 14-61. 218h Test Pattern_2

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern_2** Used for Digital Far-End Loop-Back testing.	R/W	Yes	0-0h

Register 14-62. 21Ch Test Pattern_3

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Test Pattern_3** Used for Digital Far-End Loop-Back testing.	R/W	Yes	0-0h

Register 14-63. 220h Physical Layer Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
Physical Layer Control				
0	**Port Enumerator Enable** 0 = Enumerate not enabled 1 = Enumerate enabled	HwInit	Yes	0
1	**TDM Enable** 0 = TDM not enabled 1 = TDM enabled	HwInit	Yes	0
2	***Reserved***			0
3	**Upstream Port as Configuration Master Enable** 0 = Upstream Port Cross-link not supported 1 = Upstream Port Cross-link supported	R/W	Yes	0
4	**Downstream Port as Configuration Slave Enable** 0 = Downstream Port Cross-link not supported 1 = Downstream Port Cross-link supported	R/W	Yes	0
5	**Lane Reversal Disable** 0 = Lane reversal supported 1 = Lane reversal not supported	R/W	Yes	0
6	***Reserved***			0
7	**FC-Init Triplet Enable** Flow control Initialization. 0 = Init FL1 Triplet can be interrupted by SKIP Ordered-Set/Idle Data symbol 1 = Init FL1 Triplet not interrupted	R/W	Yes	0
15:8	**N_FTS Value** N_FTS value to transmit in training sets.	R/W	Yes	40h
Physical Layer Status				
19:16	***Reserved***			0h
22:20	**Number of Ports Enumerated** Number of ports in current configuration.	HwInit	Yes	000b
23	***Reserved***			0
24	**Port 0 Deskew Buffer Error Status** 1 = Deskew Buffer overflow or underflow	R/W1C	Yes	0
31:25	***Reserved***			00h

Register 14-64. 224h Port Configuration

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Port Configuration**	HwInit	Yes	000b
31:3	***Reserved***			0-0h

Register 14-65. 228h Physical Layer Test

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Timer Test Mode Enable** 0 = Standard Physical Layer Timer parameters used 1 = Shortens Timer scale from milliseconds to microseconds	R/W	Yes	0
1	**SKIP-Timer Test Mode Enable** 0 = Disables SKIP-Timer Test mode 1 = Enables SKIP-Timer Test mode	R/W	Yes	0
2	**Port_0_x1** 1 = PCI Express interface is configured as x1	R/W	Yes	0
3	**TCB Capture Disable** 0 = Training Control Bit (TCB) Capture enabled 1 = Disables TCB Capture	R/W	Yes	0
4	**Analog Loop-Back Enable** 1 = Analog Loop-back testing enabled (Loop-Back before elastic buffer)	R/W	Yes	0
5	**Port/SerDes Test Pattern Enable Select** 1 = Test Pattern Enable bits select the port, rather than SerDes[0-3]	R/W	Yes	0
6	***Reserved***			0
7	**SerDes BIST Enable** When programmed to 1 by the serial EEPROM, enables SerDes internal Loop-Back PRBS test for 512 µs before starting link initialization.	RO	Yes	0
9:8	**PRBS Association** Selects the SerDes within the quad for PRBS generation/checking. **Value Selects PCI Express Station SerDes** 00b = 0 01b = 1 10b = 2 11b = 3	R/W	Yes	00b
15:10	***Reserved***			0-0h

Register 14-65. 228h Physical Layer Test *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
16	**PRBS Enable** When set to 1, enables PRBS sequence generation/checking on SerDes[0-3].	R/W	Yes	0
19:17	***Reserved***			000b
20	**PRBS External Loop-Back** The following bit commands are valid when the Loop-Back command is enabled in offset 230h. 0 = SerDes[0-3] establishes internal analog Loop-Back when bit 16=1 1 = SerDes[0-3] establishes external analog Loop-Back when bit 16=1	R/W	Yes	0
23:21	***Reserved***			000b
24	**PRBS Error Count Reset** When set to 1, resets the PRBS Error Counter (offset 238h[31:24]).	RO	Yes	0
27:25	***Reserved***			000b
28	**Test Pattern Enable** Enables SerDes[0-3] test pattern transmission in Digital Far-End Loop-Back mode.	R/W	Yes	0
31:29	***Reserved***			000b

Register 14-66. 22Ch Physical Layer *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	***Factory Test Only***	R/W	Yes	0-0h

Register 14-67. 230h Physical Layer Port Command

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Port 0 Loop-Back** 0 = PCI Express interface not enabled to proceed to Loop-Back state 1 = PCI Express interface enabled to proceed to Loop-Back state	R/W	Yes	0
1	**Port 0 Scrambler Disable** When serial EEPROM load sets this bit, scrambler is disabled in Configuration-Complete state. When software sets this bit when the Link is in the up state, hardware immediately disables its scrambler without executing Link Training protocol. The upstream/downstream device scrambler is not disabled. 0 = PCI Express interface scrambler enabled 1 = PCI Express interface scrambler disabled	R/W	Yes	0
2	**Port 0 Rx L1 Only** PCI Express interface Receiver enters ASPM L1. 0 = PCI Express interface Receiver allowed to proceed to ASPM L0s or L1 state when it detects Electrical Idle Ordered-Set in L0 state 1 = PCI Express interface Receiver allowed to proceed to ASPM L1 only when it detects Electrical Idle Ordered-Set in L0 state	R/W	Yes	0
3	**Port 0 Ready as Loop-Back Master** PCI Express interface LTSSM established Loop-Back as a Master. 0 = PCI Express interface not in Loop-Back Master mode 1 = PCI Express interface in Loop-Back Master mode	RO	No	0
31:4	***Reserved***			0000_000h

Register 14-68. 234h SKIP Ordered-Set Interval

Bit(s)	Description	Type	Serial EEPROM	Default
11:0	**SKIP Ordered-Set Interval** SKIP Ordered-Set Interval (in symbol times).	R/WS	Yes	49Ch
31:12	***Reserved***			0000_0h

Register 14-69. 238h Quad SerDes[0-3] Diagnostics Data

Bit(s)	Description	Type	Serial EEPROM	Default
9:0	**Expected PRBS Data** Expected PRBS SerDes[0-3] Diagnostic data.	RO	Yes	000h
19:10	**Received PRBS Data** Received PRBS SerDes[0-3] Diagnostic data.	RO	Yes	000h
23:20	***Reserved***			0h
31:24	**PRBS Error Count** PRBS SerDes[0-3] Error count (0 to 255).	RO	Yes	00h

Register 14-70. 248h SerDes Nominal Drive Current Select

Bit(s)	Description		Type	Serial EEPROM	Default
1:0	**SerDes_0 Nominal Drive Current**	The following values for Nominal Current apply to each drive: 00b = 20 mA 01b = 10 mA 10b = 28 mA 11b = 20 mA	R/WS	Yes	00b
3:2	**SerDes_1 Nominal Drive Current**		R/WS	Yes	00b
5:4	**SerDes_2 Nominal Drive Current**		R/WS	Yes	00b
7:6	**SerDes_3 Nominal Drive Current**		R/WS	Yes	00b
31:8	***Reserved***				0000_00h

Register 14-71. 24Ch SerDes Drive Current Level_1

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_0 Drive Current Level**	The following values represent the ratio of Actual Current/ Nominal Current (selected in **SerDes Nominal Drive Current Select** register) and apply to each drive: 0h = 1.00 8h = 0.60 1h = 1.05 9h = 0.65 2h = 1.10 Ah = 0.70 3h = 1.15 Bh = 0.75 4h = 1.20 Ch = 0.80 5h = 1.25 Dh = 0.85 6h = 1.30 Eh = 0.90 7h = 1.35 Fh = 0.95	R/WS	Yes	0h
7:4	**SerDes_1 Drive Current Level**		R/WS	Yes	0h
11:8	**SerDes_2 Drive Current Level**		R/WS	Yes	0h
15:12	**SerDes_3 Drive Current Level**		R/WS	Yes	0h
31:16	***Reserved***				0000h

Register 14-72. 254h SerDes Drive Equalization Level Select_1

Bit(s)	Description		Type	Serial EEPROM	Default
3:0	**SerDes_0 Drive Equalization Level**	The following values represent the percentage of Drive Current attributable to Equalization Current and apply to each drive:	R/WS	Yes	8h
7:4	**SerDes_1 Drive Equalization Level**		R/WS	Yes	8h
11:8	**SerDes_2 Drive Equalization Level**		R/WS	Yes	8h
15:12	**SerDes_3 Drive Equalization Level**		R/WS	Yes	8h
31:16	***Reserved***				0000h

I_{EQ} / I_{DR}	De-Emphasis (dB)
0h = 0.00	0.00
1h = 0.04	-0.35
2h = 0.08	-0.72
3h = 0.12	-1.11
4h = 0.16	-1.51
5h = 0.20	-1.94
6h = 0.24	-2.38
7h = 0.28	-2.85
8h = 0.32	-3.35
9h = 0.36	-3.88
Ah = 0.40	-4.44
Bh = 0.44	-5.04
Ch = 0.48	-5.68
Dh = 0.52	-6.38
Eh = 0.56	-7.13
Fh = 0.60	-7.96

Register 14-73. 260h Serial EEPROM Status and Control

Bit(s)	Description	Type	Serial EEPROM	Default
Serial EEPROM Control				
12:0	**Serial EEPROM Block Address** Serial EEPROM Block Address for 32 KB.	R/W	Yes	0000h
15:13	**Serial EEPROM Command** Commands to the Serial EEPROM Controller. 001b = Data from Serial EEPROM Status[31:24] bits written to the Serial EEPROM internal status register 010b = Write four bytes of data from the *Serial EEPROM Buffer* into memory location pointed to by the *Serial EEPROM Block Address* field 011b = Read four bytes of data from memory location pointed to by the *Serial EEPROM Block Address* field into the *Serial EEPROM Buffer* 100b = Reset Write Enable latch 101b = Data from Serial EEPROM internal status register written to the Serial EEPROM Status[31:24] bits 110b = Set Write Enable latch All other values are ***reserved***.	R/W	Yes	000b
Serial EEPROM Status				
17:16	**Serial EEPROM Present** Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM Present – no CRC error 10b = ***Reserved*** 11b = Serial EEPROM Present, but with CRC error – default reset value used	RO	Yes	00b
19:18	**Serial EEPROM Command Status** 00b = Serial EEPROM Command complete 01b = Serial EEPROM Command not complete 10b = Serial EEPROM Command complete with CRC error 11b = ***Reserved***	RO	Yes	00b
20	**Serial EEPROM Block Address Upper Bit** *Serial EEPROM Block Address* upper bit 13. Extends Serial EEPROM to 64 KB.	R/W	Yes	0
21	**CRC Disable** 0 = Serial EEPROM input data uses CRC 1 = Serial EEPROM input data CRC disabled	R/W	Yes	0
23:22	***Reserved***			00b

Register 14-73. 260h Serial EEPROM Status and Control *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM</td></tr>
<tr><td>24</td><td>Serial EEPROM_RDY#
0 = Serial EEPROM ready to transmit data
1 = Write cycle in progress</td><td>R/W</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td>Serial EEPROM_WEN
0 = Serial EEPROM Write disabled
1 = Serial EEPROM Write enabled</td><td>R/W</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td>Serial EEPROM_BP[1:0]
Serial EEPROM Block-Write Protect bits.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="3">Array Addresses Protected</th></tr>
<tr><th>16-KB Device</th><th>32-KB Device</th><th>64-KB Device</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1 (1/4)</td><td>3000h - 3FFFh</td><td>6000h - 7FFFh</td><td>C000h - FFFFh</td></tr>
<tr><td>10b</td><td>2 (1/2)</td><td>2000h - 3FFFh</td><td>4000h - 7FFFh</td><td>8000h - FFFFh</td></tr>
<tr><td>11b</td><td>3 (All)</td><td>0000h - 3FFFh</td><td>0000h - 7FFFh</td><td>0000h - FFFFh</td></tr>
</table></td><td>R/W</td><td>Yes</td><td>00b</td></tr>
<tr><td>30:28</td><td>Serial EEPROM Write Status
Value is 000b when serial EEPROM is not in an internal Write cycle.</td><td>RO</td><td>Yes</td><td>000b</td></tr>
<tr><td>31</td><td>Serial EEPROM_WPEN
Serial EEPROM Write Protect Enable. When:
= 0 and Serial EEPROM_WEN = 1, the Serial EEPROM Status register is writable.
= 1, Serial EEPROM Status register is protected.</td><td>R/W</td><td>Yes</td><td>0</td></tr>
</table>

Register 14-74. 264h Serial EEPROM Buffer

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Serial EEPROM Buffer**	R/W	No	0-0h

14.13.3 CAM Routing Registers

The CAM Routing registers contain mirror copies of the registers used for:

- **Bus Number CAM (Content-Addressable Memory)** – Used to determine configuration TLP Completion route

  This register contains a mirror copy of the PEX 8114 **Primary Bus Number**, **Secondary Bus Number**, and **Subordinate Bus Number** registers.

- **I/O CAM** – Used to determine I/O request routing

  This register contains a mirror copy of the PEX 8114 **I/O Base** and **I/O Limit** registers.

- **AMCAM (Address-Mapping CAM)** – Used to determine Memory request route

  These registers contain mirror copies of the PEX 8114 **Memory Base and Limit Address**, **Prefetchable Memory Base and Limit Address**, and **Prefetchable Memory Upper Base Address[63:32]** and **Prefetchable Memory Upper Limit Address[63:32]** registers.

These registers are automatically updated by hardware. Modifying these registers by writing to the addresses listed herein is not recommended. These mirror copies are used by the PCI Express interface.

Table 14-15. PLX-Specific CAM Routing Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				2C8h – 2E4h
Bus Number CAM 8				2E8h
Reserved				2ECh – 314h
Reserved		I/O CAM_8		318h
Reserved				31Ch – 3C4h
AMCAM_8 Memory Limit and Base				3C8h
AMCAM_8 Prefetchable Memory Limit and Base[31:0]				3CCh
AMCAM_8 Prefetchable Memory Base[63:32]				3D0h
AMCAM_8 Prefetchable Memory Limit[63:32]				3D4h
Reserved				3D8h – 65Ch
TIC Control				660h
Reserved				664h
TIC Port Enable (Factory Test Only)				668h
Reserved				66Ch – 69Ch
IOCAM_8 Limit[31:16]		IOCAM_8 Base[31:16]		6A0h
Reserved				6A4h – 6BCh

14.13.3.1 Bus Number CAM Register

Register 14-75. 2E8h Bus Number CAM 8

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Primary Bus Number** Mirror copy of *Primary Bus Number*.	R/W	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of *Secondary Bus Number*.	R/W	Yes	FFh
23:16	**Subordinate Bus Number** Mirror copy of *Subordinate Bus Number*.	R/W	Yes	00h
31:24	***Reserved***			00h

14.13.3.2 I/O CAM Register

Register 14-76. 318h I/O CAM_8

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**I/O Addressing Capability** 1h = 32-bit I/O addressing All other values are ***reserved***.	RO	Yes	1h
7:4	**I/O Base** Mirror copy of **I/O Base** value.	R/W	Yes	Fh
11:8	**I/O Addressing Capability** 1h = 32-bit I/O addressing All other values are ***reserved***.	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of **I/O Limit** value.	R/W	Yes	0h
31:16	***Reserved***			0000h

14.13.3.3 AMCAM (Address-Mapping CAM) Registers

AMCAM registers contain mirror images of the PEX 8114 **Memory Base and Limit Address**, **Prefetchable Memory Base and Limit Address**, and **Prefetchable Memory Upper Base Address[63:32]** and **Prefetchable Memory Upper Limit Address[63:32]** registers.

Register 14-77. 3C8h AMCAM_8 Memory Limit and Base

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	***Reserved***			0h
15:4	**Memory Base** Mirror copy of Memory Base value.	R/W	Yes	FFFh
19:16	***Reserved***			0h
31:20	**Memory Limit** Mirror copy of Memory Limit value.	R/W	Yes	000h

Register 14-78. 3CCh AMCAM_8 Prefetchable Memory Limit and Base[31:0]

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
15:4	**Prefetchable Memory Base** AMCAM_8 Prefetchable Memory Base[31:20].	R/W	Yes	FFFh
19:16	**Addressing Support** 0h = 32-bit addressing supported 1h = 64-bit addressing supported	RO	Yes	1h
31:20	**Prefetchable Memory Limit** AMCAM_8 Prefetchable Memory Limit[31:20].	R/W	Yes	000h

Register 14-79. 3D0h AMCAM_8 Prefetchable Memory Base[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Base[63:32]** AMCAM_8 Prefetchable Memory Base[63:32].	R/W	Yes	FFFF_FFFFh

Register 14-80. 3D4h AMCAM_8 Prefetchable Memory Limit[63:32]

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Prefetchable Memory Limit[63:32]** AMCAM_8 Prefetchable Memory Limit[63:32].	R/W	Yes	0-0h

14.13.3.4 TIC Control Registers

Table 14-16. PLX-Specific TIC Control Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
TIC Control				660h
Reserved				664h
TIC Port Enable (Factory Test Only)				668h

Register 14-81. 660h TIC Control

Bit(s)	Description	Type	Serial EEPROM	Default
0	**TIC Control** Valid in Reverse Transparent Bridge mode. Enables Configuration Transactions from the downstream port. Peer Configuration Access. When set to 1, configuration transactions (Type 0) coming upstream from a downstream port are allowed to enter the device and the Type 1 Header of the bridge is accessible.	R/W	Yes	0
1	**Disable Unsupported Request Response for *Reserved* Configuration Registers**	R/W	Yes	0
31:2	**TIC Control** ***Factory Test Only***	R/W	Yes	0-0h

Register 14-82. 668h TIC Port Enable (*Factory Test Only*)

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TIC_UNP_Status** ***Factory Test Only***	R/W	Yes	FFFF_FFFFh

14.13.3.5 I/O CAM Base and Limit Upper 16 Bits Registers

Table 14-17. PLX-Specific I/O CAM Base and Limit Upper 16 Bits Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				66Ch – 69Ch
IOCAM_8 Limit[31:16]		IOCAM_8 Base[31:16]		6A0h
Reserved				6A4h – 6BCh

Register 14-83. 6A0h I/OCAM_8 Base and Limit Upper 16 Bits

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**IOCAM_8 Base[31:16]** I/O Base Upper 16 bits.	R/W	Yes	FFFFh
31:16	**IOCAM_8 Limit[31:16]** I/O Limit Upper 16 bits.	R/W	Yes	0000h

14.13.4 Base Address Registers (BARs)

The registers defined in Table 14-18 contain a shadow copy of the two PEX 8114 Type 1 Configuration Base Address registers.

Table 14-18. PLX-Specific Base Address Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved	6C0h – 6FCh
BAR0_8	700h
BAR1_8	704h
Reserved	708h – 73Ch

Register 14-84. 700h BAR0_8

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Memory Space Indicator** 0 = Memory BAR 1 = I/O BAR Reads 0, and ignores Writes. Only value of 0 is allowed.	RO	No	0
2:1	**Memory Mapping Range** 00b = 32 bits 10b = 64 bits 01b, 11b = ***Reserved***	R/W	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable Reads 0, and ignores Writes.	RO	No	0
12:4	***Reserved***			000h
31:13	**Base Address_0** Shadow copy of Base Address 0. Where BAR0[12:4] = ***Reserved***.	R/W	Yes	0000h

Register 14-85. 704h BAR1_8

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**Base Address_1[63:32]** When BAR0[2:1] = 10b, becomes a Shadow copy of Base Address_1[63:32].	R/W	Yes	0000_0000h

14.13.5 Ingress Credit Handler (INCH) Registers

Table 14-19. PLX-Specific Ingress Credit Handler (INCH) Register Map for PCI Express Interface

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved			INCH FC Update Pending Timer	9F4h
Reserved				9F8h
Reserved		INCH Mode		9FCh
INCH Threshold VC0 Posted				A00h
INCH Threshold VC0 Non-Posted				A04h
INCH Threshold VC0 Completion				A08h
Reserved				A0Ch – B7Ch

Register 14-86. 9F4h INCH FC Update Pending Timer

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Update Timer** Update pending timer, using the guidelines as follows.	R/W	Yes	00h
31:8	***Reserved***			0000_00h

Maximum Packet Size	Link Width	Default Timer Count
128 bytes	x1	76h
	x2	40h
	x4	24h
256 bytes	x1	D0h
	x2	6Ch
	x4	3Bh

Register 14-87. 9FCh INCH Mode

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Maximum Mode Enable** ***Factory Test Only***	RO	Yes	FFh
15:8	***Reserved***			00h
19:16	***Factory Test Only***	R/W	Yes	0h
23:20	**Pending Timer Source** Pending timer register – uses serial EEPROM values.	R/W	Yes	0h
31:24	***Reserved***			00h

14.13.5.1 INCH Threshold Virtual Channel Registers

There are three Ingress Credit Handler (INCH) Threshold VC0 registers. These registers represent the maximum number of Headers or Payload credits allocated to Virtual Channel 0, for each type of transaction. The register names and address/location are defined in Table 14-19. The following registers describe the data that applies to these registers.

Register 14-88. A00h INCH Threshold VC0 Posted

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	***Reserved***			000b
8:3	**Payload** Payload = 0_0111_0b.	R/W	Yes	30Eh
13:9	**Header** Header = 01_100b.			
31:14	***Reserved***			0-0h

Register 14-89. A04h INCH Threshold VC0 Non-Posted

Bit(s)	Description	Type	Serial EEPROM	Default
8:0	**Payload** Payload = 0_0000_1010b.	R/W	Yes	140Ah
13:9	**Header** Header = 01_010b.			
31:14	***Reserved***			0-0h

Register 14-90. A08h INCH Threshold VC0 Completion

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	***Reserved***			000b
8:3	**Payload** Payload = 0_0110_0b.	R/W	Yes	28Ch
13:9	**Header** Header = 01_010b.			
31:14	***Reserved***			0-0h

14.13.6 Internal Credit Handler (ITCH) VC&T Threshold Registers

14.13.6.1 PCI Express Interface PLX-Specific Internal Credit Handler (ITCH) VC&T Threshold Registers

The registers defined in Table 14-20 control internal traffic from the PCI Express interface to the PCI-X interface. The threshold (Packet Count) units are equivalent to 8 beats, where each beat can be up to 20 bytes. Therefore, a programmed value of 1 represents 160 bytes, 2 represents 320 bytes, and so forth. The entire TLP (Header, Payload, and ECRC, if any) is used to determine a total byte size, and the total byte size is divided by 20 and rounded up to the nearest integer to ascertain the number of beats. Every 8 beats counts as 1 threshold unit.

The Upper Packet Count is the high threshold. If more units than the programmed upper count are queued, no further packets can be scheduled across the internal fabric.

Note: *Previously scheduled packets arrive in their entirety, completely unaffected by the cut-off signal.*

The Lower Packet Count is the low threshold. After cutting off a VC&T due to the high threshold, when the count returns below the low threshold, that VC&T is again turned On.

The upper and lower counts must be different, and the upper number must be at least two units larger than the lower number.

Table 14-20. PEX 8114 PCI Express Interface PLX-Specific Internal Credit Handler (ITCH) VC&T Threshold Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Interface PCI Express ITCH VC&T Threshold_1				C00h
PCI Express Interface ITCH VC&T Threshold_2				C04h
Reserved				C08h – C10h

Register 14-91. C00h PCI Express Interface PCI Express ITCH VC&T Threshold_1

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**VC0 Posted Upper Packet Count** VC0 Posted upper packet beat limit.	R/W	Yes	10h
7:5	***Not used***	R/W	Yes	000b
12:8	**VC0 Posted Lower Packet Count** VC0 Posted lower packet beat limit.	R/W	Yes	08h
15:13	***Not used***	R/W	Yes	000b
20:16	**VC0 Non-Posted Upper Packet Count** VC0 Non-Posted upper packet beat limit.	R/W	Yes	04h
23:21	***Not used***	R/W	Yes	000b
28:24	**VC0 Non-Posted Lower Packet Count** VC0 Non-Posted lower packet beat limit.	R/W	Yes	01h
31:29	***Not used***	R/W	Yes	000b

Register 14-92. C04h PCI Express Interface ITCH VC&T Threshold_2

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**VC0 Completion Upper Packet Count** VC0 Completion upper packet beat limit.	R/W	Yes	10h
7:5	***Not used***	R/W	Yes	000b
12:8	**VC0 Completion Lower Packet Count** VC0 Completion lower packet beat limit.	R/W	Yes	08h
15:13	***Not used***	R/W	Yes	000b
20:16	**VC1 Posted Upper Packet Count** VC1 Posted upper packet beat limit. This information is listed for internal and serial EEPROM configuration only – not to be changed by users.	R/W	Yes	04h
23:21	***Not used***	R/W	Yes	000b
28:24	**VC1 Posted Lower Packet Count** VC1 Posted lower packet beat limit. This information is listed for internal and serial EEPROM configuration only – not to be changed by users.	R/W	Yes	01h
31:29	***Not used***	R/W	Yes	000b

Note: *Although the PEX 8114 supports only VC0, the VC1 Posted credit fields are used for internal transactions, such as shadow Writes.*

14.13.6.2 PCI-X Interface PLX-Specific Internal Credit Handler (ITCH) VC&T Threshold Registers

The registers defined in Table 14-21 control internal traffic from the PCI-X interface to the PCI Express interface. The threshold (Packet Count) units are equivalent to 8 beats, where each beat can be up to 20 bytes. Therefore, a programmed value of 1 represents 160 bytes, 2 represents 320 bytes, and so forth. The entire TLP (Header, Payload, and ECRC, if any) is used to determine a total byte size, and the total byte size is divided by 20 and rounded up to the nearest integer to ascertain the number of beats. Every 8 beats counts as 1 threshold unit.

The Upper Packet Count is the high threshold. If more units than the programmed upper count are queued, no further packets can be scheduled across the internal fabric.

Note: *Previously scheduled packets arrive in their entirety, completely unaffected by the cut-off signal.*

The Lower Packet Count is the low threshold. After cutting off a VC&T due to the high threshold, when the count returns below the low threshold, that VC&T is again turned on.

The upper and lower counts must be different, and the upper number must be at least two units larger than the lower number.

Table 14-21. PEX 8114 PCI-X Interface PLX-Specific Internal Credit Handler (ITCH) VC&T Threshold Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-X Interface ITCH VC&T Threshold_1				F70h
PCI-X Interface ITCH VC&T Threshold_2				F74h
Reserved				F78h – F7Ch

Register 14-93. F70h PCI-X Interface ITCH VC&T Threshold_1

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**VC0 Posted Upper Packet Count** VC0 Posted upper packet beat limit.	R/W	Yes	10h
7:5	***Not used***	R/W	Yes	000b
12:8	**VC0 Posted Lower Packet Count** VC0 Posted lower packet beat limit.	R/W	Yes	08h
15:13	***Not used***	R/W	Yes	000b
20:16	**VC0 Non-Posted Upper Packet Count** VC0 Non-Posted upper packet beat limit.	R/W	Yes	04h
23:21	***Not used***	R/W	Yes	000b
28:24	**VC0 Non-Posted Lower Packet Count** VC0 Non-Posted lower packet beat limit.	R/W	Yes	01h
31:29	***Not used***	R/W	Yes	000b

Register 14-94. F74h PCI-X Interface ITCH VC&T Threshold_2

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**VC0 Completion Upper Packet Count** VC0 Completion upper packet beat limit.	R/W	Yes	10h
7:5	***Not used***	R/W	Yes	000b
12:8	**VC0 Completion Lower Packet Count** VC0 Completion lower packet beat limit.	R/W	Yes	08h
15:13	***Not used***	R/W	Yes	000b
20:16	**VC1 Posted Upper Packet Count** VC1 Posted upper packet beat limit. This information is listed for internal and serial EEPROM configuration only – not to be changed by users.	R/W	Yes	04h
23:21	***Not used***	R/W	Yes	000b
28:24	**VC1 Posted Lower Packet Count** VC1 Posted lower packet beat limit. This information is listed for internal and serial EEPROM configuration only – not to be changed by users.	R/W	Yes	01h
31:29	***Not used***	R/W	Yes	000b

Note: *Although the PEX 8114 supports only VC0, the VC1 Posted credit fields are used for internal transactions, such as shadow Writes.*

14.14 PCI-X PLX-Specific Registers

Table 14-22. PCI-X PLX-Specific Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-X Interface Device-Specific Error 32-Bit Error Status (Factory Test Only)				F80h
PCI-X Interface Device-Specific Error 32-Bit Error Mask (Factory Test Only)				F84h
Reserved			PCI-X Interface Completion Buffer Timeout	F88h

Note: *All errors in offset F80h generate MSI/INTA# interrupts, if enabled.*

Register 14-95. F80h PCI-X Interface Device-Specific Error 32-Bit Error Status *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Device-Specific Error Completion FIFO Overflow Status** 0 = No overflow detected 1 = Completion FIFO Overflow detected when 4-deep Completion FIFO for ingress, or 2-deep Completion FIFO for egress, overflows	R/W1CS	Yes	0
1	**Egress PRAM Soft Error Overflow** Egress Packet RAM 1-bit Soft Error Counter overflow. 0 = No error detected 1 = Egress PRAM 1-bit Soft Error (8-bit Counter) overflow when destination packet RAM 1-bit soft error count is greater than or equal to 256, it generates an MSI/INTA# interrupt, if enabled	R/W1CS	Yes	0
2	**Egress LLIST Soft Error Overflow** Egress Link-List RAM 1-bit Soft Error Counter overflow. 0 = No error detected 1 = Egress Link-List 1-bit Soft Error (8-bit Counter) overflow when destination module link lists RAM 1-bit soft error count is greater than or equal to 256, it generates an MSI/INTA# interrupt, if enabled	R/W1CS	Yes	0
3	**Egress PRAM ECC Error** Egress Packet RAM 2-bit error detection. 0 = No error detected 1 = Egress PRAM 2-bit ECC error detected	R/W1CS	Yes	0
4	**Egress LLIST ECC Error** Egress Link-List RAM 2-bit error detection. 0 = No error detected 1 = Egress Link-List 2-bit ECC error detected	R/W1CS	Yes	0
5	**Ingress RAM 1-Bit ECC Error** Source Packet RAM 1-bit soft error detection. 0 = No error detected 1 = Ingress RAM 1-BIT ECC error detected	R/W1CS	Yes	0
7:6	***Reserved***			00b
8	**Ingress RAM Uncorrectable ECC Error** Ingress Packet RAM 2-bit Error detection. 0 = No 2-bit error detected 1 = Packet RAM Uncorrectable ECC error detected	R/W1CS	Yes	0
31:9	***Reserved***			0-0h

Register 14-96. F84h PCI-X Interface Device-Specific Error 32-Bit Error Mask *(Factory Test Only)*

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Device-Specific Error Completion FIFO Overflow Status Mask** 0 = When enabled, error generates MSI/INTA# interrupt 1 = *Device-Specific Error Completion FIFO Overflow Status* bit is masked/disabled	R/WS	Yes	1
1	**Egress PRAM Soft Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress PRAM Soft Error Overflow* bit is masked/disabled	R/WS	Yes	1
2	**Egress LLIST Soft Error Overflow Mask** 0 = No effect on reporting activity 1 = *Egress LLIST Soft Error Overflow* bit is masked/disabled	R/WS	Yes	1
3	**Egress PRAM ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress PRAM ECC Error* bit is masked/disabled	R/WS	Yes	1
4	**Egress LLIST ECC Error Mask** 0 = No effect on reporting activity 1 = *Egress LLIST ECC Error* bit is masked/disabled	R/WS	Yes	1
5	**Ingress RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM 1-Bit ECC Error* bit is masked/disabled	R/WS	Yes	1
7:6	***Reserved***			00b
8	**Ingress RAM Uncorrectable ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress RAM Uncorrectable ECC Error* bit is masked/disabled	R/WS	Yes	1
31:9	***Reserved***			0-0h

Register 14-97. F88h PCI-X Interface Completion Buffer Timeout

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	**Target Tag Timeout**	R/W1C	Yes	00h
31:8	***Reserved***			0000_00h

14.15 Root Port Registers

Table 14-23. Root Port Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Root Control				F8Ch
Root Status				F90h
Root Error Command				F94h
Root Error Status				F98h
Error Identification				F9Ch

Register 14-98. F8Ch Root Control

Bit(s)	Description	Type	Serial EEPROM	Default
0	**System Error on Correctable Error Enable**	RO/Fwd R/W/Rev	No Yes	0 0
1	**System Error on Non-Fatal Error Enable**	RO/Fwd R/W/Rev	No Yes	0 0
2	**System Error on Fatal Error Enable**	RO/Fwd R/W/Rev	No Yes	0 0
3	**PME Interrupt Enable**	RO/Fwd R/W/Rev	No Yes	0 0
31:4	***Reserved***			0000_000h

Register 14-99. F90h Root Status

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**PME Requester ID**	RO	No	0000h
16	**PME Status**	R/W1C	No	0
17	**PME Pending**	RO	No	0
31:18	***Reserved***			0000h

Register 14-100. F94h Root Error Command

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Correctable Error Reporting Enable**	RO/Fwd R/W/Rev	No Yes	0 0
1	**Non-Fatal Error Reporting Enable**	RO/Fwd R/W/Rev	No Yes	0 0
2	**Fatal Error Reporting Enable**	RO/Fwd R/W/Rev	No Yes	0 0
31:3	***Reserved***			0-0h

Register 14-101. F98h Root Error Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Correctable Error Received**	RO/Fwd R/W1CS/Rev	No Yes	0 0
1	**Multiple Correctable Errors Received**	RO/Fwd R/W1CS/Rev	No Yes	0 0
2	**Uncorrectable Error Received**	RO/Fwd R/W1CS/Rev	No Yes	0 0
3	**Multiple Uncorrectable Errors Received**	RO/Fwd R/W1CS/Rev	No Yes	0 0
4	**First Uncorrectable Fatal**	RO/Fwd R/W1CS/Rev	No Yes	0
5	**Non-Fatal Error Message Received**	RO/Fwd R/W1CS/Rev	No Yes	0
6	**Fatal Error Message Received**	RO/Fwd R/W1CS/Rev	No Yes	0
26:7	***Reserved***			0000_0h
31:27	**Advanced Error Interrupt Message Number**	RO	No	00000b

Register 14-102. F9Ch Error Identification

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**Error Correctable Source Identification**	RO/Fwd ROS/Rev	No No	0000h 0000h
31:16	**Error Fatal/Non-Fatal Source Identification**	RO/Fwd ROS/Rev	No No	0000h 0000h

14.16 PCI-X-Specific Registers

Table 14-24. PCI-X-Specific Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Clock Enable, Strong Ordering, Read Cycle Value				FA0h
Prefetch			***Reserved***	FA4h

Register 14-103. FA0h PCI Clock Enable, Strong Ordering, Read Cycle Value

Bit(s)	Description	Type	Serial EEPROM	Default
3:0	**PCI_CLKO_EN[3:0]** PCI_CLKO_EN[0]=1 enables PCI_CLKO0 PCI_CLKO_EN[1]=1 enables PCI_CLKO1 PCI_CLKO_EN[2]=1 enables PCI_CLKO2 PCI_CLKO_EN[3]=1 enables PCI_CLKO3	R/W	Yes	0h if STRAP_CLK_MST=0 Fh if STRAP_CLK_MST=1
4	**Cache Line Prefetch Line Count** Controls the number of lines prefetched during Memory Reads. 0 = 1 Cache Line 1 = 2 Cache Lines; used only if the *Cache Line Size* field (offset 0Ch[7:0]) is less than or equal to 16 DWords (64 bytes)	R/W	Yes	0
5	**Disable Completion Timeout Timer** Refer to Section 7.7, "Transaction Transfer Failures."	R/W	Yes	0
6	**Enable Long Completion Timeout Timer** Refer to Section 7.7, "Transaction Transfer Failures."	R/W	Yes	1
7	**Disable BAR0**	R/W	Yes	0
8	**Force Strong Ordering** After data is returned to the PEX 8114 in response to a Read request, the PEX 8114 Retries the same transaction until complete and does not attempt to gather data from other outstanding transactions.	R/W	Yes	0
9	***Reserved***			0
10	**PLL Lock Control 0** Resets on loss of PLL lock, unless bits [11:10]=00b. (Refer to Table 14-25 for methods of handling loss of PLL lock.)	R/W	Yes	0
11	**PLL Lock Control 1** Reset after timer timeout on loss of PLL lock. (Refer to Table 14-25 for methods of handling loss of PLL lock.)	R/W	Yes	0
12	**Memory Read Line Multiple Enable**	R/W	Yes	0
13	**Address Stepping Enable**	R/W	Yes	0
14	**Sticky PCI-X PLL Loss Lock** Set when the PCI-X PLL loses PLL lock.	R/W1CS	Yes	0
15	**Sticky PCI Express PLL Loss Lock** Set when the PCI Express PLL loses PLL lock.	R/W1CS	Yes	0
26:16	**Maximum Read Cycle Value**	R/W	Yes	7FFh
27	**Retry Failure Status**	R/W1C	Yes	0
31:28	***Reserved***			0h

Table 14-25. Methods for Handling Loss of PLL Lock

Offset FA0h[11:10]	Description
00b	Default. Ignores loss of PLL lock.
01b	A loss of PLL lock immediately causes the PEX 8114 to reset.
10b	The PEX 8114 attempts to tolerate loss of PLL lock: • When lock is re-acquired in less than 200 µs, the PEX 8114 does not reset • When lock is not re-acquired within 200 µs, the PEX 8114 is reset
11b	The PEX 8114 does not reset if loss of PLL lock occurs.

Register 14-104. FA4h Prefetch

Bit(s)	Description	Type	Serial EEPROM	Default
7:0	***Reserved***			00h
13:8	**Prefetch Space Count** Valid only in PCI mode. Not used in PCI-X mode. Specifies the number of DWords to prefetch for Memory Reads originating on the PCI Bus that are forwarded to the PCI Express interface. Only even values between 0 and 32 are allowed. When the PEX 8114 is configured as a Forward bridge, prefetching occurs for all Memory Reads of Prefetchable and Non-Prefetchable Memory space. This occurs because the BARs are not used for Memory Reads, making it impossible to determine whether the space is prefetchable. In Reverse Transparent Bridge mode, prefetching occurs only for Memory Reads that address Prefetchable Memory space. Prefetching is Quad-word aligned, in that data is prefetched to the end of a Quad-word boundary. The number of DWords prefetched is as follows: • PEX 8114 prefetches 2 DWords when the following conditions are met: – *Prefetch Space Count* field is cleared to 00h, and – PCI_AD0 or PCI_AD1 is High – PCI_REQ64# is asserted (Low) • PEX 8114 prefetches 1 DWord when the following conditions are met: – *Prefetch Space Count* field is cleared to 00h, and – PCI_AD0 or PCI_AD1 is High – PCI_REQ64# is de-asserted (High) • When the *Prefetch Space Count* field contains an Even value greater than 0 and PCI_AD2 is High, the number of Prefetched DWords is 1 DWord less than the value in the *Prefetch Space Count* field; otherwise, the number of DWords prefetched is equal to the value in the *Prefetch Space Count* field. Only Even values between 0 and 32 are allowed. Odd values provide unexpected results.	R/W	Yes	20h
31:14	***Reserved***			0-0h

14.17 PCI Arbiter Registers

Table 14-26. PCI Arbiter Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Arbiter 0				FA8h
Arbiter 1				FACh
Arbiter 2				FB0h

Register 14-105. FA8h Arbiter 0

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Arbiter Allocation 0**	R/W	Yes	000b
7:3	***Reserved***			00000b
10:8	**Arbiter Allocation 1**	R/W	Yes	001b
15:11	***Reserved***			00000b
18:16	**Arbiter Allocation 2**	R/W	Yes	010b
23:19	***Reserved***			00000b
26:24	**Arbiter Allocation 3**	R/W	Yes	011b
31:27	***Reserved***			00000b

Register 14-106. FACh Arbiter 1

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Arbiter Allocation 4**	R/W	Yes	100b
7:3	***Reserved***			00000b
10:8	**Arbiter Allocation 5**	R/W	Yes	000b
15:11	***Reserved***			00000b
18:16	**Arbiter Allocation 6**	R/W	Yes	001b
23:19	***Reserved***			00000b
26:24	**Arbiter Allocation 7**	R/W	Yes	010b
31:27	***Reserved***			00000b

Register 14-107. FB0h Arbiter 2

Bit(s)	Description	Type	Serial EEPROM	Default
2:0	**Arbiter Allocation 8**	R/W	Yes	011b
7:3	***Reserved***			00000b
10:8	**Arbiter Allocation 9**	R/W	Yes	100b
23:11	***Reserved***			0-0h
24	**Grant Mode**	R/W	Yes	0
31:25	***Reserved***			0000_000b

14.18 Advanced Error Reporting Capability Registers

Table 14-27. Advanced Error Reporting Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset	Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status			FB8h
Uncorrectable Error Mask			FBCh
Uncorrectable Error Severity			FC0h
Correctable Error Status			FC4h
Correctable Error Mask			FC8h
Advanced Error Capabilities and Control			FCCh
Header Log_0			FD0h
Header Log_1			FD4h
Header Log_2			FD8h
Header Log_3			FDCh
Secondary Uncorrectable Error Status			FE0h
Secondary Uncorrectable Error Mask			FE4h
Secondary Uncorrectable Error Severity			FE8h
Secondary Uncorrectable Error Pointer			FECh
Secondary Header Log			FF0h … FFCh

Register 14-108. FB4h PCI Express Enhanced Capability Header

Bit(s)	Description	Type	Serial EEPROM	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset**	RO	Yes	138h

Register 14-109. FB8h Uncorrectable Error Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
3:1	***Reserved***			000b
4	**Data Link Protocol Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
11:5	***Reserved***			0000_000b
12	**Poisoned TLP Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
13	**Flow Control Protocol Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
14	**Completion Timeout Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
15	**Completer Abort Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
16	**Unexpected Completion Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
17	**Receiver Overflow Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
18	**Malformed TLP Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
19	**ECRC Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
20	**Unsupported Request Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
31:21	***Reserved***			0-0h

Register 14-110. FBCh Uncorrectable Error Mask

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
3:1	***Reserved***			000b
4	**Data Link Protocol Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
11:5	***Reserved***			0000_000b
12	**Poisoned TLP Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
13	**Flow Control Protocol Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
14	**Completion Timeout Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
15	**Completer Abort Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
16	**Unexpected Completion Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
19	**ECRC Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
31:21	***Reserved***			0-0h

Register 14-111. FC0h Uncorrectable Error Severity

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Training Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
3:1	***Reserved***			000b
4	**Data Link Protocol Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
11:5	***Reserved***			0000_000b
12	**Poisoned TLP Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
13	**Flow Control Protocol Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
14	**Completion Timeout Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
15	**Completer Abort Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
16	**Unexpected Completion Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
17	**Receiver Overflow Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
18	**Malformed TLP Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
19	**ECRC Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
20	**Unsupported Request Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
31:21	***Reserved***			0-0h

Register 14-112. FC4h Correctable Error Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Receive Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
5:1	***Reserved***			0-0h
6	**Bad TLP Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
7	**Bad DLLP Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
8	**Replay Number Rollover Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
11:9	***Reserved***			000b
12	**Replay Timer Timeout Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
31:13	***Reserved***			0-0h

Register 14-113. FC8h Correctable Error Mask

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Receive Error Mask** 0 = Error reporting not masked 1 = Error reporting masked	R/WS	Yes	0
5:1	***Reserved***			0-0h
6	**Bad TLP Mask** 0 = Error reporting not masked 1 = Error reporting masked	R/WS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting not masked 1 = Error reporting masked	R/WS	Yes	0
8	**Replay Number Rollover Mask** 0 = Error reporting not masked 1 = Error reporting masked	R/WS	Yes	0
11:9	***Reserved***			000b
12	**Replay Timer Timeout Mask** 0 = Error reporting not masked 1 = Error reporting masked	R/WS	Yes	0
31:13	***Reserved***			0-0h

Register 14-114. FCCh Advanced Error Capabilities and Control

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register.	ROS	Yes	1_1111b
5	**ECRC Generation Capable** 0 = ECRC generation not supported 1 = ECRC generation supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation disabled 1 = ECRC generation enabled	R/WS	Yes	0
7	**ECRC Checking Capable** 0 = ECRC checking not supported 1 = ECRC checking supported, but must be enabled	RO	Yes	1
8	**ECRC Checking Enable** 0 = ECRC checking disabled 1 = ECRC checking enabled	R/WS	Yes	0
31:9	***Reserved***			0-0h

Register 14-115. FD0h Header Log_0

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_0** First DWord Header. TLP Header associated with error.	ROS	Yes	0-0h

Register 14-116. FD4h Header Log_1

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_1** Second DWord Header. TLP Header associated with error.	ROS	Yes	0-0h

Register 14-117. FD8h Header Log_2

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_2** Third DWord Header. TLP Header associated with error.	ROS	Yes	0-0h

Register 14-118. FDCh Header Log_3

Bit(s)	Description	Type	Serial EEPROM	Default
31:0	**TLP Header_3** Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0-0h

Register 14-119. FE0h Secondary Uncorrectable Error Status

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Target Abort on Split Completion Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
1	**Master Abort on Split Completion Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
2	**Received Target Abort Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
3	**Received Master Abort Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
4	***Reserved***			0
5	**Unexpected Split Completion Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
6	**Uncorrectable Split Completion Message Data Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
7	**Uncorrectable Data Parity Error Detected Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
8	**Uncorrectable Attribute Parity Error Detected Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
9	**Uncorrectable Address Parity Error Detected Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
10	**Delayed Transaction Discard Timer Expired Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
11	**PERR# Assertion Detected** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
12	**SERR# Assertion Detected** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
13	**Internal Bridge Error Status** 0 = No error detected 1 = Error detected	R/W1CS	Yes	0
31:14	***Reserved***			0-0h

Register 14-120. FE4h Secondary Uncorrectable Error Mask

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Target Abort on Split Completion Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
1	**Master Abort on Split Completion Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
2	**Received Target Abort Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
3	**Received Master Abort Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
4	***Reserved***			0
5	**Unexpected Split Completion Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
6	**Uncorrectable Split Completion Message Data Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
7	**Uncorrectable Data Parity Error Detected Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1

Register 14-120. FE4h Secondary Uncorrectable Error Mask *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM	Default
8	**Uncorrectable Attribute Parity Error Detected Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
9	**Uncorrectable Address Parity Error Detected Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
10	**Delayed Transaction Discard Timer Expired Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
11	**PERR# Assertion Detected Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
12	**SERR# Assertion Detected Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	1
13	**Internal Bridge Error Mask** 0 = No mask is set 1 = Error reporting, first error update, and Header logging are masked for this error	R/WS	Yes	0
31:14	***Reserved***			0-0h

Register 14-121. FE8h Secondary Uncorrectable Error Severity

Bit(s)	Description	Type	Serial EEPROM	Default
0	**Target Abort on Split Completion Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
1	**Master Abort on Split Completion Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
2	**Received Target Abort Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
3	**Received Master Abort Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
4	***Reserved***			0
5	**Unexpected Split Completion Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
6	**Uncorrectable Split Completion Message Data Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
7	**Uncorrectable Data Parity Error Detected Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
8	**Uncorrectable Attribute Parity Error Detected Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
9	**Uncorrectable Address Parity Error Detected Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
10	**Delayed Transaction Discard Timer Expired Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
11	**PERR# Assertion Detected Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
12	**SERR# Assertion Detected Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	1
13	**Internal Bridge Error Severity** 0 = Error reported as non-fatal 1 = Error reported as fatal	R/WS	Yes	0
31:14	***Reserved***			0-0h

Register 14-122. FECh Secondary Uncorrectable Error Pointer

Bit(s)	Description	Type	Serial EEPROM	Default
4:0	**Secondary Uncorrectable Error Pointer**	ROS	No	00000b
31:5	***Reserved***			0000_000h

Register 14-123. FF0h – FFCh Secondary Header Log

Bit(s)	Description	Type	Serial EEPROM	Default
35:0	**Transaction Attribute**	ROS	No	0-0h
39:36	**Transaction Command Lower**	ROS	No	0-0h
43:40	**Transaction Command Upper**	ROS	No	0-0h
63:44	***Reserved***			0-0h
127:64	**Transaction Address**	ROS	No	0-0h

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Chapter 15 Test and Debug

15.1 Physical Layer Loop-Back Operation

15.1.1 Overview

Physical layer loop-back functions are used to test SerDes in the PEX 8114, connections between devices, SerDes of external devices, and certain PEX 8114 and external digital logic.

The PEX 8114 supports five types of loop-back operations:

- **Internal Loop-Back** – Connects SerDes serial Tx output to serial Rx input. The PRBS generator is used to create a pseudo-random data pattern that is transmitted and returned to the PRBS checker.
- **Analog Loop-Back Master** – This SerDes test depends on an external device or dumb connection (*such as* a cable) to loop back the transmitted data to the PEX 8114. If an external device is used, it must not include its elastic buffer in the Loop-Back data path because no SKIP Ordered-Sets are transmitted. Use the PRBS generator and checker to create and check the data pattern.
- **Digital Loop-Back Master** – As with the Analog Loop-Back Master mode, this method depends upon an external device to loop back the transmitted data. This method is best utilized with an external device that includes at least its elastic buffer in the Loop-Back data path. The PEX 8114 provides user-definable data pattern generators and checkers that insert the SKIP Ordered-Set at the proper intervals.
- **Analog Loop-Back Slave** –The PEX 8114 enters Analog Loop-Back Slave mode when an external device transmits training sets with the **Physical Layer Port Command** register *Port 0 Loop-Back* bit (offset 230h[0]) set, and the **Physical Layer Test** register *Analog Loop-Back Enable* bit (offset 228h[4]) is set. The received data is looped back from the SerDes 10-bit receive interface to the 10-bit transmit interface. All digital logic is excluded from the Loop-Back data path.
- **Digital Loop-Back Slave** – The PEX 8114 enters Digital Loop-Back Slave mode when an external device transmits training sets with the **Physical Layer Port Command** register *Port 0 Loop-Back* bit set, and the *Analog Loop-Back Enable* bit is clear. In this mode, the data is looped back at an 8-bit level, which includes the PEX 8114 elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Loop-Back data path.

15.1.2 Loop-Back Test Modes

The PEX 8114 supports all Loop-Back modes described in the *PCI Express Base 1.0a*. To establish the PEX 8114 as a Loop-Back Master, the serial EEPROM is used to Write 1 to the **Physical Layer Port Command** register *Port 0 Ready as Loop-Back Master* bit (offset 230h[3]). This enables the PEX 8114 to set its *Port 0 Loop-Back* bit (offset 230h[0]) in the training sets during the *Configuration.Linkwidth.Start* state.

After the PEX 8114 is established as a Loop-Back Master, the **Physical Layer Port Command** register *Port 0 Ready as Loop-Back Master* bit is set. Depending on the capability of the Loop-Back Slave, the PRBS generator or Bit-Pattern generator is used to create a bit stream that is checked by checking logic.

When the PEX 8114 is established as a Loop-Back Slave, it can operate as an Analog or Digital (default) Far-End device.

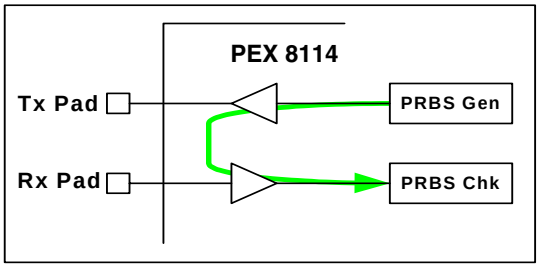
- Analog Loop-Back mode is selected by setting the **Physical Layer Test** register *Analog Loop-Back Enable* bit (offset 228h[4]) to 1. In Analog Loop-Back mode, the received data is looped back from the 10-bit received data, to the 10-bit transmit data.
- When Digital Loop-Back mode is selected (power-on default), the data is looped back from the 8-bit decoded received data to the 8-bit transmit data path. This loop-back point allows the elastic buffer 8b/10b decoder, and 8b/10b encoder to be included in the test data path. Digital Loop-Back mode requires that SKIP Ordered-Sets are included in the data stream.

15.1.2.1 Internal Loop-Back

Figure 15-1 illustrates the Loop-Back data path when Internal Loop-Back mode is enabled. The only items in the data path are the serializer and de-serializer. Loop-Back mode is used when the SerDes Built-In Self-Test (BIST) is enabled.

SerDes BIST is intended to overlap with the serial EEPROM load operation. To achieve this overlap, the **Physical Layer Test** register *SerDes BIST Enable* bit (offset 228h[7]) is written early in the serial EEPROM load operation. After the *SerDes BIST Enable* bit is set, SerDes is placed in Loop-Back mode and the PRBS generator is started. The BIST is run for 512 µs; if an error is detected on a SerDes, then the **Quad SerDes[0-3] Diagnostics Data** register (offset 238h) logs the number of PRBS errors generated for the group of SerDes lanes. While the SerDes BIST is in progress, the PRBS test data is present on the external TxP and TxN balls. The Tx Pad TxN signals must have an AC-coupled, 50-Ohm termination to ground. The reloading of the Serial EEPROM register load has no effect on the SerDes BIST.

Figure 15-1. Internal Loop-Back (Analog near End) Data Path



15.1.2.2 Analog Loop-Back Master

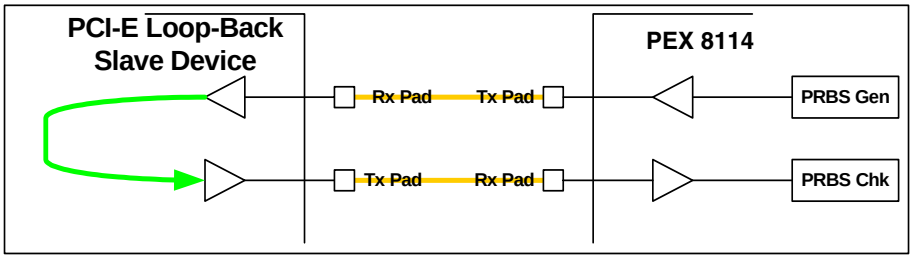
Analog Loop-Back mode is normally used for Analog Far-End testing; however, the mode can also be used to re-create the previously described BIST by looping back the data with a cable. (Refer to Figure 15-2.)

Looping back with a cable includes the internal bond, external balls, any board trace, and connectors in the test data path. (Refer to Figure 15-3.)

To cause the PEX 8114 to request to become a Loop-Back Master, the following must be accomplished:

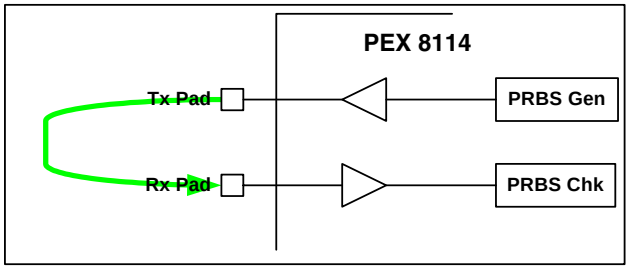
1. After the link is up, a Configuration Write to the **Physical Layer Port Command** register *Port 0 Loop-Back* bit (offset 230h[1]) causes the PEX 8114 to transition from the L0 state to Recovery, then to the Loop-Back state:
   - If a cable is used for a loop-back, the PEX 8114 transitions from the Configuration state to the Loop-Back state. Connect this cable only after the upstream link is up and Configuration Writes are possible.
   - If the cable is connected before the upstream device is able to set the *Analog Loop-Back Enable* bit, the link with the cable can reach the L0 state and not go to the Loop-Back state.
   - Cable length is limited only by the PCI Express drivers and cable properties.
2. After the PEX 8114 is in the Loop-Back state, the **Physical Layer Port Command** register *Port 0 Ready as Loop-Back Master* bit is set:
   - At this time, the PRBS engine is enabled by setting the *PRBS Enable* bit (offset 228h[16]).
   - The returned PRBS data is checked by the PRBS checker. Errors are logged in the **Quad SerDes[0-3] Diagnostics Data** register (offset 238h).

Figure 15-2. Analog Far-End Loop-Back



PCI-E = PCI Express

Figure 15-3. Cable Loop-Back



15.1.2.3 Digital Loop-Back Master

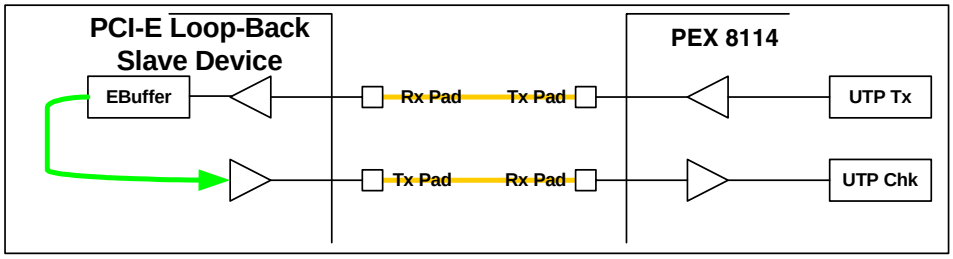
The only difference between the Analog and Digital Loop-Back Master modes is that the external device is assumed to possess certain digital logic in the Loop-Back data path. Because this includes the elastic buffer, SKIP Ordered-Sets must be included in the test data pattern. For the PEX 8114, this precludes PRBS engine use.

The PEX 8114 provides the User Data Patterns (offsets 210h through 21Ch) transmitter for Digital Far-End Loop-Back testing. The following must be accomplished:

1. After Loop-Back Master mode is established, Configuration Writes are used to fill the Test Data Pattern registers. The **Physical Layer Test** register *Test Pattern Enable* bit (offset 228h[28]) is set; this starts the transmission of the user data pattern on all lanes:
   - If the **Physical Layer Test** register *Port/SerDes Test Pattern Enable Select* bit (offset 228h[5]) is also set, the test pattern is transmitted on all lanes, regardless of width.
   - If the *Port/SerDes Test Pattern Enable Select* bit is clear, then the test pattern is transmitted only on the lanes.
2. SKIP Ordered-Sets are inserted at the interval determined by the value in the SKIP Interval register (default value is 1,180 symbol times) at the nearest data pattern boundary.

   The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loop-Back Slave, because the number of SKIP symbols received are different from the number transmitted.
3. All other data is compared to the data transmitted and errors are logged in the **Quad SerDes[0-3] Diagnostics Data** register.

Figure 15-4. Digital Far-End Loop-Back

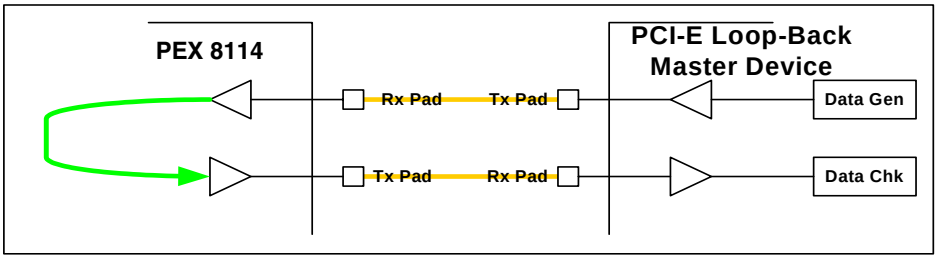


15.1.2.4 Analog Loop-Back Slave

The PEX 8114 becomes an Analog Loop-Back Slave if it receives training sets with the **Physical Layer Port Command** register *Port 0 Loop-Back* bit (offset 230h[0]) set while the **Physical Layer Test** register *Analog Loop-Back Enable* bit (offset 228h[4]) is set. (Refer to Figure 15-5.)

While an Analog Loop-Back Slave, the PEX 8114 only includes the de-serializer and serializer in the Loop-Back data path. The Loop-Back Master must provide the test data pattern and data pattern checking. It is unnecessary for the Loop-Back Master to include SKIP Ordered-Sets in the data pattern.

Figure 15-5. Analog Loop-Back Slave Mode



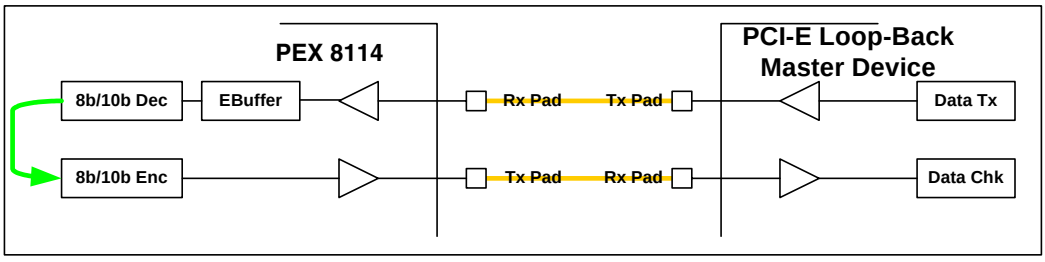
15.1.2.5 Digital Loop-Back Slave

The PEX 8114 becomes a Digital Loop-Back Slave if it receives training sets with the **Physical Layer Port Command** register *Port 0 Loop-Back* bit set while the **Physical Layer Test** register *Analog Loop-Back Enable* bit is clear. (Refer to Figure 15-6.)

When the PEX 8114 is a Digital Loop-Back Slave, it includes the elastic buffer and 8b/10b decoder and encoder in the Loop-Back data path. The Loop-Back Master must provide the test data pattern and data pattern checker. Additionally, the Master must transmit valid 8b/10b symbols, for the Loop-Back data from the Slave to be valid.

The Loop-Back Master must also transmit SKIP Ordered-Sets with the data pattern. The data checker must make provisions for the PEX 8114 to return more or fewer SKIP symbols than it received.

Figure 15-6. Digital Loop-Back Slave Mode



15.2 Pseudo-Random and Bit-Pattern Generation

The SerDes quad contains a PRBS generator and checker. The PRBS generator is based on a 7-bit Linear Feedback Shift register (LFSR), which can generate up to $(2^7 - 1)$ unique patterns. The PRBS logic is assigned to a SerDes within the quad by manipulating the **Physical Layer Test** register *PRBS Association* field (offset 228h[9:8]). The PRBS bit stream is used for internal SerDes or analog far-end loop-back testing.

The PEX 8114 also provides a method of creating a repeating user-defined bit pattern. Each of the four 32-bit Test Pattern registers are loaded with a 32-bit data pattern. After the PEX 8114 is established as a Loop-Back Master, the **Physical Layer Test** register *Test Pattern Enable* bit (offset 228h[28]) is set to 1. The PEX 8114 proceeds to transmit the data pattern on all lanes, starting with byte 0 of the **Test Pattern_0** register, and continuing in sequence through the byte 3 of the **Test Pattern_3** register. SKIP Ordered-Sets are inserted at the proper intervals, which makes this method appropriate for Digital Far-End Loop-Back testing. The received pattern is checked/compared for errors. The errors are logged and retrieved by reading the **Quad SerDes[0-3] Diagnostics Data** register.

15.3 JTAG Interface

The PEX 8114 provides a JTAG Boundary Scan interface, which is utilized to debug board connectivity for each ball.

15.3.1 *IEEE 1149.1* and *1149.6* Test Access Port

The *IEEE 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG (Joint Test Action Group) debug port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal bridge facilities, using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. These enhancements, which comply with *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG debug port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS – and optional JTAG_TRST# signal
- Clock Requirements – The JTAG_TCK signal frequency ranges from DC to 10 MHz
- JTAG Reset Requirements – Refer to Section 15.3.4, "JTAG Reset Input TRST#"

15.3.2 JTAG Instructions

The JTAG debug port provides the *IEEE Standard 1149.1-1990* EXTEST, SAMPLE/PRELOAD, BYPASS, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. *PRIVATE* instructions are for PLX use only. Invalid instructions behave as *BYPASS* instructions. Table 15-1 defines the JTAG instructions, along with their input codes.

The PEX 8114 returns the IDCODE values listed in Table 15-2.

Table 15-1. JTAG Instructions

Instruction	Input Code	Comments
EXTEST	00000b	*IEEE Standard 1149.1-1990*
IDCODE	00001b	
SAMPLE/PRELOAD	00010b	
BYPASS	11111b	
EXTEST_PULSE	00011b	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	00100b	
PRIVATE[a]		

*a. **Warning: Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.***

Table 15-2. PEX 8114 JTAG IDCODE Values

Unit of Measure	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	1000b	0001_1111_1011_0010b	001_1100_1101b	1
Hex	8h	1FB2h	1CDh	1h
Decimal	8	8114	461	1

15.3.3 JTAG Boundary Scan

Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture.* BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, defines a rigorous description of testability features in components which comply with the *Standard*. It is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical port description, physical ball map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the PEX 8114 balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the PEX 8114 logical ports to the physical balls of a specific package. A BSDL description can have several physical ball maps; each map is given a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction Register to place the PEX 8114 in the various test modes defined by the *Standard*. Instruction set statements also support descriptions of instructions that are unique to the PEX 8114.

The Boundary register description lists each cell or shift stage of the Boundary register. Each cell has a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains further details, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

15.3.4 JTAG Reset Input TRST#

The JTAG_TRST# input ball is the asynchronous JTAG logic reset. When JTAG_TRST# is asserted, it causes the PEX 8114 JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8114 normal logic path (core-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- When JTAG functionality is required, consider one of the following:
  - JTAG_TRST# input signal to use a Low-to-High transition once during the PEX 8114 boot-up, along with the system PEX_PERST# signal
  - Hold the PEX 8114 TMS ball High while transitioning the PEX 8114 JTAG_TCK ball five times
- When JTAG functionality is not required, directly connect the JTAG_TRST# signal to Ground

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Chapter 16 Electrical Specifications

16.1 Introduction

This chapter contains the PEX 8114 Power-On Sequencing rules and electrical specifications.

16.2 PEX 8114 Power-On Sequence

The PEX 8114 requires three voltage sources:

- 3.3V for I/O power and Clock PLL power, supplied by the VDD33 and VDD33A balls
- 1.35 to 1.8V for SerDes Transmitter Common-mode biasing, supplied by the VTT_PEX[1:0] balls
- 1.0V ±0.1V for SerDes/Core power, supplied by the VDD10, VDD10A, and VDD10S balls

VDD10, VDD10A, and VDD10S must power-up first and power-down last. If properly sequenced, all supply rails power-up within 50 ms of one another.

16.3 Absolute Maximum Ratings

Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8114 at these limits is not recommended.

Table 16-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD33	-0.5 to +4.6	V
PLL Supply Voltage	VDD33A	-0.5 to +4.6	V
SerDes Analog Supply Voltage	VDD10A	-0.3 to +1.65[a]	V
SerDes Digital Supply Voltage	VDD10S	-0.3 to +1.65[a]	V
SerDes Termination Supply Voltage	VTT_PEX[1:0]	2.5	V
Core (logic) Supply Voltage	VDD10	-0.3 to +1.65	V
Input Voltage (3.3V Interface)	V_I	-0.3 to +4.6	V
Core VDD Voltage	VDD10	1.0 ±0.1	V
Operating Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

a. The SerDes Analog and Digital power supplies must track within 0.01V of one another.

Table 16-2. Capacitance for Logic/Control I/O

Item	Symbol	Conditions	Min	Typ	Max	Unit
Input Ball	C_{IN}	VDD33/A = 0.0V, VDD10/A/S = 0.0V		4	6	pF
Output Ball	C_{OUT}			6	10	pF
Input/Output and Three-State Ball	$C_{I/O}$			6	10	pF

Table 16-3. Power Dissipation

Parameter	Symbol	Conditions[a]	Min.	Typ	Max	Unit
Power Dissipation	PD	VDD33/A = 3.3V, ±10% VDD10/A/S = 1.0V, ±10% VTT_PEX[1:0] = 1.5V, ±10%	300 1.475 115		375 1.93 150	mW W mW

a. PEX_REFCLKn/p = 100 MHz. A 250-MHz clock is synthesized from PEX_REFCLKn/p and used internally to clock the SerDes and core logic.

16.4 Digital Logic Interface Operating Characteristics

Unless specified otherwise, general operating conditions are:

VDD33 = 3.3V ±0.3V, VDD10 = 1.0V ±0.1V, T_A = -40 to +85°C

Table 16-4. Digital Logic Interface Operating Electrical Characteristics

Symbol	Parameter	Test Conditions	Ranges and Limits			Units
			Min	Typ	Max	
VDD33	Operating Voltage (I/O)		3.0	3.3	3.6	V
VDD33A	Operating Voltage for PLL		3.0	3.3	3.6	V
VDD10	Operating Voltage (Core)		0.9	1.0	1.1	V
VTT_PEX	SerDes Termination Supply Voltage		1.35	1.5	1.8	V
V_{IL}	Input Low Voltage for PCI/PCI-X inputs		-0.5		0.3 VDD33	V
	Input Low Voltage for TTL inputs[a]				0.8	V
V_{IH}	Input High Voltage for PCI/PCI-X inputs		0.5 VDD33		VDD33 +0.5	V
	Input High Voltage for TTL inputs[a]		2.0			V
I_{IN}	Input Leakage Current	0V < V_{IN} < VDD33 I/O balls set to High Impedance	-10.0[b]		+10.0[b]	µA
V_{OL}	Output Low Voltage PCI/PCI-X outputs	I_{LOAD} = 1500 µA			0.1 VDD33	V
	Output Low Voltage TTL outputs[a]	I_{LOAD} = 8 mA[c]			0.4	V
V_{OH}	Output High Voltage PCI/PCI-X outputs	I_{LOAD} = -500 µA	0.9 VDD33			V
	Output High Voltage TTL outputs[a]	I_{LOAD} = -8 mA[d]	2.4			V

a. CMOS Technology designed as TTL-compatible.

b. Current into the ball is shown as "+" and current out of the ball is shown as "-".

c. Exception – I_{LOAD} = +12 mA for EE_DO ball.

d. Exception – I_{LOAD} = -12 mA for EE_DO ball.

16.4.1 SerDes/Lane Interface DC Characteristics

Unless specified otherwise, general operating conditions are:

VDD33A = 3.3V ±0.3V, VDD10S = VDD10A = 1.0V ±0.1V, T_A = -40 to +85°C

Table 16-5. SerDes Interface DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
VTT_PEX[1:0]	SerDes Termination Voltage		1.35	1.5	165	V
VDD10A	SerDes Analog Supply Voltage[a]		0.9	1.0	1.1	V
VDD10S	SerDes Digital Supply Voltage[a]		0.9	1.0	1.1	V
I_{DDA}	SerDes Supply Current	PEX_REFCLKn/p = 100 MHz		65	97.5	mA
I_{DDS}	SerDes Supply Current	PEX_REFCLKn/p = 100 MHz		140	210	mA
I_{VTT_PEX}	SerDes Termination Supply Current			87	105	mA
PEX_PET Transmit Outputs						
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	1.3V < V_{TT} < 1.6V[b]	0.8	1.0	1.2	V
$V_{TX\text{-}CM\ AC\_P}$	RMS A Peak Output Voltage				20	mV
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute Delta between DC Common-mode during L0 and Electrical Idle		0.0		100	mV
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Maximum Common Mode Voltage Delta between PEX_PETn[3:0] and PEX_PETp[3:0]				25	mV
$V_{TX\text{-}DE\text{-}RATIO}$	De-Emphasis differential output voltage ratio		0.0[c]	-3.5	-7.96[c]	dB
$V_{TX\text{-}IDLE\_DIFF\_PS}$	Maximum Peak output voltage during link idle state				20	mV
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of common-mode voltage change allowed during receiver detection				600	mV
$I_{TX\text{-}SHORT}$	Output Short-Circuit current	$V_{TX\text{-}OUT}$ = 0.0V			90	mA
$Z_{TX\text{-}DIFF\text{-}DC}$	Differential Output Impedance		80	100	120	Ohm
$Z_{TX\text{-}DC}$	Output Impedance for each transmitter in all power states		40			Ohm
$RL_{TX\text{-}DIFF}$	Differential Return Loss		12			dB
$RL_{TX\text{-}CM}$	Common-mode Return Loss		6			dB

Table 16-5. SerDes Interface DC Electrical Characteristics *(Cont.)*

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
PEX_PERn[3:0]/PEX_PERp[3:0] Receiver Inputs						
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Input Voltage		0.175		1.200	V
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Idle detect threshold voltage		65		175	mV
$V_{RX\text{-}CM\ AC}$	Receiver Common-mode voltage for AC Coupling				150	mV
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance		80	100	120	Ohm
$Z_{RX\text{-}DC}$	DC Input Impedance		40	50	60	Ohm
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Input Impedance during power down conditions		200K			Ohm
$RL_{RX\text{-}DIFF}$	Differential Return Loss		15			dB
$RL_{RX\text{-}CM}$	Common-mode Return Loss		6			dB

a. The SerDes Analog and Digital power supplies must track within 0.01V of one another.

b. For V_{TT} voltages between 1.0 to 1.8V, refer to Table 16-1. [The V_{TT} test condition for $V_{TX\text{-}DIFFp\text{-}p}$ (listed above) is derived from Table 16-1.]

c. $V_{TX\text{-}DE\text{-}RATIO}$ can be programmed to exceed the PCI Express r1.0a of MIN -3.0, MAX -4.0.

16.5 SerDes Interface AC Specifications

Unless specified otherwise, general operating conditions are:

VDD33A = 3.3V ± 0.3V, VDD10S = VDD10A = 1.0V ± 0.1V, T_A = -40 to +85°C

Table 16-6. SerDes Interface AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
PEX_PET Transmit Outputs						
UI	Unit Interval		399.88	400	400.12	ps
$T_{TX-Rise}$	Differential signal rise time	20 to 80%	0.125		0.3	UI
$T_{TX-Fall}$	Differential signal fall time	20 to 80%	0.125		0.3	UI
$T_{TX-IDLE-MIN}$	Minimum idle time for transmitter		50			UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Transmitter recovery time from Idle state to fully active transmit state				20	UI
T_{TX-EYE}	Transmitter Eye width		0.7			UI
$L_{TX-SKEW}$	Lane-to-lane static output skew for all lanes in port/link				1.3	ns
PEX_PER Receive Inputs						
UI	Unit Interval		399.88	400	400.12	ps
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Maximum time required for receiver to recognize and signal an unexpected idle on link				10	ms
T_{RX-EYE}	Receiver Eye width		0.4			UI
$T_{RX-SKEW}$	Total Skew				20	ns

Table 16-7. PEX_REFCLOCK AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
PEX_REFCLK	100 MHz Differential Reference Clock Input			100		MHz
V_{CM}	Input Common Mode Voltage		0.6	0.65	0.7	V
$ClkIn_{DC}$	Input Clock Duty Cycle		40	50	60	%
T_R/T_F	Input Clock Rise/Fall Times				1.5	ns
V_{SW}	Differential Input Voltage Swing[a]		0.25		1.6	V
R_{TERM}	Reference Clock Differential Termination			110		Ohm

a. AC coupling required.

Table 16-8. PCI 33-MHz AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	Notes
T_{cyc}	PCI CLK Cycle Time		30		–	ns	
T_{val}	CLK to Signal Valid Delay – Bused Signals		2		11	ns	1, 2, 3, 8
$T_{val}(ptp)$	CLK to Signal Valid Delay – Point-to-Point Signals		2		12	ns	1, 2, 3, 8
T_{on}	Float to Active Delay		2			ns	1, 8, 9
T_{off}	Active to Float Delay				28	ns	1, 9
T_{su}	Input Setup Time to CLK – Bused Signals		7			ns	3, 4, 10
$T_{su}(ptp)$	Input Setup Time to CLK – Point-to-Point Signals		10, 12			ns	3, 4
T_{h}	Input Hold Time from CLK		0			ns	4
T_{rst}	Reset Active Time after Power Stable		1			ms	5
$T_{rst-clk}$	Reset Active Time after CLK Stable		100			µs	5
$T_{rst-off}$	Reset Active to Output Float Delay				40	ns	5, 6
T_{rrsu}	PCI_REQ64# to PCI_RST# Setup Time		$10T_{cyc}$			ns	
T_{rrh}	PCI_RST# to PCI_REQ64# Hold Time		0		50	ns	
T_{rhfa}	PCI_RST# High to First Configuration Access		2^{25}			clocks	
T_{rhff}	PCI_RST# High to First PCI_FRAME# Assertion		5			clocks	
T_{ckskew}	Clock Skew between Any PCI_CLKO[3:0] Outputs				130	ps	

Notes:

1. *Refer to the timing measurement conditions in the PCI r3.0, Figure 7-3. It is important that all driven signal transitions drive to their V_{oh} or V_{ol} level within one T_{cyc}.*
2. *Minimum times are measured at the package ball with the load circuit illustrated in the PCI r3.0, Figure 7-7. Maximum times are measured with the load circuit illustrated in the PCI r3.0, Figures 7-5 and 7-6.*
3. *PCI_GNT# and PCI_REQ# are point-to-point signals and have different input setup times than bused signals. The setup for PCI_GNT# and PCI_REQ# at 66 MHz is 5 ns. All other signals are bused.*
4. *Refer to the timing measurement conditions in the PCI r3.0, Figure 7-4.*
5. *When PCI_M66EN is asserted, CLK is stable when it meets the requirements in the PCI r3.0, Section 7.6.4.1. PCI_RST# is asserted and de-asserted asynchronously with respect to CLK. (Refer to the PCI r3.0, Section 4.3.2, for further details.)*
6. *Float all output drivers when PCI_RST# is active. (Refer to the PCI r3.0, Section 4.3.2, for further details.)*
8. *When PCI_M66EN is asserted, the minimum specification for $T_{val}(min)$, $T_{val}(ptp)(min)$, and T_{on} can be reduced to 1 ns if a mechanism is provided to guarantee a minimum value of 2 ns when PCI_M66EN is de-asserted.*
9. *For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined as when the total current delivered through the component ball is less than or equal to the leakage current specification.*
10. *Setup time applies when the PEX 8114 is not driving the ball. Devices cannot concurrently drive and receive signals. (Refer to the PCI r3.0, Section 3.10, item 9, for further details.)*

Table 16-9. PCI 66-MHz AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	Notes
T_{cyc}	PCI CLK Cycle Time		15		30	ns	
T_{val}	CLK to Signal Valid Delay – Bused Signals		2		6	ns	1, 2, 3, 8
$T_{val}(ptp)$	CLK to Signal Valid Delay – Point-to-Point Signals		2		6	ns	1, 2, 3, 8
T_{on}	Float to Active Delay		2			ns	1, 8, 9
T_{off}	Active to Float Delay				14	ns	1, 9
T_{su}	Input Setup Time to CLK – Bused Signals		3			ns	3, 4, 10
$T_{su}(ptp)$	Input Setup Time to CLK – Point-to-Point Signals		5			ns	3, 4
T_{h}	Input Hold Time from CLK		0			ns	4
T_{rst}	Reset Active Time after Power Stable		1			ms	5
$T_{rst-clk}$	Reset Active Time after CLK Stable		100			µs	5
$T_{rst-off}$	Reset Active to Output Float Delay				40	ns	5, 6
T_{rrsu}	PCI_REQ64# to PCI_RST# Setup Time		$10T_{cyc}$			ns	
T_{rrh}	PCI_RST# to PCI_REQ64# Hold Time		0		50	ns	
T_{rhfa}	PCI_RST# High to First Configuration Access		2^{25}			clocks	
T_{rhff}	PCI_RST# High to First PCI_FRAME# Assertion		5			clocks	
T_{ckskew}	Clock Skew between Any PCI_CLKO[3:0] Outputs				130	ps	

Notes:

1. *Refer to the timing measurement conditions in the PCI r3.0, Figure 7-3. It is important that all driven signal transitions drive to their V_{oh} or V_{ol} level within one T_{cyc}.*
2. *Minimum times are measured at the package ball with the load circuit illustrated in the PCI r3.0, Figure 7-7. Maximum times are measured with the load circuit illustrated in the PCI r3.0, Figures 7-5 and 7-6.*
3. *PCI_GNT# and PCI_REQ# are point-to-point signals and have different input setup times than bused signals. The setup for PCI_GNT# and PCI_REQ# at 66 MHz is 5 ns. All other signals are bused.*
4. *Refer to the timing measurement conditions in the PCI r3.0, Figure 7-4.*
5. *When PCI_M66EN is asserted, CLK is stable when it meets the requirements in the PCI r3.0, Section 7.6.4.1. PCI_RST# is asserted and de-asserted asynchronously with respect to CLK. (Refer to the PCI r3.0, Section 4.3.2, for further details.)*
6. *Float all output drivers when PCI_RST# is active. (Refer to the PCI r3.0, Section 4.3.2, for further details.)*
8. *When PCI_M66EN is asserted, the minimum specification for $T_{val}(min)$, $T_{val}(ptp)(min)$, and T_{on} can be reduced to 1 ns if a mechanism is provided to guarantee a minimum value of 2 ns when PCI_M66EN is de-asserted.*
9. *For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined as when the total current delivered through the component ball is less than or equal to the leakage current specification.*
10. *Setup time applies when the PEX 8114 is not driving the ball. Devices cannot concurrently drive and receive signals. (Refer to the PCI r3.0, Section 3.10, item 9, for further details.)*

Table 16-10. PCI-X 133-MHz AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	Notes
T_{cyc}	PCI CLK Cycle Time		7.5		30	ns	
T_{val}	CLK to Signal Valid Delay – Bused Signals		0.7		3.8	ns	1, 2, 3, 10, 11
$T_{val}(ptp)$	CLK to Signal Valid Delay – Point-to-Point Signals		0.7		3.8	ns	1, 2, 3, 10, 11
T_{on}	Float to Active Delay		0			ns	1, 7, 10, 11
T_{off}	Active to Float Delay			7		ns	1, 7, 11
T_{su}	Input Setup Time to CLK – Bused Signals		1.2			ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to CLK – Point-to-Point Signals		1.2			ns	3, 4
T_{h}	Input Hold Time from CLK		0.5			ns	4
T_{rst}	Reset Active Time after Power Stable		1			ms	5
$T_{rst-clk}$	Reset Active Time after CLK Stable		100			µs	5
$T_{rst-off}$	Reset Active to Output Float Delay				40	ns	5, 6
T_{rrsu}	PCI_REQ64# to PCI_RST# Setup Time		10			clocks	
T_{rrh}	PCI_RST# to PCI_REQ64# Hold Time		0		50	ns	9
T_{rhfa}	PCI_RST# High to First Configuration Access		2^{26}			clocks	
T_{rhff}	PCI_RST# High to First PCI_FRAME# Assertion		5			clocks	
T_{pvrh}	Power Valid to PCI_RST# High		100			ms	
T_{prsu}	PCI-X Initialization Pattern to PCI_RST# Setup Time		10			clocks	
T_{prh}	PCI_RST# to PCI-X Initialization Pattern Hold Time		0		50	ns	9

Table 16-10. PCI-X 133-MHz AC Specifications *(Cont.)*

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	Notes
T_{rlcx}	Delay from PCI_RST# Low to CLK Frequency CHange		0			ns	
T_{ckskew}	Clock Skew between Any PCI_CLKO[3:0] Outputs				130	ps	

Notes:

1. *Refer to the timing measurement conditions in the PCI-X r1.0b, Figure 9-6.*
2. *Minimum times are measured at the package ball (not the test point) with the load circuit illustrated in the PCI-X r1.0b, Figure 9-10. Maximum times are measured with the test point and load circuit illustrated in the PCI-X r1.0b, Figures 9-8 and 9-9.*
3. *Setup time for point-to-point signals applies only to PCI_GNT# and PCI_REQ#. All other signals are bused.*
4. *Refer to the timing measurement conditions in the PCI-X r1.0b, Figure 9-7.*
5. *PCI_RST# is asserted and de-asserted asynchronously with respect to CLK.*
6. *Float All output drivers when PCI_RST# is active.*
7. *For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined as when the total current delivered through the component ball is less than or equal to the leakage current specification.*
8. *Setup time applies only when the PEX 8114 is not driving the ball. Devices cannot concurrently drive and receive signals.*
9. *Maximum value is also limited by delay to the first transaction (T_{rhff}). The PCI-X initialization pattern controls signals and PCI_REQ64# after the rising edge of PCI_RST# must be de-asserted no later than two clocks before the first PCI_FRAME# and float no later than one clock before PCI_FRAME# is asserted.*
10. *A PCI-X device is permitted the minimum values shown for T_{val}, $T_{val}(ptp)$, and T_{on} only in PCI-X mode. In Conventional PCI mode, the device must meet the requirements specified in the PCI r3.0 for the appropriate clock frequency.*
11. *The PEX 8114 must meet this specification, independent of the amount of outputs switched simultaneously.*

Chapter 17 Mechanical Specifications

17.1 PEX 8114 Package Specifications

The PEX 8114 is offered in a 256-Ball, 17-mm square Plastic Ball Grid Array (BGA) package. Table 17-1 defines the package specifications.

Table 17-1. PEX 8114 256-Ball PBGA Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array
Package Dimensions	17 x 17 mm (approximately 1.86 mm high)
Ball matrix pattern	16 x 16 mm
Ball pitch	1.00 mm
Ball diameter	0.50 ±0.10 mm
Ball spacing	0.40 mm

17.2 Thermal Characteristics

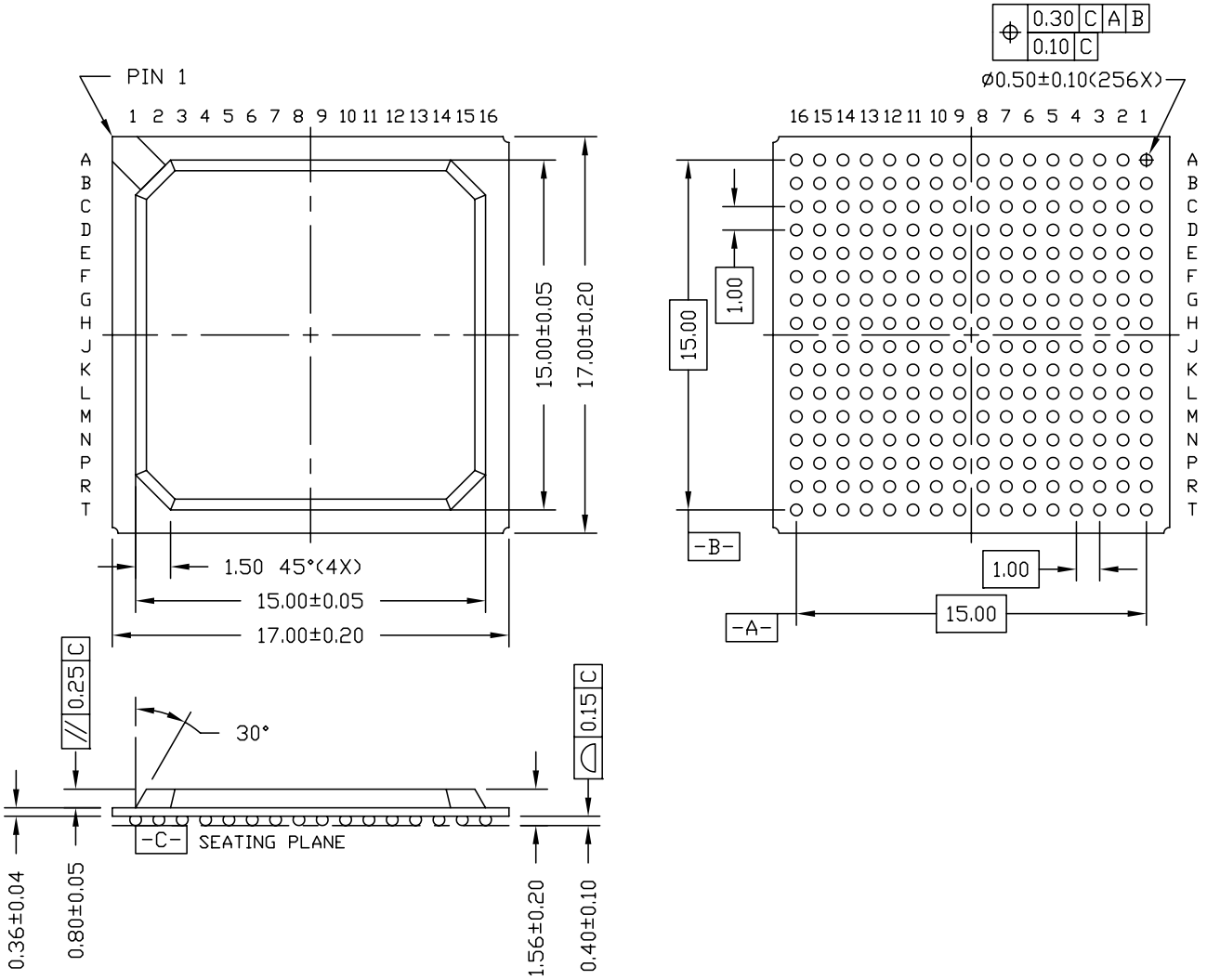
Table 17-2. PEX 8114 Package Thermal Resistance Airflow, Θ_{j-c} = 4.6 °C/W[a]

Theta	0 m/s	1 m/s	2 m/s
°C/W (Θ_{j-a})[b]	17.8	15.9	14.8

a. Relevant for packages used with external heat sinks.
b. Relevant for packages used without external heat sinks.
c. The PEX 8114 does not require a heat sink during standard operating conditions.

17.3 Mechanical Dimensions

Figure 17-1. PEX 8114 Mechanical Dimensions



Appendix A Serial EEPROM Map

For serial EEPROM addresses without corresponding register callout (indicated as ***Reserved***), those register locations must be padded with zeros (0000h) when loading the serial EEPROM. The last DWord in each serial EEPROM map is the CRC value. The offset for the CRC is at 03ECh.

A.1 Serial EEPROM Map

Table A-1. Serial EEPROM Map

Register Address	Register Name	Serial EEPROM Byte Offset
000h	Product Identification	0000h
004h	Command/Status	0004h, 0378h (refer to Note)
008h	Class Code and Revision ID	0008h
00Ch	Miscellaneous Control	000Ch
010h	Base Address 0	0010h
014h	Base Address 1	0014h
018h	Bus Number	0018h
01Ch	Secondary Status, I/O Limit, and I/O Base	001Ch
020h	Memory Base and Limit Address	0020h
024h	Prefetchable Memory Base and Limit Address	0024h
028h	Prefetchable Memory Upper Base Address[63:32]	0028h
02Ch	Prefetchable Memory Upper Limit Address[63:32]	002Ch
030h	I/O Base Address[31:16] and I/O Limit Address[31:16]	0030h
034h	New Capability Pointer ***(no serial EEPROM Write)***	0034h
038h	Expansion ROM Base Address ***(Not Supported)***	0038h
03Ch	Bridge Control and Interrupt Signal	003Ch, 037Ch (refer to Note)
040h	Power Management Capability List, Capabilities	0040h
044h	Power Management Status and Control	0044h, 03B8h, 03BCh, 03C0h, 03C4h (refer to Note)
048h	Message Signaled Interrupt Capability List, Control	0048h
04Ch	Lower Message Address[31:0]	004Ch
050h	Upper Message Address[63:32]	0050h
054h	Message Data	0054h
058h	PCI-X Capability List, Secondary Status	0058h
05Ch	PCI-X Bridge Status	005Ch
060h	Upstream Split Transaction Control	0060h
064h	Downstream Split Transaction Control	0064h
068h	PCI Express Capability List, Capabilities	0068h
06Ch	Device Capabilities	006Ch, 03A4h (refer to Note)
070h	Device Status and Control	0070h, 03A8h (refer to Note)
074h	Link Capabilities	0074h
078h	Link Status and Control	0078h, 03ACh (refer to Note)
07Ch	Slot Capabilities (Reverse Transparent Bridge Mode Only)	007Ch
080h	Slot Status and Control (Reverse Transparent Bridge Mode Only)	0080h
084h - 0FCh	***Register Addresses Skipped***	

Table A-1. Serial EEPROM Map *(Cont.)*

Register Address	Register Name	Serial EEPROM Byte Offset
100h	Device Serial Number Extended Capability	0084h
104h	Serial Number (Low)	0088h
108h	Serial Number (High)	008Ch
10Ch	***Reserved***	0090h
110h	***Reserved***	0094h
114h	***Reserved***	0098h
118h	***Reserved***	009Ch
11Ch	***Reserved***	00A0h
120h	***Reserved***	00A4h
124h	***Reserved***	00A8h
128h	***Reserved***	00ACh
12Ch	***Reserved***	00B0h
130h	***Reserved***	00B4h
134h	***Reserved***	00B8h
138h	Device Power Budgeting Extended Capability	00BCh
13Ch	Data Select	00C0h, 03CCh, 03D0h, 03D4h, 03D8h, 03DCh, 03E0h, 03E4h, 03E8h (refer to Note)
140h	Power Data	00C4h
144h	Power Budget Capability	00C8h
148h	Virtual Channel Budgeting Extended Capability	00CCh
14Ch	Port VC Capability 1	00D0h
150h	Port VC Capability 2 ***(Not Supported)***	00D4h
154h	Port VC Status and Control ***(Not Supported)***	00D8h, 03C8h (refer to Note)
158h	VC0 Resource Capability ***(Not Supported)***	00DCh
15Ch	VC0 Resource Control	00E0h
160h	VC0 Resource Status	00E4h
164h - 1C4h	***Register Addresses Skipped***	
1C8h	ECC Check Disable	00E8h
1CCh	Device-Specific Error 32-Bit Error Status (Factory Test Only)	00ECh
1D0h	Device-Specific Error 32-Bit Error Mask (Factory Test Only)	00F0h
1D4h	***Reserved***	00F4h
1D8h	***Reserved***	00F8h
1DCh	***Reserved***	00FCh
1E0h	Power Management Hot Plug User Configuration	0100h
1E4h	Egress Control and Status	0104h
1E8h	Bad TLP Count	0108h
1ECh	Bad DLLP Count	010Ch
1F0h	TLP Payload Length Count	0110h
1F4h	***Reserved***	0114h
1F8h	ACK Transmission Latency Limit	0118h
1FCh	***Reserved***	011Ch
200h	***Reserved***	0120h
204h	***Reserved***	0124h

Table A-1. Serial EEPROM Map *(Cont.)*

Register Address	Register Name	Serial EEPROM Byte Offset
208h	***Reserved***	0128h
20Ch	***Reserved***	012Ch
210h	Test Pattern_0	0130h
214h	Test Pattern_1	0134h
218h	Test Pattern_2	0138h
21Ch	Test Pattern_3	013Ch
220h	Physical Layer Status and Control	0140h
224h	Port Configuration	0144h
228h	Physical Layer Test	0148h
22Ch	Physical Layer (Factory Test Only)	014Ch
230h	Physical Layer Port Command	0150h
234h	SKIP Ordered-Set Interval	0154h
238h	Quad SerDes[0-3] Diagnostics Data	0158h
23Ch	***Reserved***	015Ch
240h	***Reserved***	0160h
244h	***Reserved***	0164h
248h	SerDes Nominal Drive Current Select	0168h
24Ch	SerDes Drive Current Level_1	016Ch
250h	***Reserved***	0170h
254h	SerDes Drive Equalization Level Select_1	0174h
258h - 25Ch	***Register Addresses Skipped***	
260h	Serial EEPROM Status and Control	0178h
264h - 2E4h	***Register Addresses Skipped***	
2E8h	Bus Number CAM 8	017Ch, 0388h (refer to Note)
2ECh	***Reserved***	0180h
2F0h	***Reserved***	0184h
2F4h	***Reserved***	0188h
2F8h	***Reserved***	018Ch
2FCh	***Reserved***	0190h
300h	***Reserved***	0194h
304h	***Reserved***	0198h
308h	***Reserved***	019Ch
30Ch	***Reserved***	01A0h
310h	***Reserved***	01A4h
314h	***Reserved***	01A8h
318h	I/O CAM_8	01ACh, 038Ch (refer to Note)
31Ch - 3C4h	***Register Addresses Skipped***	
3C8h	AMCAM_8 Memory Limit and Base	01B0h, 0390h (refer to Note)
3CCh	AMCAM_8 Prefetchable Memory Limit and Base[31:0]	01B4h, 0394h (refer to Note)
3D0h	AMCAM_8 Prefetchable Memory Base[63:32]	01B8h, 0398h (refer to Note)
3D4h	AMCAM_8 Prefetchable Memory Limit[63:32]	01BCh, 039Ch (refer to Note)
3D8h - 544h	***Register Addresses Skipped***	
548h	***Reserved***	01C0h

Table A-1. Serial EEPROM Map *(Cont.)*

Register Address	Register Name	Serial EEPROM Byte Offset
54Ch - 65Ch	***Register Addresses Skipped***	
660h	TIC Control	01C4h
664h	***Reserved***	01C8h
668h	TIC Port Enable (Factory Test Only)	01CCh
66Ch	***Reserved***	01D0h
670h	***Reserved***	01D4h
674h	***Reserved***	01D8h
678h	***Reserved***	01DCh
67Ch	***Reserved***	01E0h
680h	***Reserved***	01E4h
684h	***Reserved***	01E8h
688h	***Reserved***	01ECh
68Ch	***Reserved***	01F0h
690h	***Reserved***	01F4h
694h	***Reserved***	01F8h
698h	***Reserved***	01FCh
69Ch	***Reserved***	0200h
6A0h	I/OCAM_8 Base and Limit Upper 16 Bits	0204h, 03A0h (refer to Note)
6A4h	***Reserved***	0208h
6A8h	***Reserved***	020Ch
6ACh	***Reserved***	0210h
6B0h	***Reserved***	0214h
6B4h	***Reserved***	0218h
6B8h	***Reserved***	021Ch
6BCh	***Reserved***	0220h
6C0h	***Reserved***	0224h
6C4h	***Reserved***	0228h
6C8h	***Reserved***	022Ch
6CCh	***Reserved***	0230h
6D0h	***Reserved***	0234h
6D4h	***Reserved***	0238h
6D8h	***Reserved***	023Ch
6DCh	***Reserved***	0240h
6E0h	***Reserved***	0244h
6E4h	***Reserved***	0248h
6E8h	***Reserved***	024Ch
6ECh	***Reserved***	0250h
6F0h	***Reserved***	0254h
6F4h	***Reserved***	0258h
6F8h	***Reserved***	025Ch
6FCh	***Reserved***	0260h
700h	BAR0_8	0264h, 0380h (refer to Note)
704h	BAR1_8	0268h, 0384h (refer to Note)

Table A-1. Serial EEPROM Map *(Cont.)*

Register Address	Register Name	Serial EEPROM Byte Offset
708h - 9F0h	***Register Addresses Skipped***	
9F4h	INCH FC Update Pending Timer	026Ch
9F8h	***Reserved***	0270h
9FCh	INCH Mode	0274h
A00h	INCH Threshold VC0 Posted	0278h
A04h	INCH Threshold VC0 Non-Posted	027Ch
A08h	INCH Threshold VC0 Completion	0280h, 03B0h (refer to Note)
A0Ch - B7Ch	***Register Addresses Skipped***	
B80h	***Reserved***	0284h
B84h	***Reserved***	0288h
B88h	***Reserved***	028Ch
B8Ch	***Reserved***	0290h
B90h	***Reserved***	0294h
B94h	***Reserved***	0298h
B98h	***Reserved***	029Ch
B9Ch	***Reserved***	02A0h
BA0h - BE8h	***Register Addresses Skipped***	
BECh	***Reserved***	02A4h
BF0h	***Reserved***	02A8h
BF4h	***Reserved***	02ACh
BF8h	***Reserved***	02B0h
BFCh	***Reserved***	02B4h
C00h	PCI Express Interface PCI Express ITCH VC&T Threshold_1	02B8h
C04h	PCI Express Interface ITCH VC&T Threshold_2	02BCh
C08h	***Reserved***	02C0h
C0Ch	***Reserved***	02C4h
C10h	***Reserved***	02C8h
C14h - F50h	***Register Addresses Skipped***	
F54h	***Reserved***	02CCh
F58h	***Reserved***	02D0h
F5Ch	***Reserved***	02D4h
F60h	***Reserved***	02D8h
F64h	***Reserved***	02DCh
F68h	***Reserved***	02E0h
F6Ch	***Reserved***	02E4h
F70h	PCI-X Interface ITCH VC&T Threshold_1	02E8h
F74h	PCI-X Interface ITCH VC&T Threshold_2	02ECh
F78h	***Reserved***	02F0h
F7Ch	***Reserved***	02F4h
F80h	PCI-X Interface Device-Specific Error 32-Bit Error Status (Factory Test Only)	02F8h
F84h	PCI-X Interface Device-Specific Error 32-Bit Error Mask (Factory Test Only)	02FCh
F8Ch	PCI-X Interface Completion Buffer Timeout	0300h

Table A-1. Serial EEPROM Map *(Cont.)*

Register Address	Register Name	Serial EEPROM Byte Offset
F8Ch	Root Control	0304h
F90h	Root Status ***(no serial EEPROM Write)***	0308h
F94h	Root Error Command	030Ch
F98C	Root Error Status	0310h
F9Ch	Error Identification ***(no serial EEPROM Write)***	0314h
FA0h	PCI Clock Enable, Strong Ordering, Read Cycle Value	0318h
FA4h	Prefetch	031Ch
FA8h	Arbiter 0	0320h
FACh	Arbiter 1	0324h
FB0h	Arbiter 2	0328h
FB4h	PCI Express Enhanced Capability Header	032Ch
FB8h	Uncorrectable Error Status	0330h
FBCh	Uncorrectable Error Mask	0334h
FC0h	Uncorrectable Error Severity	0338h
FC4h	Correctable Error Status	033Ch
FC8h	Correctable Error Mask	0340h
FCCh	Advanced Error Capabilities and Control	0344h, 03B4h (refer to Note)
FD0h	Header Log_0	0348h
FD4h	Header Log_1	034Ch
FD8h	Header Log_2	0350h
FDCh	Header Log_3	0354h
FE0h	Secondary Uncorrectable Error Status	0358h
FE4h	Secondary Uncorrectable Error Mask	035Ch
FE8h	Secondary Uncorrectable Error Severity	0360h
FECh	Secondary Uncorrectable Error Pointer ***(no serial EEPROM Write)***	0364h
FF0h	Secondary Header Log ***(no serial EEPROM Write)***	0368h
FF4h		036Ch
FF8h		0370h
FFCh		0374h
NA	Location of Serial EEPROM Check Sum	03ECh

Note: *Multiple Writes to the register are required to trigger the state machine, indicating that the serial EEPROM is downloaded and to proceed to the next step in the sequence of events.*

Appendix B Sample C Code Implementation of CRC Generator

```
const unsigned long LCRCpoly = 0xDB710641;
////////////////////////////////////////////////////////////////
// Function name           : fCalcLCRC
// Description             :
// Return type             : unsigned long
//
// Argument                : unsigned long lfsr
// Argument                : unsigned long plain
//
unsigned long fCalcLCRC( unsigned long lfsr, unsigned long plain )
{
 int j;
 for( j=0; j<32; ++j ) lfsr = (lfsr << 1) ^ ( ((lfsr ^ (plain << j))
& (1<<31)) ? LCRCpoly : 0 );
 return lfsr;
}
////////////////////////////////////////////////////////////////
// Function name           : CalculateCRC
// Description             :
// Return type             : unsigned int
//
// Argument                : DWORD *eeprom
// Argument                : int eepromsize
//
unsigned long CalculateCRC(unsigned long *eeprom, int eepromsize)
{
 unsigned long    crcvalue;
 int ii;
crcvalue = CRCSEED;
 for (ii = 0; ii < eepromsize-1; ii++)
 {
 crcvalue = fCalcLCRC(crcvalue, eeprom[ii]);
 }
#ifdef DUMP_TRACE
 dbg_printf("CRC Value>\t%x.\n",crcvalue);
#endif
 eeprom[eepromsize-1] = crcvalue;
 return(crcvalue);
}
```

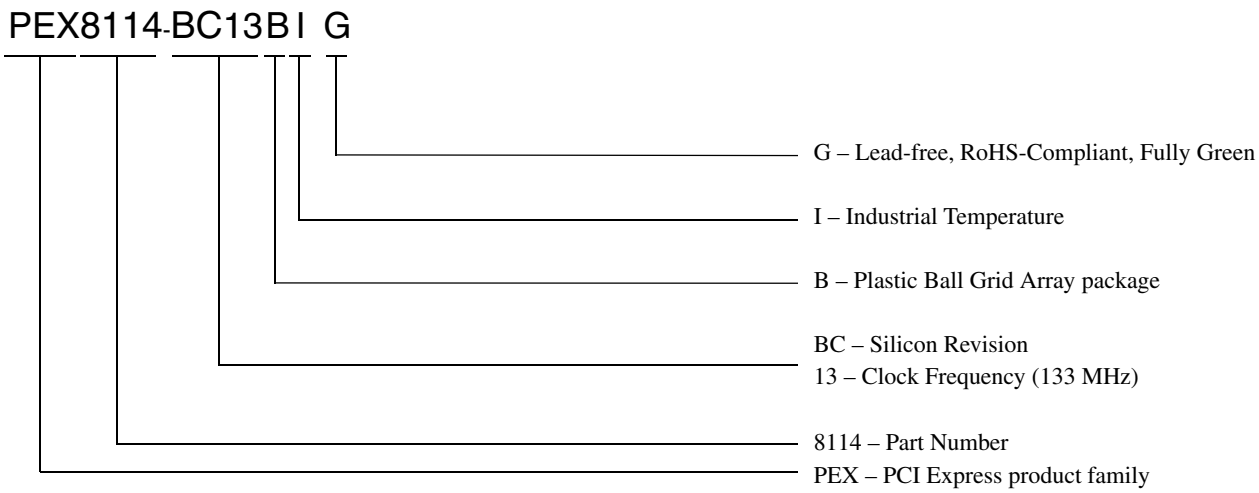
```
//////////////////////////////////////////////////////////////
// Function name           : CheckCRC
// Description             :
// Return type             : unsigned int
//
// Argument                : DWORD *eeprom
// Argument                : int eepromsize
//
unsigned long CheckCRC(unsigned long *eeprom, int eepromsize)
{
 unsigned long    crcvalue;
 int ii;
 crcvalue = CRCSEED;
 for (ii = 0; ii < eepromsize-1; ii++)
 {
 crcvalue = fCalcLCRC(crcvalue, eeprom[ii]);
 }
#ifdef DUMP_TRACE
 dbg_printf("CRC Value>\t%x.\n",crcvalue);
#endif
 if(eeprom[eepromsize-1] == crcvalue)
 return (crcvalue);
 else
 return (0);
}
```

Appendix C General Information

C.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table C-1. Product Ordering Information

Part Number	Description
PEX8114-BC13BI	PEX 8114 PCI Express-to-PCI/PCI-X Bridge Plastic BGA Package (17-mm square, 256-ball)
PEX8114-BC13BI G	PEX 8114 PCI Express-to-PCI/PCI-X Bridge Plastic BGA Package (17-mm square, 256-ball), Lead-Free RoHS Green package
	
PEX 8114RDK-F	PEX 8114 Forward Bridge Rapid Development Kit
PEX 8114RDK-R	PEX 8114 Reverse Bridge Rapid Development Kit

C.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

C.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support/, or call 800 759-3735 (domestic only) or 408 774-9060.