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F100K ECL Dual Rail Translators

INTRODUCTION

The complex electronic systems being designed today often require mixed technologies to incorporate the most efficient balance of performance, speed, power, and cost. In order for one technology to communicate with the other, an interface is needed. One of the most common mix of technologies seen today is high speed ECL with the slower, but very popular TTL and CMOS. To make this interface as quick and clean as possible, level translators are used. This applications note will discuss ECL to TTL and TTL to ECL level translators available from Fairchild Semiconductor's F100K ECL 300 Series product line. Focus will be on Dual Rail Translators (translators which require both ECL and TTL power supplies for normal operation), their differentiating features and possible uses.

TRANSLATOR SELECTION

Fairchild Semiconductor offers translators of all different types. Table 1 shows the TTL to ECL and ECL to TTL translators that are presently available. The first 300 Series translators designed were the 100324 and 100325. With these devices, unidirectional translation is possible in either direction (TTL to ECL with the 100324, ECL to TTL with the 100325). As systems and data widths become larger, more bits need to be translated. This need was satisfied with the introduction of 8- and 9-bit translators. The 8-bit translator (100329) also offer bidirectional translation functionality for applications which require two way communication. In many cases, communication over significant distances is needed in noisy environments. In applications where high output drive is needed after an ECL to TTL translation the 9-bit 100395 can be used. The 64 mA I_{OL} output current capability is ideal for driving long lines and achieving faster switching times by discharging the line it is tied to faster when in the LOW output state. These outputs are also capable of driving higher fanouts than the lower output current devices.

If the designer only has a +5V supply available (i.e., An additional ECL supply cannot be used), single rail translators can be used. For more information on single rail translation refer to applications note AN-780 "Operating ECL From a Single Positive Supply".

TABLE 1. 300 Series Dual Rail Translators

Features	100324	100325	100329	100395
Data Bits	6	6	8	9
ECL to TTL		X	X	X
TTL to ECL	X		X	
Latched				
Registered			X	X
ECL Differential	OUT	IN (Note 1)		
ECL Drive (Ohms)	50		50	
ECL Cutoff			X	
TTL Drive I_{OL}/I_{OH} (mA)		20/–2	24/–3	64/–15
TTL 3-STATE			X	X
ECL Control Pins			X	X
TTL Control Pins	X			
TPD ECL to TTL (ns Max)		4.8	7.7	6.4
TPD TTL to ECL (ns Max)	3.0		3.9	
I_{EE} (mA Max)	–70	–37	–199	–67
I_{CC} (mA Max)	38	65	74	65

Note 1: V_{BB} output available for 100325

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TRANSLATOR OPERATION SPEED ADVANTAGES

Designers who have primarily a TTL system will often use ECL in areas such as clock distribution, backplanes, and differential data transmission where speed is most important. This can be accomplished by level translating from TTL to ECL, performing the desired ECL operation, and then translating back to TTL. As intimidating as this approach sounds, the propagation delay savings gained can be very significant. Consider as an example the TTL "error capture circuit" shown in Figure 1 and the same function performed using ECL shown in Figure 3. In Figure 1, a TTL system with control lines CR0 and CR1 is being monitored for errors. The error capture circuit consists of a buffer, decoder, and six counters. The buffer transfers signals from the control lines to the inputs of the decoder. The decoder determines which type of error is present and then

feeds into a 2 stage counter to keep track of how many times a particular error occurs.

Table 2 gives conditions for all possible levels on the control lines. When a counter reaches a terminal count of 256 for any type of error, a signal is fed to the TTL controller which initiates a service routine for that particular type of error. For the PDIP devices shown in Figure 1, the maximum propagation delay at room temperature for the error capture circuit is approximately 51 ns.

TABLE 2. System Errors

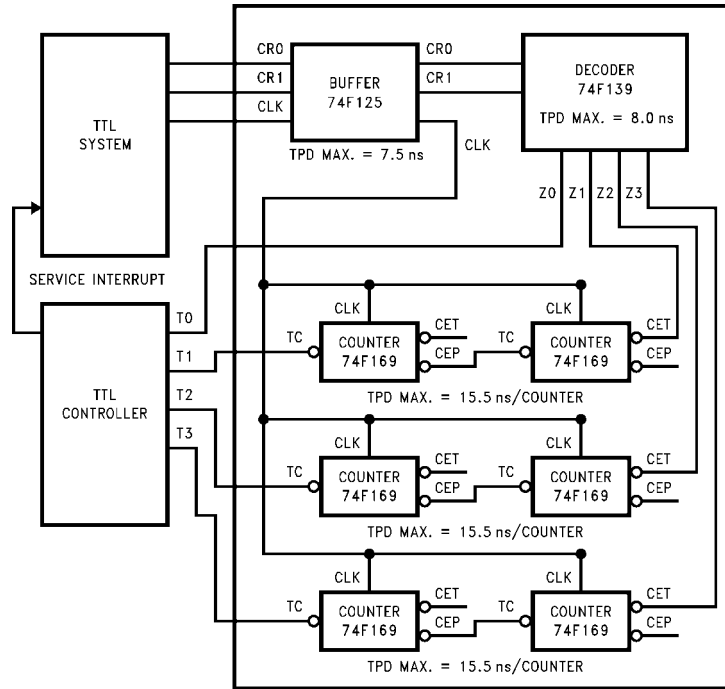| CR0	CR1	Z0	Z1	Z2	Z3	Operation
L	L	L	H	H	H	No Errors
H	L	H	L	H	H	Type 1 Error (T1)
L	H	H	H	L	H	Type 2 Error (T2)
H	H	H	H	H	H	Type 3 Error (T3)

FIGURE 1. TTL Error Capture Circuit

A significant amount of time can be saved by using translators and performing the error capture with ECL. In Figure 3, an ECL error capture solution is implemented. In this case, a 100324 TTL to ECL translator is used to buffer the control line signals and provide the required ECL voltage levels. Data is then fed into the 100370 decoder and inverted for counter input. As in the TTL circuit (see Figure 1), when the count reaches 256 for any type of error, a signal is fed into the controller for service routine activation. The ECL signal is first converted to TTL by use of the 100325 before being transferred to the controller. The error circuit for Figure 3 has a maximum propagation delay (using CDIP package at 25°C) of approximately 20 ns.

A comparison of the ECL and TTL error capture circuits shows that ECL offers a 31 ns advantage in speed over the equivalent TTL design. This is a savings of more than half of the entire TTL timing budget. Another benefit of using ECL in high speed applications is that as frequency increases, TTL power increases while ECL power remains constant. In fact, as system bandwidth requirements exceed 50 MHz, ECL shows a power advantage over TTL. Since the translators in Table 1 have either TTL inputs or outputs, the power will increase slightly with frequency, but not as much as pure TTL devices.

POWER SUPPLY AND NOISE CONSIDERATIONS

The primary consideration with mixed voltage, dual rail translators is to insure maximum noise protection between the TTL and ECL ground. The ECL bandgap circuit (shown in Figure 2) is used to generate internal reference voltages. The internally generated reference voltage used to set the input and output threshold levels is called V_{BB}. The potential generated to control the level of the active current source is called V_{CS}. These reference voltages (V_{BB} and V_{CS}) set up by the bandgap circuitry are referenced to the ECL ground (V_{CC}). Any noise on this ground will be injected into the reference voltages (V_{BB} and V_{CS}) producing reduced noise immunity. This implies that a stable, noise free ECL ground is needed.
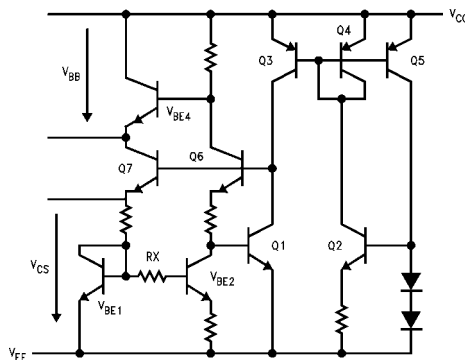
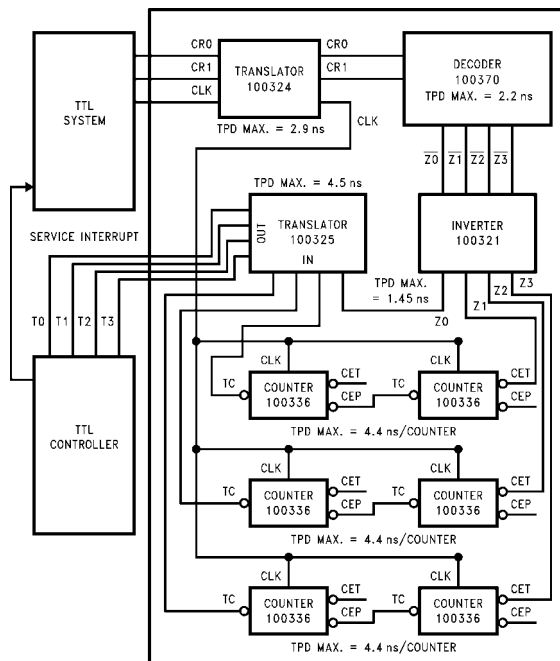**FIGURE 2. ECL Bandgap Circuit**

FIGURE 3. ECL Error Capture Circuit

Ground bounce has been a concern of TTL designers for many years. Figure 4 shows the TTL totem pole output structure. The intrinsic inductance in the ground lead (TTL GND) and power lead (V_{TTL}) are labeled as L1 and L2, respectively. In order to switch from HIGH to LOW, current (marked I1 in Figure 4) must flow through Q3 and L2 to discharge the load capacitance. As this current changes, a voltage is developed across the inductor L2 (Recall: V2 = L2 (dI2/dt). Since the inductor (L2) is between system ground and the device ground, there will be a voltage drop between them. This voltage difference between device and system ground will cause the device input and output levels to be offset because they are referenced to the internal device ground. The devices which are driving inputs or being driven by the outputs are referenced to the system ground (TTL GND in Figure 4). This effect is known as ground bounce.

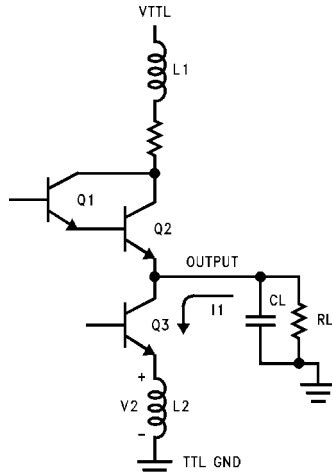# POWER SUPPLY AND NOISE CONSIDERATIONS (Continued)

FIGURE 4. TTL Totem Pole Output

To insure maximum noise protection, it is recommended that the ECL and TTL ground planes on the printed circuit board (PCB) are run independently, and are only connected back at the low impedance source of the power supply. Likewise separate power planes will be used for the TTL positive supply (V_{TTL}), ECL negative supply (V_{EE}), and ECL output load power supply (V_T). This leads to five layers of a multi-layer PCB being dedicated to power planes. Additional layers, either internal or on the surface, can be used to run signal lines. Figure shows a typical layout for a seven layer TTL/ECL PCB. Signals are run on both sides of the board.

LAYER 1	Signal
LAYER 2	TTL Ground
LAYER 3	TTL +5V (V_{TTL})
LAYER 4	VT
LAYER 5	ECL −4.5V (V_{EE})
LAYER 6	ECL 0.0V (V_{CC})
LAYER 7	Signal

FIGURE 5. PC Board Power Planes

Consideration should be made with regard to the power up sequencing of translators. Table 3 describes the conditions observed for the various translators when ECL or TTL power is lost.

Control pins should be driven by power up referenced signals, so that during power up sequencing, the Output Enable pins are driven to the disable state.

DESIGN CONSIDERATIONS

Translator Pin Connections

Dual rail translation implies that both positive (V_{TTL}) and negative (V_{EE}) voltage supplies must be used. These voltages are typically +5V and −5V respectively. V_{CC} and V_{CCA} pins are used for the ground connection to 0V. The F100K 300 Series translators offer a 28-pin Plastic Leadless Chip Carrier (PLCC) package for surface mount capability to reduce board space. This package includes three V_{EES} pins which are used to dissipate heat from the package. These pins are connected internally through the substrate to V_{EE}. It is recommended that these pins be connected to the V_{EE} power plane and *NEVER* to V_{CC}, V_{CCA}, or V_{TTL}.

Translator Location

When using ECL with TTL or CMOS, it is important to group CMOS and TTL devices away from the ECL devices. This will reduce the possibility of corruption of ECL signals caused by noisy TTL or CMOS switching. Translators with TTL outputs should be grouped with the TTL devices on the printed circuit board (PCB), and translators with ECL outputs should be grouped with the ECL devices.

**TABLE 3. Output State Under Power Loss**

Product	Loss of V_{TTL}		Loss of V_{EE}	
	ECL Output State	TTL Output State	ECL Output State	TTL Output State
100324	V_{OH}	N/A	V_{OH}	N/A
100325	N/A	HI-Z	N/A	HI-Z
100329	V_{OH}	HI-Z	V_{OH}	HI-Z
100395	N/A	HI-Z	N/A	HI-Z

APPLICATIONS

Some of the many uses for ECL/TTL translators are:

High Speed Cache Memory: Figure 6 shows a two way set associative cache system. Data is transferred from the ECL memory to cache with the use of a single 8-bit 100328 bidirectional translator. Once the data reaches the cache, it can be moved to the microprocessor quickly for manipulation. Since the data bus is a two way communication system, a bidirectional translator is needed. The address bus, on the other hand, requires only a one way communication.

This implies a unidirectional translator could be used to interface the address to ECL memory. It would take three hex 100324 devices for the 16-bit line shown in Figure 6, but to reduce package count two 8-bit 100329 devices are used. The ECL memory based system allows reading and writing access within one clock cycle. Since the memory is accessed quickly, the wait states produced by memory read and write are virtually eliminated which results in a faster operating system.
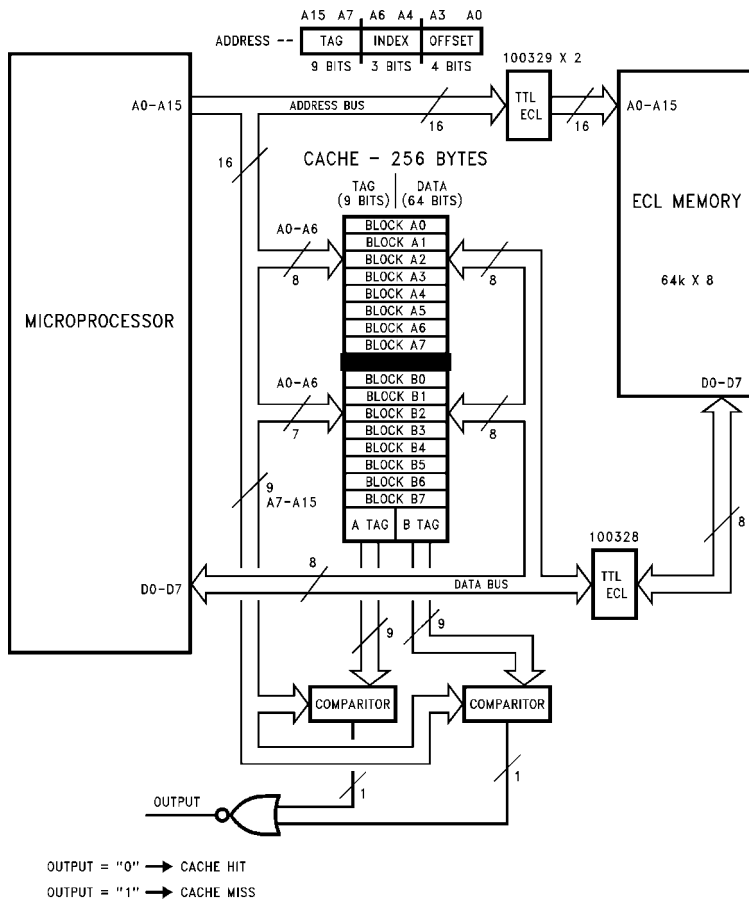

Memory Division

1 block = 16 bytes

1 set = 2 blocks

8 sets in cache

FIGURE 6. Two Way Set Associative Cache System

Peripheral Interface Applications: The 100395 9-bit translator is ideal for translation applications where an 8-bit data bus with parity is used. An example of this situation is shown in Figure 7. In this case, ECL data and parity is transferred through an ECL controller and sent to the ECL-to-TTL translator. Data and parity is then converted to TTL levels and sent through a cable to the peripheral unit (such as a printer) for parity checking and data transfer. The 9-bit

ECL-to-TTL translator (100395) allows for an 8-bit data transfer and 1 bit for parity. The 9-bit function of the 100395 also enables the translation to be performed with one chip which reduces chip count and board space. These translators also have a 64 mA output drive which is needed to drive the long length of cable associated with the printer hook up.

APPLICATIONS (Continued)
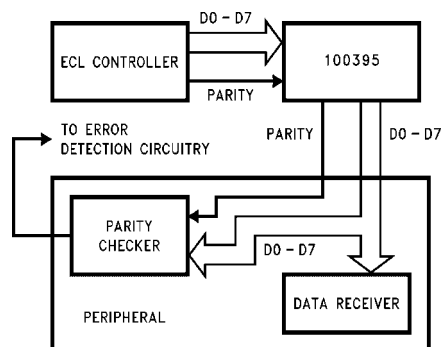
FIGURE 7. Peripheral Interface Application

TTL/CMOS Dynamic Random Access Memories (DRAMs): In instances where high speed ECL CPUs are used, low power/low cost DRAMs can be addressed as bulk storage for non-speed critical operations by interfacing the ECL CPU with DRAM via the 100329. This enables you to perform all of your high speed data processing tasks in ECL and use more readily available TTL/CMOS DRAMs for data storage.

High Speed Coprocessor: A high speed ECL coprocessor can be added to a lower speed processor for enhancement of high density computations. This will increase the speed and improve the overall system performance. The 100324 and 100325 would allow differential communication to the ECL coprocessor and the differential ECL signals give noise immunity from the surrounding TTL system.

ECL Bussing: All the translators give TTL systems the ability to use high speed and low EMI ECL backplanes. ECL backplane applications typically use mixed technologies off the backplane which means that quick and reliable translation is needed. Refer to the "ECL Backplane Design", applications note for additional information.

Graphics: The 100324/100329 give TTL to ECL conversion for use in high speed ECL graphics applications. The graphics will be in parallel form in the TTL state, converted to ECL then turned into serial form by either the 100341/100336 shift registers, before being fed to a high speed graphics driver.

REFERENCES

D. Bush, "ECL Backplane Design", April 1991 Applications Note AN-768.

J. Davis, "Operating ECL From a Single Positive Supply", June 1991 Applications Note AN-780

W. Blood, "MECL® System Design Handbook", Fourth Edition, 1988. Copyright Motorola, Inc.

"F100K ECL Logic Databook and Design Guide", 1990 Edition.