MAS6283

IC FOR 1.5625 MHz – 40.0000 MHz VCXO

- **Low Power**
- **Wide Supply Range**
- **CMOS (Square Wave) Output**
- **Very Low Phase Noise**
- **Low Cost**
- **Divider Function**
- **Tri State output**

DESCRIPTION

MAS6283 is an integrated circuit well suited to build a VCXO for telecommunication and other applications. To build a VCXO only one additional component, a crystal, is needed.

FEATURES

- Very small size
- Low current consumption
- Wide operating temperature range
- Phase noise < -130 dBc/Hz at 1 kHz offset
- CMOS (Square wave) output

APPLICATIONS

- VCXO modules
- VCXO for telecommunications systems
- VCXO for set-top boxes
- VCXO for MPEG decoder

BLOCK DIAGRAM

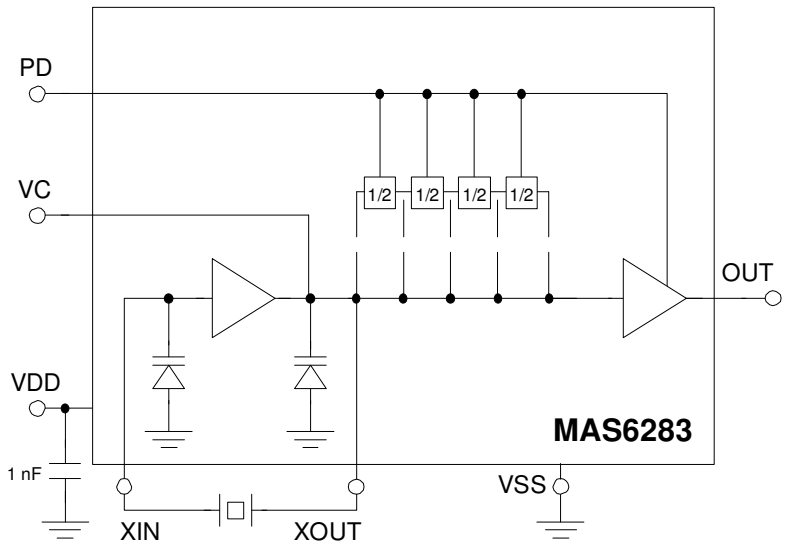


Figure 1. Block diagram of MAS6283.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit	Note
Supply Voltage	V_{DD} - V_{SS}		-0.3	6.0	V	
Input Pin Voltage			V_{SS} -0.3	V_{DD} + 0.3	V	
Power Dissipation (max)	P_{MAX}			100	mW	
Storage Temperature	T_{ST}		-55	150	°C	
Latchup Current Limit	I_{LUT}		±100		mA	1)

Note: Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

Note 1: Not valid for pins XIN and XOUT.

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.5	3.3	5.5	V	1)
Operating Temperature	T_{OP}		-40		+85	°C	
Crystal R_S	R_S			30	60	Ω	2)

Note 1: It is recommended to connect a 1 nF SMD capacitor between the VDD and VSS pins. Assure that capacitor resonance frequency is high enough to filter 3rd harmonic.
Note 2: See figure 5 for negative resistance at different frequencies.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Crystal Frequency Range	f_c		25		40	MHz	1)
Output Frequency Range	f_o		25		40	MHz	2)
Output Frequency Range	f_o		1.5625		20	MHz	3)
Voltage Control Range	V_C		0		V_{DD}	V	
Voltage Control impedance	Z_{VC}			1.2		MΩ	
Supply Current V_{DD} = 3.3V, f_c = 35 MHz	I_{DD}	No Load C_{LOUT} = 10 pF C_{LOUT} = 30 pF C_{LOUT} = 50 pF			2.0 9.3 23.8 38.3	mA	
Supply Current V_{DD} = 5.0V, f_c = 35 MHz	I_{DD}	No Load C_{LOUT} = 10 pF C_{LOUT} = 30 pF C_{LOUT} = 50 pF			3.0 14.0 36.0 58.0	mA	
Supply Current XPD = 0 V	I_{XPD}	V_{DD} = 3.3 V V_{DD} = 5.0 V		0.9 0.9	1.5 1.7	mA	
Output Symmetry			45	48-52	55	%	
Startup Time	T_{START}			2		ms	
Output Buffer Enabled Disabled	XPD		 1.6 0		 V_{DD} 0.55	V	4)
Crystal Load Capacitance	C_L	V_C = 1.65 V		8		pF	5)
Pulling Range 0.0V < V_C < 5.0V		Crystal S= 30 ppm/pF		 285		ppm	6)

Note 1: Crystal frequency can be divided by 2, 4, 8 and 16.
Note 2: Direct output.
Note 3: Depending on chosen output divider.
Note 4: If the XPD pin is floating the output buffer is active. Oscillator is always running. At power down mode the output is at high impedance.
Note 5: Crystal load capacitance is dependent on a V_C voltage. See figure 4 for C_L for other V_C voltages.
Note 6: For calculating crystal pulling (S), see equation 1 on the page 5.

PIN DESCRIPTION

Pin Description	Symbol	x-coordinate	y-coordinate
Crystal Oscillator Output	XOUT	214	141
Voltage Control Input	VC	885	142
Power Supply Ground	VSS	1080	141
Buffer Output	OUT	1106	699
Power Supply Voltage	VDD	579	698
Output Buffer Power Down Control	XPD	339	698
Crystal/Varactor Oscillator Input	XIN	153	698

Note: Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.
Note: Pad coordinates are measured from the left bottom corner of the chip to the center of the pads. The coordinates may vary depending on sawing width and location. However, the distances between pads are accurate.

IC OUTLINES

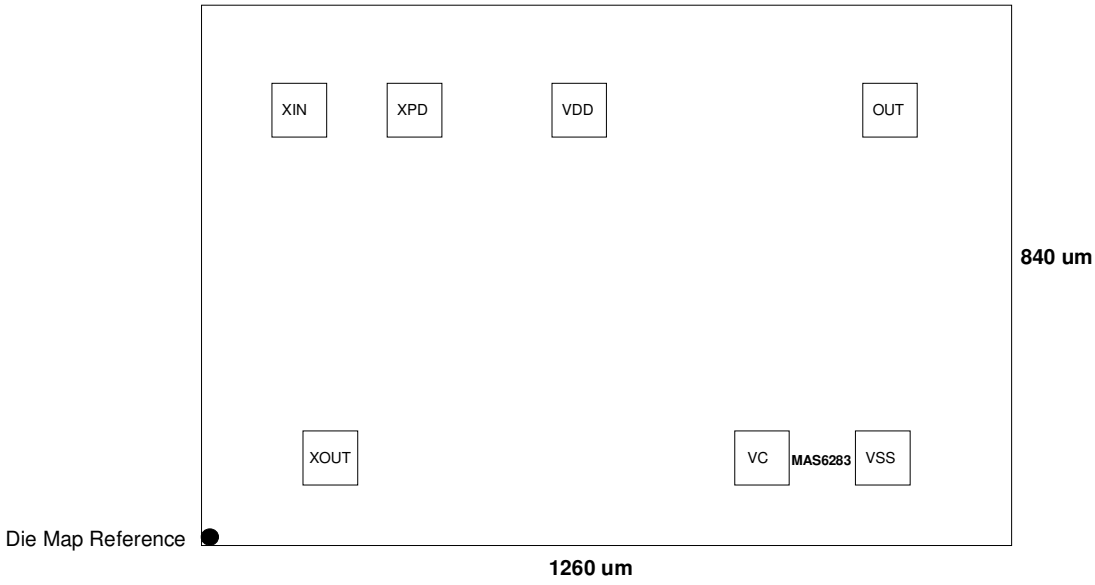


Figure 2. IC outline of MAS6283.

Note1: Die map reference is the actual left bottom corner of the sawn chip.
Note2: See coordinates in pin description.
Note3: Die dimensions include 80 µm scribes for both sides. The actual dimensions are a bit less due to the saw width.

EXTERNAL COMPONENT SELECTION

Quartz Crystal and VCXO Module Information

To ensure the best system performance, the crystal parameters should be considered carefully. Pulling is an important parameter which can be calculated according to an equation 1. Layout guidelines in the following section should be followed. The frequency of the crystal is tuned by load capacitors. There are integrated variable load capacitors on the MAS6283 and they are controlled by an external voltage at the VC pin. It is recommended to connect a 1 nF capacitor between VDD and VSS. The external crystal should be located as close to the chip as possible. In case of a PCB mounted module, it is usually advisable to mount a crystal on the same side with the VCXO IC to minimize stray capacitance. Often vias between the crystal pins and the XIN and XOUT pins of the VCXO IC increase stray capacitance. There should be no noisy signal traces underneath or close to the crystal.

Equation 1

Crystal Pulling Sensitivity $S = -\frac{C_1}{\frac{2(C_0 + C_L)^2}{10^6}} \frac{ppm}{pF}$ [values are given in the units described below]

Where,

C_L = Load capacitance in series with the crystal
C_0 = Shunt capacitance of the crystal
C_1 = Motional capacitance of the crystal

Example 1

If we choose a crystal with the following values

C_L = 8.0 pF,
C_0 = 2.0 pF,
C_1 = 6.7 fF

the equation 1 yields $S = \frac{-6.7 \times 10^{-15}}{\frac{2\left(2.0 \times 10^{-12} + 8.0 \times 10^{-12}\right)^2}{10^6}} = -33.5 \frac{ppm}{pF}$

If a crystal load differs from 8 pF the oscillator will have frequency offset at V_C = 1.65 V. Thus if you need to use 1.65 V VC voltage with a crystal which C_L is other than 8 pF you have to design the crystal for a specific nominal frequency. The following guidelines show how to define the crystal's nominal frequency.

Separate crystal C_L as C_{L_XTAL} and MAS IC C_L as C_{L_IC}.

To define specific nominal frequency for the crystal first calculate load difference ΔC_L [pF] as in an equation 2.

Equation 2

$$\Delta C_L = C_{L\_IC} - C_{L\_XTAL}$$

Calculate frequency difference Δf [ppm] as in an equation 3. Pulling S comes from the equation 1.

Equation 3

$$\Delta f = \Delta C_L \times S$$

The crystal nominal frequency f_{NOM_XTAL} is calculated, as shown in an equation 4.

Equation 4

$$f_{NOM\_XTAL} = f_{NOM} \times \left(1 + \frac{\Delta f}{10^6}\right)$$

Where,

f_{NOM} = Desired nominal frequency of the VCXO module
f_{NOM_XTAL} = Crystal nominal frequency (without MAS IC load capacitance)

Crystal nominal frequency optimization is calculated in an example 2.

Example 2

VCXO module target frequency f_{NOM} is 35 MHz. Crystal characteristics are crystal load C_{L_XTAL} = 12.5 pF and pulling S = 30 ppm/pF.

MAS6283 C_{L_IC} = 8 pF when V_C = 1.65 V.

Calculate load difference ΔC_L according to the equation 2.

$$\Delta C_L = C_{L\_IC} - C_{L\_XTAL} = 8\,pF - 12.5\,pF = -4.5\,pF$$

Calculate frequency difference Δf according to the equation 3.

$$\Delta f = \Delta C_L \times S = -4.5\,pF \times 30\frac{ppm}{pF} = -135\,ppm$$

Now f_{NOM} = 35 MHz.

According to the equation 4

$$f_{NOM\_XTAL} = f_{NOM} \times \left(1 + \frac{\Delta f}{10^6}\right) = 35 \times 10^6 \times \left(1 + \frac{-135}{10^6}\right) = 34995275\,Hz$$

The specified crystal has to have a nominal frequency of 34.995275 MHz without load capacitance. This offset is compensated with 8 pF load capacitance though a crystal C_L = 12.5 pF.

VOLTAGE CONTROL (V_C)

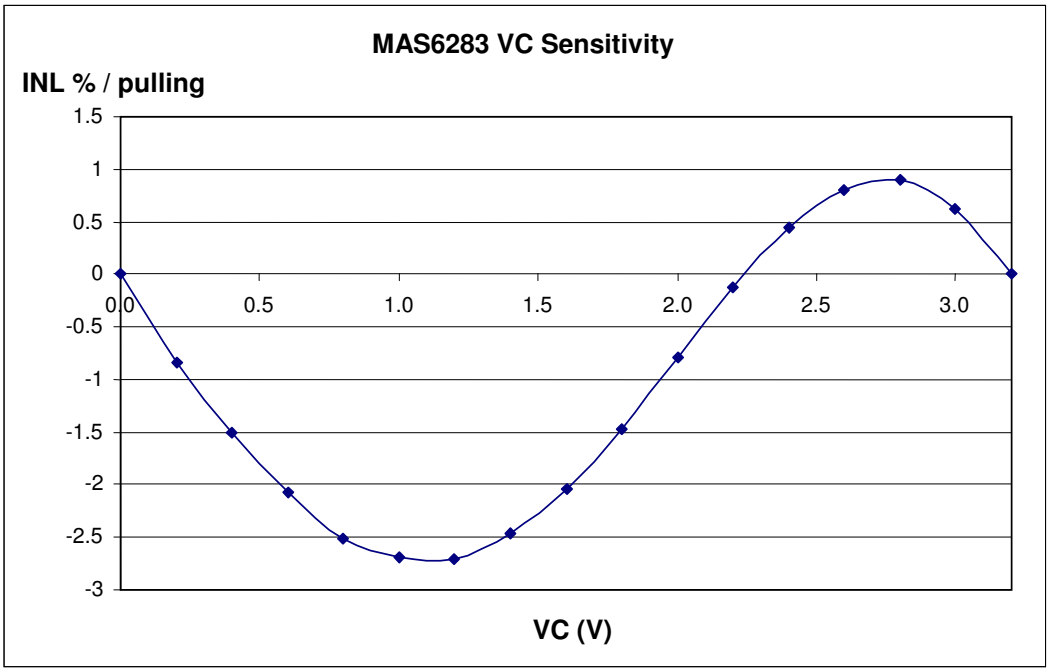


Figure 3. MAS6283AA V_C sensitivity measured as INL % / pulling vs V_C (V).

MAS6283 Voltage control sensitivity graph in figure 3 is measured by using 40.0 MHz crystal (C_L = 8.5 pF, C_1 = 4.9 fF, C_L = 1.5 pF). For crystal pulling see equation 1 in a page 5.

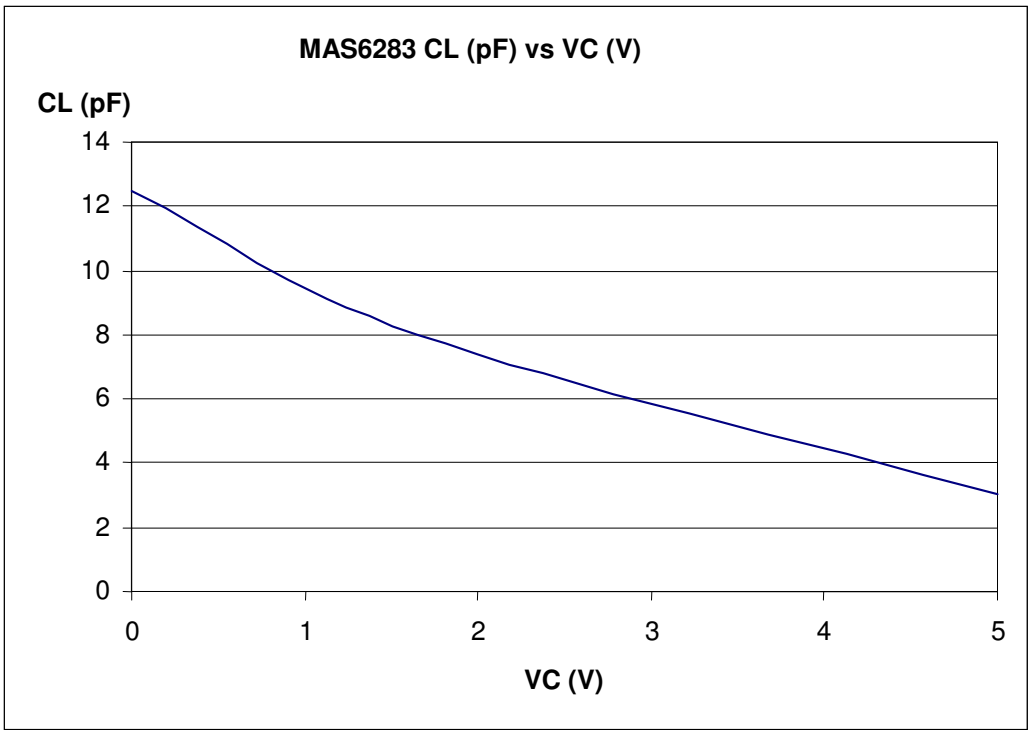


Figure 4. MAS6283 C_L vs V_C voltage

Figure 4 shows MAS6283 C_L over the different V_C voltages.

Negative Resistance

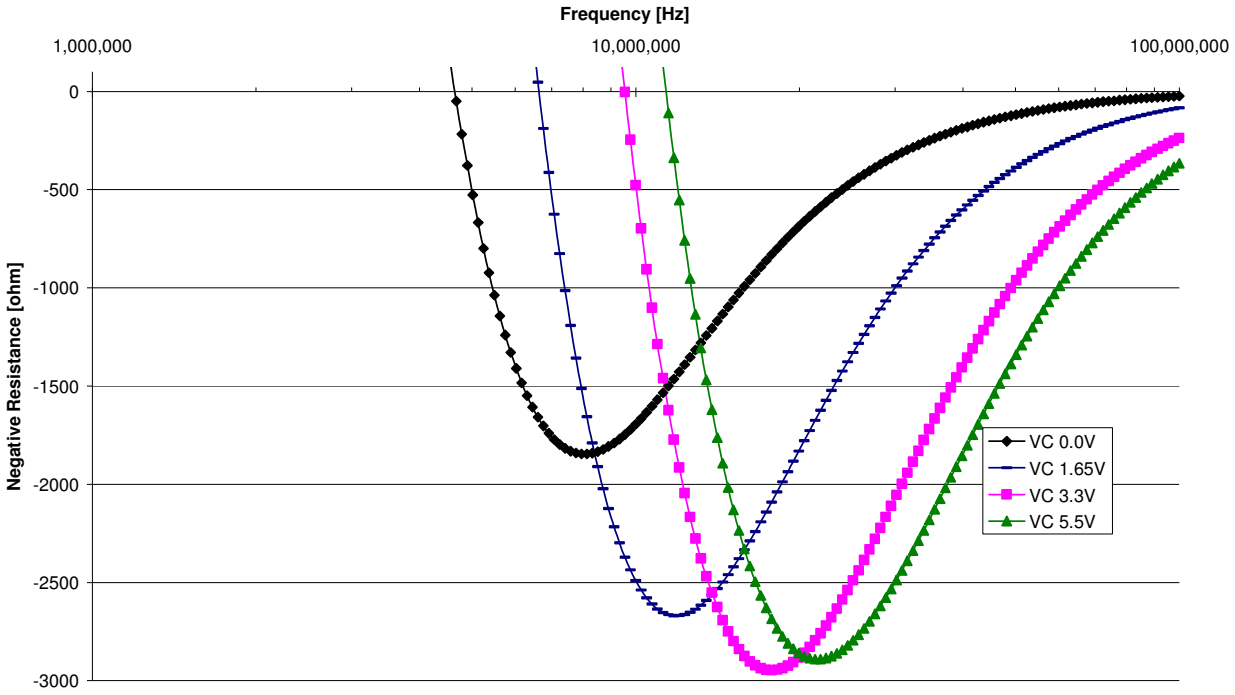
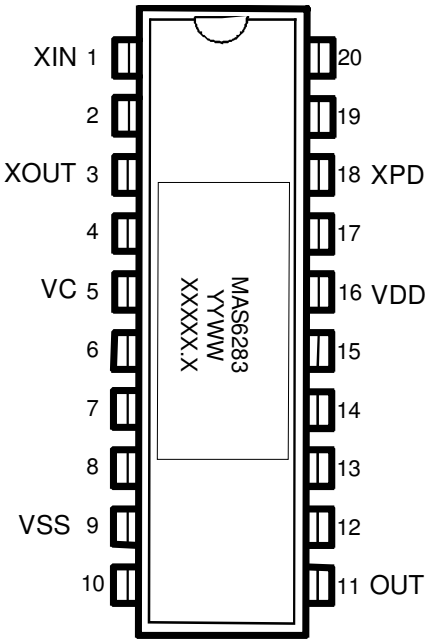


Figure 5. MAS6283 negative resistance.

Figure 5 shows MAS6283 negative resistance vs frequency with different VC voltage values measured at a room temperature. Negative resistance should be at least three times crystal R_S to ensure a reliable oscillation.

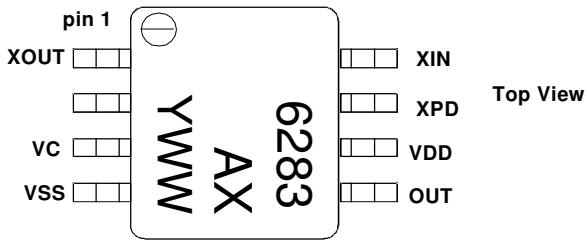
SAMPLES IN SB20 DIL PACKAGE



Top marking:
YYWW = Year, Week
XXXXX.X = Lot number

Figure 8. MAS6283 SB20 DIL package.

DEVICE OUTLINE CONFIGURATION

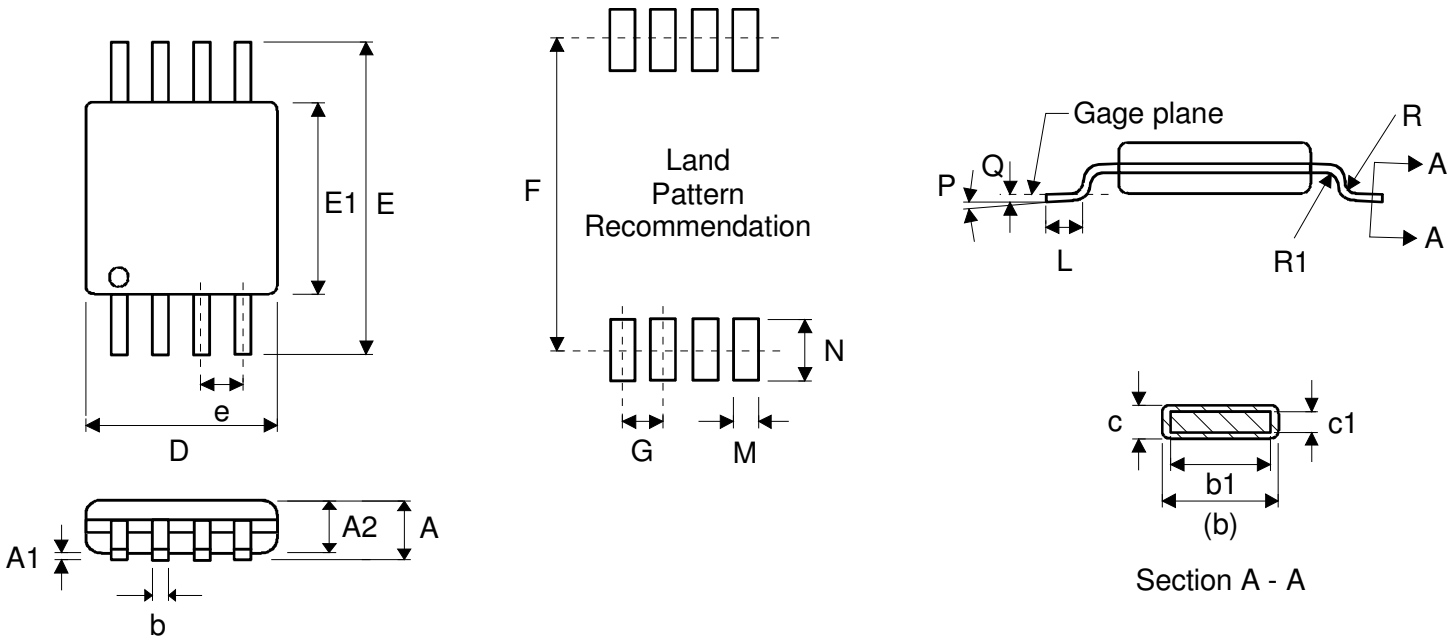


A = product version
X = MAS internal code
Y = year
WW= week

MSOP8

Figure 9. MAS6283 MSOP-8 package.

PACKAGE (MSOP-8) OUTLINE



Symbol	Min	Nom	Max	Unit
A			1.10	mm
A1	0		0.15	mm
A2	0.75	0.85	0.95	mm
b	0.22		0.38	mm
b1	0.22	0.30	0.33	mm
c	0.08		0.23	mm
c1	0.08		0.18	mm
D		3.00 BSC		mm
E		4.90 BSC		mm
E1		3.00 BSC		mm
e		0.65 BSC		mm
F		4.8		mm
G		0.65		mm
L (Terminal length for soldering)	0.40	0.60	0.80	mm
M		0.41		mm
N		1.02		mm
P	0°		8°	
Q		0.25 BSC		mm
R	0.07			mm
R1	0.07			mm

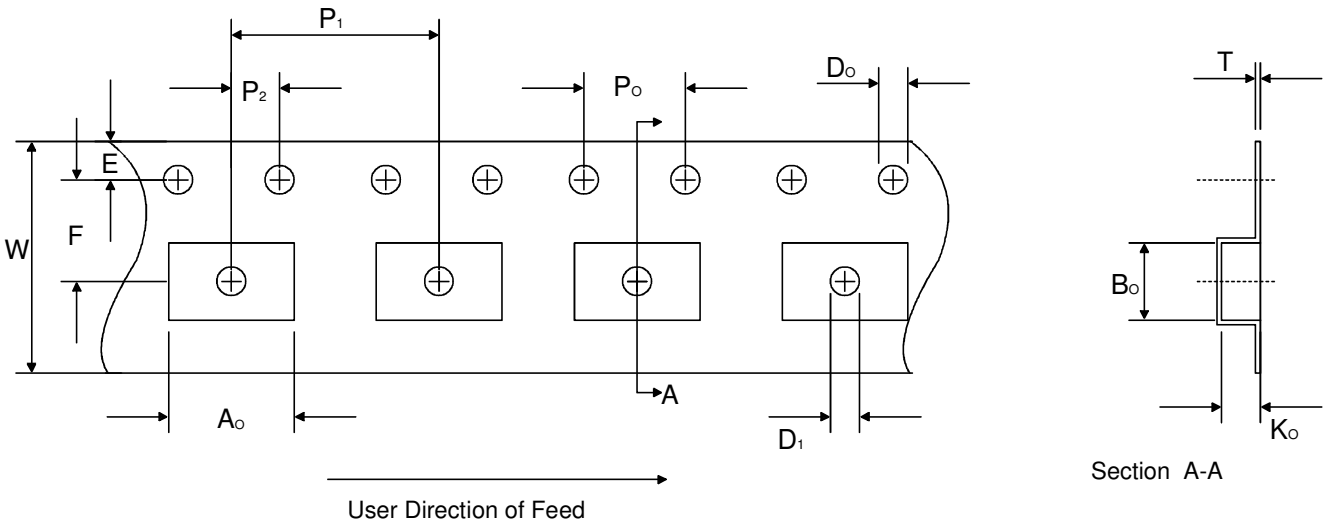
Dimensions do not include mold or interlead flash, protrusions or gate burrs.
All measurement according to JEDEC standard MO-187.

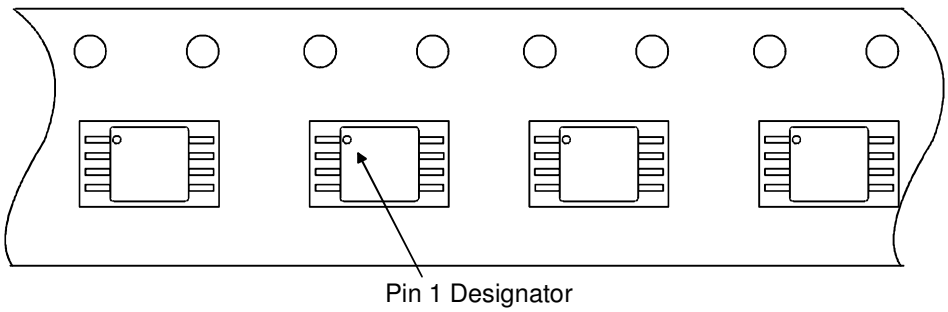
SOLDERING INFORMATION

◆ **For Pb-Free**

Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin
Moisture Sensitivity Level (MSL)	1

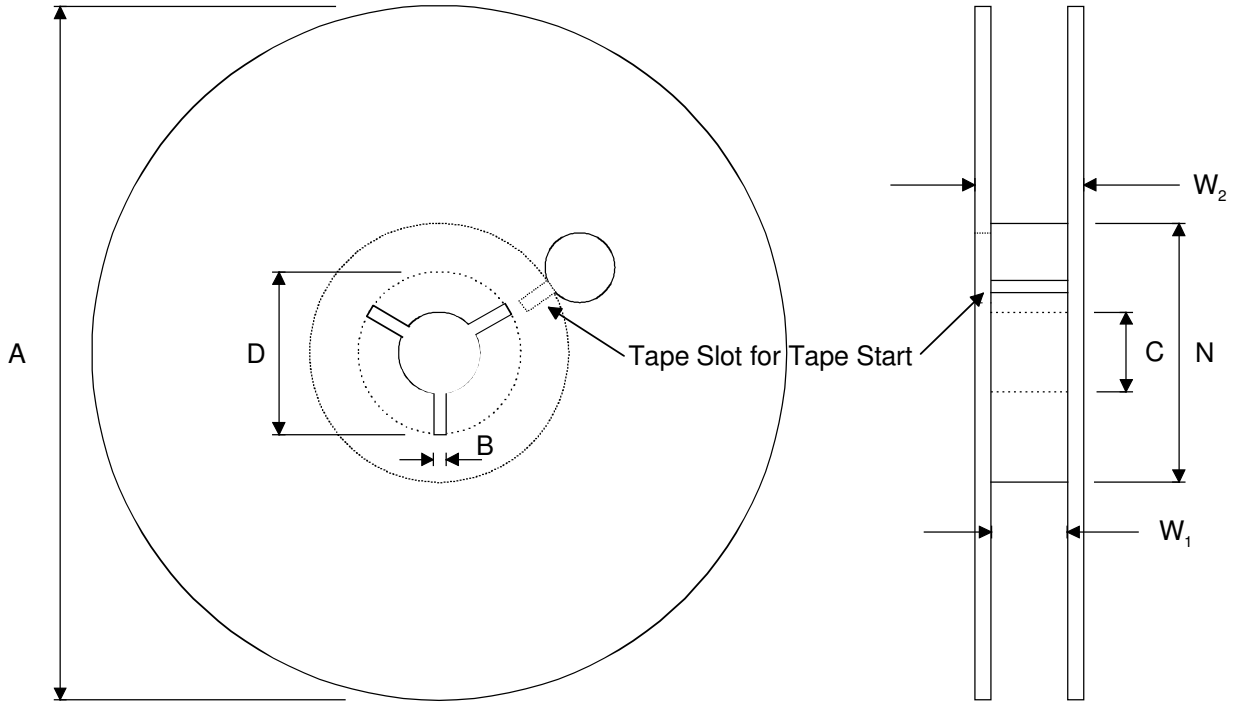
EMBOSSED TAPE SPECIFICATIONS (MSOP-8)





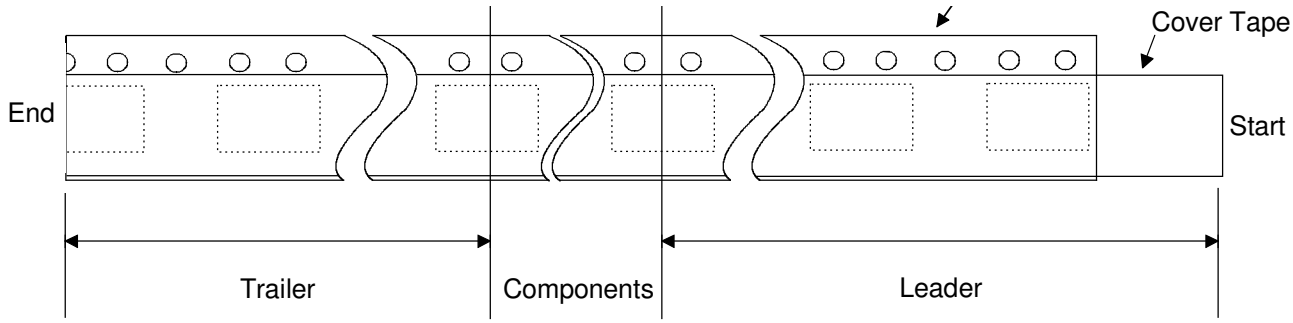
Dimension	Min/Max	Unit
Ao	5.00 ±0.10	mm
Bo	3.20 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
D1	1.50 min	mm
E	1.75	mm
F	5.50 ±0.05	mm
Ko	1.45 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 +0.30/-0.10	mm

REEL SPECIFICATIONS (MSOP-8)



5000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Output Frequency	Package
MAS6283AATG00	f_c	EWS tested wafers 215 µm
MAS6283AASN06	f_c	MSOP-8, T&R 5000 pcs / r, Pb free RoHS
MAS6283ABTG00	f_c / 2	EWS tested wafers 215 µm
MAS6283ACTG00	f_c / 4	EWS tested wafers 215 µm
MAS6283AETG00	f_c / 16	EWS tested wafers 215 µm

Contact Micro Analog Systems Oy for divider options.
Contact Micro Analog Systems Oy for other wafer thickness.

◆ **The formation of product code**

Product name	Design version	Output frequency	Package type	Delivery format
MAS6283	A	A = f_c	TG = 215 µm thick EWS tested wafer	00 = tested wafer
		B = f_c / 2	SN = MSOP Pb free RoHS	06 = tape & reel
		C = f_c / 4		
		E = f_c / 16		

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy Kutomotie 16 FI-00380 Helsinki, FINLAND	Tel. +358 10 835 1100 Fax +358 10 835 1119 http://www.mas-oy.com