

## FDD8453LZ\_F085

### N-Channel Power Trench® MOSFET

40V, 50A, 6.5mΩ

#### Features

- Typ  $r_{DS(on)}$  = 5mΩ at  $V_{GS} = 10V$ ,  $I_D = 15A$
- Typ  $r_{DS(on)}$  = 6mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 13A$
- HBM ESD protection level > 7kv typical
- RoHS Compliant
- Qualified to AEC Q101

#### General Description

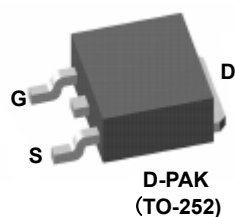
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

#### Applications

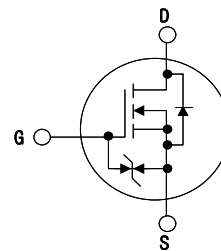
- Inverter
- Synchronous Rectifier



#### Package



#### Symbol



## MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Package limited) $T_C = 25^\circ\text{C}$	50	A
	- Pulsed	Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	88	mJ
$P_D$	Power Dissipation	118	W
	Dereate above $25^\circ\text{C}$	0.79	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	1.27	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in <sup>2</sup> copper pad area	52	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8453LZ	FDD8453LZ_F085	D-PAK(TO-252)	13"	12mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.8	3.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 15\text{A}, V_{GS} = 10\text{V}$	-	5.0	6.5	$\text{m}\Omega$
		$I_D = 13\text{A}, V_{GS} = 4.5\text{V}$	-	6.0	7.8	$\text{m}\Omega$
		$I_D = 15\text{A}, V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$	-	9.4	12.2	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 15\text{A}$	-	91	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	2935	-	pF	
$C_{oss}$	Output Capacitance		-	340	-	pF	
$C_{rss}$	Reverse Transfer Capacitance		-	260	-	pF	
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	1.8	-	$\Omega$	
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	$V_{DD} = 20\text{V}, I_D = 15\text{A}, I_g = 1\text{mA}$	-	60	78	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0$ to 5V		-	32	42	nC
$Q_{gs}$	Gate to Source Gate Charge			-	7.5	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	13	-	nC

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Switching Characteristics**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{on}$	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 15\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	34	ns
$t_{d(on)}$	Turn-On Delay Time		-	12	-	ns
$t_r$	Rise Time		-	10	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	43	-	ns
$t_f$	Fall Time		-	7	-	ns
$t_{off}$	Turn-Off Time		-	-	80	ns

**Drain-Source Diode Characteristics**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 2\text{A}$	-	0.7	1.2	V
		$I_{SD} = 15\text{A}$	-	0.8	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 15\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	25	33	ns
$Q_{rr}$	Reverse Recovery Charge		-	14	19	nC

**Notes:**

1: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11\text{mH}$ ,  $I_{AS} = 40\text{A}$ ,  $V_{DD} = 36\text{V}$  during inductor charging and  $V_{DD} = 0\text{V}$  during the time in Avalanche.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>  
 All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

### Typical Characteristics

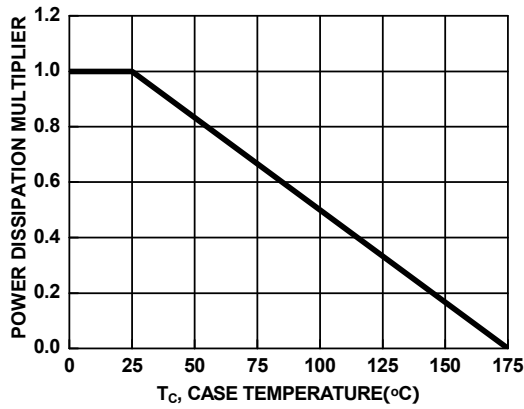


Figure 1. Normalized Power Dissipation vs Case Temperature

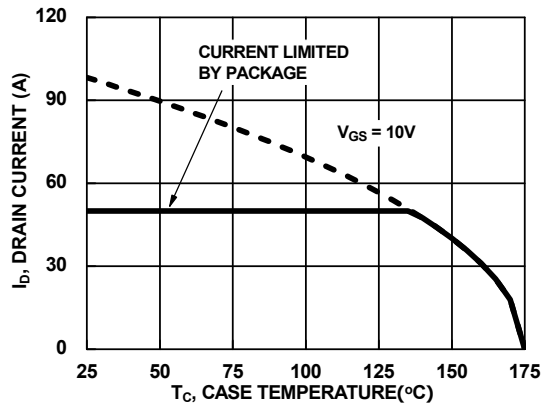


Figure 2. Maximum Continuous Drain Current vs Case Temperature

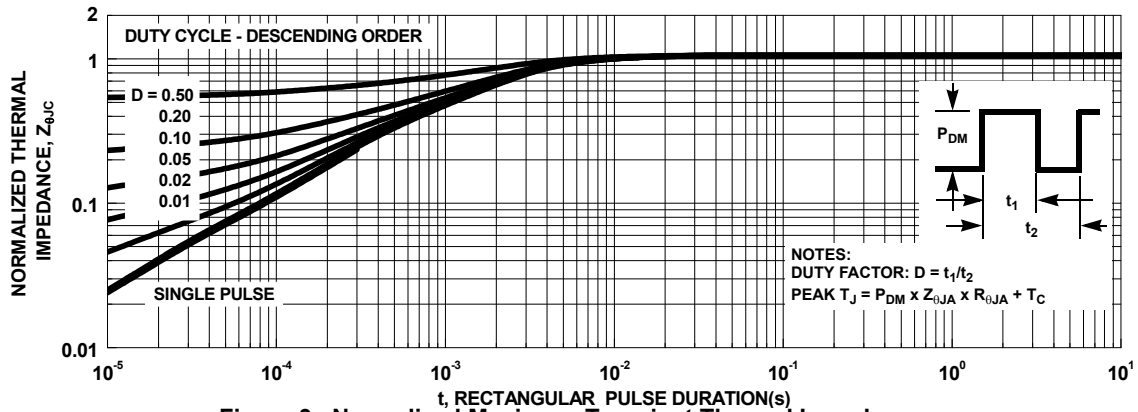


Figure 3. Normalized Maximum Transient Thermal Impedance

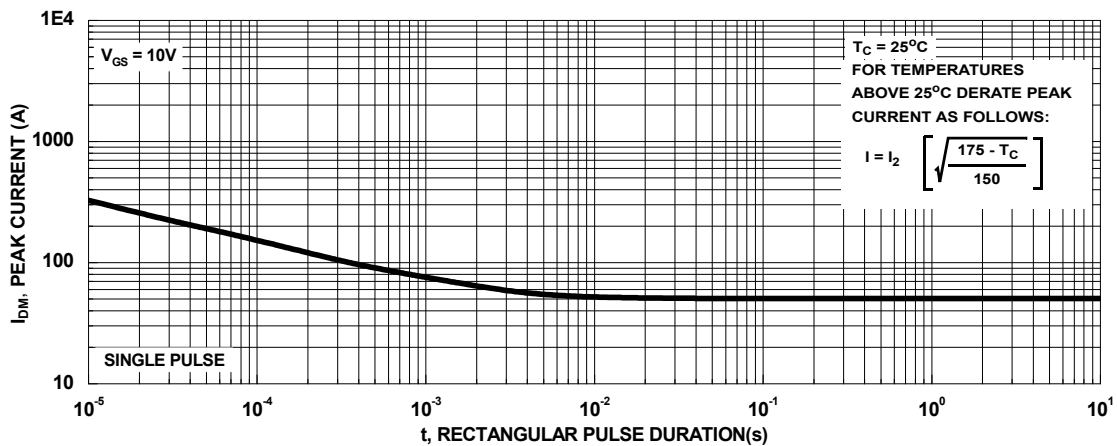


Figure 4. Peak Current Capability

### Typical Characteristics

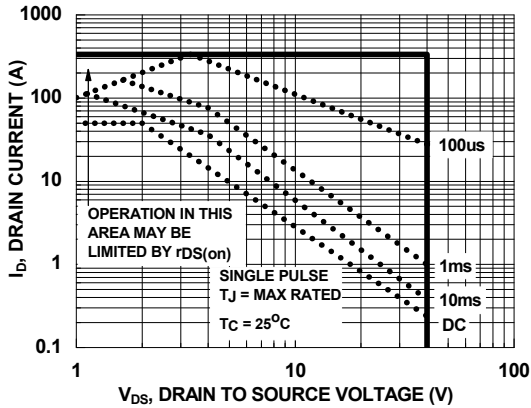
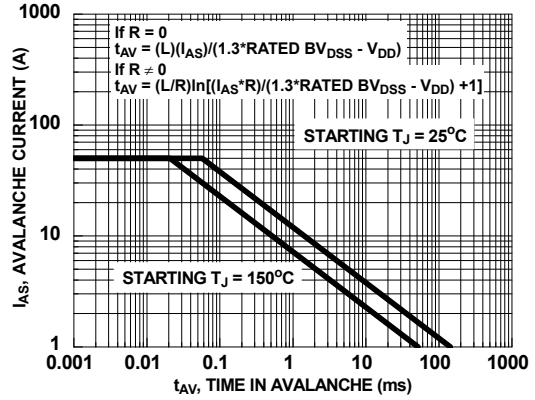


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
 Figure 6. Unclamped Inductive Switching Capability

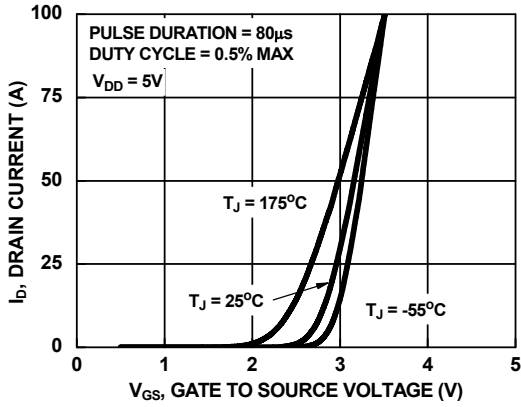


Figure 7. Transfer Characteristics

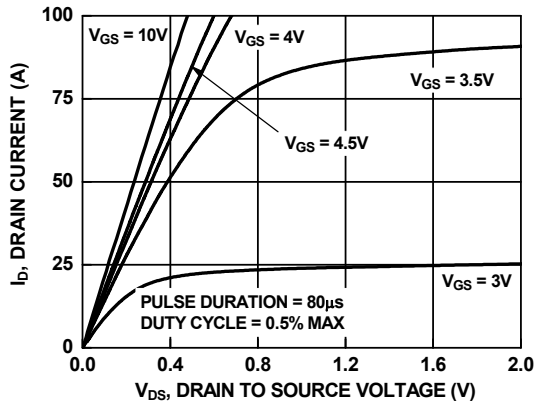


Figure 8. Saturation Characteristics

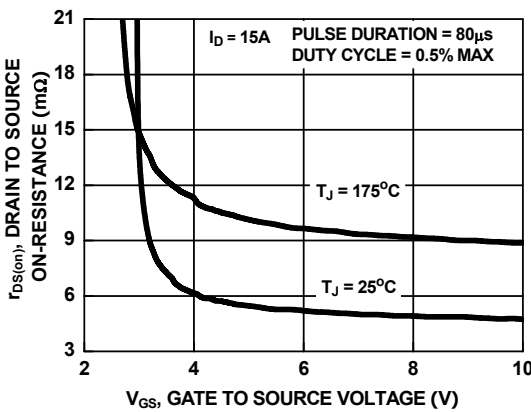


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

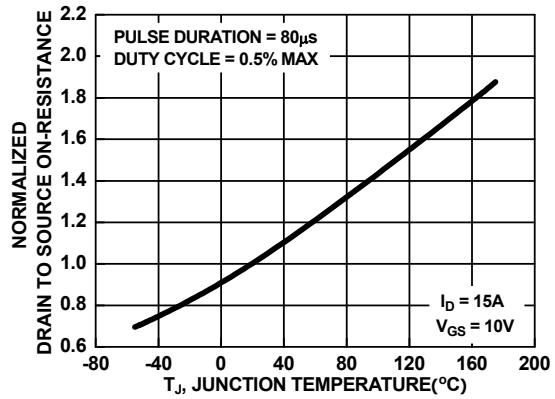


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

## Typical Characteristics

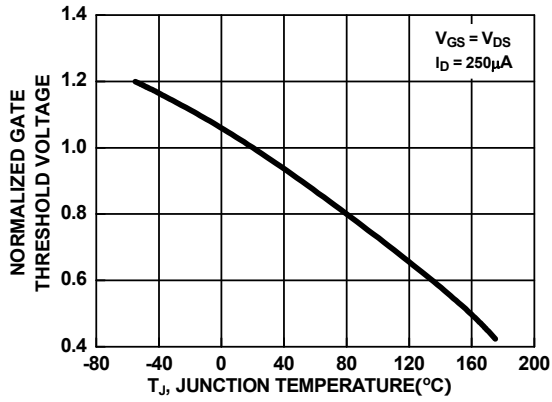


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

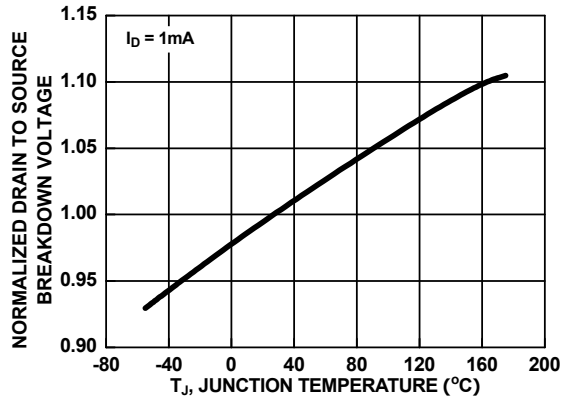


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

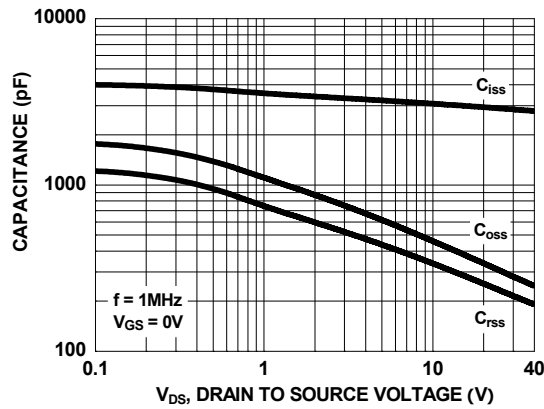


Figure 13. Capacitance vs Drain to Source Voltage

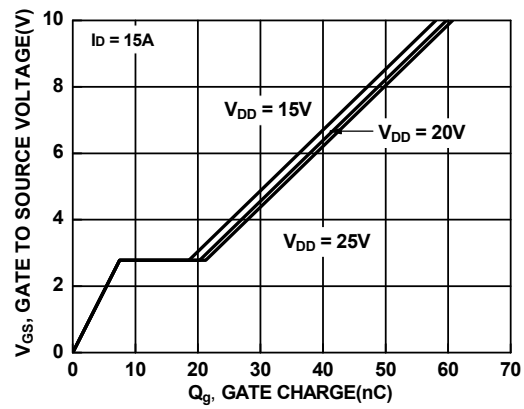






Figure 14. Gate Charge vs Gate to Source Voltage



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| AX-CAP™*  | FRFET®                              | PowerXS™  | <b>power</b>  |
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