UMC

T-52-33-63

# UM83C021

PRELIMINARY

## Hard Disk Controller

### Features

- Serializer-deserializer
- Programmable track format, compatible with WD Track format
- External drive select and head select registers for expandability
- With Hardware ECC capability
- Internal phase detector for phase lock oscillator
- Interface options: ST-506, ST-412, ST-412HP, ESDI, FLOPPY, and QIC-36 TAPE
- Sector options: SOFT, HARD, ESDI ADDRESS MARKS, ESDI BYTE and ESDI BYTE CLOCKS
- Recording options: UNENCODED, FM, MFM or RLL
- Error checking and correcting options: ECC or CRC
- Write data options: PULSE, NRZ or NRZI
- Read data options: PULSE, NRZ or NRZI
- TTL compatible inputs and outputs. Outputs drive 8 LSTTL loads

### General Description

The UM83C021 Hard Disk Controller is a CMOS LSI device which performs a majority of the functions for controlling floppy drives, Winchester drives and QIC-36 streaming tape drives.

#### Interface Options

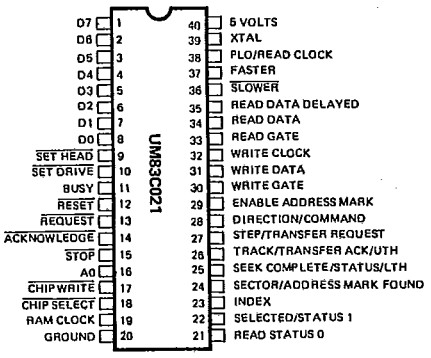
ST-506 (non-buffered seek Winchesters)
ST-412 (buffered seek Winchesters)
ST-412HP (10 mbos buffered seek Winchesters)
ESDI STEP/SERIAL MODES (10 mbos Winchesters)
SA-450 (5" and 3" floppies)
SA800/850 (8" floppies)
QIC-36 (streaming tape drives)

#### Sector Options

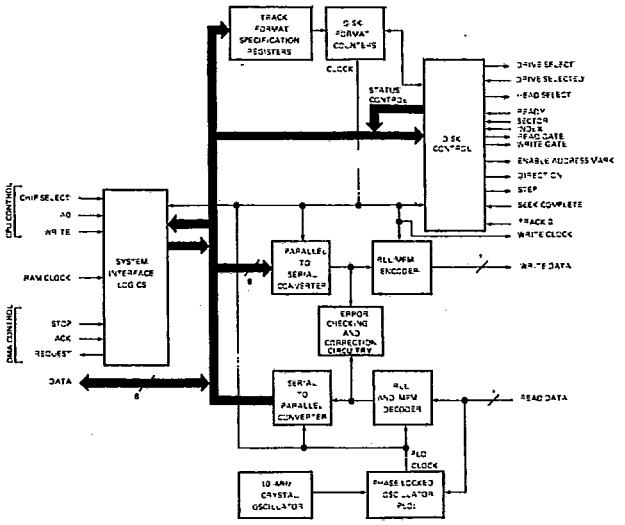
SOFT-SECTORING (floppy and Winchester)
HARD-SECTORING (floppy and Winchester)
ESDI ADDRESS MARKS (ESDI drives)
ESDI BYTE CLOCKS (ESDI drives)

Storage

### Pin Configuration




### Block Diagram



**Recording Codes**

UNENCODED (for ESDI drives)
FM (Frequency Modulation)
MFM (Modified Frequency Modulation)
RLL (Run Length Limited)

**Error Checking**

CRC (CCITT CRC-16)
ECC (4 byte, corrects 11 contiguous erroneous bits)

**Data Options**

NRZ (non-return to zero)
NRZI (non-return to zero inverted)
PULSE

**Track Format**

Extensive control over the track format is provided by allowing the length of fields and content of ADDRESS MARKS and identifier bytes, etc. to be programmed into registers.

There are 23 registers related to TRACK FORMAT inside the UM83C021 (Refer to Figure 1). 18 of these registers contain lengths of fields within a track. Others contain "content" information. Length fields are written with length−1 giving them a range of 1 to 256 inclusive. The Data Field Length Register is 2 bytes yielding a maximum data field length of 65,536 bytes. .

## Absolute Maximum Ratings*

Power Supply Voltage, $V_{DD}$ . . . . . −0.5 to +7.0V
Input Voltage, $V_I$ . . . . . −0.5V to $V_{DD}$ +0.5V
Operating Temperature, $T_{OPT}$ . . . . . 0°C to +85°C
Storage Temperature, $T_{STG}$ . . . . . −65 to +150°C

## *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

($T_A$ = 0 to +70°C, $V_{DD}$ = 5V ± 5%)

| Parameter | Symbol | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V | |
| Input Voltage | $V_I$ | 0 | | $V_{DD}$ | V | |
| Low-level Input Voltage | $V_{IL}$ | 0 | | 0.8 | V | TTL Level |
| High-level Input Voltage | $V_{IH}$ | 2.0 | | $V_{DD}$ | V | TTL Level |
| Input Rise/Fall Times | $t_R$, $t_F$ | 0 | | 10 | us | |

## DC Electrical Characteristics

| Parameter | Symbol | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Static Current | $I_L$ | | 0.1 | 200 | μA | $V_I = V_{DD}$ or GND |
| Dynamic Current | $I_{DD}$ | | 4 | | μA | 1 MHz/cell |
| Input Current | $I_I$ | 0.1 | | 10 | μA | $V_I = V_{DD}$ or GND |
| Low-level Output Current | $I_{OL}$ | 3.2 | 9 | | mA | $V_{OL} = 0.4V$ |
| High-level Output Current | $I_{OH}$ | 1 | 3 | | mA | $V_{OH} = V_{DD} - 0.4V$ |
| Low-level Output Voltage | $V_{OL}$ | | | 0.1 | V | $I_O = 0$ |
| High-level Output Voltage | $V_{OH}$ | $V_{DD} - 0.1$ | | | V | $I_O = 0$ |

## AC Characteristics

| Parameter | Symbol | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum Operating Frequency | $f_{MAX}$ | DC | | 20 | MHz | |
| Output Rise Time | $t_R$ | | 8 | | ns | $C_L = 15$ pF |
| Output Fall Time | $t_F$ | | 4 | | ns | $C_L = 15$ pF |

Storage

## Track Format

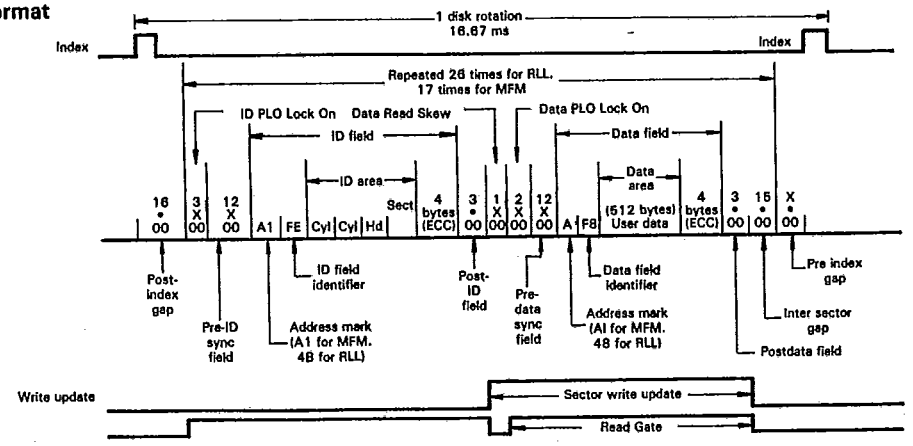



**Figure 1. UM83C021 Track Format Diagram**

| HEX Register Address | Function | ***Range (In Bytes) |
|---|---|---|
| 00 | POST INDEX GAP | 1 – 256 |
| 01 | ID PLO LOCK-ON | 1 – 64 |
| 02 | PRE ID | 1 – 64 |
| 03 | ID ADDRESS MARK | 1 – 4 |
| 04 | FE BYTE | 1 (fixed) |
| 05 | ID | 1 – 16 |
| 06 | ID ECC | 1 – 4 |
| 07 | POST ID | 1 – 4 |
| 08 | DATA READ SKEW | 1 – 64 |
| 09 | DATA PLO LOCK-ON | 1 – 64 |
| A | PRE DATA | 1 – 64 |
| B | DATA ADDRESS MARK | 1 – 4 |
| C | F8 BYTE | 1 (fixed) |
| D | DATA FIELD | |
| | LOW BYTE | 1 – 65, 536 |
| 0E | HIGH BYTE | |
| 0F | DATA ECC | 1 – 4 |
| 10 | POST DATA | 1 – 4 |
| 11 | INTER-RECORD GAP | 1 – 256 |
| 12 | SECTORS PER TRACK | 1 – 256 |
| 1C | ** GAP VALUE REGISTER | 1 |

*** SET REGISTERS TO n–1 TO GET n BYTE LENGTH
** WRITE 4E for MFM encoding, 33 for RLL encoding

**Table 1. Programmable Format Variables**

**Pin Description**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 – 8 | DATA LINES D0 – D7 (TO/FROM HOST) | These 8 data lines are used for PROCESSOR and DMA READS and WRITES. They change synchronously with RAM CLOCK rising edge. |
| 9 | $\overline{\text{SET HEAD}}$ | This signal is used to clock the HEAD ADDRESS, for the drive, into an external HEAD SELECT register. Writing to REGISTER ADDRESS 3D produces a pulse for loading the external head select onto this line. |
| 10 | $\overline{\text{SET DRIVE}}$ | This signal is the load pulse for the external drive selection register. Writing to REGISTER ADDRESS 3E produces the load pulse on this pin. |
| 11 | BUSY | Pin 11 goes high to indicate that the DISK CONTROLLER is busy doing a disk READ or WRITE operation. This pin can be used, if desired, to cause an interrupt for the host processor at the end of a disk READ or WRITE operation. |
| 12 | $\overline{\text{RESET}}$ | The $\overline{\text{RESET}}$ line is intended to be an initial power on reset line. In order to be efficient, it should go low or be low for a minimum of 100 nanoseconds at the beginning of power on. This line is a hard reset line and will immediately terminate any disk READ or WRITE operations or any other functions and reset the chip to an initial state. It should be used essentially as a power on RESET and is not intended for use as a termination command. |

**Pin Description (Continued)**

| Pin No. | Symbol | Description |
|---|---|---|
| 13 | $\overline{\text{REQUEST}}$ | The $\overline{\text{REQUEST}}$ line, in conjunction with the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14), are the "HANDSHAKING" lines for the DMA data transfer for the chip. The DISK CONTROLLER has a byte of information ready to transfer to RAM or needs a byte of information from RAM to write to the disk when the signal at pin 13 is pulled low. The RAM BUFFER CONTROLLER chip (UM83C002) will respond by driving the $\overline{\text{ACKNOWLEDGE}}$ signal (Pin 14) low and giving the DISK CONTROLLER access to the RAM BUFFER. The DMA transfer operations are run synchronously with the RAM CLOCK signal (Pin 19). The rising edge of the RAM CLOCK pulse defines the cycle boundaries for the RAM. |
| 14 | $\overline{\text{ACKNOWLEDGE}}$ | This input is driven low to indicate that the requested DMA byte transfer is currently taking place. The $\overline{\text{ACKNOWLEDGE}}$ signal should be a full RAM CLOCK cycle in width.<br><br>On a disk read operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C021 to gate a byte of data onto the D0 – D7 data lines. On a disk write or verify operation, the $\overline{\text{ACKNOWLEDGE}}$ signal causes the UM83C021 to accept a byte of data from the D0 – D7 data lines.<br><br>To assure proper "Handshaking" with the $\overline{\text{REQUEST}}$ line, this line must change state while the RAM CLOCK signal is high.<br><br>If data is not transferred fast enough to keep up with the requirements of the disk or tape, then the OVERRUN/UNDERRUN bit will be set to one (register address 05 bit 1). If this happens, the current disk operation will be terminated at the end of the current sector. |
| 15 | $\overline{\text{STOP}}$ | This input goes low to indicate the last cycle of a DMA transfer. It is normally driven low by the UM83C002 when the byte counter of the active DMA channel has reached zero. The UM83C021 will continue reading or writing until the end of the current sector is reached and then stop. However, it will not generate any more data requests after the $\overline{\text{STOP}}$ line has been activated. On a sector write, the remainder of the sector will be filled with the last byte that was transferred.<br><br>This line is ignored unless $\overline{\text{ACKNOWLEDGE}}$ is also low. |
| 16 | A0 | The UMC DISK CONTROLLER (UM83C021) occupies two I/O port locations selected by the A0 pin. A0 driven low selects the REGISTER ADDRESS POINTER or STATUS REGISTER and A0 driven high selects the READ or WRITE REGISTERS. (Refer to table 2) |
| 17 | $\overline{\text{CHIP WRITE}}$ | This input is driven by the CPU to indicate whether a register read or write is to be performed. A low indicates a write; a high indicates a read. This line has meaning only when $\overline{\text{CHIP SELECT}}$ is low; and it is ignored when $\overline{\text{CHIP SELECT}}$ is high. |
| 18 | $\overline{\text{CHIP SELECT}}$ ($\overline{\text{CSEL}}$) | The $\overline{\text{CHIP SELECT}}$ line ($\overline{\text{CSEL}}$) is driven low by the processor to read from or write to the registers inside the UM83C021. This signal is intended to be gated by processor's ACKNOWLEDGE signal. |
| 19 | RAM CLOCK (RAMCLK) | This clock input synchronizes all CPU and DMA operations of the UM83C021. Cycle boundaries are defined by the rising edge of this clock. |

**Pin Description (Continued)**

| Pin No. | Symbol | Description |
|---|---|---|
| 20 | GROUND | Negative Supply |
| 21 | READY<br>STATUS 0 | This input status line is available to the Host Processor at READ REGISTER 04 Bit 6. This line performs no logical function within the UM83C021 and hence the DRIVE READY signal or any other desired status signal may be connected to this pin. |
| 22 | SELECTED or<br>STATUS 1 | This input status line is available to the Host Processor at READ REGISTER 04 Bit 7. This line performs no logical function within the UM83C021, hence the DRIVE SELECTED signal or any other desired status signal may be connected to this pin. |
| 23 | INDEX | The rising edge of this INDEX signal from the selected drive is used to define the beginning of the track. It occurs once per revolution. |
| 24 | SECTOR or<br>ADDRESS MARK<br>FOUND | SECTOR<br>For hard sectored drives, the rising edge of this input defines the beginning of sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX.<br><br>ADDRESS MARK FOUND<br>For soft sectored ESDI drives, the rising edge of this ADDRESS MARK FOUND defines the leading edge of every sector except sector 0. The beginning of sector 0 is defined by the rising edge of INDEX. |
| 25 | SEEK COMPLETE<br>or STATUS or<br>LTH | SEEK COMPLETE<br>The SEEK COMPLETE input is available to the Host Processor as STATUS REGISTER Bit 2.<br><br>STATUS<br>For ESDI drives, the serial status line is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2.<br><br>LTH (LOWER TAPE HOLE)<br>For QIC-36 tapes the LOWER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 2. |
| 26 | TRACK 0 or<br>TRANSFER ACK<br>or UTH | TRACK 0<br>For ST-506 type drives, the TRACK 0 signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1.<br><br>TRANSFER ACK (ESDI DISK)<br>For ESDI drives, the TRANSFER ACKNOWLEDGE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1.<br><br>UTH (UPPER TAPE HOLE – QIC-36 TAPE)<br>For QIC-36 tapes, the UPPER TAPE HOLE signal is input at this pin and is available to the Host Processor as STATUS REGISTER Bit 1. |

**Pin Description (Continued)**

| Pin No. | Symbol | Description |
|---|---|---|
| 27 | STEP<br>TRANSFER<br>REQUEST | STEP<br>This output is the STEP pulses for ST-506 drives. This line goes high whenever a one is written to register 1F bit 0. This line goes low whenever a zero is written to register 1F bit 0.<br><br>TRANSFER REQUEST<br>This output is used for TRANSFER REQUEST for ESDI drives. |
| 28 | DIRECTION<br>COMMAND | DIRECTION<br>This output is the DIRECTION signal for ST-506 drives and goes high whenever a one is written to register 1E Bit 7.<br><br>COMMAND<br>This output is the SERIAL COMMAND line for ESDI drives. |
| 29 | ENABLE<br>ADDRESS MARK | This signal is required for the ESDI interface. When writing, it causes the ESDI drive to write an address mark on the track. When reading, it causes the ESDI drive to search for an ADDRESS MARK. When the ESDI drive finds an ADDRESS MARK it will activate the ADDRESS MARK FOUND signal at Pin 24. For ESDI drives, WRITE REGISTER 1 should be set to zeros to produce a 3 byte wide ENABLE ADDRESS MARK signal on format writes. |
| 30 | WRITE GATE | This signal goes directly to the disk interface and must be HIGH to write data to the disk. |
| 31 | WRITE DATA | This signal is the WRITE DATA that goes to the disk drive. This WRITE DATA may be un-encoded or encoded either MFM or RLL and may be either in a pulse format, an NRZ format or NRZI format. |
| 32 | WRITE CLOCK | This signal is the code/encoded data rate and is intended for use as a WRITE CLOCK for the ESDI drive interface. |
| 33 | READ GATE | This signal indicates that the controller is in an ID for DATA area and is attempting to phase lock onto the READ DATA. This signal is used in the ESDI interface. This signal remains ACTIVE even though the DISK CONTROLLER chip is not actually performing a READ. The BUSY signal (Pin 11) can be used in conjunction with the READ GATE signal to produce a signal enabling an external phase comparator if desired. |
| 34 | READ DATA | This signal is the raw DATA pulses that are sent directly from the drive. |
| 35 | READ DATA<br>DELAYED | This signal is the same as the READ GATE (Pin 34) with the exception that it is delayed by one half of a READ DATA CYCLE. For example: If you are running MFM data with a code rate of 10 MHZ yielding a READ DATA CYCLE of 100 nanoseconds, then the data on this pin would be DELAYED by one half of the 100 nanoseconds equaling 50 nanoseconds. An external delay line is utilized to produce this READ DATA DELAYED signal. |

**Pin Description (Continued)**

| Pin No. | Symbol | Description |
|---|---|---|
| 36<br>37 | $\overline{\text{SLOWER}}$ and<br>FASTER | These two signals are used as comparison inputs to an external VOLTAGE CONTROLLED OSCILLATOR so that it can produce the PLO signal at Pin 38. |
| 38 | PLO/READ CLOCK | The PHASE LOCK OSCILLATOR (PLO) Input is a READ CLOCK signal which is phase locked onto the READ DATA. The rising edge of the PLO clock should occur at the same time as the rising edge of the READ DATA delayed signal at Pin 35. If the DISK CONTROLLER chip is used to control an ESDI interface drive, the input to this pin would be the READ CLOCK signal coming directly from the ESDI interface. |
| 39 | XTAL (Crystal) | This is the crystal oscillator input which is the reference clock for writing to the hard disk. The XTAL frequency should be the code frequency going to the disk. For example: If running at MFM with a 5 megabit disk data rate, the MFM code going to the disk would be at a 10 MHz rate and the XTAL input would be at 10 MHz. If using RLL code with a 7 1/2 megabit disk data rate, the code rate going to the disk would be 15 MHz and the XTAL input would be 15 MHz. For ESDI drives, the READ CLOCK would be input at this pin. |
| 40 | 5 VOLTS | Positive Supply |

**Register Addresses**

Data Lines (D0-D7), in conjunction with the software controlled A0 signal (as an enabling signal), are decoded to select either a write or read operation to be performed and the REGISTER ADDRESSES to be utilized. (Table 2 is a chart of the A0 REGISTER ADDRESSES)

| | | Read | Write |
|---|---|---|---|
| | BIT | STATUS | REGISTER ADDRESS |
| A0 = 0 | 7 | CONTROLLER BUSY | AUTO-INCREMENT |
| | 6 | DISK OP IN PROGRESS | DISK DATA |
| | 5 | WRITE GATE | REG A5 |
| | 4 | DATA REQUESTED | REG A4 |
| | 3 | DATA AVAILABLE | REG A3 |
| | 2 | SEEK COMPLETE | REG A2 |
| | 1 | TRACK 0 | REG A1 |
| | 0 | ERROR | REG A0 |
| A0 = 1 | BIT | DATA | DATA |
| | 7 | D7 | D7 |
| | 6 | D6 | D6 |
| | 5 | D5 | D5 |
| | 4 | D4 | D4 |
| | 3 | D3 | D3 |
| | 2 | D2 | D2 |
| | 1 | D1 | D1 |
| | 0 | D0 | D0 |

**Table 2. Register Addressing**

### Auto-Increment

If bit 7 of the REGISTER ADDRESS is set, the address will be automatically incremented after every register read or write.

There are two exceptions to AUTO-INCREMENT: (1) There is no increment after writing the STEP REGISTER (address 9F); and (2) After reading or writing the DATA REGISTER (address C0).

### Status Register

The STATUS REGISTER informs the host of certain events performed by the UM83C021 as well as reporting status from the drive control.

| Bit | Signal | Description |
|---|---|---|
| 7 | Controller Busy | If bit 7 comes up, this indicates that either a disk read/write is in progress or the controller is still working on the last byte written or it is incrementing the register address. |
| 6 | Disk Operation in Progress | If bit 6 comes up, a disk read/write operation is in progress. |
| 5 | Write Gate | This bit reflects the state of the WRITE GATE pin from the UM83C021 indicating that the controller is writing to the drive. Normally, registers should not be changed while writing to the disk. |
| 4 | Data Request | This bit indicates that the controller requires a byte to be written into the DISK DATA register. It is used for non-DMA data transfers. |
| 3 | Data Available | This bit indicates that there is a byte for the host processor to read from the data disk register. It is used for non-DMA data transfers. |
| 2 | Track 0/XFR ACK/UTH | This bit reflects the state of its pin (Pin 26) on the UM83C021 (i.e. if the signal at this pin is high, bit 2 will be high). It is used to indicate that the selected drive is at track 0; that an ESDI drive has acknowledged a COMMAND/STATUS transfer; or that a QIC-36 tape drive has detected the upper tape hole. |
| 1 | Seek Complete/ Status Data/LTH | This bit reflects the state of its pin (Pin 25) on the UM83C021 (i.e. if the signal at this pin is high, bit 1 will be high). It is used to indicate that the selected drive has completed any head positioning sequence; the state of a bit in the CONFIGURATION/ STATUS word on an ESDI drive; or that a QIC-36 tape has detected the lower tape hole. |
| 0 | Error | This bit is set whenever any bit in the CONTROLLER ERROR register is set. It is the logical OR of the CONTROLLER ERROR register bits and may be used by the host to quickly check successful completion of a command. This bit is reset when a new command is written into the DISK OPERATION register. |

### Available Registers

There are 64 available REGISTER ADDRESSES in the UM83C021; however, only 41 are used. Table 3 is a list of available WRITE registers and Table 4 is a list of available READ registers.

| Register Address Decimal | HEX | Auto Incr HEX | Register |
|---|---|---|---|
| 0 | 00 | 80 | POST-INDEX GAP |
| 1 | 01 | 81 | ID PLO LOCK-ON |
| 2 | 02 | 82 | PRE-ID |
| 3 | 03 | 83 | ID ADDRESS MARK |
| 4 | 04 | 84 | FE BYTE |
| 5 | 05 | 85 | ID |
| 6 | 06 | 86 | ID ECC |
| 7 | 07 | 87 | POST-ID |
| 8 | 08 | 88 | DATA READ SKEW |
| 9 | 09 | 89 | DATA PLO LOCK-ON |
| 10 | 0A | 8A | PRE-DATA |
| 11 | 0B | 8B | DATA ADDRESS MARK |
| 12 | 0C | 8C | F8 BYTE |
| 13 | 0D | 8D | DATA LOW |
| 14 | 0E | 8E | DATA HIGH |
| 15 | 0F | 8F | DATA ECC |
| 16 | 10 | 90 | POST DATA |
| 17 | 11 | 91 | INTER-RECORD GAP |
| 18 | 12 | 92 | SECTORS PER TRACK |
| 19 | 13 | 93 | ID START LOCATION |
| 20 | 14 | 94 | ADDRESS MARK FIRST HALF |
| 21 | 15 | 95 | ADDRESS MARK LAST HALF/UNENCODED ADDRESS MARK |
| 22 | 16 | 96 | RECORDING CODE |
| 23 | 17 | 97 | CLOCK DIVIDER |
| 24 | 18 | 98 | FE |
| 25 | 19 | 99 | F8 |
| 26 | 1A | 9A | SECTOR SIZE |
| 27 | 1B | 9B | SECTOR OPTIONS |
| 28 | 1C | 9C | GAP VALUE |
| 29 | 1D | 9D | |
| 30 | 1E | 9E | DIRECTION |
| 31 | 1F | 9F* | STEP |
| 56 | 38 | B8 | CYLINDER HI |
| 57 | 39 | B9 | CYLINDER LO |
| 58 | 3A | BA | HEAD |
| 59 | 3B | BB | SECTOR |
| 60 | 3C | BC | TRANSFER COUNT |
| 61 | 3D | BD | HEAD SELECT |
| 62 | 3E | BE | DRIVE SELECT |
| 63 | 3F | BF | DISK OP |
| 64 | 40 | C0* | DATA TO/FROM DISK READ/WRITE |

*These Addresses do not Auto-Increment.

**Table 3. Write Register Addresses**

Storage

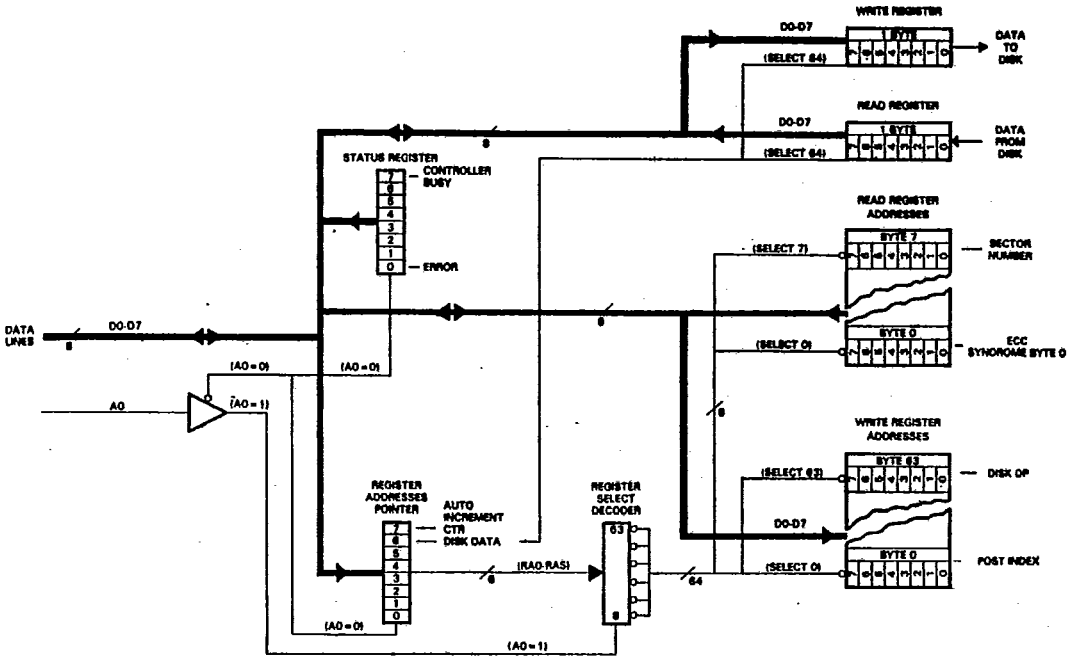



**Figure 3. UM83C021 Register Addresses and Selection**

### Write Register Address Descriptions

The WRITE registers, Hex 0 – 17, control the length of the fields of the track format. To set the length, set the appropriate register with the desired byte count–1.

The following is a description of the available registers within the UM83C021 including the appropriate hex Register Address:

#### (HEX 00) POST INDEX GAP

Number of bytes after the index pulse.
FIELD LENGTH = 1 – 256 BYTES

#### (HEX 01) ID PLO LOCK-ON

Read gate starts at the beginning of this field. This field is to allow the PLO to lock onto the read data.
FIELD LENGTH = 1 – 64 BYTES

#### (HEX 02) PRE-ID

The Address Mark search begins in this field.
FIELD LENGTH = 1 – 64 BYTES

#### (HEX 03) ID ADDRESS MARK

This field is used on soft sectored media so that the controller can identify the start of ID and DATA fields. ADDRESS MARKS in FM or MFM are recorded with certain clock pulses missing and are unique from all other data and gap bytes recorded on the track. ADDRESS MARKS in RLL use an illegal sequence violating the Encoding scheme of 2 to 7 zeros between flux reversals.
FIELD LENGTH = 1 – 4 BYTES

#### (HEX 04) FE BYTE

This field is used to identify that you are in an ID field. The value of register 18, field identifier byte, (normally an FE) is expected in this field.
FIELD LENGTH = 1 BYTE (fixed)

#### (HEX 05) ID

The ID information: CYL-HI, CYL-LO, HEAD and SECTION NUMBER areas are stored in this field.
FIELD LENGTH = 1 – 16 BYTES

**(HEX 06) ID ECC**

This field contains the CRC or ECC bytes for the ID area.
FIELD LENGTH = 1 – 8 BYTES

**(HEX 07) POST-ID**

This field should contain 00's. It is required to ensure proper recording and recovery of the last bits of the ID CRC/ECC field. On write data operations, the WRITE GATE goes active at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

**(HEX 08) DATA READ SKEW**

On READ DATA operations, the READ GATE goes active at the end of this field. This field is intended to allow the PLO to skip over the write splice area before it begins trying to sync onto the read data.
FIELD LENGTH = 1 – 64 BYTES

**(HEX 09) DATA PLO LOCK-ON**

The READ GATE goes active at this point.
FIELD LENGTH = 1 – 4 BYTES

**(HEX 0A) PRE-DATA**

The search for ADDRESS MARK starts here.
FIELD LENGTH = 1 – 64 BYTES

**(HEX 0B) DATA ADDRESS MARK**

See ID ADDRESS MARK
FIELD LENGTH FOR HARD DISK = 1 BYTE
FIELD LENGTH FOR FLOPPY = 3 BYTES

**(HEX 0C) F8 BYTE**

FIELD LENGTH = 1 BYTE (fixed)

**(HEX 0D) DATA LOW**
**(HEX 0E) DATA HIGH**

These two bytes define the length of the DATA FIELD

0D = Low Byte of DATA LENGTH
0E = High Byte of DATA LENGTH

FIELD LENGTH = 1 – 65,536 BYTES

**(HEX 0F) DATA ECC**

See ID CRC/ECC field.
FIELD LENGTH = 1 – 8 BYTES

**(HEX 10) POST DATA**

Data WRITES stop at the end of this field.
FIELD LENGTH = 1 – 4 BYTES

**(HEX 11) INTER-RECORD GAP**

This field provides a separation between each sector to allow speed tolerances; write to read recovery time (time between deassertion of WRITE GATE and assertion of READ GATE) head switching time and controller decision making time between sectors and variations in detecting INDEX and SECTOR.
FIELD LENGTH = 1 – 256 BYTES

**(HEX 12) SECTORS PER TRACK**

Write N-1 to this register
FIELD LENGTH = 1 – 256 BYTES

**(HEX 13) ID START LOCATION**

This register is set to specify which internal register follows the FE register in the ID field. This register is set as shown below.

| ID Start Value | Next Byte Following FE | |
|---|---|---|
| 00 | FE | (causes FE to be used twice) |
| 01 | CYLINDER HI | (normal setting for hard disk) |
| 02 | CYLINDER LO | (normal setting for floppy) |
| 03 | HEAD | |
| 04 | SECTOR | |
| 05 | SECTOR SIZE | |

Storage

**(HEX 14) ADDRESS MARK FIRST HALF**
**(HEX 15) ADDRESS MARK SECOND HALF**

HEX 14 = The first half of the encoded ADDRESS MARK
HEX 15 = The second half of the encoded ADDRESS MARK or the whole unencoded ADDRESS MARK when running in unencoded mode.

ADDRESS MARKS are special bytes recorded at the beginning of each ID and DATA field. These bytes are unique and do not occur anywhere else on the disk. They are used to identify the exact beginning of the ID and DATA fields. These ADDRESS MARKS are made unique by violating the rules for encoding the data.

When using MFM encoding, the ADDRESS MARK is an A1 data byte with one of the clock bits dropped.

MFM CLOCK BITS 0 0 0 0 1 1 1 0
DATA BITS 1 0 1 0 0 0 0 1

MFM ADDRESS MARK
01010100 10001001 = HEX 54 and HEX 89
└ This bit has been dropped
HEX 54 = First half in location HEX 14
HEX 89 = Second half in location HEX 15

When using UM83C021 RLL encoding, the ADDRESS MARK is a 4B data byte with one of the bits dropped. This results in a unique pattern with 8 zeros in a row.

| | | | |
|---|---|---|---|
| 4B | 010 | 010 | 11 |
| RLL CODE FOR 4B | 000100 | 000100 | 1000 |
| RLL ADDRESS MARK | 000100 | 000000 | 1000 = HEX 10 and HEX 08 |

This bit has been dropped

HEX 10 = First half in location HEX 14
HEX 08 = Second half in location HEX 15

In 2,7 RLL encoding, the maximum number of zeros in a row is 7.

**(HEX 16) RECORDING CODE**

| | | |
|---|---|---|
| 80 | 00 | NRZ WRITE DATA |
| 40 | 01 | NRZI WRITE DATA |
| | 10 | PULSE WRITE DATA |
| | 11 | |
| 20 | 00 | NRZ READ DATA |
| 10 | 01 | NRZI READ DATA |
| | 10 | PULSE READ DATA |
| | 11 | |
| 08 | 000 | UNENCODED |
| 04 | 001 | FM |
| 02 | 010 | MFM |
| | 011 | RLL 2,7 |
| 01 | Should be 0 | |

**(HEX 17) CLOCK DIVIDER**

Through the use of a PLO divider circuit, the disk controller chip is capable of controlling several devices that do not operate at the same data rates without requiring a separate PLO circuit for each. For example, the controller can operate a hard disk, a floppy disk, and a tape drive using only a single PLO running at 10 MHz or 15 MHz. If running a 15 MHz PLO for an RLL encoded hard disk, the controller is divided by 15 to run the tape drive and divided by 30 to run the floppy disk.

The PLO divider can divide from 1 to 256. To divide by a number n, the number n-1 must be written into the Clock Divider at register address 17 hexadecimal.

In order to improve PLO lock-on performance, the Clock Divider is synchronized to the first data pulse at the beginning of every read operation.

Bytes that are written to or read from the UM83C021 at RAM CLOCK speed are internally synchronized to the WRITE CLOCK. This synchronization can take up to 5 write clock cycles. During this synchronization, the CONTROLLER BUSY bit (Status Register bit 7) will be one.

If additional bytes are written to or read from the chip during this synchronization, the results will be unpredictable.

When using a divided down clock, the length of time required for this synchronization may become significant. For example: when working with a 5-1/4 inch floppy, the disk clock would be 2 microseconds. The synchronization could take up to 5 x 2 = 10 microseconds. When designing your system, insure that reads and writes to the UM83C021 are always farther apart than 10 microseconds whenever the clock is divided down to a 2 microsecond period. This can be done by inserting extra instructions in the host program or by monitoring the CONTROLLER BUSY bit.

**(HEX 18) FE**

ID field identifier byte
Write FE to this register.

**(HEX 19) F8**

Data field identifier byte.
Write F8 to this register for hard disk or FB for floppies.

**(HEX 1A) SECTOR SIZE**

This byte follows the sector number in the ID field and is normally used with floppies – not with a hard disk.

**(HEX 1B) SECTOR OPTIONS**

The UM83C021 handles soft or hard sectored disks or ESDI disks using ESDI Address Marks. ESDI byte clock operation requires an external counter to create hard sector pulses.

| | | | |
|---|---|---|---|
| BIT 7 to 2 | = 0 | | |
| BIT 1 | = 02 | 00 | SOFT SECTORED |
| BIT 0 | = 01 | 01 | HARD SECTORED |
| | | 10 | ESDI ADDRESS MARKS |
| | | 11 | ESDI BYTE CLOCKS |

**(HEX 1C) GAP VALUE**

Write 4E for MFM encoding
Write 33 for RLL encoding

**(HEX 1E) DIRECTION**

Bit 7 of the register is sent directly to the DIRECTION output pin. Writing a HEX 80 to this address will make the pin high; a HEX 00 will make it low. This pin is used for direction control of ST506 drives or for command data on ESDI drives.

**(HEX 1F) STEP**

Bit 0 of this register is sent directly to the STEP output pin. Writing a HEX 01 to this address will make the pin high; a HEX 00 will make it low. This pin is used for STEP CONTROL of ST506 drives or for TRANSFER REQUEST on ESDI drives. Auto-increment is disabled for this address because it must be written repetitively to create multiple STEP pulses at the drive interface.

**(HEX 38) CYLINDER HI**

This register contains the HI 8 bits of the cylinder number. The contents of this register and the next 3 registers are used for writing or searching for ID FIELDS on the disk.

**(HEX 39) CYLINDER LO**

This register contains the LO 8 bits of the cylinder number.

**(HEX 3A) HEAD**

This register contains the HEAD number.

**(HEX 3B) SECTOR**

This register contains the SECTOR number. On multi-sector operations, this register is incremented after each sector is read or written and may be read at address 07.

**(HEX 3C) TRANSFER COUNT**

This register contains the number of sectors desired for this command –1. On multi-sector operations, this register is decremented after each sector is read or written and may be read at address 06.

**(HEX 3D) HEAD SELECT**

When this register is written, the external $\overline{\text{SET HEAD}}$ pin strobes low to latch the head number from the data bus.

**(HEX 3E) DRIVE SELECT**

When this register is written, the external $\overline{\text{SET DRIVE}}$ pin STROBES low so that the external drive register can latch the drive number from the data bus.

**(HEX 3F) DISK OP**

Writing to this register starts or stops DISK READ or WRITE operations. The commands are listed below and are described in more detail in the DISK COMMAND section.

00 STOP DISK OPERATION
80 NO-OP
81 WRITE DATA
82 READ DATA
83 READ ID
84 WRITE FIRST SECTOR
85 WRITE NEXT SECTOR
86 FORMAT WRITE INTERLEAVED
87 FORMAT WRITE SEQUENTIAL
88 READ DATA IMMEDIATE
89 WRITE SECTOR IMMEDIATE
8A WRITE GAP IMMEDIATE
8B VERIFY DATA
8C READ LONG
8D WRITE LONG
8E COMPUTE ERROR SHORT, CORRECTION SPAN 5, 11 BITS
8F COMPUTE ERROR LONG, CORRECTION SPAN 11, 22 BITS

**(HEX 40) DATA TO/FROM DISK**

Data written to this register is serialized and sent as data to the disk. Writing to this register resets the DATA REQUESTED status bit (Bit 4). If data is not written fast enough to keep up with the disk, the OVERRUN/UNDERRUN status bit (register 05 Bit 1) will be set.

### Read Register Address Descriptions

| Register Address Decimal | Hex | Auto Inch Hex | | Register | | |
|---|---|---|---|---|---|---|
| 0 | 00 | 80 | | Not used | | |
| 1 | 01 | 81 | | Not used | | |
| 2 | 02 | 82 | | Not used | | |
| 3 | 03 | 83 | | Not used | | |
| 4 | 04 | 84 | | Disk status | | |
| 5 | 05 | 85 | | Controller status | | |
| 6 | 06 | 86 | | Transfer count | | |
| 7 | 07 | 87 | | Sector number | | |
| | | | | ECC 56 Bit | ECC 32 Bit | CRC 16 Bits |
| 8 | 08 | 88 | | Not used | Not used | Not used |
| 9 | 09 | 89 | | 0 | Not used | Not used |
| 10 | 0A | 8A | Error | 1 | Not used | Not used |
| 11 | 0B | 8B | Syndrome | 2 | Not used | Not used |
| 12 | 0C | 8C | Bytes | 3 | 0 | Not used |
| 13 | 0D | 8D | | 4 | 1 | Not used |
| 14 | 0E | 8E | | 5 | 2 | 0 |
| 15 | 0F | 8F | | 6 | 3 | 1 |
| 64 | 40 | C0 * | | Data from disk | | |

* This address does not auto-increment

**Table 4. Read Register Addresses**

**(HEX00 – HEX03) NOT USED**

**(HEX04) DISK STATUS**

BIT 7 = DRIVE SELECTED/STATUS 1 (HEX 80)
This bit has a dual role when controlling a Winchester drive. It indicates that a drive has been successfully selected. This pin directly reads the logic level of pin 27 on the chip.

Storage

BIT 6 = READY/STATUS 0 (HEX 40)

This bit also has a dual role. When controlling floppy and Winchester drives, it indicates that a drive is up to speed and ready for read or write. This pin directly reads the logic level of pin 21 on the chip.

BIT 5 = SECTOR ADDRESS MATCH (HEX 20)

This bit is set when a sector ID matches what was set into the Sector Address Registers during a read/write operation.

BIT 4 = LAST SECTOR ON TRACK (HEX 10)

This bit is set during the last sector of a track. (Sector # in ID field = Sector per track.) See Multi-Sector transfers.

BITS 3 THRU 0 = FIELD COUNTER

The FIELD COUNTER indicates what field is passing under the heads on a read or write.

| FIELD COUNT | HEX COUNT | FIELD LOCATION ON DISK |
|---|---|---|
| 0 | 00 | INTER-RECORD GAP or POST-INDEX GAP |
| 1 | 01 | ID PLO LOCK-ON |
| 2 | 02 | PRE-ID |
| 3 | 03 | ID AM |
| 4 | 04 | FE |
| 5 | 05 | ID |
| 6 | 06 | ID ECC |
| 7 | 07 | POST-ID |
| 8 | 08 | DATA READ SKEW |
| 9 | 09 | DATA PLO LOCK-ON |
| 10 | 0A | PRE-DATA |
| 11 | 0B | DATA AM |
| 12 | 0C | F8 |
| 13 | 0D | DATA |
| 14 | 0E | DATA ECC |
| 15 | 0F | POST-DATA |

**(HEX 05) CONTROLLER STATUS**

BIT 7 = NO RECORD FOUND (HEX 80)

Indicates that on a read or write, the controller has received two successive index pulses without finding an ID field that matched the Sector Address registers. Sector pulses are not input on the INDEX pin).

BIT 6 = MISSING DATA AM (F8 MISCOMPARE) (HEX 40)

This bit is set if the byte after the Data Address Mark does not match the contents of register 19, the Data Field Indentifier byte, indicating that a data field probably does not exist.

BIT 5 = ID ECC/CRC ERROR (HEX 20)

When set indicates that a read/write sector to the addressed sector was found, but that the CRC/ECC was in error.

BIT 4 = DATA ECC ERROR (HEX 10)

When set indicates that a read of the addressed sector was found, but that the DATA field CRC/ECC bytes was in error.

BIT 3 = DATA MISMATCH (HEX 08)

Indicates that the Verify command has stopped with a data mismatch error. See Verify command.

BIT 2 = DATA TRANSFER STOPPED (STOP RECEIVED) (HEX 04)

Indicates that during a read or write the DMA-STOP pin was activated and that the transfer has stopped.

BIT 1 = OVERRUN/UNDERRUN (HEX 02)

Indicates that data was not transferred to or from the controller quick enough for the Serializer/Deserializer section.

BIT 0 = NOT USED

**(HEX 06) TRANSFER COUNT**

This register contains the number of sectors remaining (including the current) for Multi-sector operations and it is decremented after each successful sector read or write.

**(HEX 07) SECTOR NUMBER**

This register contains the SECTOR NUMBER for the operation that the controller is currently performing. It is incremented after each multi-sector operation but is not incremented if an error occurs.

**(HEX 08) NOT USED**

**(HEX 09) 56 BIT ECC SYNDROME BYTE 0**

**(HEX 0A) 56 BIT ECC SYNDROME BYTE 1**

**(HEX 0B) 56 BIT ECC SYNDROME BYTE 2**

**(HEX 0C) 56 BIT ECC SYNDROME BYTE 3**

**(HEX 0D) 56 BIT ECC SYNDROME BYTE 4**

**(HEX 0E) 56 BIT ECC SYNDROME BYTE 5**

## Disk Commands

Writing to the COMMAND register at location 3F causes a disk operation to begin. All registers used in the disk operation should be set up prior to writing to the COMMAND register.

**(HEX 00) ABORT**

This command will immediately terminate any operation in progress.

**(HEX 80) NO OP**

This command causes no disk operation.

### (HEX 81) WRITE DATA

This command writes data from memory into the data field of the sector whose address has been written into the sector address registers in the chip. Multi-sector writes are possible up to 256 sectors.

### (HEX 82) READ DATA

This command reads the data field from the sector whose ID has been set into the registers on the disk controller. The data field is transferred to memory by DMA. It may optionally be transferred under program control if the disk speed is slow enough for the computer to keep up with it. The F8 byte immediately following the data address mark is not transferred but is checked to assure that a data field is present.

At the end of every sector transfer, the Transfer Count is checked. If it is zero, the operation stops. If it is non-zero, it is decremented, the sector number is incremented, and the next sector is read. This process continues until the Transfer Count goes to zero, the end of the track is reached, or an error occurs.

The DMA data transfer may be stopped by having $\overline{\text{STOP}}$ go low during a DMA cycle ($\overline{\text{ACK}}$ low). If this happens, the disk controller will immediately cease data transfer and will halt the operation at the end of the current sector. In this case, the Transfer Count will not be decremented and the sector number will not be incremented.

The residual Transfer Count and the sector number registers can be read to determine where to continue.

### (HEX 83) READ ID

This command reads the next ID fields and ID ECC fields that are encountered on the disk or tape. It transfers both fields to memory. The ID ECC field is checked for errors.

It can be used to establish track orientation on tape or disk. It can also be used in error recovery procedures to determine if the read-write heads are positioned over the correct track.

### (HEX 84) WRITE FIRST SECTOR

This command begins writing at the Index Pulse and writes both ID fields and data fields. Information for the index field comes from the internal sector address registers. Information for the data fields is transferred from memory.

Multi-sector writes can write up to 256 sectors.

If this command is terminated by the transfer count going to zero, it stops writing at the end of the post-data field of the last sector. If this command is terminated by the sectors per track counter going to zero, it will continue writing the postdata field until the next Index Pulse is reached or until a Reset Command (00 hexadecimal) is received.

This command can be used to format and write data to a track in a single operation.

### (HEX 85) WRITE NEXT SECTOR

This command begins writing at the end of the post-data field of the sector whose address has been set into the internal sector address registers. It writes ID fields as well as data fields. It stops writing at the end of the post-data field when the transfer count goes to zero.

Multi-sector writes can be done up to 256 sectors.

This command can be used to repair the ID field of a damaged sector.

### (HEX 86) FORMAT INTERLEAVED

This command is similar to the Format Sequential (See HEX 87) command. However, in this command the ID fields to be written on the disk come from memory rather than from the internal registers on the ID Numbers written are totally programmable and can be interleaved in any manner desired.

For each sector written the disk controller will fetch all bytes of the ID field plus one byte of filler (usually a hexadecimal E5) for the data field. The hexadecimal FE byte immediately following the ID Address Mark is not fetched from memory but is written from the internal register in the disk controller.

For a typical hard disk format the ID field length would be 4, and the following 5 bytes would be fetched from memory for each sector.

Cylinder High
Cylinder Low
Head
Sector
Data Filler Byte (usually E5)

If the track is being formatted with 26 sectors, then a total of 5 x 26 = 130 bytes will be fetched from memory during the Format Interleaved command execution.

**(HEX 87) FORMAT SEQUENTIAL**

This command is used to format a single track on a disk. It begins writing at index and continues writing to the next index. It writes all ID and data fields using the information set into the on-chip ID and DATA registers.

| ID Byte | Register Address | Data Filler Byte | Register Address |
|---|---|---|---|
| CYLINDER HI | HEX 38 | DATA | HEX 40 |
| CYLINDER LO | HEX 39 | | |
| HEAD | HEX 3A | | |
| SECTOR SIZE | HEX 1A | | |

After each sector is written, the sector number register is incremented by one and the track size register is decremented by one. When the track size register reaches zero, one last sector is written and the remainder of the track is written with zero.

No data is transferred to or from memory during a format sequential command.

**(HEX 88) READ DATA IMMEDIATE**

It differs in that when it is issued, the track orientation counters are reset to the post-index gap and the read operation begins there. It is intended primarily for use when controlling tape drives where there is no index pulse to establish position on the track. With this command the microprocessor is responsible for maintaining track orientation.

Data transfer occurs the same as with the Read Data command. Up to 256 sectors can be transferred with a single command.

**(HEX 89) WRITE IMMEDIATE**

Write Immediate is a formatting type write in that it writes the ID field of each sector as well as the data field. It is intended primarily for use when controlling tape where there is no index pulse to establish track orientation. When it is issued, the track orientation counters are set to post-index gap and WRITE GATE goes high immediately.

ID field information is written from the internal sector address registers. Data field information is transferred from memory. The sector number is incremented after every sector is written. Up to 256 sectors can be written with a single Write Immediate command.

Writing stops at the end of the post-data field when the transfer count goes to zero.

If Write Immediate is terminated by the physical sector count going to zero, the controller will continue writing the post-data field until it is stopped by the microprocessor issuing a Reset Command (00 hexadecimal) or until an Index Pulse is received. This allows tapes to be written with a long trailer gap after the last data block.

**(HEX 8A) WRITE GAP IMMEDIATE**

When the Write Gap command is issued, the track orientation counters are set to post-index gap and the controller immediately begins writing zeroes. Writing continues until index is reached or until this command is terminated by issuing another command or a halt command.

This command is intended primarily for writing header or trailer zero fields on tape.

**(HEX 8B) VERIFY DATA**

This command begins reading data from the disk at the addressed sector and comparing it to the data transferred from memory. If the disk data and the data from memory do not match, this command will terminate with the Data Mismatch bit set (Read Register 0D bit 3).

**(HEX 8C) READ LONG**

This command is used primarily for checking the ECC and CRC circuitry. It reads and transfers to memory the data field and data ECC field of the addressed sector.

The ID ECC field and the data ECC field are checked and error latches are set if they are not correct. An error in the ID ECC field will not stop the data field from being transferred as it would with the Read Data command. However, an error in either ECC field will terminate a multi-sector Read Long at the end of the post-data field of the sector containing the error.

After using the Read Long command, the ECC Syndrome registers containing the EGG bits read from the disk instead of error bits.

This command also allows the reading of records that were written by controllers that use different ECC or CRC generators.

**(HEX 8D) WRITE LONG**

This command is used primarily for checking the ECC and CRC circuitry. It writes from memory the data field and the data ECC field of the addressed sector. This command permits the creation of errors to assist in testing the error detection circuits.

An error in the ID ECC field will not prevent writing to the addressed sector.

**(HEX 8E) COMPUTE ERROR**

This command is used to compute ECC error. It's correction span is 5 & 11 bits for 32 & 56 bits ECC.

**(HEX 8F) COMPUTE ERROR LONG**

This command is used to compute ECC error. It's correction span is 11 and 22 bits for 32 and 56 bits ECC.

### Timing Specs and Diagrams

This section is devoted to the timing of signals and their relationship to each other in order to make the maximum use of the UM83C021. The following tables and diagrams are to be used as design tools when incorporating the UM83C021 into your system.

| Signal | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| XTAL | | 20 | | MHZ |
| PLO | | 20 | | MHZ |
| READ DATA | | 10 | | MBITS/SEC |

**Table 5. Signal Frequencies**

| Signal | LO | HI | Units |
|---|---|---|---|
| XTAL | 13 | 20 | NANOSECONDS |
| PLO | 13 | 20 | |
| MCLK | 30 | 30 | |
| RESET | 100 | | |

**Table 6. Signal Widths**

| Delays From | To | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| XTAL HI | WRITE DATA | | 35 | 70 | NANOSECONDS |
| XTAL | WRITE CLOCK | | 30 | 60 | |
| XTAL OR PLO HI | REQUEST LO | | 32 | 63 | |
| ACK & MCLK LO | REQUEST HI | | 36 | 72 | |
| MCLK LO | SET HEAD LO | | 30 | 59 | |
| MCLK HI | SET HEAD HI | | 21 | 42 | |
| MCLK LO | SET DRIVE LO | | 30 | 59 | |
| MCLK HI | SET DRIVE HI | | 21 | 42 | |
| XTAL OR PLO HI | DIRECTION | | 43 | 85 | |
| XTAL OR PLO HI | STEP | | 38 | 77 | |
| CSEL HI OR WRT LO | D0-D7 TRI-STATE | | 25 | 50 | |
| CSEL LO & WRT HI | D0-D7 ACTIVE | | 29 | 57 | |
| ACK HI OR WRT LO | D0-D7 TRI-STATE | | 31 | 61 | |
| ACK LO & WRT HI | D0-D7 ACTIVE | | 29 | 57 | |
| XTAL HI | WRGT | | 32 | 63 | |
| PLO HI | RDGT | | 36 | 71 | |
| XTAL OR PLO HI | ENAM | | 36 | 71 | |
| XTAL OR PLO HI | BUSY | | 31 | 62 | |
| RDEL HI | FSTR HI | | 26 | 51 | |
| PLO HI | FSTR LO | | 26 | 51 | |
| PLO HI | SLWR LO | | 26 | 51 | |
| RDEL HI | SLWR HI | | 26 | 51 | |

**Table 7. Delays**

Storage

| From Changing Signal | Set-Up | To | Hold | Units |
|---|---|---|---|---|
| ACKNOWLEDGE | 4.0 | RAMCLK LO | | NANOSECONDS |
| ACKNOWLEDGE | | RAMCLK HI | 0 | |
| WRITE | 15 | RAMCLK LO | | |
| WRITE | | RAMCLK HI | 15 | |
| CHIP SELECT | 15 | RAMCLK LO | | |
| CHIP SELECT | | RAMCLK HI | 15 | |
| A0 | 15 | RAMCLK LO | | |
| A0 | | RAMCLK HI | 15 | |
| NOTE THAT ALL THE ABOVE SIGNALS SHOULD CHANGE WHEN RAMCLK IS HIGH AND BE STABLE WHEN RAMCLK IS LOW | | | | |
| DATA (D0 – D7) | 2 | RAMCLK HI | 12 | NANOSECONDS |
| STOP | 6 | RAMCLK HI | 3 | |

**Table 8. Set Up and Hold Time**

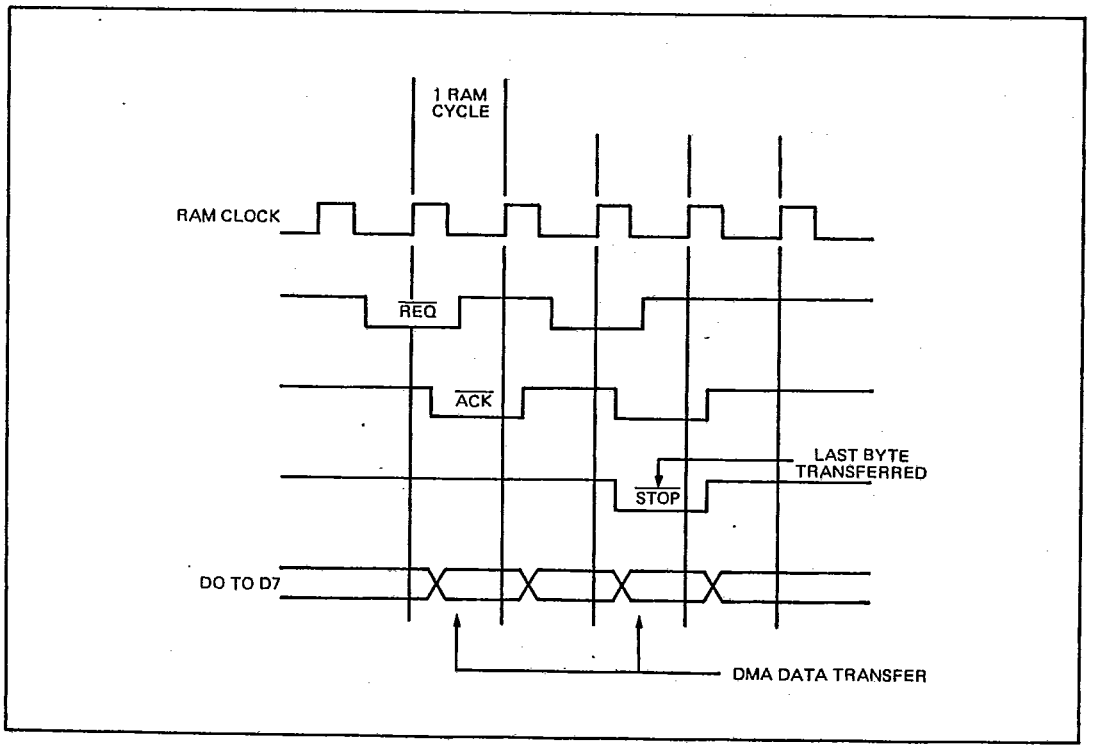



**Figure 4. DMA Data Transfer Cycles**

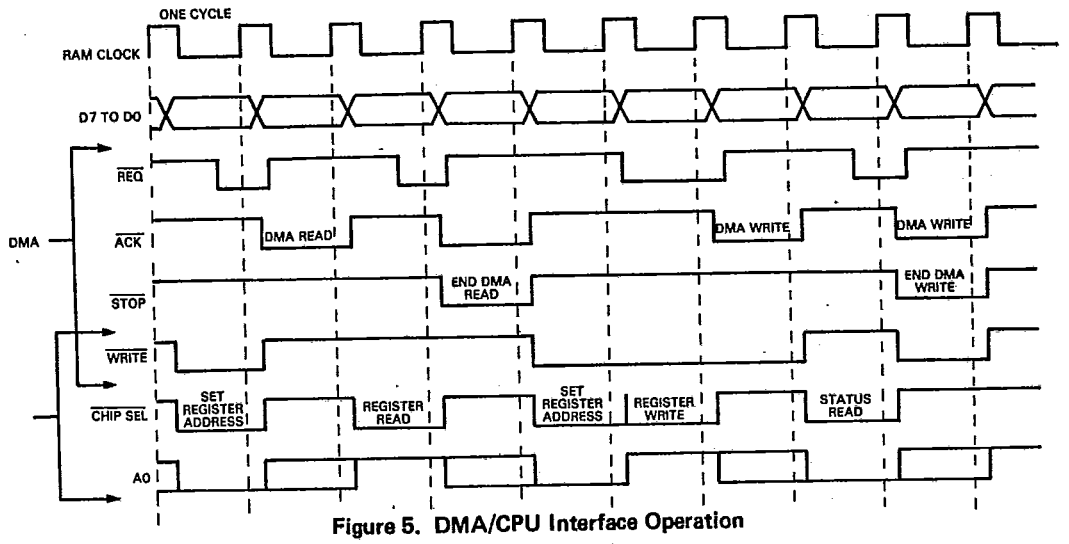



**Figure 5. DMA/CPU Interface Operation**