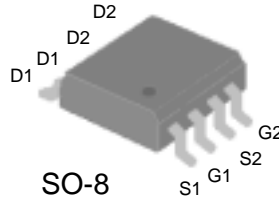


COMPLEMENTARY N- AND P-CHANNEL ENHANCEMENT-MODE POWER MOSFETS

Simple drive requirement
 Lower gate charge
 Fast switching characteristic

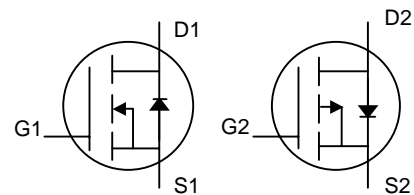


N-CH	BV_{DSS}	40V
	$R_{DS(ON)}$	25m Ω
	I_D	7.6A
P-CH	BV_{DSS}	-40V
	$R_{DS(ON)}$	33m Ω
	I_D	-6.5A

Description

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM4565M is in the SO-8 package, which is widely preferred for commercial and industrial surface mount applications, and is well suited for low voltage applications such as DC/DC converters.



 This device is available with Pb-free lead finish (second-level interconnect) as SSM4565GM.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current ³	7.6	-6.5	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current ³	6	-5.2	A
I_{DM}	Pulsed Drain Current ¹	30	-30	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ C/W$

N-channel Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.03	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=7A$	-	-	25	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	-	32	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=7A$	-	12	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=32V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=7A$	-	17	27	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=32V$	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	10	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=20V$	-	11	-	ns
t_r	Rise Time	$I_D=1A$	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	30	-	ns
t_f	Fall Time	$R_D=20\Omega$	-	11	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1400	2240	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	250	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	170	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1.7A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=7A, V_{GS}=0V$	-	26	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	21	-	nC

P-channel Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=-1\text{mA}$	-	-0.03	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-6A$	-	-	33	$m\Omega$
		$V_{GS}=-4.5V, I_D=-4A$	-	-	42	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-6A$	-	10	-	S
I_{DSS}	Drain-Source Leakage Current ($T=25^\circ\text{C}$)	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T=70^\circ\text{C}$)	$V_{DS}=-32V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-6A$	-	20	32	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-32V$	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	10	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-20V$	-	11	-	ns
t_r	Rise Time	$I_D=-1A$	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-10V$	-	67	-	ns
t_f	Fall Time	$R_D=20\Omega$	-	43	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1440	2300	pF
C_{oss}	Output Capacitance	$V_{DS}=-25V$	-	250	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	190	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-1.7A, V_{GS}=0V$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=-6A, V_{GS}=0V$	-	27	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	23	-	nC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board ; 135°C/W when mounted on min. copper pad.

N-channel

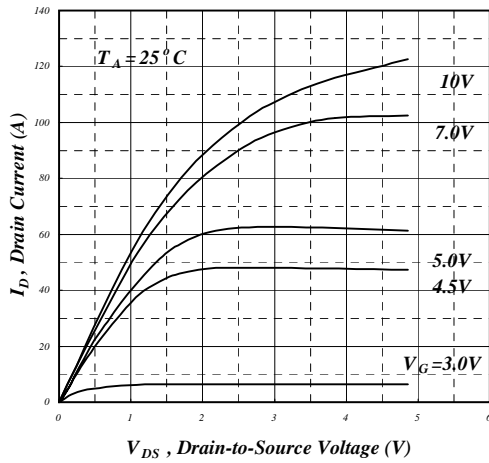


Fig 1. Typical Output Characteristics

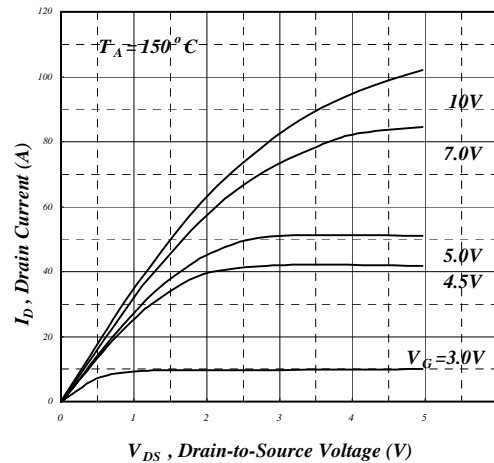


Fig 2. Typical Output Characteristics

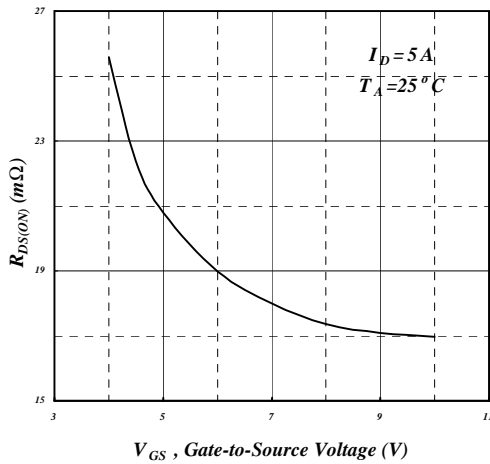


Fig 3. On-Resistance vs. Gate Voltage

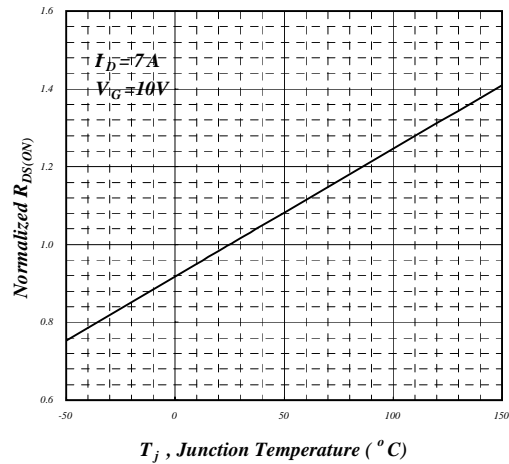


Fig 4. Normalized On-Resistance vs. Junction Temperature

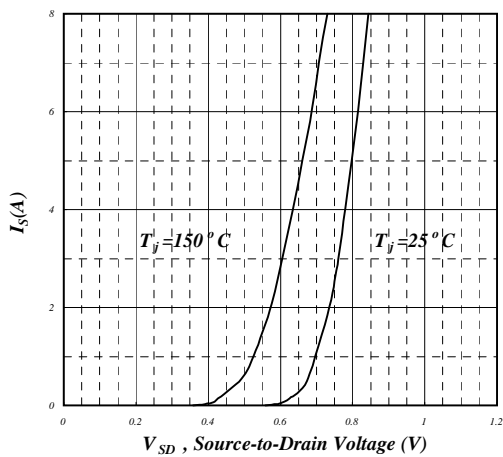


Fig 5. Forward Characteristic of Reverse Diode

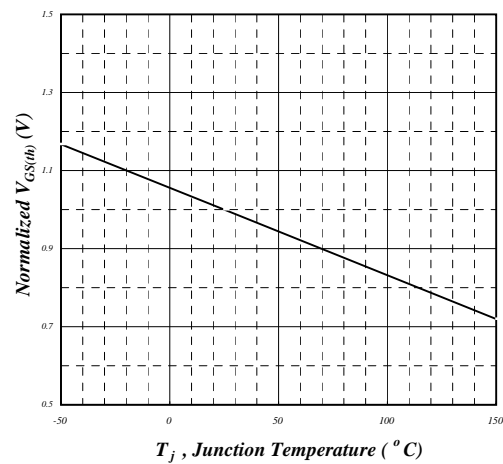


Fig 6. Gate Threshold Voltage vs. Junction Temperature

N-channel

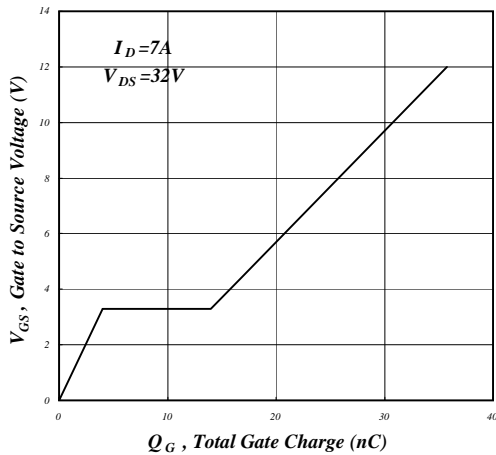


Fig 7. Gate Charge Characteristics

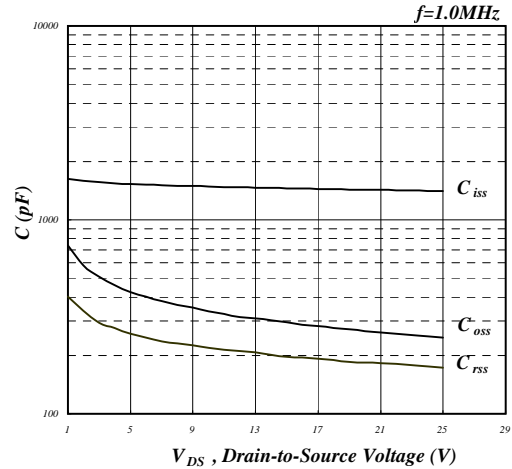


Fig 8. Typical Capacitance Characteristics

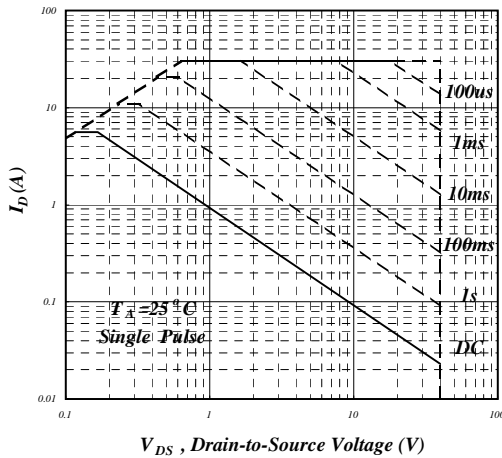


Fig 9. Maximum Safe Operating Area

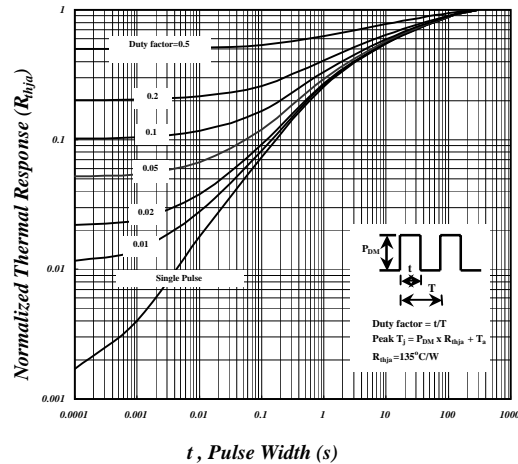


Fig 10. Effective Transient Thermal Impedance

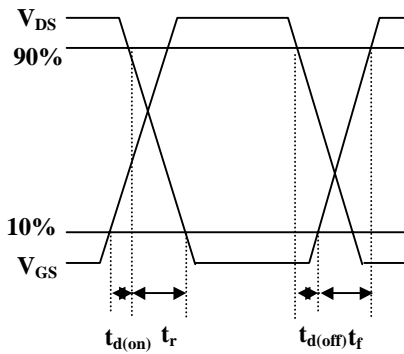


Fig 11. Switching Time Waveform

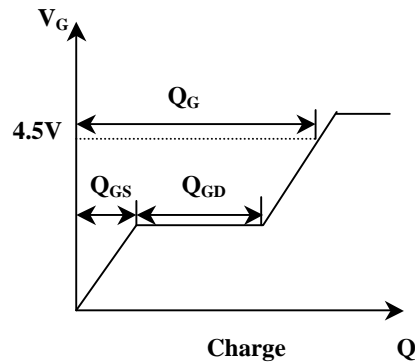


Fig 12. Gate Charge Waveform

P-channel

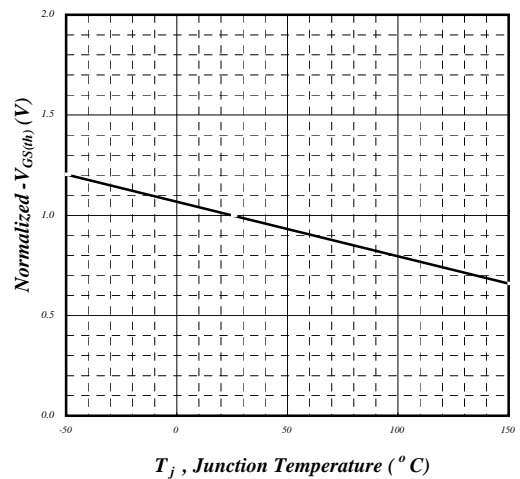
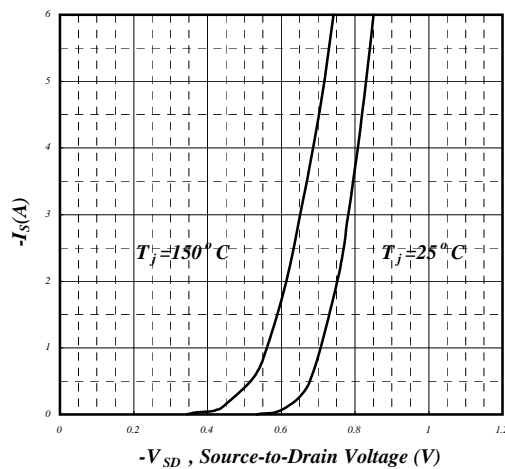
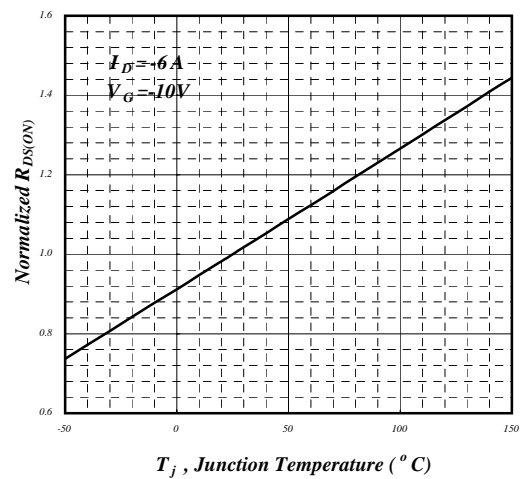
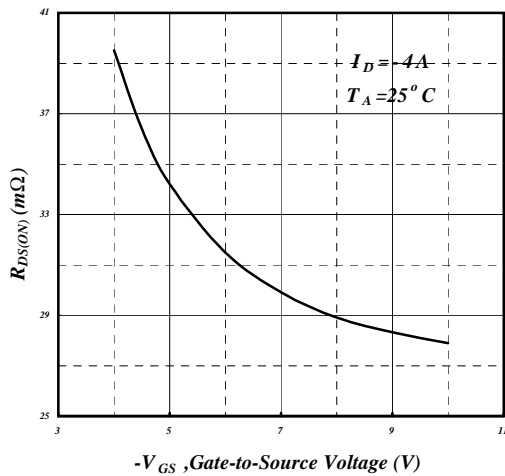
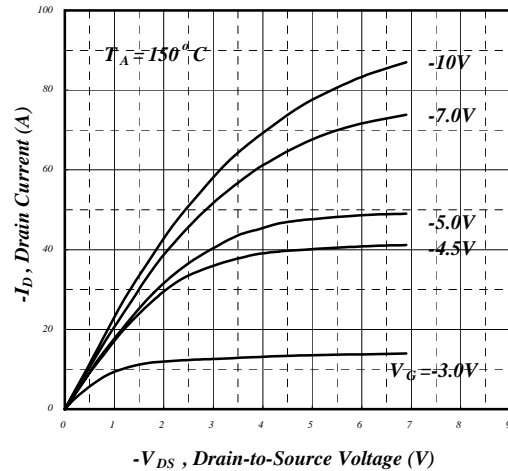
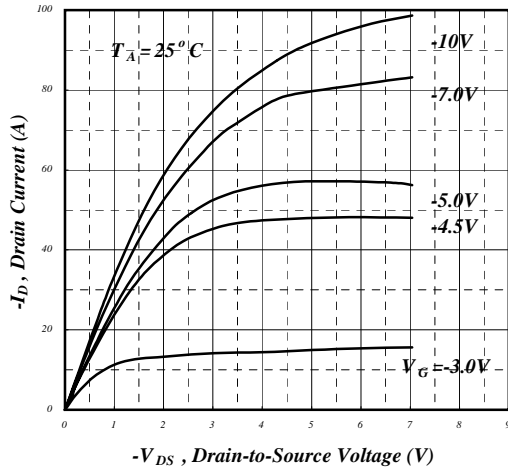


Fig 5. Forward Characteristic of Reverse Diode

Fig 6. Gate Threshold Voltage vs. Junction Temperature

P-channel

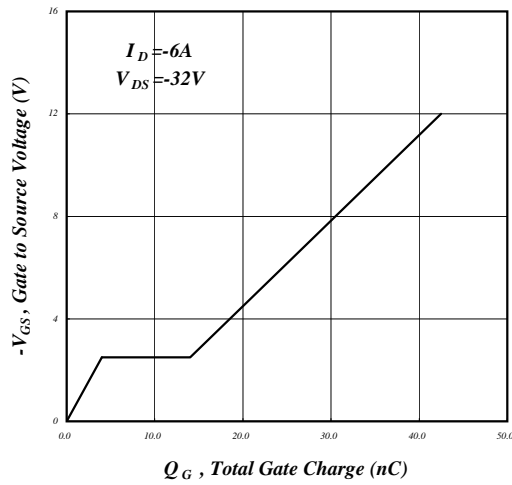


Fig 7. Gate Charge Characteristics

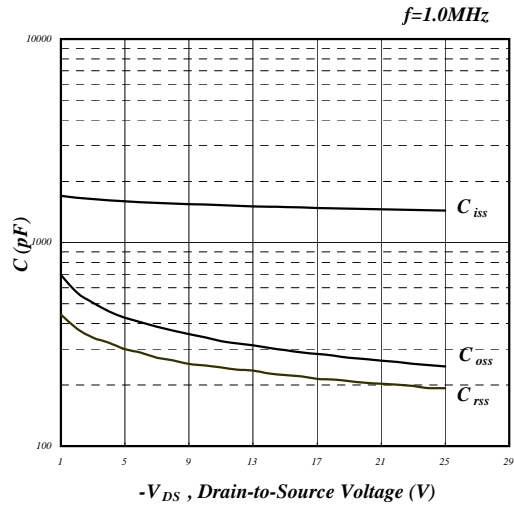


Fig 8. Typical Capacitance Characteristics

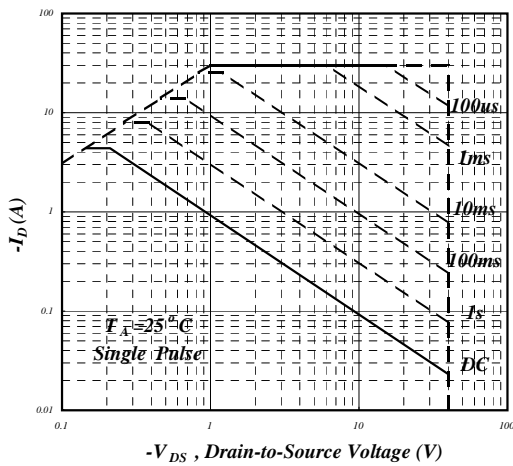


Fig 9. Maximum Safe Operating Area

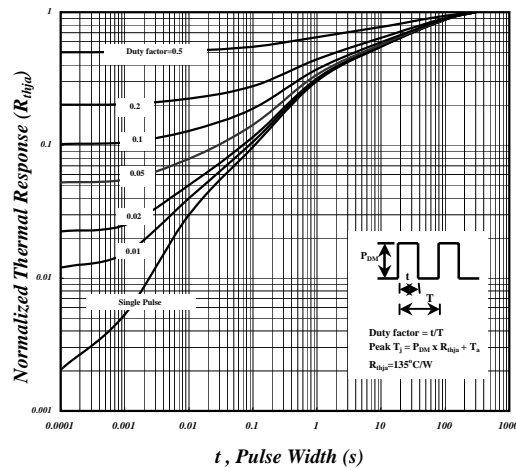


Fig 10. Effective Transient Thermal Impedance

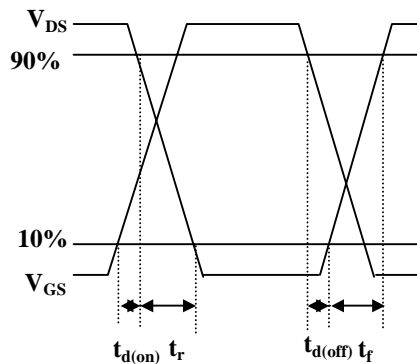


Fig 11. Switching Time Waveform

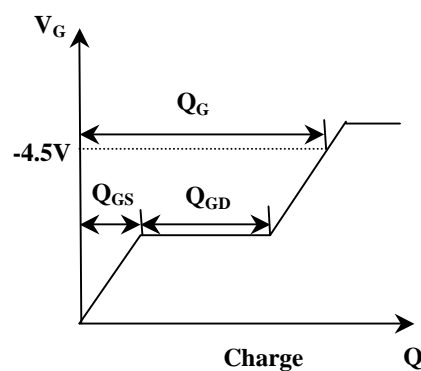


Fig 12. Gate Charge Waveform

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