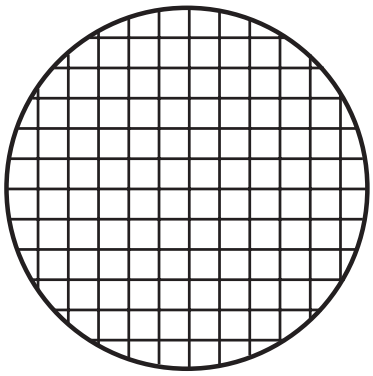
M65KA128AE

128Mbit (4 Banks x 2M x 16) 1.8 V Supply, Low Power SDRAM

Features summary

- 128Mbit Synchronous Dynamic RAM
  - Organized as 4 Banks of 2MWords, each 16 bits wide
- Synchronous Burst Read and Write
  - Fixed Burst Lengths: 1, 2, 4, 8 Words or Full Page
  - Burst Types: Sequential and Interleaved.
  - Maximum Clock frequency: 133MHz
  - Clock Valid to Output Delay ($\overline{CAS}$ Latency): 3 at maximum clock frequency
  - Burst Control by Burst Stop and Precharge Command
- Supply Voltage
  - $V_{DD} = V_{DDQ} = 1.7$ to 1.95V
- Automatic and controlled Precharge
- Byte control by LDQM and UDQM
- Low-power features:
  - Partial Array Self Refresh (PASR),
  - Automatic Temperature Compensated Self Refresh (TCSR)
  - Driver Strength (DS)
  - Deep Power-Down Mode
- Auto Refresh and Self Refresh
- LVCMOS Interface compatible with multiplexed addressing
- Operating temperature range
  - – 25 to 90°C



Wafer

M65KA128AE IS ONLY AVAILABLE AS PART OF A MULTIPLE MEMORY PRODUCT

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1 Summary description

The M65KA128AE is a 128Mbit Low Power Synchronous DRAM (SDRAM). The memory array is organized as 4 Banks of 2,097,152 Words of 16 bits each.

The LPSDRAM achieves low power consumption and high-speed data transfer using the pipeline architecture.

It is well suited for handheld battery powered applications like PDAs, 2.5 and 3G mobile phones and handheld computers.

The device architecture is illustrated in *Figure 2: Functional Block Diagram*. It uses Burst mode to read and write data. It is capable of one, two, four, eight-Word and full-page, sequential and interleaved Burst.

To minimize current consumption during self-refresh operations, the M65KA128AE includes three mechanisms configured via the Extended Mode Register:

- Automatic Temperature Compensated Self Refresh (ATCSR) used to adapt the refresh time according to the operating temperature (see *Table 5: Extended Mode Register Definition*)
- Partial Array Self Refresh (PASR) performs a limited refresh of part of the PSRAM memory array. This area can be configured to half bank, a quarter of bank, one bank, two banks or all banks. This mechanism allows to reduce the device Standby current by refreshing only the part of the memory array that contains essential data.
- The Deep Power-Down (DPD) mode completely halts the refresh operation and achieves minimum current consumption by cutting off the supply voltage from the whole memory array.

The device is programmable through two registers, the Mode Register and the Extended Mode Register:

- The Mode Register is used to select the $\overline{\text{CAS}}$ Latency, the Burst Type (sequential, interleaved) and the Burst Length (1-, 2-, 4-, 8-Word width or full page) through programming the A6 to A4 bits, the A3 bit and the A2 to A0 bits, respectively (see *Table 4*).
- The Extended Mode Register is used to program the low-power features (PASR, ATCSR) and Driver Strength) to reduce the current consumption during the Self Refresh operations. For more details, refer to *Table 5: Extended Mode Register Definition*, and to *Section 4.2: Extended Mode Register Set command*.

Figure 1. Logic Diagram

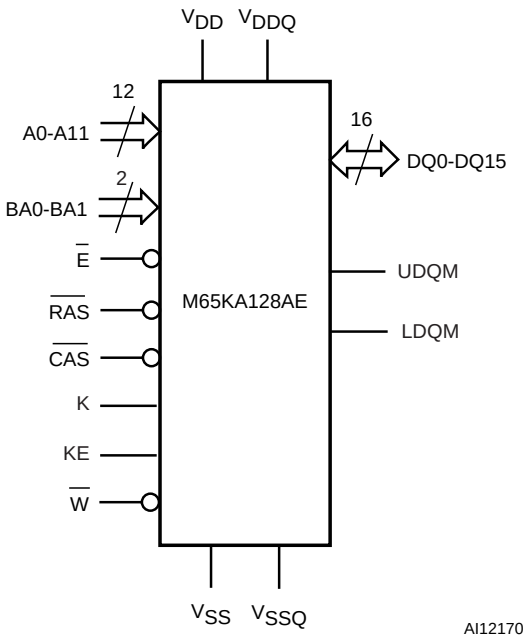
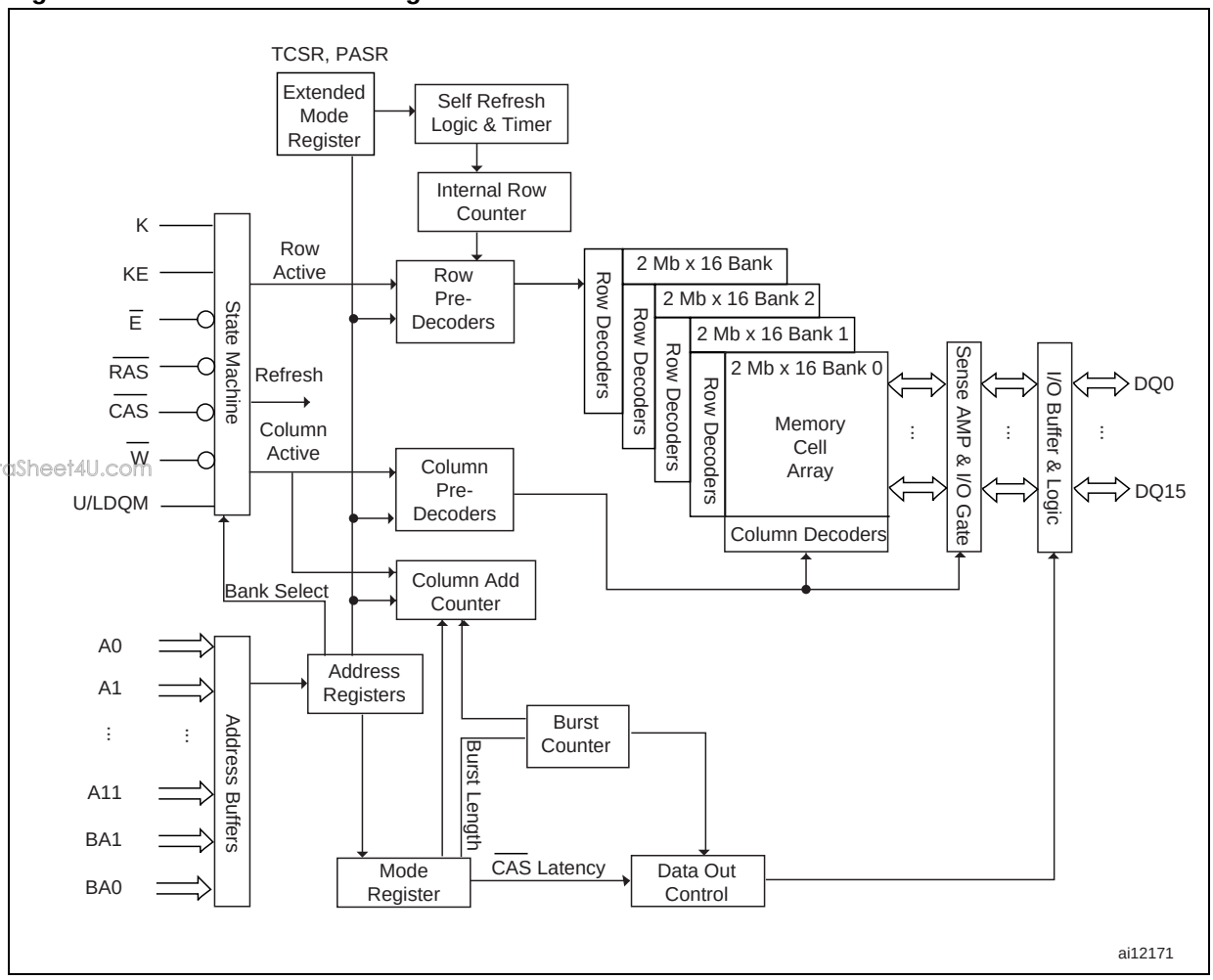


Table 1. Signal Names

A0-A11	Address Inputs
BA0-BA1	Bank Select Inputs
DQ0-DQ15	Data Inputs/Outputs
K	Clock Input
KE	Clock Enable Input
$\overline{E}$	Chip Select Input
$\overline{W}$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
UDQM	Upper Data Input/Output Mask
LDQM	Lower Data Input/Output Mask
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground

Figure 2. Functional Block Diagram



2 Signal descriptions

See *Figure 1: Logic Diagram*, and *Table 1: Signal Names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A11)

The A0-A11 Address Inputs are used to select the row or column to be made active. If a row is selected, all thirteen, A0-A11 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used. If A10 is High (set to '1') during Read or Write, the Read or Write operation includes an Auto Precharge cycle. If A10 is Low (set to '0') during Read or Write, the Read or Write cycle does not include an Auto Precharge cycle.

2.2 Bank Select Address Inputs (BA0-BA1)

The BA0 and BA1 Banks Select Address Inputs select the bank to be made active.

The device must be enabled, the Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}$, and $\overline{W}$ must be High, V_{IH}, when selecting the addresses. The address inputs are latched on the rising edge of the clock signal, K.

2.3 Data Inputs/Outputs (DQ0-DQ15)

The Data Inputs/Outputs output the data stored at the selected address during a Read operation, or are used to input the data during a write operation.

2.4 Chip Select ($\overline{E}$)

The Chip Select input $\overline{E}$ activates the memory state machine, address buffers and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.5 Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a Read or Write.

2.6 Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing.

2.8 Clock Input (K)

The Clock signal, K, is used to clock the Read and Write cycles. During normal operation, the Clock Enable pin, KE, is High, V_{IH}. The clock signal K can be suspended to switch the device to the Self-Refresh, Power-Down or Deep Power-Down mode by driving KE Low, V_{IL}.

2.9 Clock Enable (KE)

The Clock Enable, KE, pin is used to control the synchronizing of the signals with Clock signal K. If KE is High, V_{IH}, the next Clock rising edge is valid. When KE is Low, V_{IL}, the signals are no longer clocked and data Read and Write cycles are extended. KE is also involved in switching the device to the Self-Refresh, Power-Down and Deep Power-Down modes.

2.10 Lower/Upper Data Input/Output Mask (LDQM, UDQM)

Lower Data Input/Output Mask and Upper Data Input/Output Mask pins are input signals used to mask the Read or Write data. The DQM latency is two clock cycles for read operations and there is no latency for write operations.

2.11 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read and Write).

2.12 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid certain conditions that would result in data corruption.

2.13 V_{SS} Ground

Ground, $V_{SS,}$ is the reference for the core power supply. It must be connected to the system ground.

2.14 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package).

3 Operations

There are 7 operating modes that control the memory. Each of these is described in this section, see *Table 2: Operating Modes*, for a summary.

3.1 Power-Up

The Low-Power SDRAM has to be powered up and initialized in a well determined manner. Power must be applied to V_{DD} and V_{DDQ} simultaneously and, at the same time, the clock signal must be started. After Power-Up, a minimum initial pause of 200µs is required. From power-up until the Precharge command is issued, the KE and DQM signals must be held High.

The Precharge command must then be issued to all banks, and 2 or more Auto Refresh cycles must be executed after the precharge is completed and the minimum t_{RP} is satisfied. Once these cycles are completed, a Mode Register Set command must be issued to program the specific operation mode ($\overline{CAS}$ Latency, Burst Length, etc.). After issuing the Mode Register Set command, the device will not accept any other command for t_{RSC}. An Extended Mode Register Set command must also be issued to program the Self Refresh operation mode (PASR and DS). After issuing the Extended Mode Register Set command the device will not accept any other command for t_{RSC}.

The Auto refresh, mode register programming and extended mode register programming can be performed in a random sequence.

CKE and DQM must be held high until the Precharge command is issued to ensure the data bus High-Z level.

The device is now ready for normal operation.

Refer to *Figure 22* for a detailed description of the Power-Up AC waveforms.

3.2 Burst Read

The Read command is used to switch the device to Burst Read mode (see *Section 4.5: Read command* for details). In Burst Read mode the data is output in bursts synchronized with the clock. A valid Burst Read operation is initiated by driving $\overline{E}$ and $\overline{CAS}$ Low, V_{IL}, and $\overline{W}$ and $\overline{RAS}$ High, V_{IH}, at the positive edge of the clock signal, K.

Burst Read can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to '1') when the Burst Read command is issued, the Burst Read operation will be followed by an Auto Precharge cycle. If A10 is Low (set to '0'), the row will remain active for subsequent accesses.

BA1 and BA0 are used to select the bank, and the A8-A0 address inputs are used to select the starting column location. During a Burst Read operation, the memory reads data from the activated bank. The Burst Length (1, 2, 4, 8 Words or full page), Burst Type (sequential or interleaved), and $\overline{CAS}$ Latency depend on the values programmed by issuing a Mode Register Set command (see *Section 5.1: Mode Register description*).

After a Burst Read operation is completed, data outputs become High-Z.

Refer to *Figure 6*, *Figure 7*, *Figure 8*, *Figure 9*, *Figure 10*, *Figure 11* and *Figure 12* for a detailed description of Burst Read AC waveforms.

3.3 Burst Write

The Write command is used to switch the device to Burst Write mode (see *Section 4.4: Write command* for details). In Burst Write mode the data is input in bursts synchronized with the clock. A valid Burst Write initiated by driving $\overline{E}$, $\overline{CAS}$ and $\overline{W}$ Low, V_{IL}, and $\overline{RAS}$ High, V_{IH}, at the positive edge of the clock signal, K.

Burst Write can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to '1') when the Write command is issued, the Write operation will be followed by an Auto Precharge cycle. If A10 is Low (set to '0'), Auto Precharge is not selected and the row will remain active for subsequent accesses.

BA1 and BA0 are used to select the bank, and the A8-A0 address inputs are used to select the starting column location. During Burst Write operation, the memory writes data to the activated bank. As for Burst Read, different Burst Types and Lengths can be utilized, programmed in the same fashion.

Refer to *Figure 13*, *Figure 14*, *Figure 16*, *Figure 17*, *Figure 18*, *Figure 19* and *Figure 20* for a detailed description of Burst Write AC waveforms.

3.4 Self Refresh

In Self Refresh mode, the data contained in the Low-Power SDRAM memory array is retained and refreshed. The Low-Power SDRAM refresh cycles are asynchronous.

All banks must be precharged prior to executing a Self-Refresh operation. The Self-Refresh mode is entered by driving KE Low (set to '0'), with $\overline{E}$, $\overline{RAS}$, and $\overline{CAS}$ Low, and $\overline{W}$ High (set to '1'). When in this mode, the device is not clocked any more.

The Self Refresh mode is exited by driving KE from Low to High, with $\overline{E}$ High, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

The Self Refresh operation is performed according to the settings of Extended Mode Register bits EMR0 to EMR2. They configure the amount of the memory to be refreshed (Partial Array Self Refresh).

3.5 Auto Refresh

The Auto Refresh mode is used to refresh the Low-Power SDRAM in normal operation mode whenever needed.

All banks must be precharged prior to executing an Auto Refresh operation.

During the Auto Refresh, KE must be kept High, V_{IH} and the address bits are "Don't Care", because the specific address bits are generated by the internal refresh address counter.

3.6 Power-Down

In Power-Down mode, the current is reduced to the standby current (I_{DD3P}).

All banks must be precharged before entering Power-Down mode. For the memory to enter the Power-Down mode, KE must be held Low (set to '0'), after the Precharge Time t_{RP}, with $\overline{E}$ High (set to '1'), $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

The Power-Down mode is exited by driving KE High, with $\overline{E}$ High, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

3.7 Deep Power-Down

The purpose of this mode is to achieve maximum power reduction by cutting the power supply to the whole memory array. Data is no longer retained when the device enters Deep Power-Down Mode.

All banks must be precharged before entering Deep Power-Down mode. The M65KA128AE enters Deep Power Down Mode by holding $\overline{E}$ and $\overline{W}$ Low with $\overline{RAS}$ and $\overline{CAS}$ High at the rising edge of the clock, K, while driving KE Low (see *Figure 26: Deep Power-Down Entry AC Waveforms*).

The M65KA128AE exits Deep Power-Down mode by asserting KE High. A special sequence is then required before the device can take any new command into account:

1. Maintain No Operation status conditions for a minimum of 200µs,
2. Issue a Precharge command to all banks of the device (see *Section 4.6: Precharge command* for details),
3. Issue a Mode Register Set command to initialize the Mode Register bits,
4. Issue an Extended Mode Register Set command to initialize the Extended Mode Register bits,
5. Issue 2 or more Auto Refresh commands.

The Deep Power-Down mode exit sequence is illustrated in *Figure 27: Deep Power-Down Exit AC Waveforms*.

Note: The 2 Auto Refresh commands can be issued either after or before the configuration of the Mode and Extended Mode Registers.

Table 2. Operating Modes

Operating Mode	$\overline{E}$	$\overline{RAS}$(1)	$\overline{CAS}$(1)	$\overline{W}$(1)	KEn-1	KEn(1)	A10(1)	A9, A11(1)	A0-A8(1)	BA0-BA1(1)	UDQM/ LDQM(1)
Burst Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	Valid	Start Column Address	Bank Select	Valid
Burst Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	Valid	Start Column Address	Bank Select	Valid
Self Refresh	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X	X
Auto Refresh	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X	X
Power-Down with Precharge	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	X			X	X
	V_{IH}	X	X	X							
Deep Power-Down	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X			X	X
Device Deselect	V_{IH}	X	X	X	V_{IH}	X	X	X	X	X	X
No Operation	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X				X

1. X = Don't Care V_{IL} or V_{IH}.

4 Commands

There are 14 basic commands that control the memory. They can be combined to obtain 21 higher level commands shown in *Table 3: Commands*.

4.1 Mode Register Set command

The Mode Register Set command is issued by applying V_{IL} to $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ and by setting BA1 to '0', and BA0 to '0'.

The Mode Register Set command is used to configure the specific mode of operation of the device by programming the Mode Register:

- Burst Length (1, 2, 4, 8, Full Page)
- $\overline{CAS}$ Latency (2, or 3)
- Burst Type (sequential or interleaved).

The Mode Register Set command must be executed after the Power-Up sequence prior to issuing a Bank (Row) Activate command (see *Figure 15: Mode Register Set AC Waveforms*). The execution of a Mode Register Set command will re-program the Mode Register, modifying its contents.

4.2 Extended Mode Register Set command

The Extended Mode Register Set command is issued by applying V_{IL} to $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$, and then by setting BA1 to '1', and BA0 to '0'.

The Extended Mode Register Set command is used to configure the self refresh operation of the device and the driver strength by programming the Extended Mode Register bits:

- Partial arrays to be refreshed (all banks, two banks, one bank),
- Driver strength (full, 1/2 strength, 1/4 strength, 1/8 strength).

The Extended Mode Register bit controlling the Automatic TSCR (A9) should always be cleared to '0' (A9 = '1' is reserved).

The Extended Mode Register Set command must be executed after the Power-Up sequence prior to issuing a Bank (Row) Activate command.

The execution of an Extended Mode Register Set command will re-program the Extended Mode Register, modifying its contents.

4.3 Bank (Row) Activate command

The Bank (Row) Activate command is used to activate a row in a specific bank of the device. This command is initiated by driving $\overline{E}$ and $\overline{RAS}$ Low, $V_{IL,}$ and $\overline{CAS}$ and $\overline{W}$ High, V_{IH}, at the positive edge of the clock signal, K. The value on BA1 and BA0 selects the bank, and the value on A0-A11 selects the row. The selected row remains active for column access until a Precharge command is issued to that bank.

A minimum time of t_{RCD} is required after issuing the Bank (Row) Active command prior to initiating Read and Write operations from and to the activated bank.

4.4 Write command

The Write command is used to switch the Low-Power SDRAM to Burst Write mode (see *Section 3.3: Burst Write* mode).

4.5 Read command

The Read command is used to switch the Low-Power SDRAM to Burst Read mode (see *Section 3.2: Burst Read*).

4.6 Precharge command

The Precharge command is used to close the open row in a particular bank or the open row in all banks. When the precharge command is issued with address A10 driven High, all banks will be precharged. If A10 is driven Low, the open row in a particular bank will be precharged. The bank(s) will be available when the minimum t_{RP} time has elapsed after the precharge command has been issued.

4.7 Auto Precharge command

The Auto Precharge command is used to close the open row in a specific bank after a Read or Write operation. Read or Write with Auto Precharge is initiated if A10 is High, V_{IH}, when a Read (or Write) command is issued.

The t_{RAS} must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

4.8 Burst Stop command

The Burst Stop command is used to stop a Burst operation. A Burst operation can be interrupted by using the Precharge command (see *Section 4.6: Precharge command* for details), or by issuing the Burst Stop command. Issuing the Burst Stop command during a Burst Read or Write cycle will stop the burst while leaving the bank open.

4.9 Data Mask command

The Data Mask command is used to mask Read or Write data. A Data Mask command issued during a Read operation will disable the data outputs, switching them to the high impedance state after a delay of two clock cycles. A Data Mask command issued during a Write operation will disable the data inputs with no delay.

4.10 Clock Suspend command

The Clock Suspend command is used to interrupt the internal clock of the LPSDRAM. The command is controlled by the Clock Enable input, KE, which is kept High, V_{IH}, in normal access mode. The Clock Suspend command is issued by driving KE Low, V_{IL}, thus freezing the internal clock, and extending data Read and Write operations.

4.11 Auto Refresh command

The Auto Refresh command is used to put the device in Auto refresh mode (see *Section 3.5: Auto Refresh* and *Figure 24: Auto Refresh*).

4.12 Self Refresh command

The purpose of the Self Refresh command is used to put the device in Self Refresh mode to retain and refresh the data contained in the Low-Power SDRAM memory array. In Self Refresh mode, the Low-Power SDRAM runs Refresh cycles asynchronously.

The Self Refresh cycle is performed according to the Extended Mode Register bits EMR0 to EMR2 that configure the part of the memory array being refresh (Partial Array Self Refresh).

For more information on how the command is issued, refer to *Figure 25: Self Refresh*.

4.13 Power-Down command

The Power-Down command is used to put the device in Power-Down mode where the operating current is reduced to the Standby current.

All banks must be precharged and a minimum time of t_{RP} must elapse before issuing the Power-Down command.

4.14 Deep Power-Down command

The Deep Power-Down command is used to switch the Low-Power SDRAM to Deep Power-Down Mode. This mode provides maximum power reduction as it cuts the power of the entire memory array of the device. For more information on how the command is issued and its exit sequence, see *Section 3.7: Deep Power-Down*, *Figure 26: Deep Power-Down Entry AC Waveforms*, and *Figure 27: Deep Power-Down Exit AC Waveforms*.

Table 3. Commands

Command	KE_{n-1}	KE_n(1)	$\overline{E}$(1)	$\overline{RAS}$(1)	$\overline{CAS}$(1)	$\overline{W}$(1)	UDQM/ LDQM(1)	DQ0-DQ15(1)	Addr (1)(2)	A10(1)	BA0-BA1(1)
Mode Register Set(3)	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	Op Code		
Extended Mode Register Set(3)	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	Op Code		
Bank (Row) Activate	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	Row Address		V
Read	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	Column	V_{IL}	V
Read with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	Column	V_{IH}	V
Write	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	X	Column	V_{IL}	V
Write with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	X	Column	V_{IH}	V
Precharge All Banks	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{IH}	X
Precharge Selected Bank	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{IL}	V
Burst Stop	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X		X
Clock Suspend Entry	V_{IH}	V_{IL}	X	X	X	X	X	X	X		X
Clock Suspend Exit	V_{IL}	V_{IH}	X	X	X	X	X	X	X		X
Data Mask / Output Enable	V_{IH}	X	X	X	X	X	V_{IL}	Valid	X		X
Data Mask / Output Disable	V_{IH}	X	X	X	X	X	V_{IH}	High-Z	X		X
Auto-Refresh	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X		X
Self-Refresh Entry	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X		X
Self-Refresh Exit(4)	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X	X		X
			V_{IL}	V_{IH}	V_{IH}	V_{IH}	X				
Power-down Entry	V_{IH}	V_{IL}	V_{IH}	X	X	X	X	X	X		X
			V_{IL}	V_{IH}	V_{IH}	V_{IH}	X				
Power-down Exit	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X	X		X
			V_{IL}	V_{IH}	V_{IH}	V_{IH}	X				
Deep Power-down Entry	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X		X
Deep Power-down Exit	V_{IL}	V_{IH}	X	X	X	X	X	X	X		X

1. X = Don't Care (V_{IL} or V_{IH}), V = Valid Data.
2. Addresses A0 to A11 except A10.
3. BA1 and BA0 must both be set to '0' to issue the Mode Register Set Command, and to '1' and '0', respectively, to issue the Extended Mode Register Set Command.
4. The Self-Refresh mode is exited by asynchronously driving KE from Low to High.

5 Register descriptions

5.1 Mode Register description

The Mode Register is used to select the $\overline{CAS}$ Latency (2 or 3), the Burst Type (sequential, interleaved), the Burst Length (1-, 2-, 4-, 8-Word width or full page).

It is loaded by issuing a Mode Register Set command that programs A0 to A11 address bits. The values placed on the address lines are then latched into the Mode Register. BA0-BA1 must be set to '0'.

See *Table 4: Mode Register Definition*, for more details.

5.2 Burst Length bits (MR0 to MR2)

Bits 0 to 2 (MR0 to MR2) of the Mode Register are used to configure the Burst Length. The burst Length is the number of Words that are output or input during a read or a write operation, respectively. It can be set to 1, 2, 4, 8 Words or full page.

5.3 Burst Type bit (MR3)

Bit 3 (MR3) of the Mode Register is used to set the Burst Type. The Burst Type defines the order in which the address locations are accessed during a burst operation. It can be either sequential or interleaved.

The type of application microprocessor must be taken into account when selecting the Burst Type: some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing.

Both Burst Types support burst length of 1, 2, 4 or 8 Words. Full page burst is also available when the sequential burst type is selected.

5.4 $\overline{CAS}$ Latency bits (MR4 to MR6)

The $\overline{CAS}$ latency is the most critical of the Mode Register parameters. It defines the number of clocks cycles between the detection of a Read command to the first data output valid. It can be set to two or three clock cycles.

The value of this parameter is determined by the frequency of the clock and the speed grade of the device.

Table 4. Mode Register Definition

Address Bits	Mode Register Bit	Register Description	Value	Description
A11-A7	-	-	00000	
A6-A4	MR6-MR4	$\overline{CAS}$ Latency Bits	010	2 Clock Cycles
			011	3 Clock Cycles(1)
			Other configurations reserved	
A3	MR3	Burst Type	0	Sequential
			1	Interleaved
A2-A0	MR2-MR0	Burst Length Bit	000	1 Word (A3 is Don't Care)
			001	2 Words (A3 is Don't Care)
			010	4 Words (A3 is Don't Care)
			011	8 Words (A3 is Don't Care)
			111	Full Page if A3 = 0 Reserved if A3 = 1
			Other configurations reserved	
BA1-BA0	-	-	00	

1. At the maximum clock frequency, the $\overline{CAS}$ Latency must be set to 3.

5.5 Extended Mode Register description

The Extended Mode Register is used to configure the low-power self-refresh operation of the device (PASR, DS). It is used to select the area of the memory array refreshed during Partial Array Self Refresh operations, and the driver strength.

It is loaded by issuing a Extended Mode Register Set command that programs A0 to A11 address bits. The values placed on the address lines are then latched into the Extended Mode Register. BA0 and BA1 must be set to '0' and '1' respectively.

See *Table 5: Extended Mode Register Definition*, for more details.

5.5.1 Partial Array Self Refresh bits (EMR0-EMR2)

Bits EMR0 to EMR2 of the Extended Mode Register allow to configure the amount of memory that will be refreshed during a Self Refresh operation (see *Section 3.4: Self Refresh*). It can be set to:

- All Banks (banks 0, 1, 2, and 3)
- Two Banks (banks 0 and 1)
- One Bank (bank 0)

It is important to note that the data stored in the banks or portion of banks which are not refreshed, are lost. As an example, data stored in banks 1, 2 and 3 are lost when the PASR is set to one bank (bank 0 refreshed).

5.5.2 Driver Strength bit (EMR5-EMR6)

Extended Mode Register bits, EMR5 and EMR6, can be used to select the driver strength of data outputs. This value should be set according to the application requirements.

5.5.3 Automatic Temperature Compensated Self Refresh bits(EMR3-EMR4)

The M65KA128AE has a built-in temperature sensor that controls automatically the internal self refresh rate.

Table 5. Extended Mode Register Definition

Address Bits	Mode Register Bit	Description	Value	Description
A11-A10	-	-	00	
A9	EMR9	Automatic Temperature Compensated Self-Refresh (ATCSR)	0	Enabled
			1	Reserved
A8-A7	-	-	00	
A6-A5	EMR6-EMR5	Driver Strength Bits	00	Full Strength
			01	1/2 Strength
			10	1/4 Strength
			11	1/8 Strength
A4-A3	-	-	00	
A2-A0	EMR2-EMR0	Partial Array Self-Refresh Bits	000	All Banks
			001	Two Banks (BA1=0)
			010	One Bank (BA0 and BA1 =0)
			Other configurations reserved	
BA1-BA0	-	-	10	

6 Maximum Rating

Stressing the device above the ratings listed in *Table 6: Absolute Maximum Ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_J	Operating Junction Temperature		– 25	90	°C
T_{STG}	Storage Temperature		– 55	125	°C
V_{IO}	Input or Output Voltage		– 0.5	2.3	V
V_{DD}, V_{DDQ}	Supply Voltage		– 0.5	2.3	V
I_{OS}	Short Circuit Output Current		50		mA
P_D	Power dissipation		1.0		W

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 7: Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Symbol	Parameter(1)(2)		Min	Max	Units
V_{DD}	Supply Voltage		1.7	1.95	V
V_{DDQ}	Input/Output Supply Voltage		1.7	1.95	V
T_J	Operating Junction Temperature		– 25	90	°C
C_L	Load Capacitance		30		pF
t_R, t_F	Input Rise/Fall Time		0.5		ns
V_{IL}	Input Pulses Low Voltage		0.2		V
V_{IH}	Input Pulses High Voltage		1.6		V
V_{REF}	Input and Output Timing Ref. Voltages		0.9		V

1. T_J = 25°C, f = 1MHz
2. All voltages are referenced to V_{SS} = 0V.

Figure 3. AC Measurement I/O Waveform

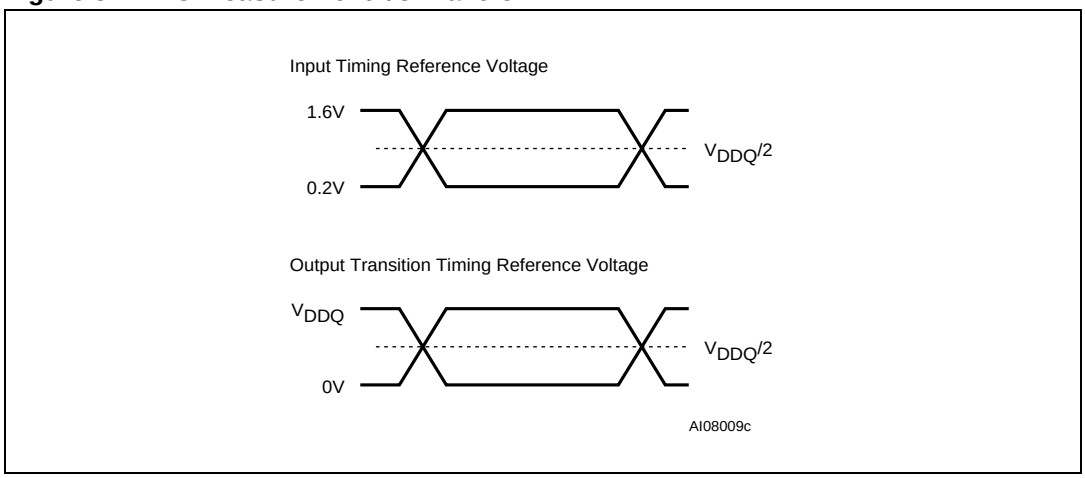


Figure 4. AC Measurement Load Circuit

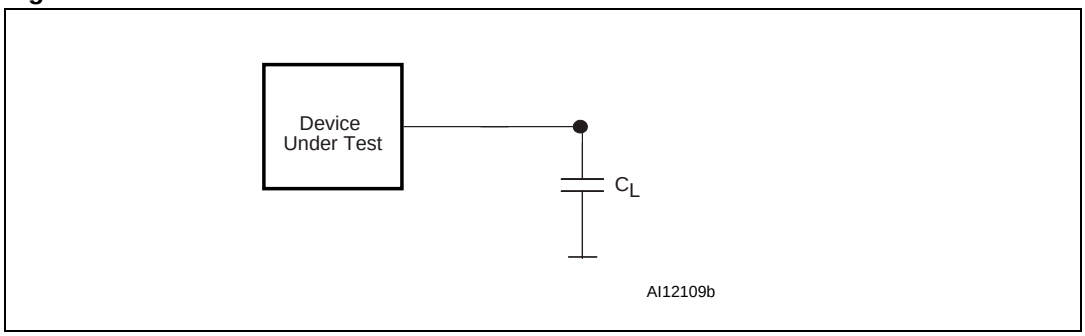


Table 8. Capacitance

Symbol	Parameter	Signal	M65KA128AE(1)		Unit
			Min.	Max.	
CI1	Input Capacitance	K	2.0	4.5	pF
CI2		A0-A11, BA0, BA1, KE, $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, UDQM, LDQM	2.0	4.5	pF
C_{IO}	Data I/O Capacitance	DQ0-DQ15	3.5	6.0	pF

1. T_J = 25°C, f = 1MHz

Table 9. DC Characteristics 1

Symbol	Parameter	Test Condition(1)	M65KA128AE		Unit
			Min.	Max.	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$ (2)	– 2	2	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$	– 1.5	1.5	µA
V_{IL}(2)	Input Low Voltage	V_{IN} = 0V	– 0.3 (3)	0.3	V
V_{IH}(4)	Input High Voltage	V_{IN} = 0V	0.8 V_{DDQ}	V_{DDQ} + 0.3 (5)	V
V_{OL}	Output Low Voltage	I_{OUT} = 100µA V_{IN} = 0V		0.2	V
V_{OH}	Output High Voltage	I_{OUT} = –100µA V_{IN} = 0V	V_{DDQ}– 0.2		V

1. These parameters are measured in the temperature conditions specified in *Table 7*.
2. Data outputs are disabled.
3. V_{IL} (min.) = –0.5V (pulse width ≤ 5ns)
4. V_{DDQ} must not exceed the level of V_{DD}.
5. V_{IH} (max.) = 2.3V (pulse width ≤ 5ns)

Table 10. DC Characteristics 2(1)

Symbol	Parameter		Test Condition(2)	Max.	Unit
I_{DD1} (3)(4)	Operating Current		Burst length = 1, one bank active $t_{RC} \geq t_{RC}(min)$, I_{OL} = 0mA	45	mA
I_{DD2P}	Precharge Standby Current in Power-Down Mode		KE ≤ V_{IL}(max), $t_K = t_{K(min)}$	0.8	mA
I_{DD2PS}			KE ≤ V_{IL}(max), $t_K = \infty$	0.6	
I_{DD2N}	Precharge Standby Current in Non Power-Down Mode		KE ≥ V_{IH} (min), $\overline{E} \geq V_{IH}$ (min), $t_K = t_{K(min)}$, Input signals changed once in 2 clock cycles	4	mA
I_{DD2NS}			KE ≥ V_{IH} (min), $t_K = \infty$ Input signals are stable	2	
I_{DD3P}	Active Standby Current in Power-Down Mode		KE ≤ V_{IL}(max), $t_K = t_{K(min)}$	3.0	mA
I_{DD3PS}			KE ≤ V_{IL}(max), $t_{K(MIN)} = \infty$	1.2	
I_{DD3N}	Active Standby Current in Non Power-Down Mode		KE ≥ V_{IH} (min), $\overline{E} \geq V_{IH}$ (min), $t_K = t_{K(min)}$, Input signals changed once in 2 clock cycles	10	mA
I_{DD3NS}			KE ≥ V_{IH} (min), $t_K = \infty$ Input signals are stable	7	
I_{DD4} (3)(4)	Burst Mode Current	CL = 2	$t_K \geq t_K$ (min), I_{OL} = 0mA All banks active	50	mA
		CL = 3		80	
I_{DD5}(5)	Auto-Refresh Current		$t_{RRC} \geq t_{RRC}$ (min), All banks active	55	mA
I_{DD6}(6)	Self-Refresh Current		KE ≤ 0.2V	See *Table 11*	µA
I_{DD7}	Standby Current in Deep Power-down Mode		KE ≤ 0.2V	10	µA

1. CL stands for $\overline{CAS}$ Latency.
2. These parameters are measured in the temperature conditions specified in *Table 7*.
3. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open. They are measured on condition that the addresses are changed only once during t_{CK}(min.).
4. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open.
5. I_{DD5} is measured on condition that the addresses are changed only once during t_{CK}(min.). The minimum value of t_{RC} (RAS cycle time for Refresh operations) is shown in *Table 13: AC Characteristics 2*.
6. I_{DD6} is measured on condition that the device is in Self Refresh mode long enough after a read and write operations, and the specified T_J is respected.

Table 11. Self-Refresh Current (I_{DD6}) Values in Normal Operating Mode

Temperature (°C)	Memory Array(1)						Unit
	4 Banks		2 Banks		1 Bank		
	Typ	Max	Typ	Max	Typ	Max	
$70 \le T_J \le 90$		250		200		160	µA
$40 \le T_J \le 70$		200		170		150	µA
$-25 \le T_J \le 40$		160		150		140	µA

1. These parameters are measured in the temperature conditions specified in *Table 7*.

Table 12. AC Characteristics 1(1)(2)

Symbol	Alt.	Parameter		Min.	Max.	Unit
t_{CK}	t_{CK}	Clock Cycle Time	CL = 3	7.5		ns
			CL = 2	15		ns
t_{CHW}	t_{CH}	Clock High Pulse Width		2.5	-	ns
t_{CLW}	t_{CL}	Clock Low Pulse Width		2.5	-	ns
t_{AC}	t_{AC}	Access Time From Clock	CL = 3	-	6	ns
			CL = 2	-	8	ns
t_{OH}	t_{OH}	Data-out Hold Time		2.0	-	ns
t_{DS} (3)	t_{DS}	Data-Input Setup Time		1.9	-	ns
t_{DH} (3)	t_{DH}	Data-Input Hold Time		0.9	-	ns
t_{AS}	t_{AS}	Address Setup Time		1.9	-	ns
t_{AH}	t_{AH}	Address Hold Time		0.9	-	ns
t_{CKS}	t_{CKS}	Clock enable Setup Time		1.9	-	ns
t_{CKSP}	t_{CKSP}	Clock Enable Setup Time (Power-Down Exit)		1.9	-	ns
t_{CKH}	t_{CKH}	Clock enable Hold Time		0.9	-	ns
t_{CS}	t_{CMS}	Command Setup Time		1.9	-	ns
t_{CH}	t_{CMH}	Command Hold Time		0.9	-	ns
t_{OLZ}	t_{LZ}	Clock to Data Output in Low-Z Time		0	-	ns
t_{OHZ}	t_{HZ}	Clock to Data Output in High-Z Time	CL = 3	0	6	ns
			CL = 2	0	8	ns

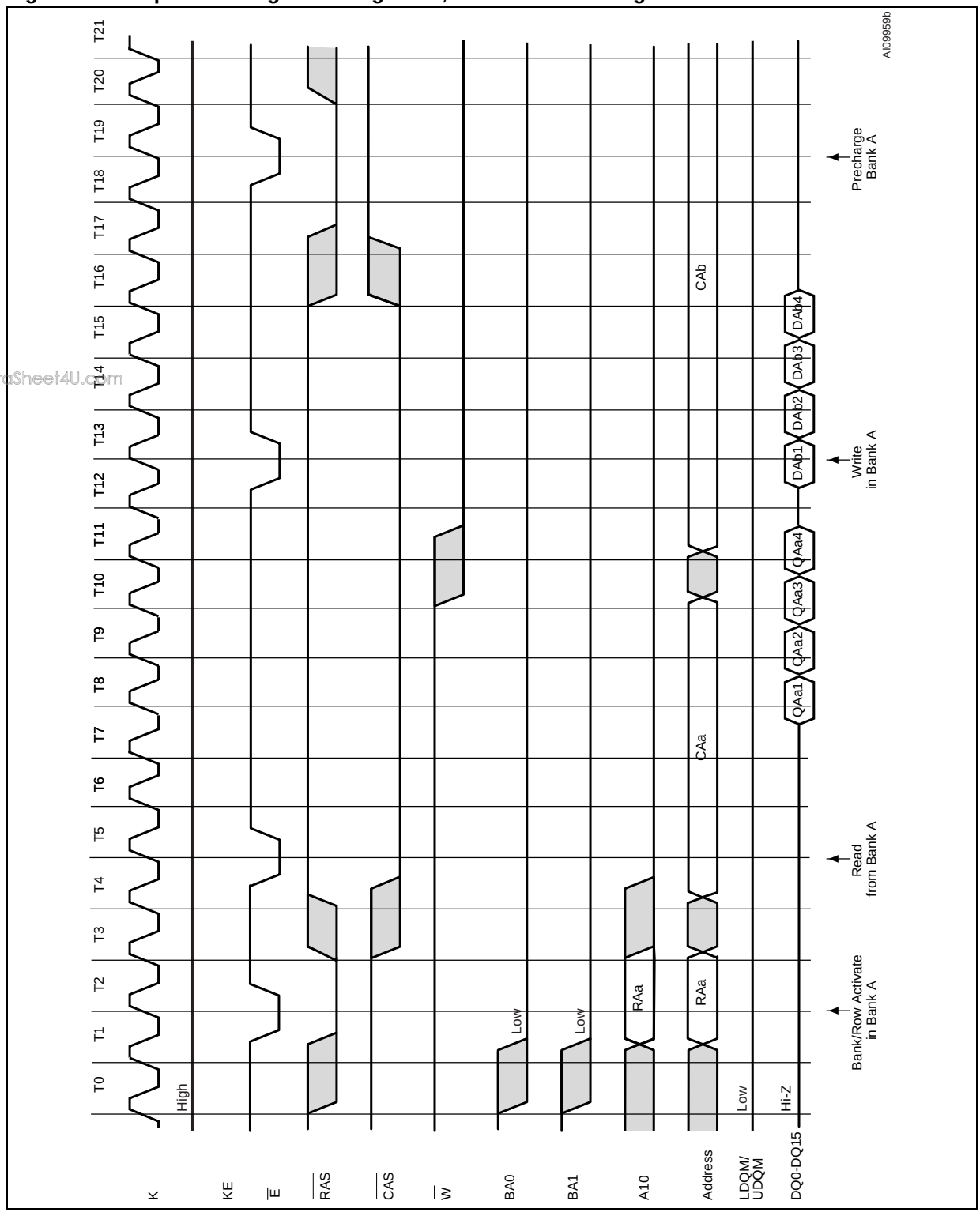
1. These parameters are measured in the Operating and AC Conditions specified in *Table 7*.
2. CL stands for $\overline{CAS}$ Latency.
3. If t_T is greater than 0.5ns (t_T-0.5) or ((t_R+t_F)/2-0.5) should be added

Table 13. AC Characteristics 2(1)(2)

Symbol	Alt.	Parameter		Min.	Max.	Unit
t_{RC}	t_{RC}	$\overline{RAS}$ Cycle Time (normal operation)		75	-	ns
t_{RC1}	t_{RC1}	$\overline{RAS}$ Cycle Time (refresh operation)		105	-	ns
t_{RC2}	t_{RC2}	$\overline{RAS}$ Cycle Time (Self Refresh Exit to Refresh or Bank/Row Activate Command)		120	-	ns
t_{RCD}	t_{RCD}	Delay Time, $\overline{RAS}$ Active to $\overline{CAS}$ Active		30	-	ns
t_{RAS}	t_{RAS}	$\overline{RAS}$ Active Time		52.5	120,000	ns
t_{RP}	t_{RP}	$\overline{RAS}$ Precharge Time		22.5	-	ns
t_{RRD}	t_{RRD}	Delay Time, $\overline{RAS}$ Active to $\overline{RAS}$ Bank Active		2	-	(3)
t_{DPL}	t_{DPL}	Delay Time, Write Command to Data Input		2	-	(3)
t_{DAL}	t_{DAL}	Data Input Valid to Precharge Command	CL = 3	$2t_{CK}+22.5$		ns
			CL = 2			ns
t_{MRD}	t_{RSC}	Mode Register Set Cycle Time		2	-	(3)
t_{REF}	t_{REF}	Refresh Time		-	64	ms
t_T	t_T	Transition Time		0.5	30	ns

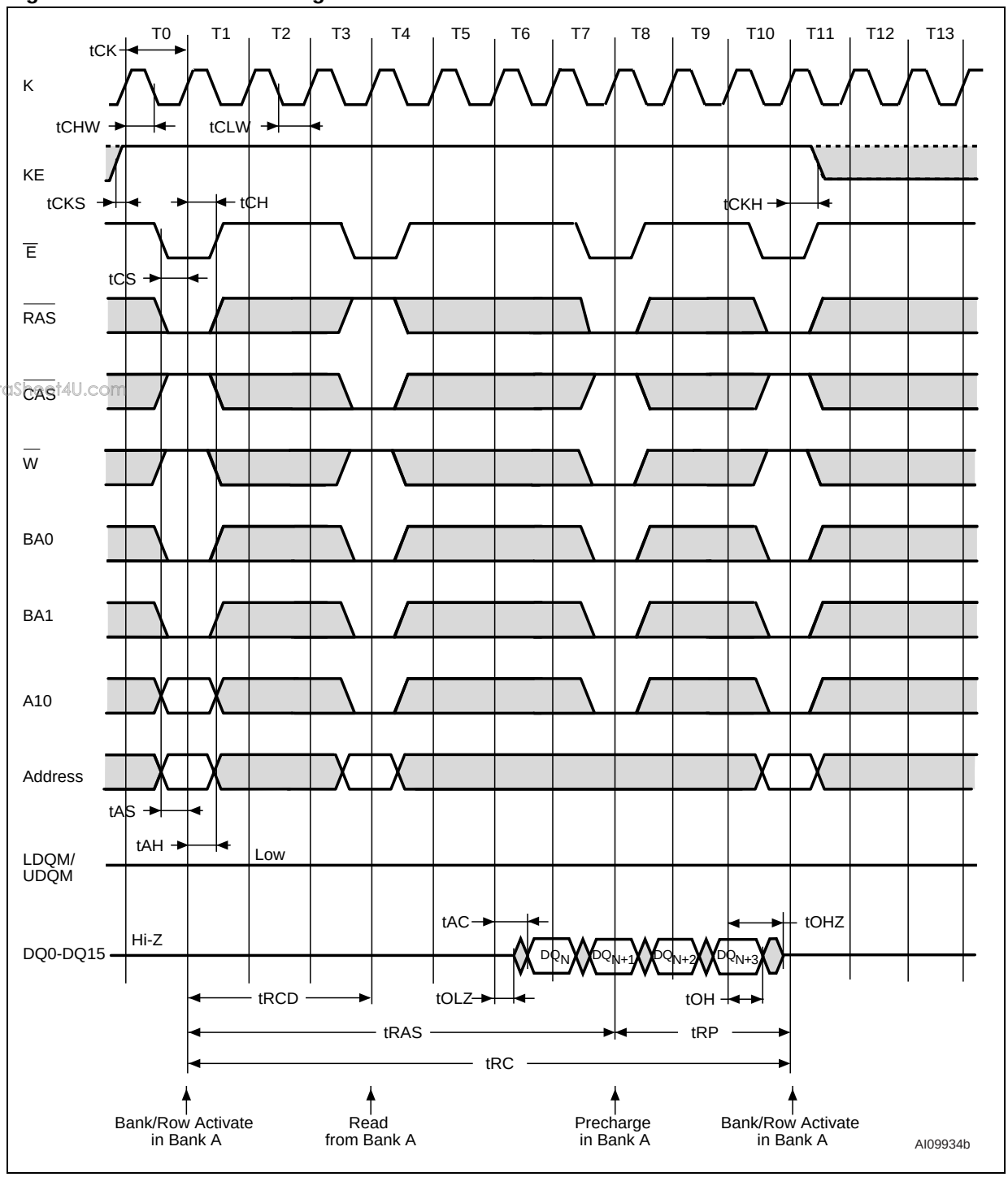
1. These parameters are measured in the Operating and AC Conditions specified in *Table 7*.
2. CL stands for $\overline{CAS}$ Latency.
3. The unit is the system Clock cycle time.

Figure 5. Chip Enable Signal During Read, Write and Precharge



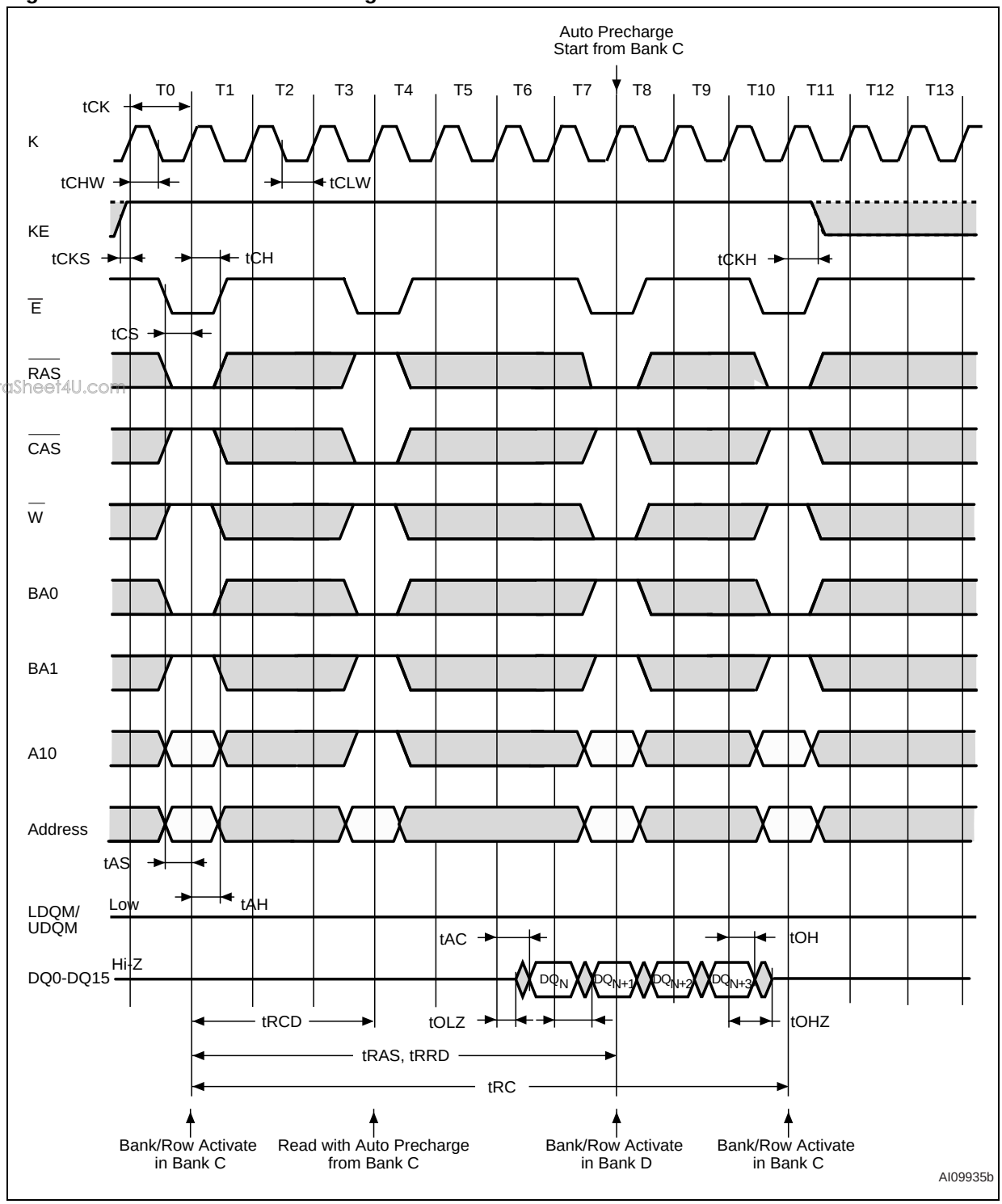
1. The Chip Enable signal, $\overline{E}$, must be issued at a minimum rate with respect to the other signals.
2. Burst Length = 4 Words, Latency = 3 clock cycles.
3. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A, DAan= Data n written to Column a in Bank A.

Figure 6. Read with Precharge AC Waveforms



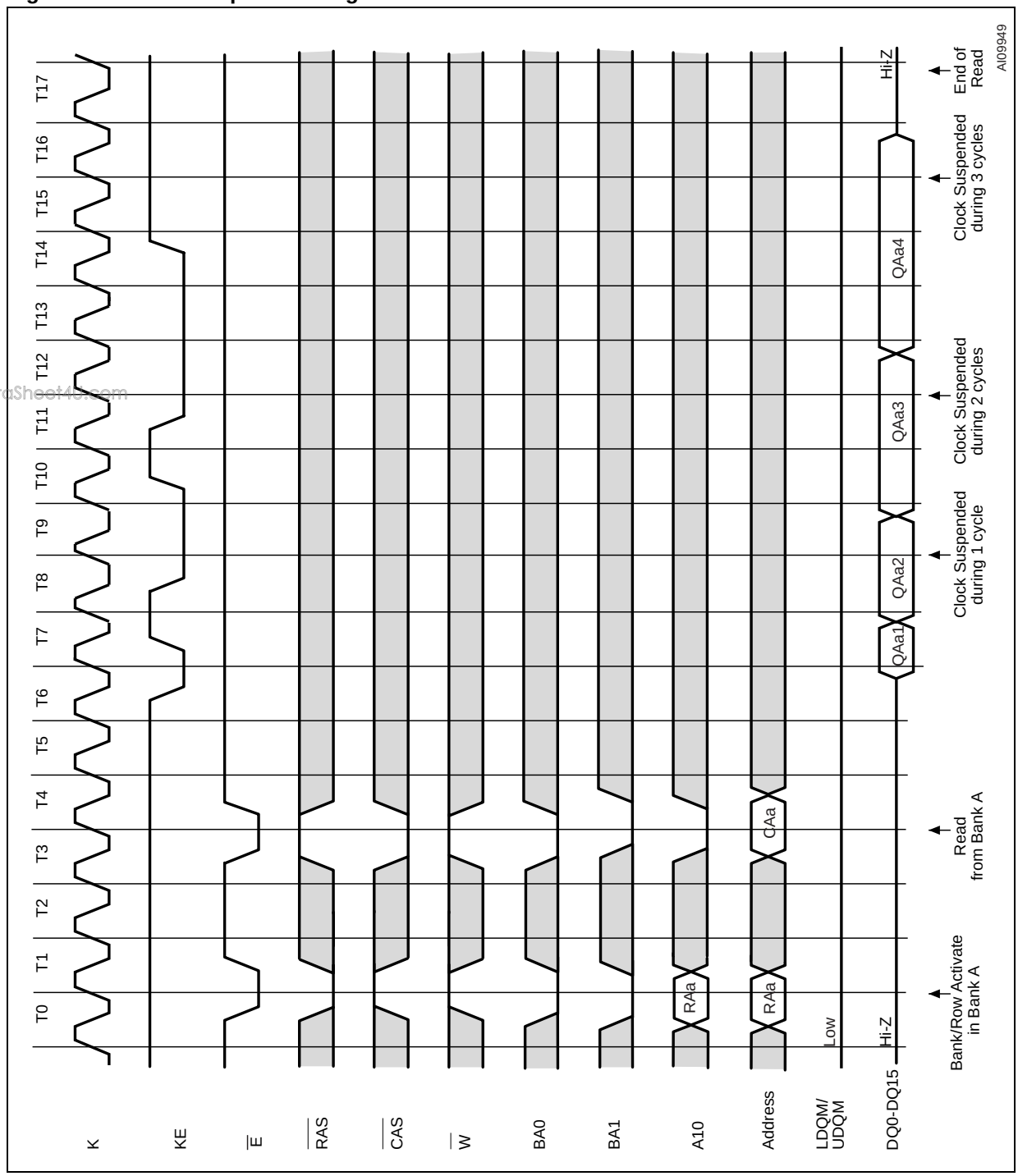
1. Burst Length = 4 Words, Latency = 3 clock cycles.

Figure 7. Read with Auto Precharge AC Waveforms



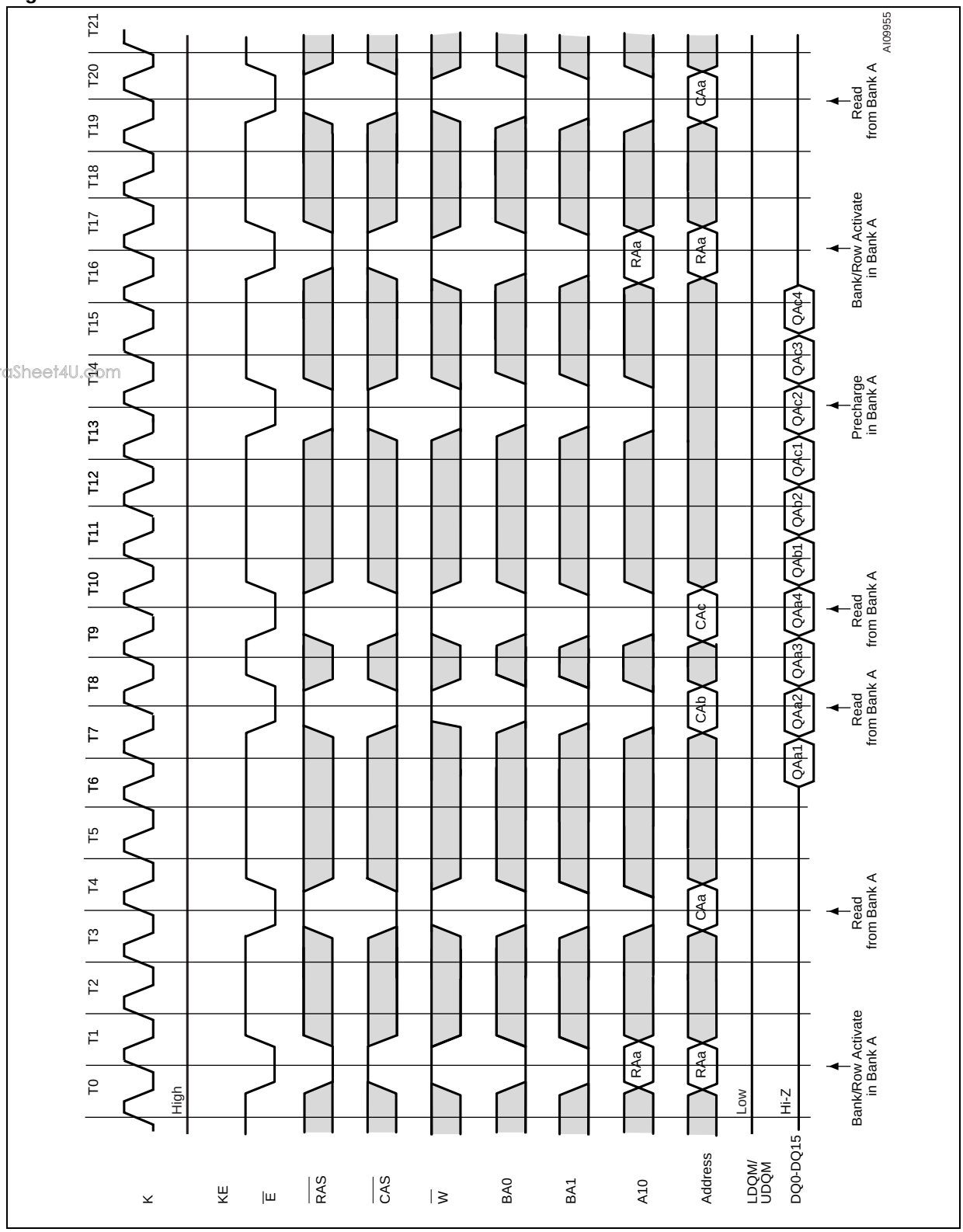
1. Burst Length = 4 Words, Latency = 3 clock cycles.

Figure 8. Clock Suspend During Burst Read AC Waveforms



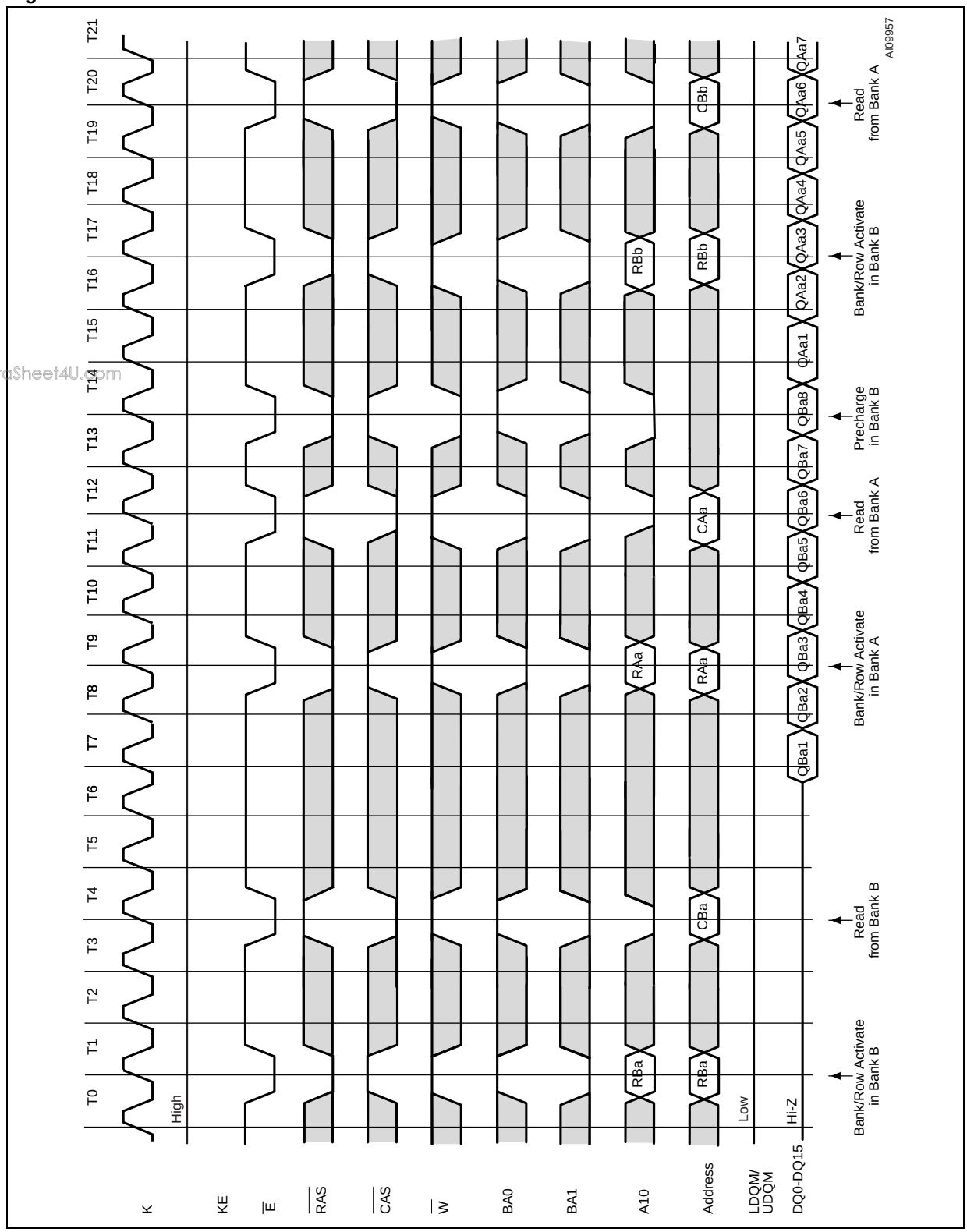
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A.

Figure 9. Random Column Read AC Waveforms



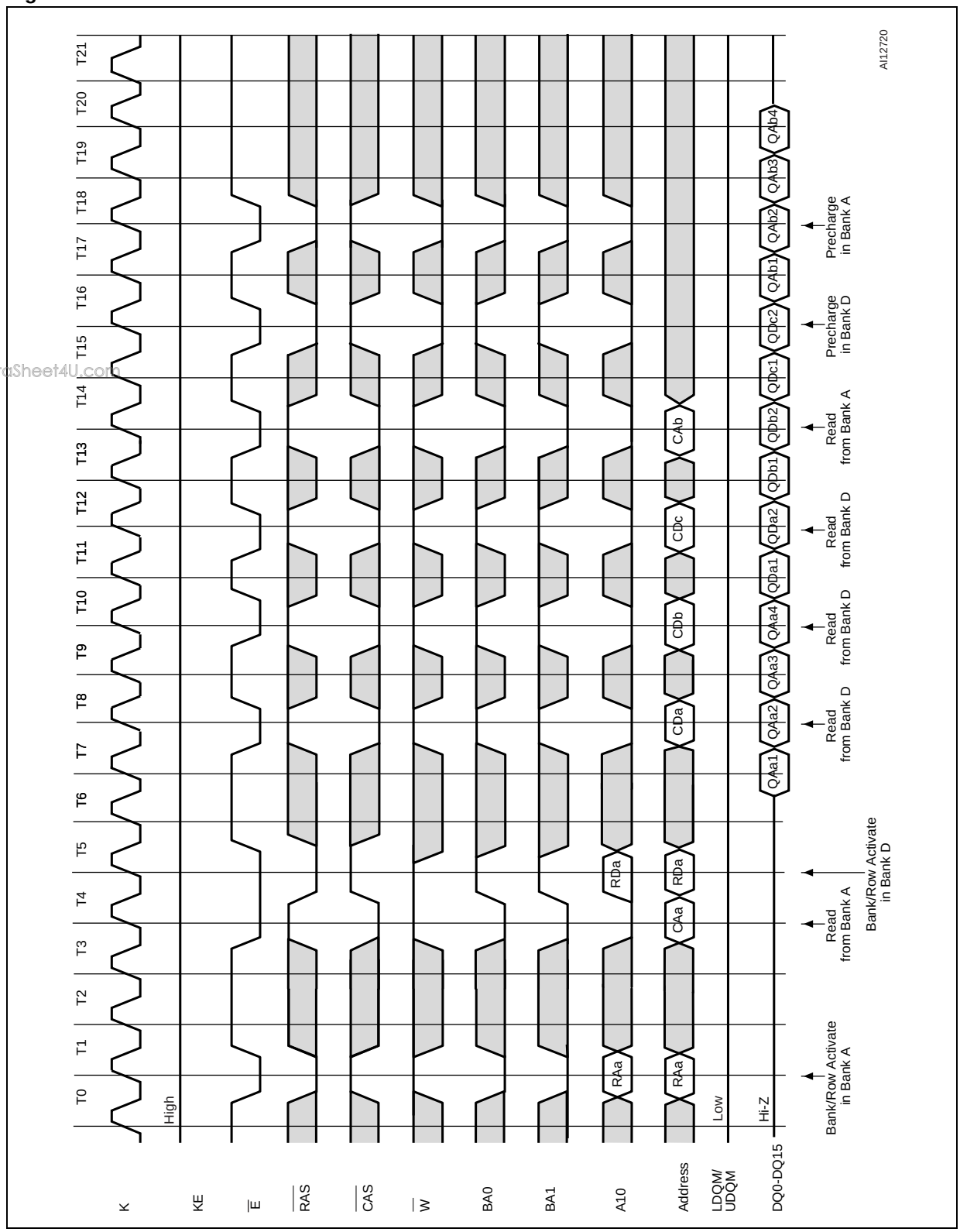
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from Column m in Bank A.

Figure 10. Random Row Read AC Waveforms



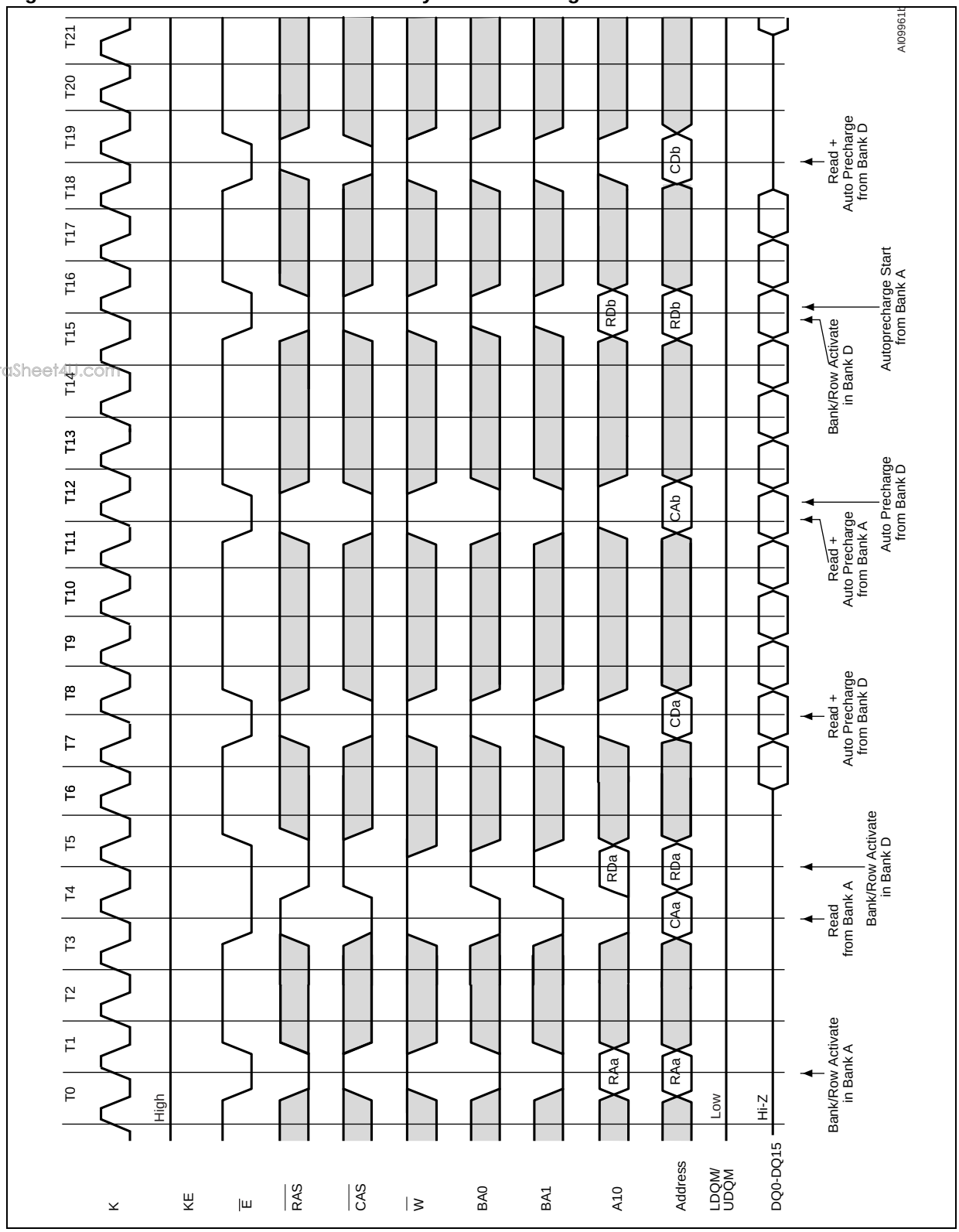
1. Burst Length = 8 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from row m in Bank A.

Figure 11. Column Interleaved Read AC Waveforms



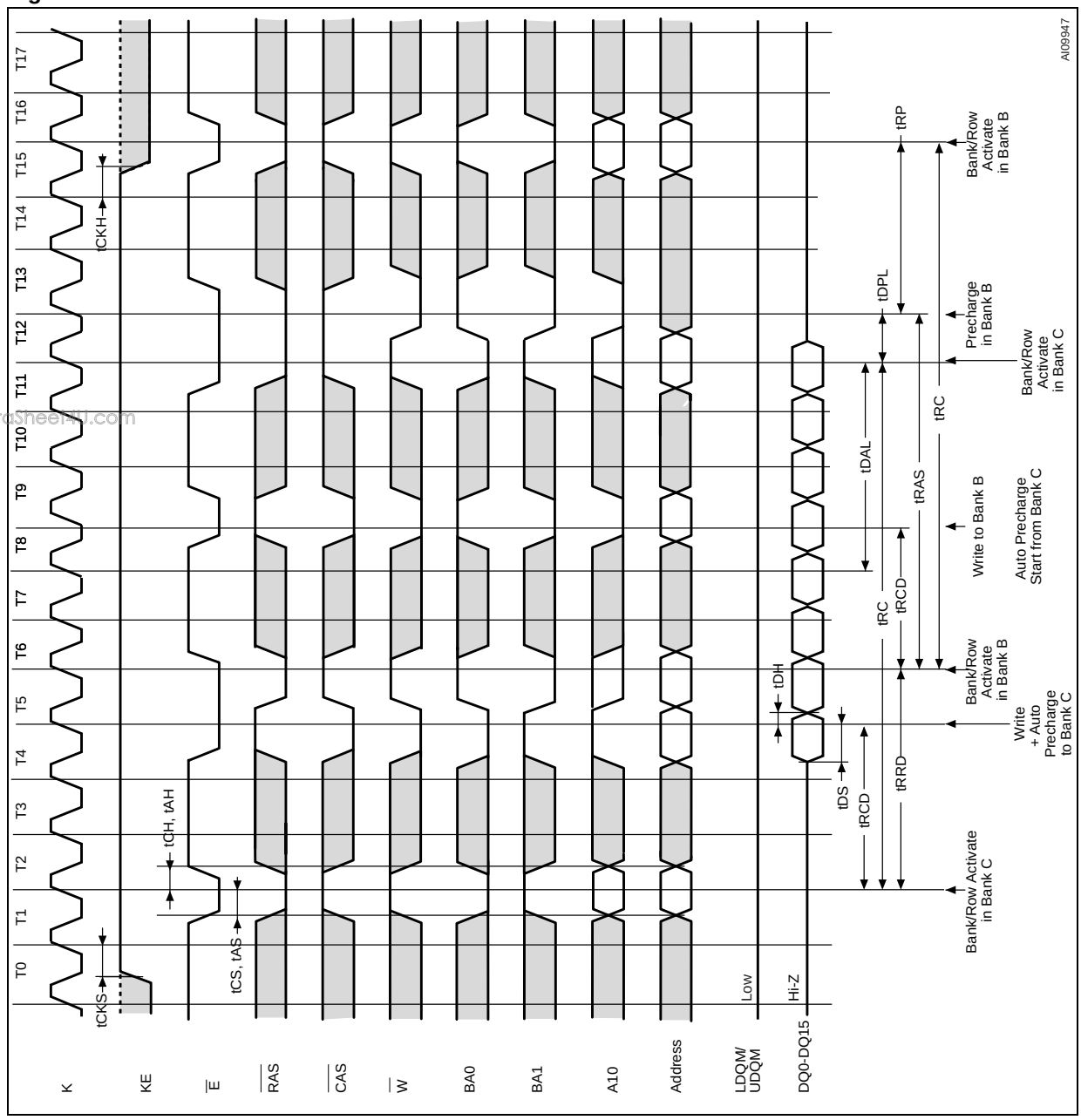
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from Column m in Bank A.

Figure 12. Burst Column Read Followed by Auto Precharge AC Waveforms



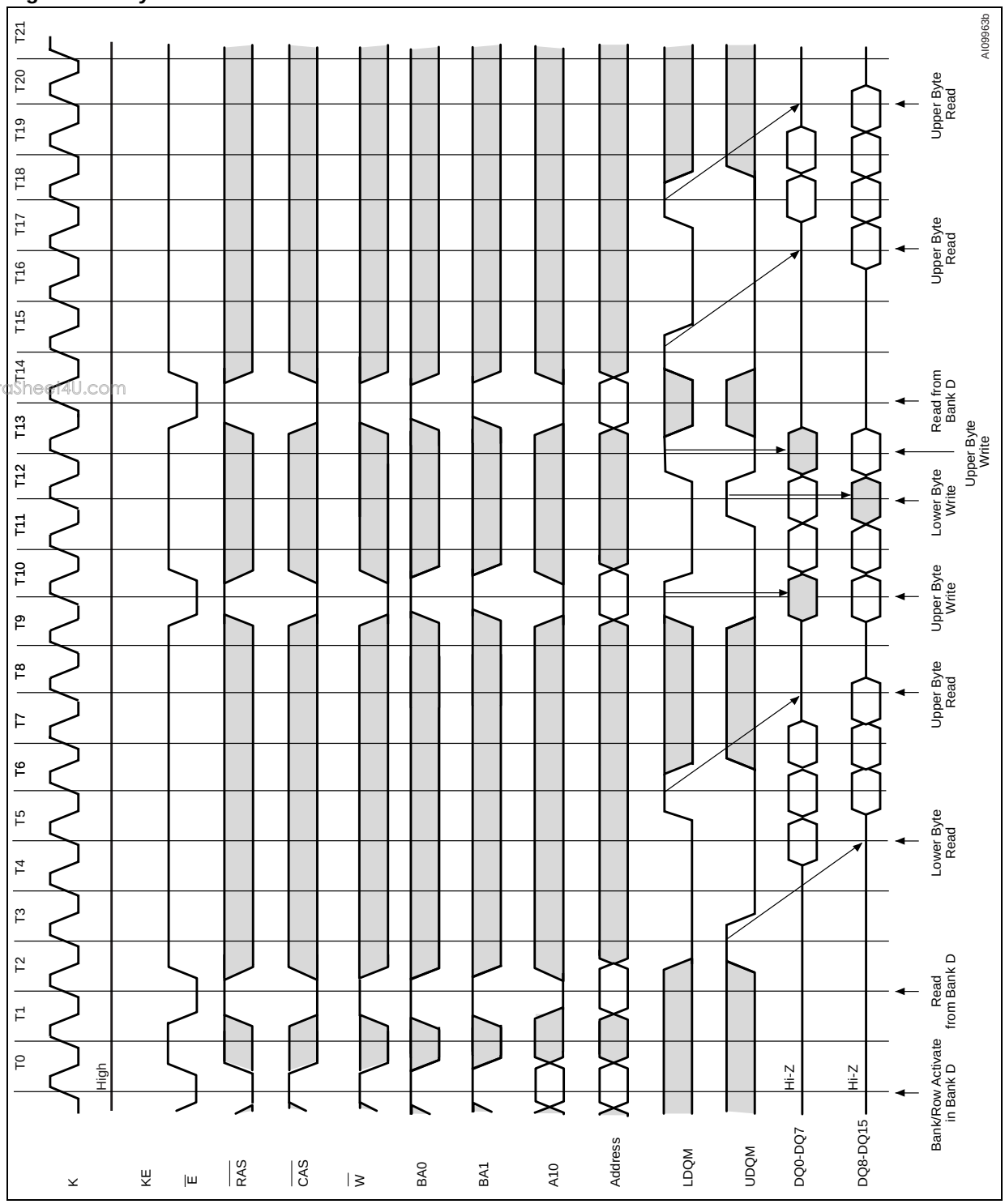
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A.

Figure 13. Write AC Waveforms



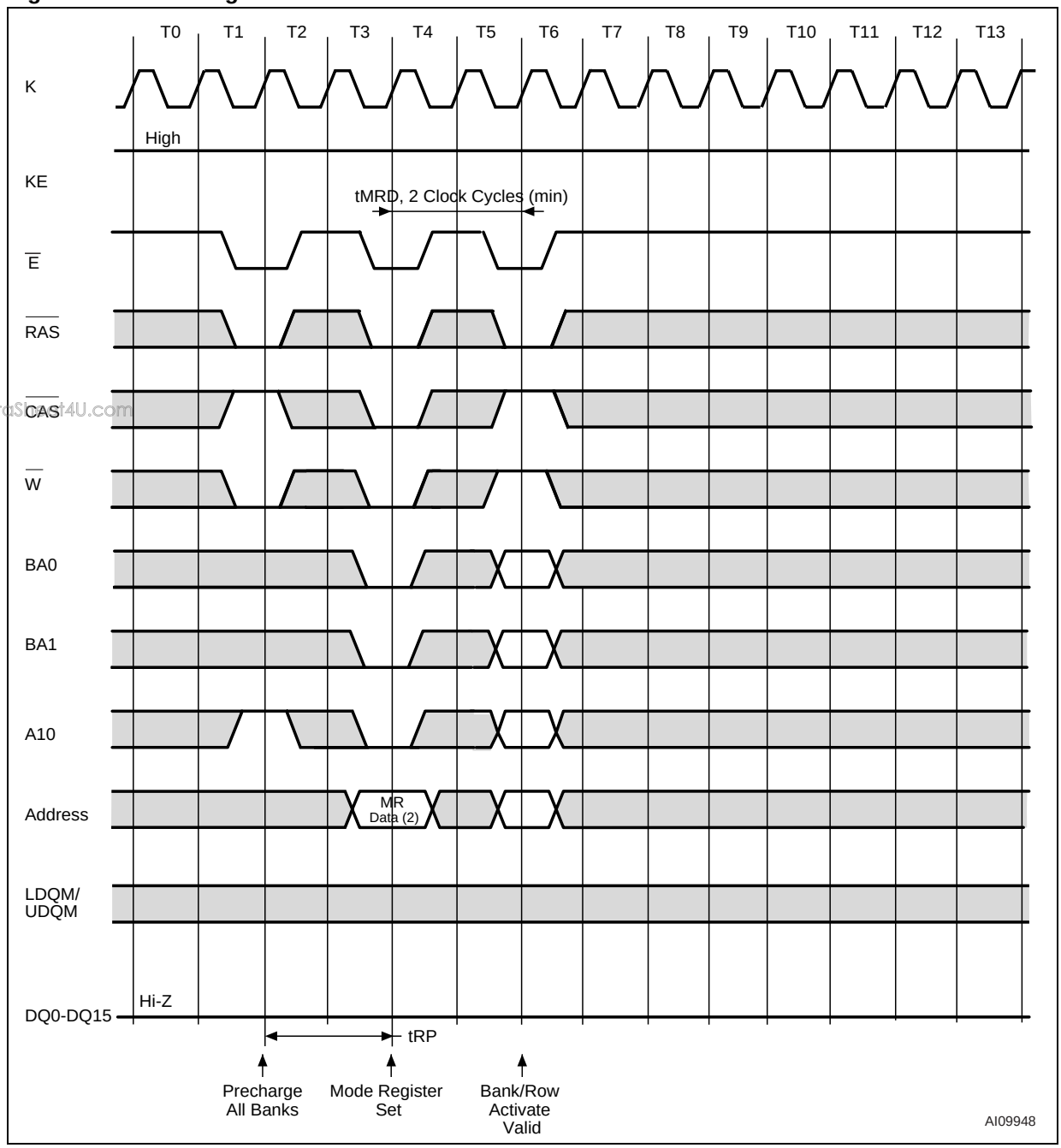
1. Burst Length = 4 Words.

Figure 14. Byte Write AC Waveforms



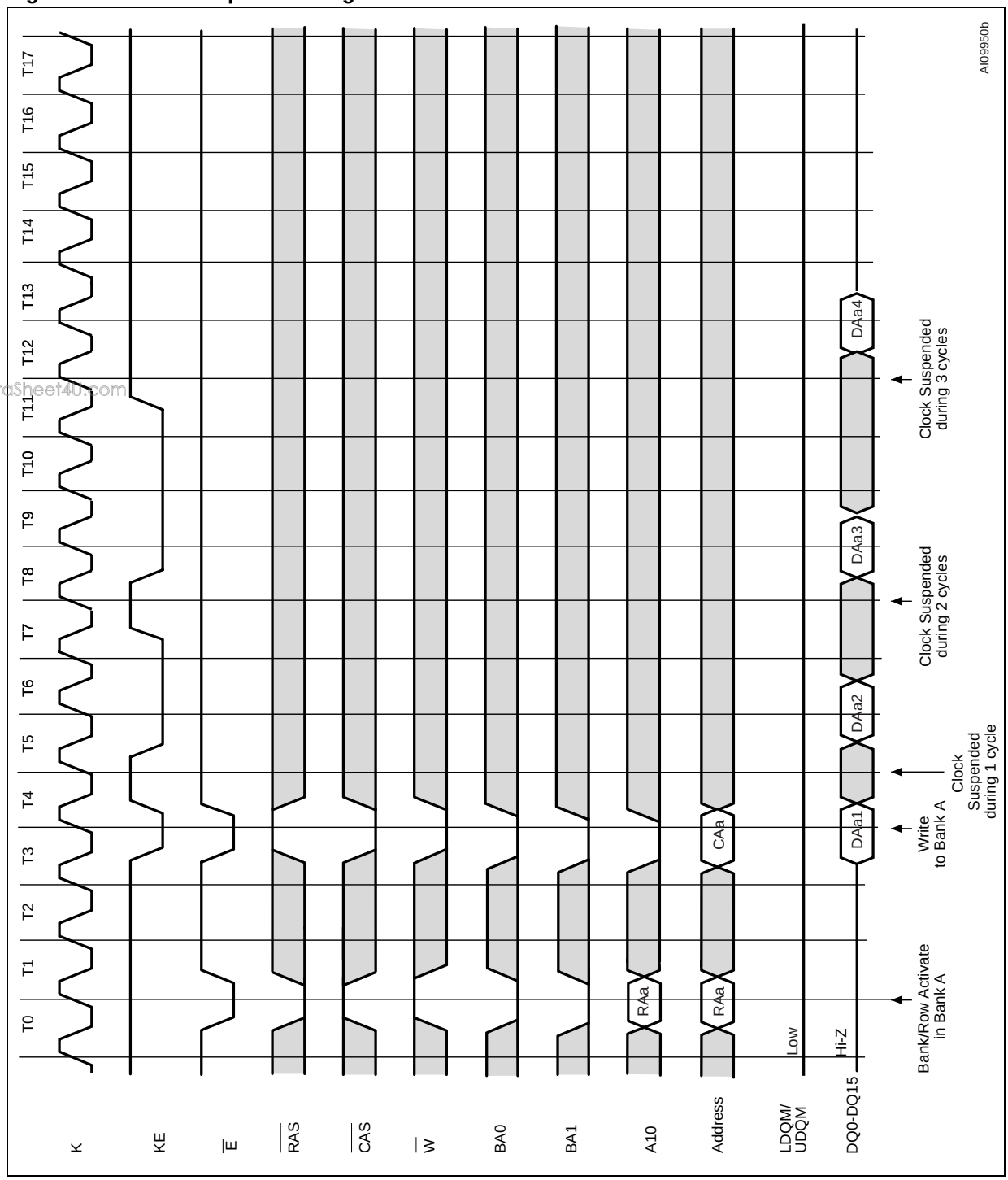
1. Burst Length = 4 Words.

Figure 15. Mode Register Set AC Waveforms



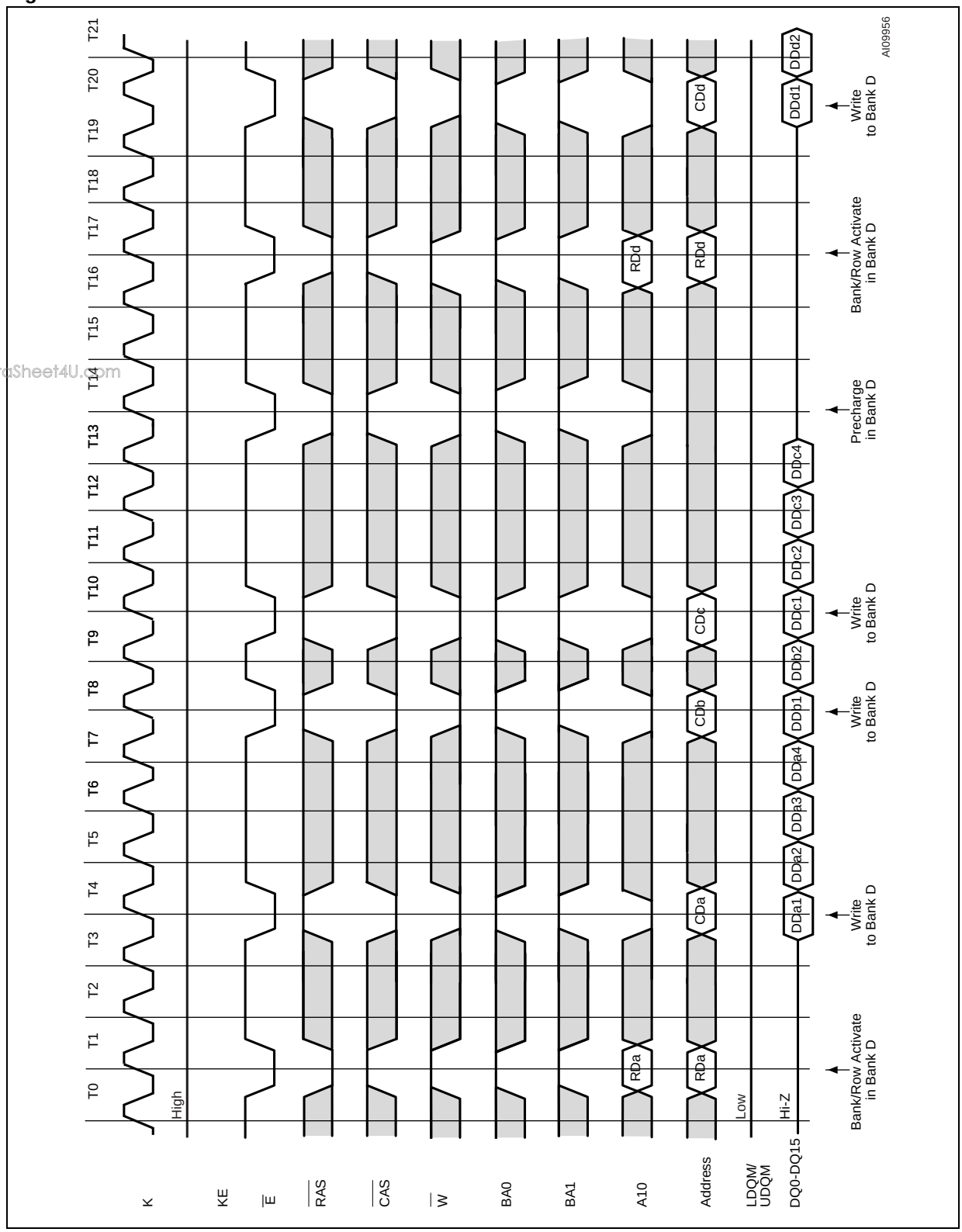
1. To program the Extended Mode Register, BA0 and BA1 must be set to ‘0’ and ‘1’ respectively, and A0 to A11 to the Extended Mode Register Data.
2. MR Data is the value to be written to the Mode Register.

Figure 16. Clock Suspend During Burst Write AC Waveforms



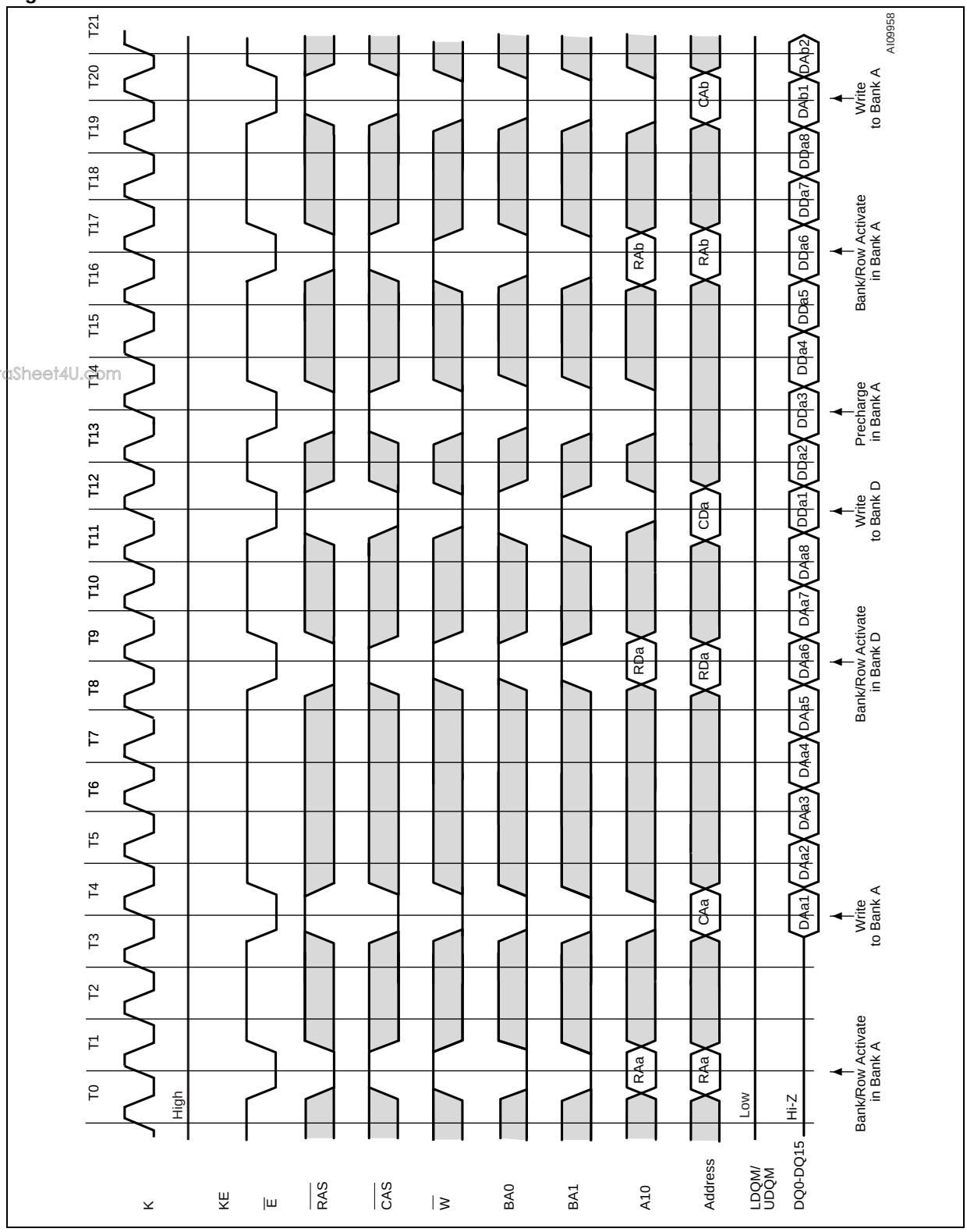
1. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAan= Data n Written to Column a in Bank A.

Figure 17. Random Column Write AC Waveforms



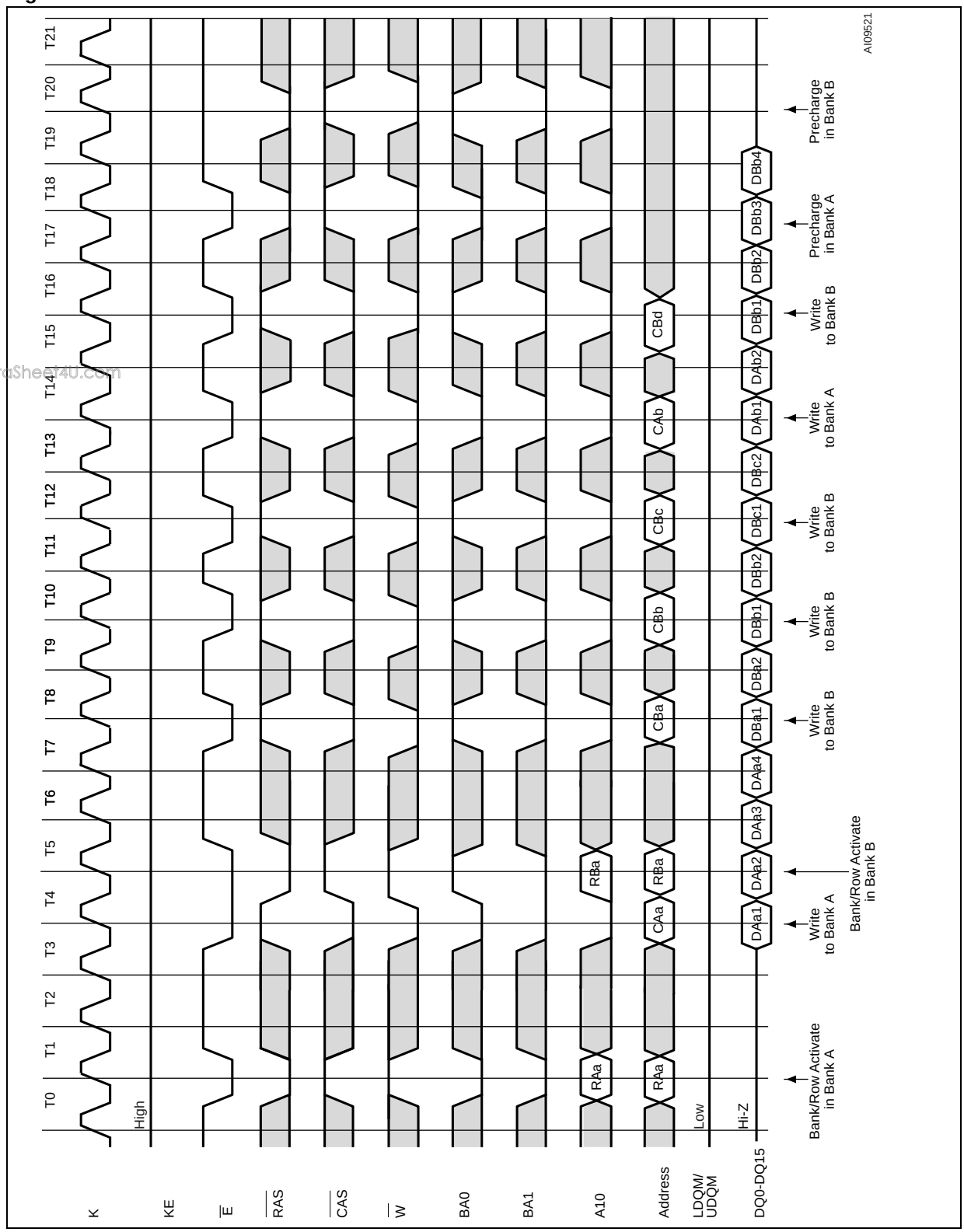
1. Burst Length = 4 Words.
2. RDa = Address of Row a in Bank D, CDa = Address of Column a in Bank D, DDmn= Data n written to Column m in Bank D.

Figure 18. Random Row Write AC Waveforms



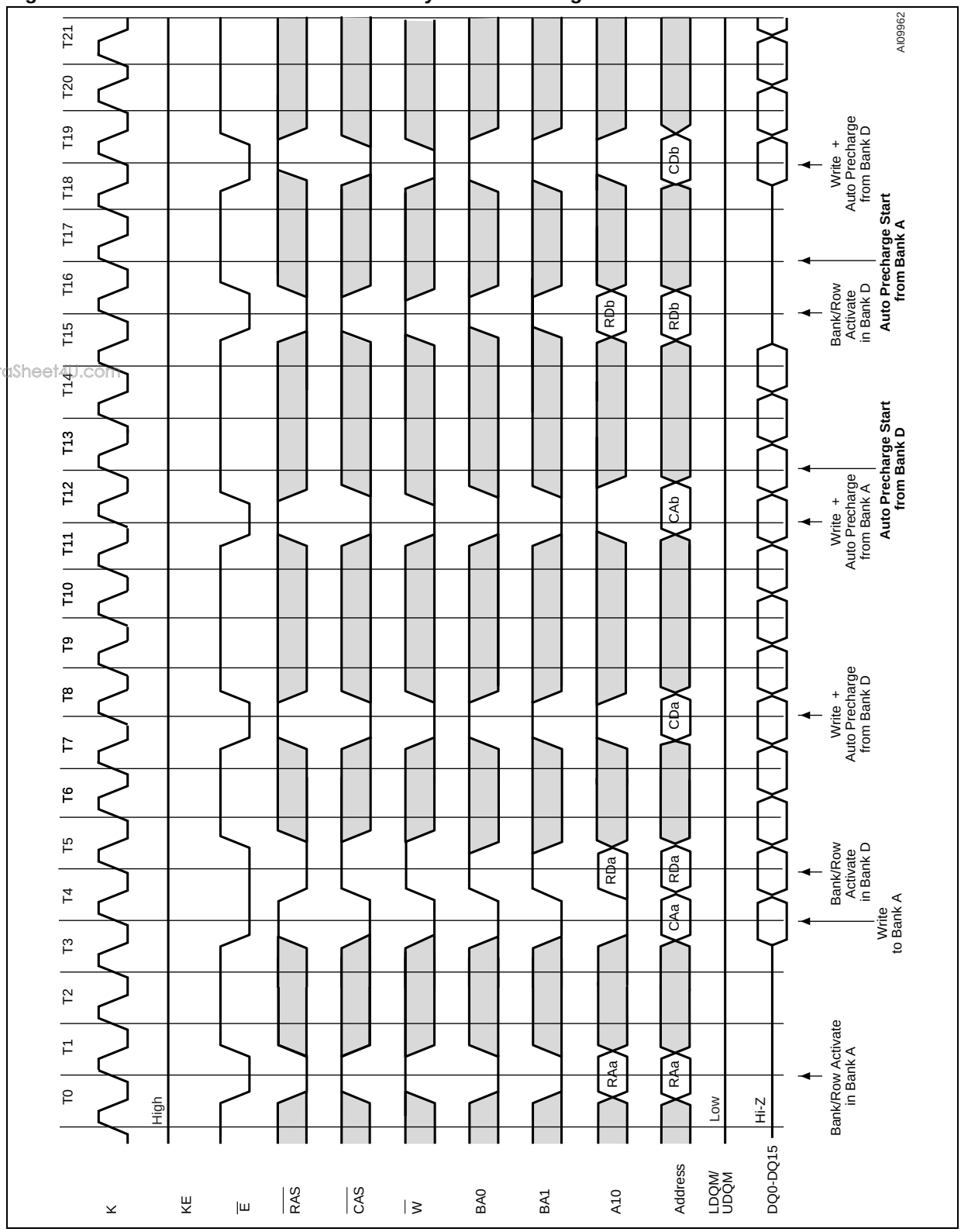
1. Burst Length = 8 Words.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAmn= Data n written to row m in Bank A.

Figure 19. Column Interleaved Write AC Waveforms



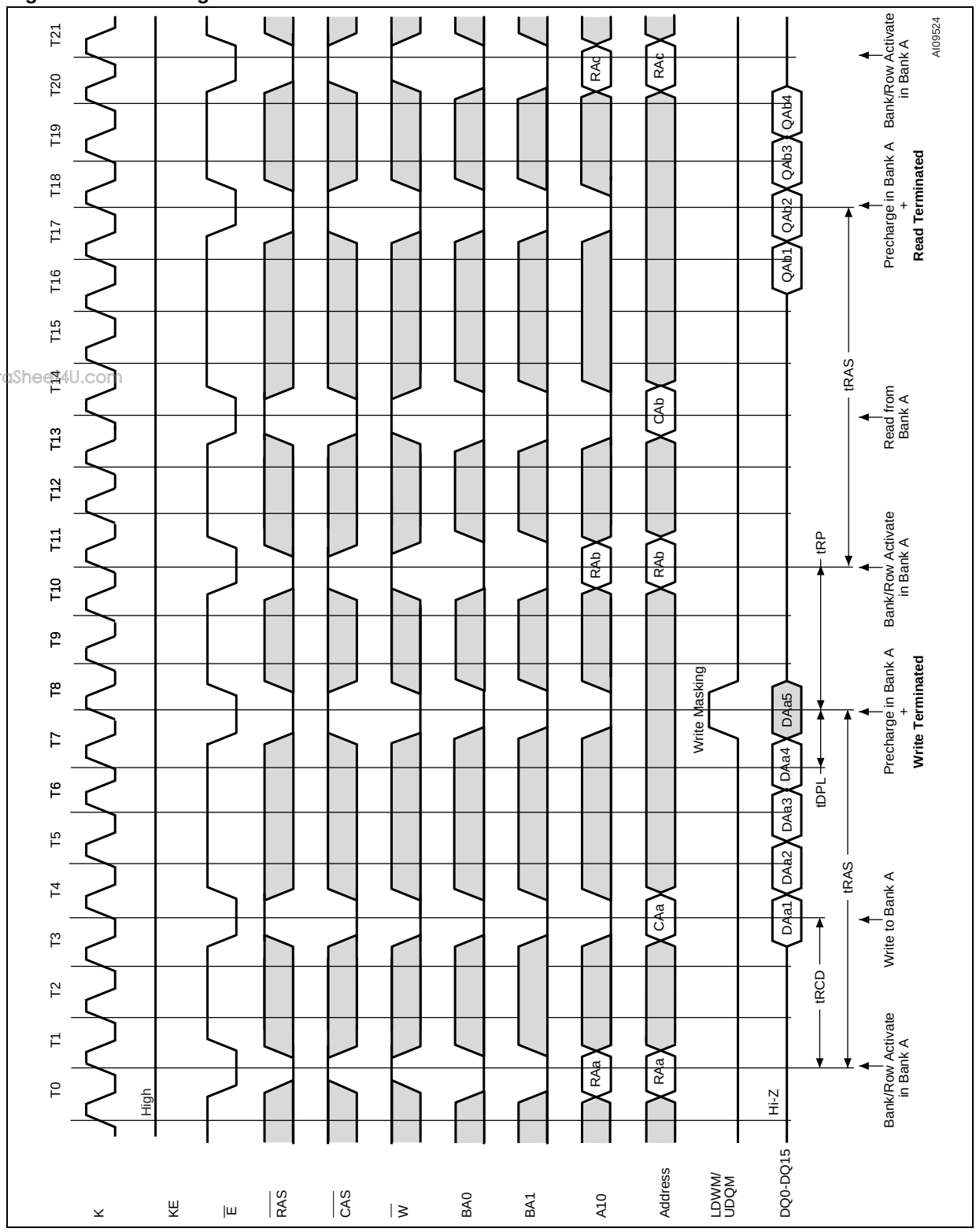
1. Burst Length = 4 Words.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAmn= Data n written to Column m in Bank A.

Figure 20. Burst Column Write Followed by Auto Precharge AC Waveforms



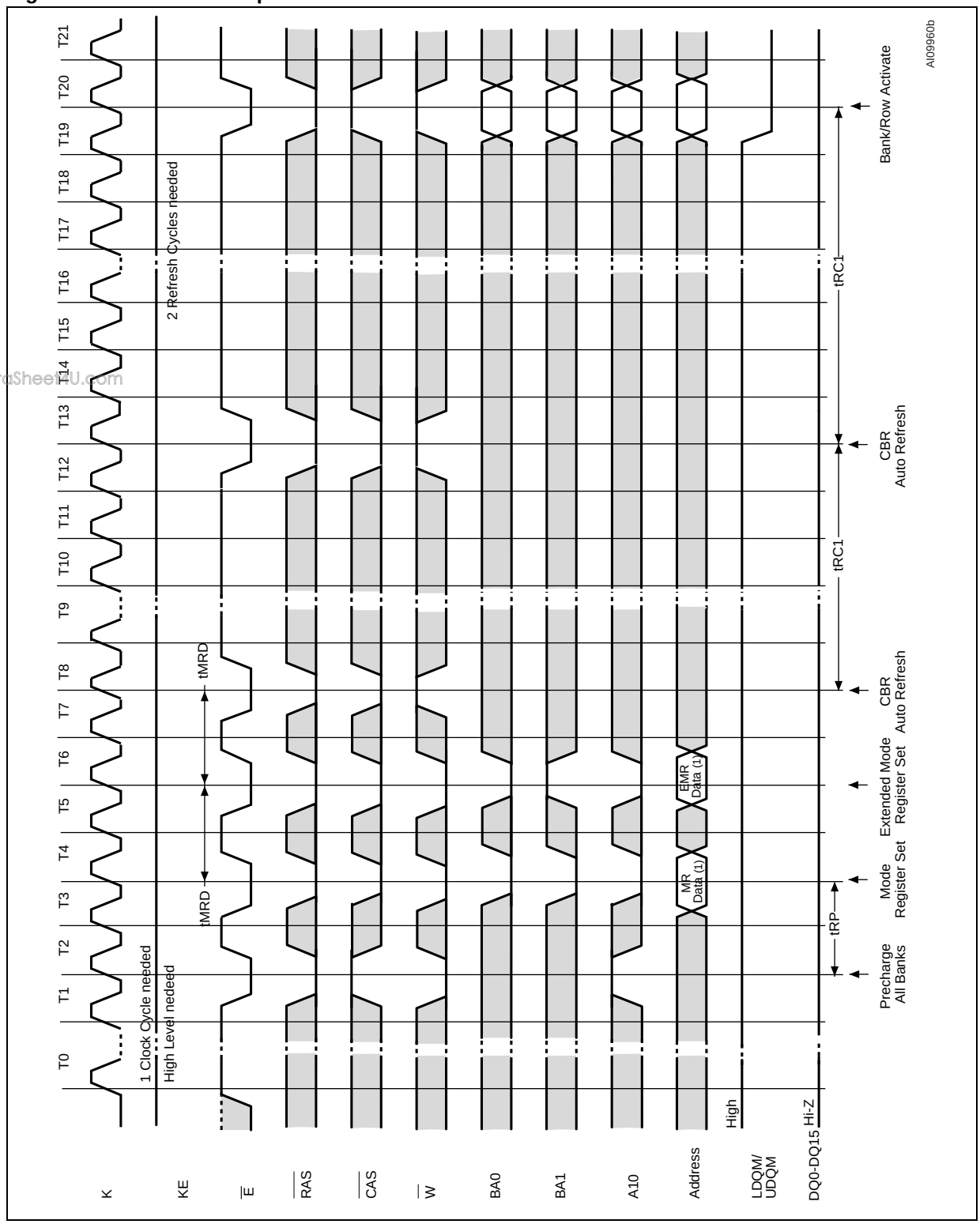
1. Burst Length = 4 Words
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A.

Figure 21. Precharge Termination



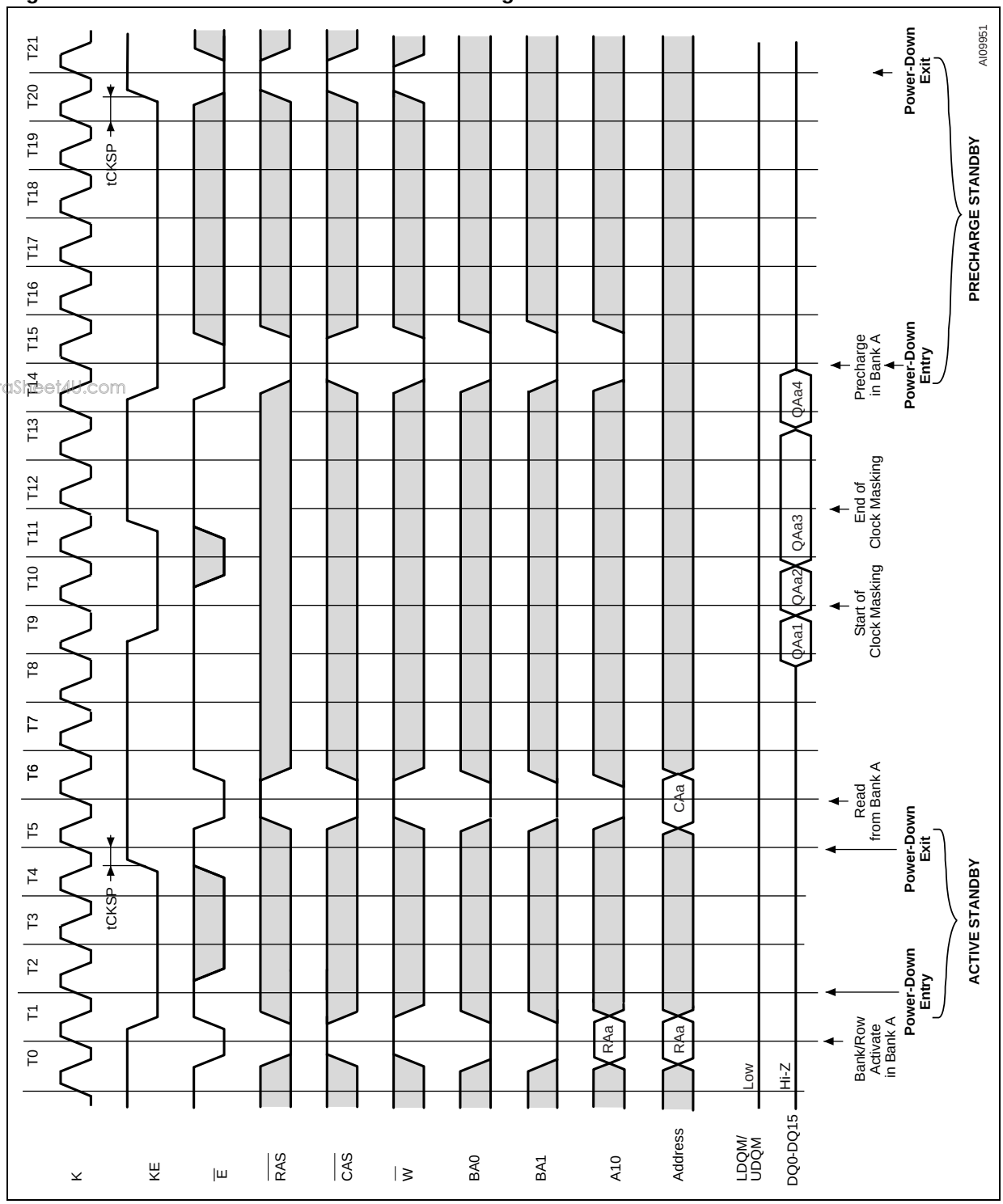
1. Burst Length = 8 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A, DAan= Data n written to Column a in Bank A.

Figure 22. Power-On Sequence



1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

Figure 23. Power-Down Mode and Clock Masking AC Waveforms



1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A.

Figure 24. Auto Refresh

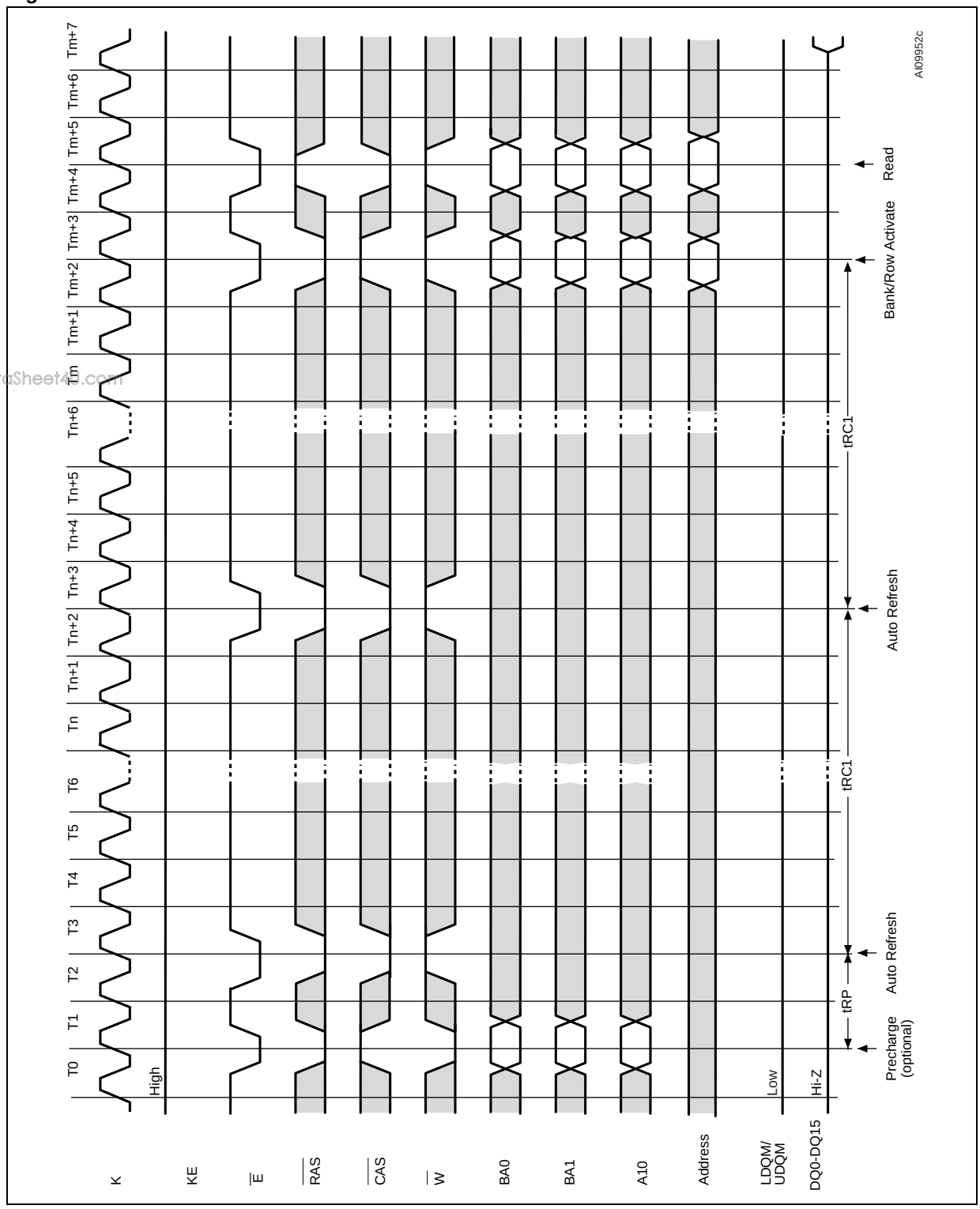


Figure 25. Self Refresh

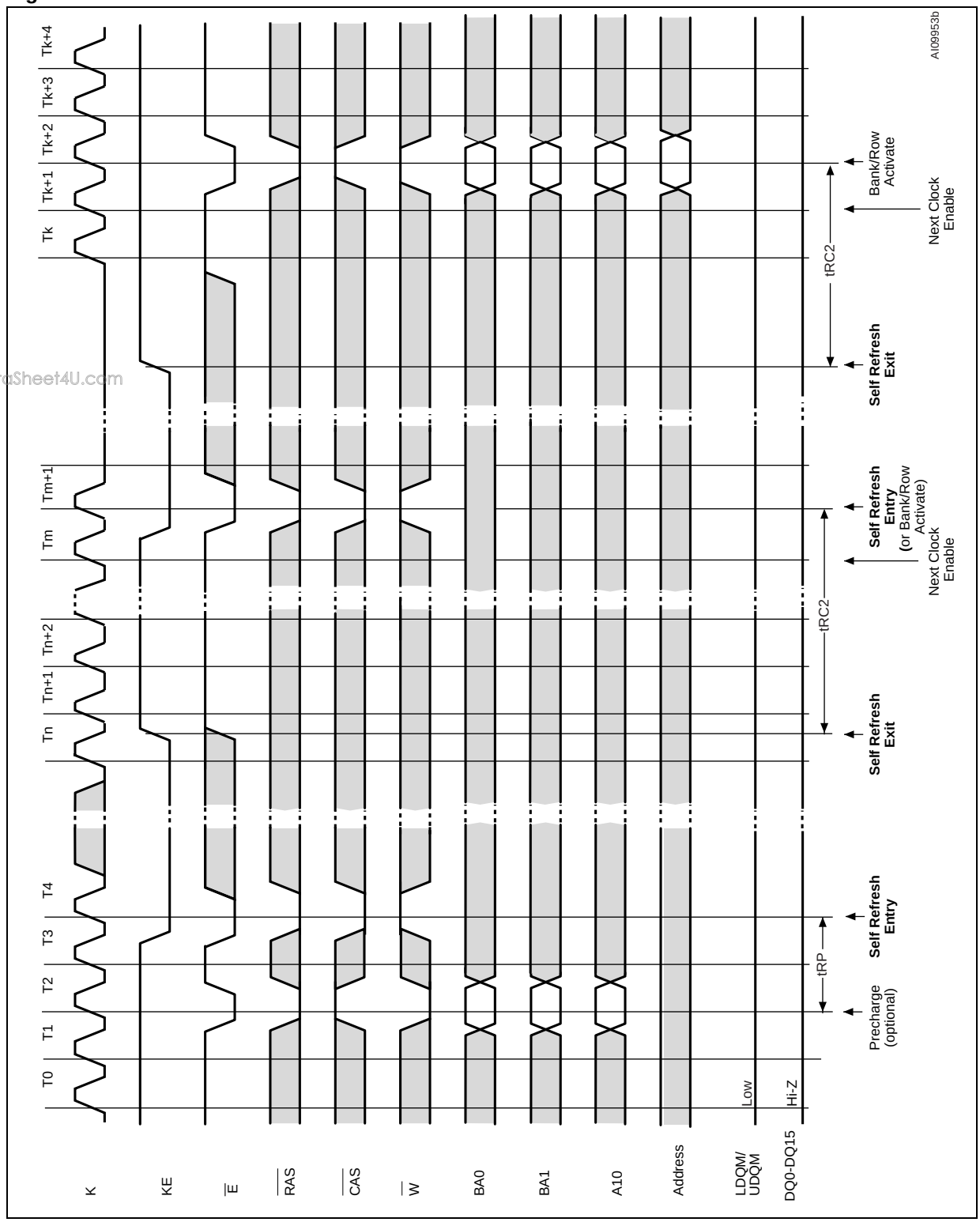
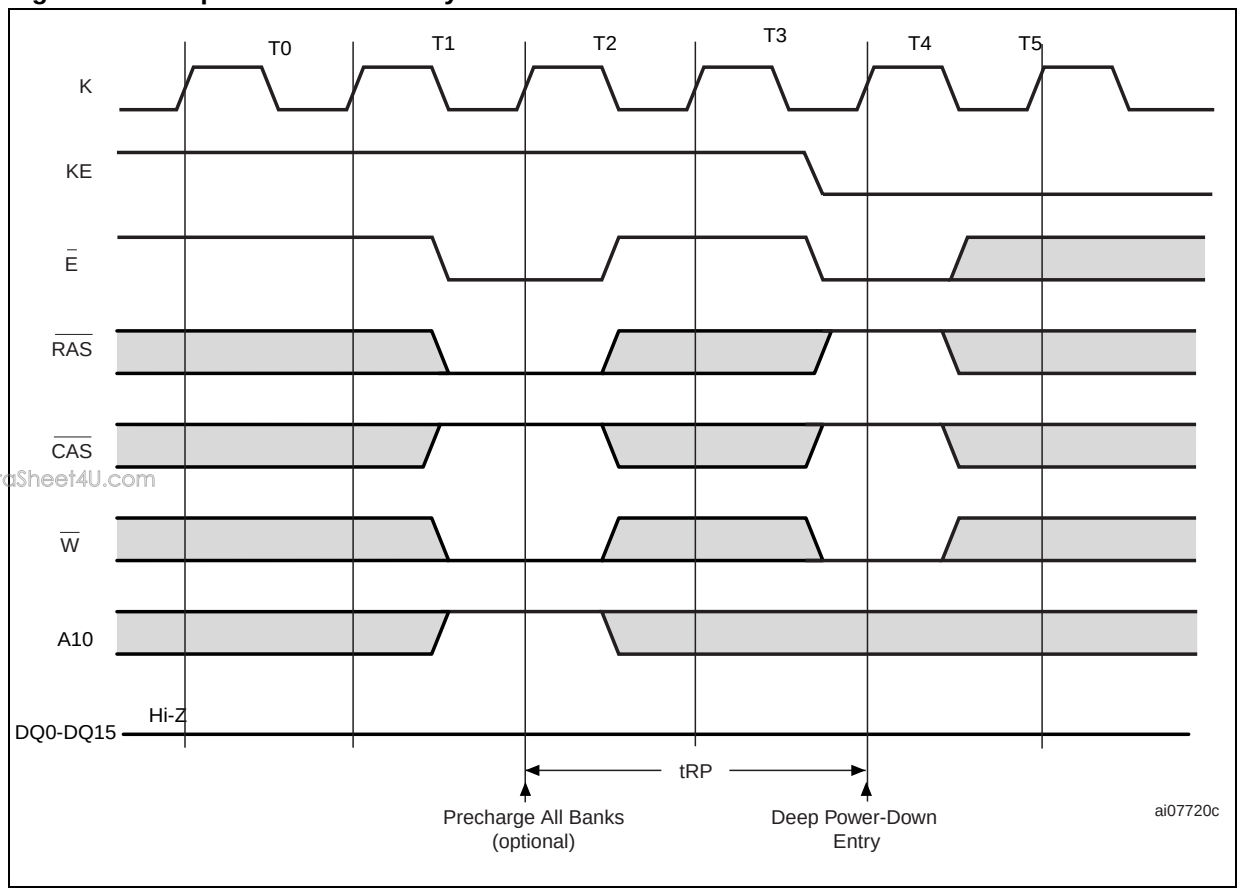
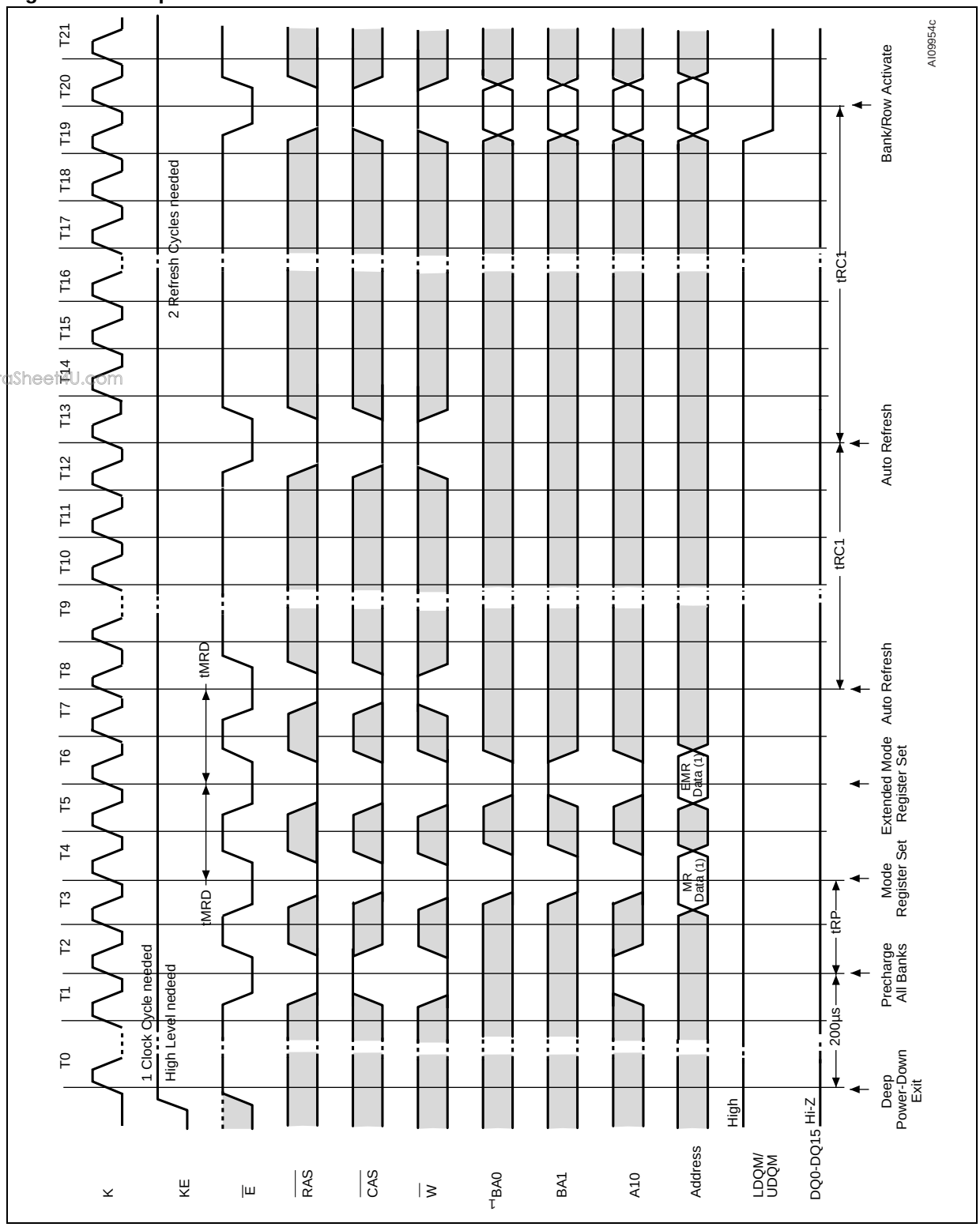


Figure 26. Deep Power-Down Entry AC Waveforms



1. BA0, BA1 and address bits A0 to A11 (except A10) are ‘Don’t Care’.

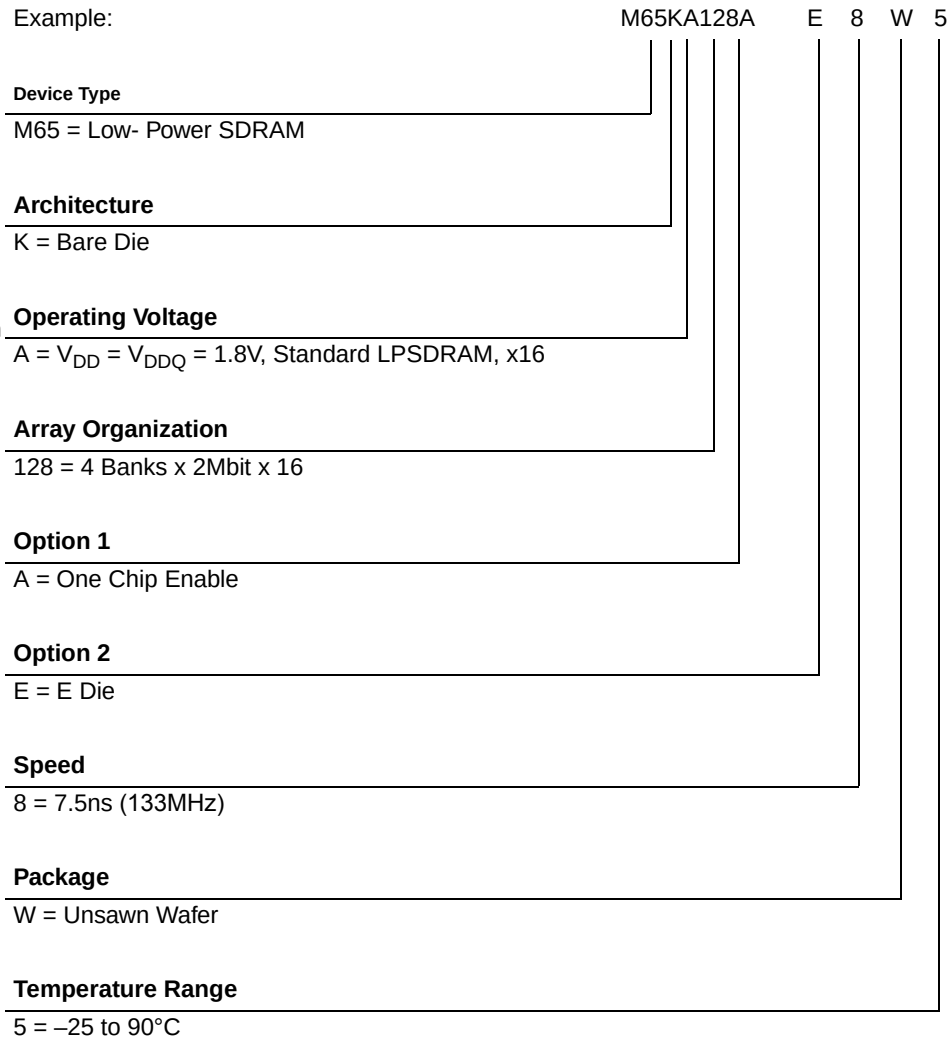
Figure 27. Deep Power-Down Exit AC Waveforms



1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

8 Part numbering

Table 14. Ordering Information Scheme



For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

9 Revision history

Table 15. Document revision history

Date	Revision	Changes
03-Apr-2005	0.1	Initial release.
8-Aug-2006	1	Updated maximum clock frequency. Renamed Burst Terminate command to Burst Stop. Updated to Datasheet status.

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