

FX503A QTC Tone Encoder

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- * EIA TONESET VERSION
- * GENERATES FULL QTC CHARACTER TONESET
- * TONE PERIOD TIMING OUTPUT
- * DELAYED - TX OUTPUT BIAS FACILITY
- * LOW DISTORTION SINEWAVE OUTPUT
- * AUTO REPEAT-TONE ENCODING
- * LOW POWER CMOS PROCESS

**Obsolete Product
- For Information Only -**

FX503A

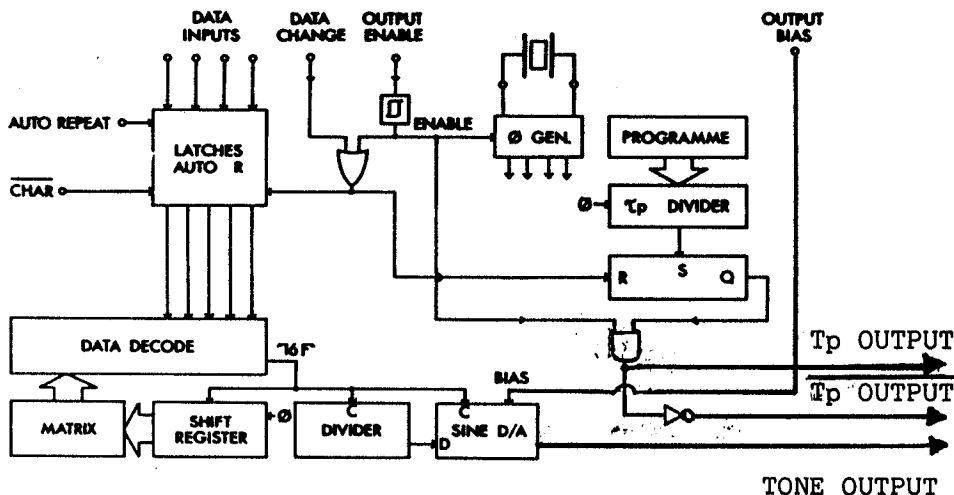


Fig. 1 Internal Block Diagram

The FX503A is a 15 tone generator for use with the EIA toneset, as specified in the HSC character tone table. The output tone is a low distortion 16-step pseudo sine wave of VDD-VSS peak-peak amplitude from a nominal $1k\Omega$ source impedance. The total harmonic distortion is less than 10% and all harmonics are less than 120dB. Output tones and timing signals are provided by a reference oscillator of 560kHz, comprising an on-chip inverter and external ceramic resonator: an external clock may be used if required (Fig 2 and 3).

The output periods are controlled by on-chip circuitry. Timing periods are

as defined by the EIA international toneset. At the end of the tone period the Tp (Tone Period Expired) output goes to Logic 1 and remains there until the next DATA CHANGE which resets the output and commences next timing period. The output tone can be delayed by a period (Td) after the OUTPUT ENABLE function is activated. This is achieved by an external RC time constant (see Fig. 6) and a Schmitt trigger input on the OUTPUT ENABLE pin. Note that if diode (D1) is present, the tone output will go to VSS as soon as OUTPUT ENABLE goes from 1 - 0. The device uses nominal 5V supply.

PIN DESCRIPTION FUNCTION
 FX503A (16-pin D.I.L. package only)

- | | | |
|----|---------------------------------|--|
| 1 | Tone Output: | Pseudo-sinewave (approx. 16 steps). $Z_o \sim 1k\Omega$. VDD-VSS peak-to-peak. Total harmonic distortion <10%, individual harmonics <-20dB. Can be biased to approx. 40% VDD by use of output bias (pin 3), or disabled (to VSS) by use of output enable (pin 4). Output periods controlled by on-chip circuitry. |
| 2 | Tp Output: | Tone period timer - goes to 1 (i.e. 33 ms) after receipt of output enable 0 - 1 edge or D/C 0 - 1 edge. Is reset to logic 0 and timing restarts at subsequent D/C 0 - 1 edge. |
| 3 | Output Bias: | Logic 1 (with output enable at logic 0) will set tone output to approx. 40% VDD. |
| 4 | Output Enable: | Schmitt input. Logic 0 (with output bias at logic 0) will set tone output to VSS + this also reduces current consumption. Will also disable Tp output. Logic 1 + tone is output. |
| 5 | Data Change: | Controls the output in two ways: Logic 1 + output tone controlled by data inputs; 1 + 0 latches input data. |
| 6 | Auto Repeat: | Logic 1 will enable auto repeat circuitry: two consecutive equal data characters will output character tone followed by repeat tone, i.e. data is input TRUE as read. |
| 7 | $\overline{\text{Tp Output}}$: | This output is the inverted form of pin 2. |
| 8 | VSS: | Negative Supply. |
| 9 | D ₀) Data | These inputs are strobed by data change or output enable 0 - 1 edge. |
| 10 | D ₁) Inputs: | |
| 11 | D ₂) | |
| 12 | D ₃) | |
| 13 | $\overline{\text{Char}}$: | Acts as a fifth data input. Logic 1 overrides D ₀ -D ₃ , (but still strobed by D/C) and sets tone output to 40% VDD until new data is loaded. |
| 14 | 560 kHz) | It uses an on-chip inverter for use with a 560 kHz ceramic resonator [or external clock can be fed into ϕ -in pin (pin 14)]. |
| 15 | Xtal I/P) | |
| | (clock I/P) | |
| 15 | $\overline{\text{Xtal Osc.}}$) | |
| | O/P) | |
| | (Clock O/P) | |
| 16 | VDD: | Positive supply. |

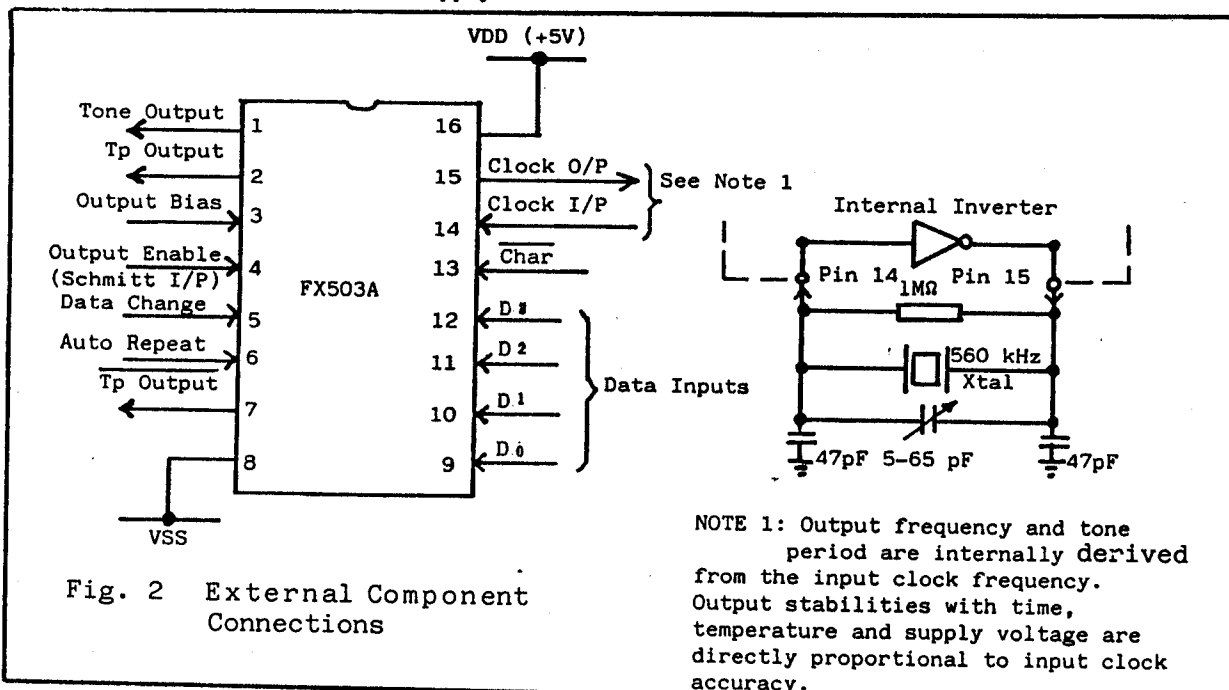
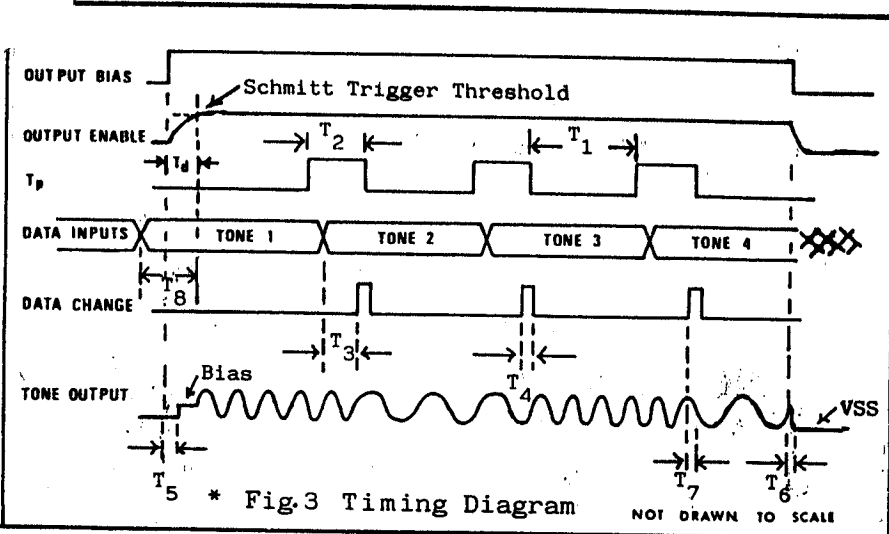


Fig. 2 External Component Connections

NOTE 1: Output frequency and tone period are internally derived from the input clock frequency. Output stabilities with time, temperature and supply voltage are directly proportional to input clock accuracy.



*** References:**

- Td as required
- T₁ (Tone period) See Character Tone Table
- T₂ Minimum 6μs
- T₃ (Data Set-up time) minimum 0μs
- T₄ (Data Change) minimum 4μs
- T₅ (Delay from pin 3 = '1' to O/P $\approx \frac{VDD}{2}$) 4μs
- T₆ (Delay from pin 4 = '0' to O/P VSS) 8μs
- T₇ (Delay from D.C. = '1' to fo change) 8μs
- T₈ (Data set-up time) 0μs

FX503A CHARACTER TONE TABLE			
Tone	Data Inputs D ₃ D ₂ D ₁ D ₀	* Tone frequency (Hz) (Actual)	EIA Specified frequency (Hz)
0	0000	599.6	600
1	0001	740.7	741
2	0010	883.3	882
3	0011	1021.9	1023
4	0100	1161.8	1164
5	0101	1302.3	1305
6	0110	1443.3	1446
7	0111	1590.9	1587
8	1000	1728.4	1728
9	1001	1866.7	1869
A(Group)	1010	2153.9	2151
B	1011	2434.8	2433
C	1100	2014.4	2010
D	1101	2295.1	2292
E(Repeat)	1110	459.0	459
F	1111	Notone	Notone

Internally generated tone period timing pulse: 93ms ± 0.01%
 * With the oscillator frequency adjusted to 560kHz.

Figure 4 shows a typical tone output generated by the FX503A together with the associated general harmonic distribution.

Figure 4 (ii) shows the filtered waveform which can be produced by connecting a 22nF capacitor between the output and VSS. This simple filtering improves the harmonic distortion of the tone waveform and harmonic distribution.

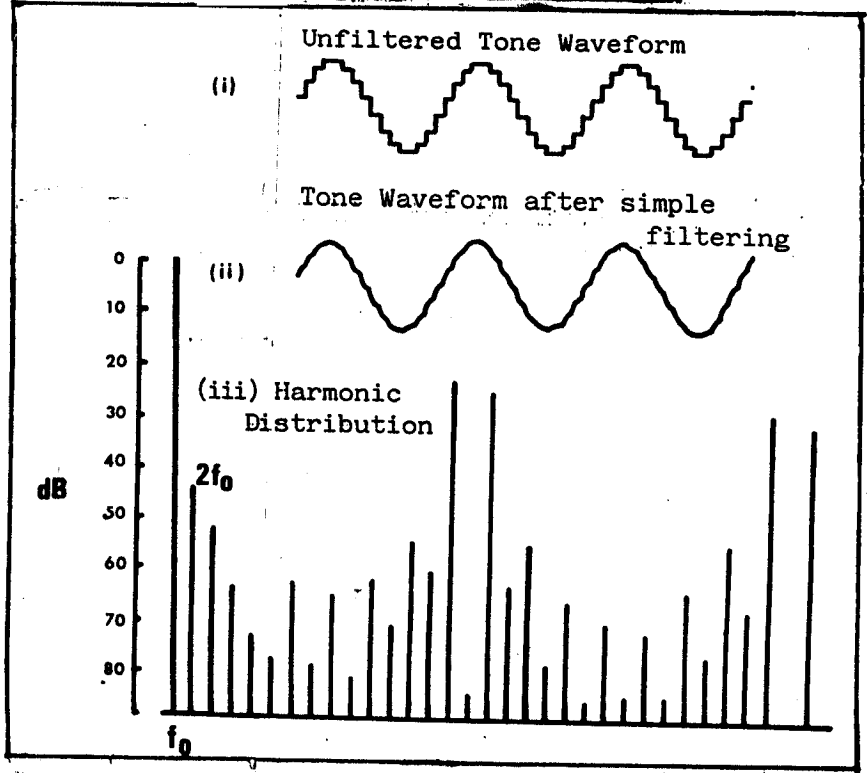


Fig. 4 Tone Output and Harmonic Distribution →

SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

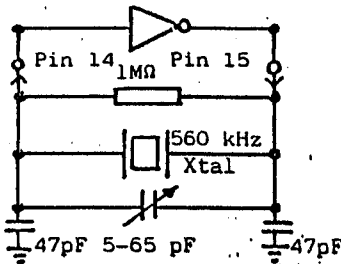
Supply voltage 4.5V to 5.5V
 Input voltage at any pin (ref V_{SS} = 0V)
 Output sink/source current (total) = mA
 Operating temperature range -30°C to +85°C
 Storage temperature range -55°C to +125°C
 Maximum device dissipation 100mW

OPERATING LIMITS

V_{DD} = 5V, T_A = 25°C, φ = 560kHz, Δf_o = 0
 All characteristics measured using the standard test circuit.

	CHARACTERISTIC	MIN	TYP	MAX	UNIT	COMMENT
V _{DD}	Supply voltage (V _{SS} = 0)	4.5	5	5.5	V	
I _{DD}	Supply current - no output tone		700		μA	} no load } connected
I _{DD}	Supply current - generating tone		2		mA	
f _o	Output frequency (from nominal)	-0.2		+0.25	%	} φ = 560kHz
T _p	Output tone period		33		ms	} See Note 1 } Fig. 2
V _{OH}	Logic '1' output level I _{source} = 0.1mA	4.0			V	} pins 2,7
V _{OL}	Logic '0' output level I _{source} = 0.1mA			1.0	V	
V _{IH}	Logic '1' input level	3.5			V	} pins 5,6 } 9-13
V _{IL}	Logic '0' input level			1.5	V	
	Input level to activate pins 3 & 4		3.25		V	} Schmitt } trigger } inputs
	Input level to deactivate pins 3 & 4		1.75		V	
T _A	Working temperature range	-30		+85	°C	
T _{stg}	Storage temperature range	-55		+125	°C	

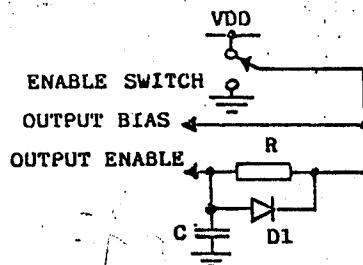
Fig. 5
 560 kHz Resonator Circuit
 Internal Inverter



Calibration Procedure for Ceramic Resonator Oscillator

To ensure that the generated outputs are correct the oscillator frequency must be 560.0kHz. The loading of a frequency counter on the oscillator circuitry can cause an error. The preferred method is to monitor Pin 1 while the FX 503A is generating Tone E (exact set-up conditions will depend on the system arrangement). Adjust the oscillator to obtain a tone output of 459.0Hz.

Fig. 6 Circuit to provide Transmit Delay Function



Transmit Delay Function

A transmit delay can be arranged as shown in Fig. The tone output will step to the bias condition for the delay period before commencing to generate tones.

HANDLING PRECAUTIONS

The FX503A is a CMOS-LSI integrated circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

Fig. 7: FX503A Package Outlines

	inches	mm
A	0.21	20.5
B	0.2	7.6
C	0.6	15.7
D	0.11	2.8
E	0.01	0.25
F	0.25	6.5
G	0.7	17.8
H	0.1	2.54
I	0.028	0.68
J	0.13	3.3

