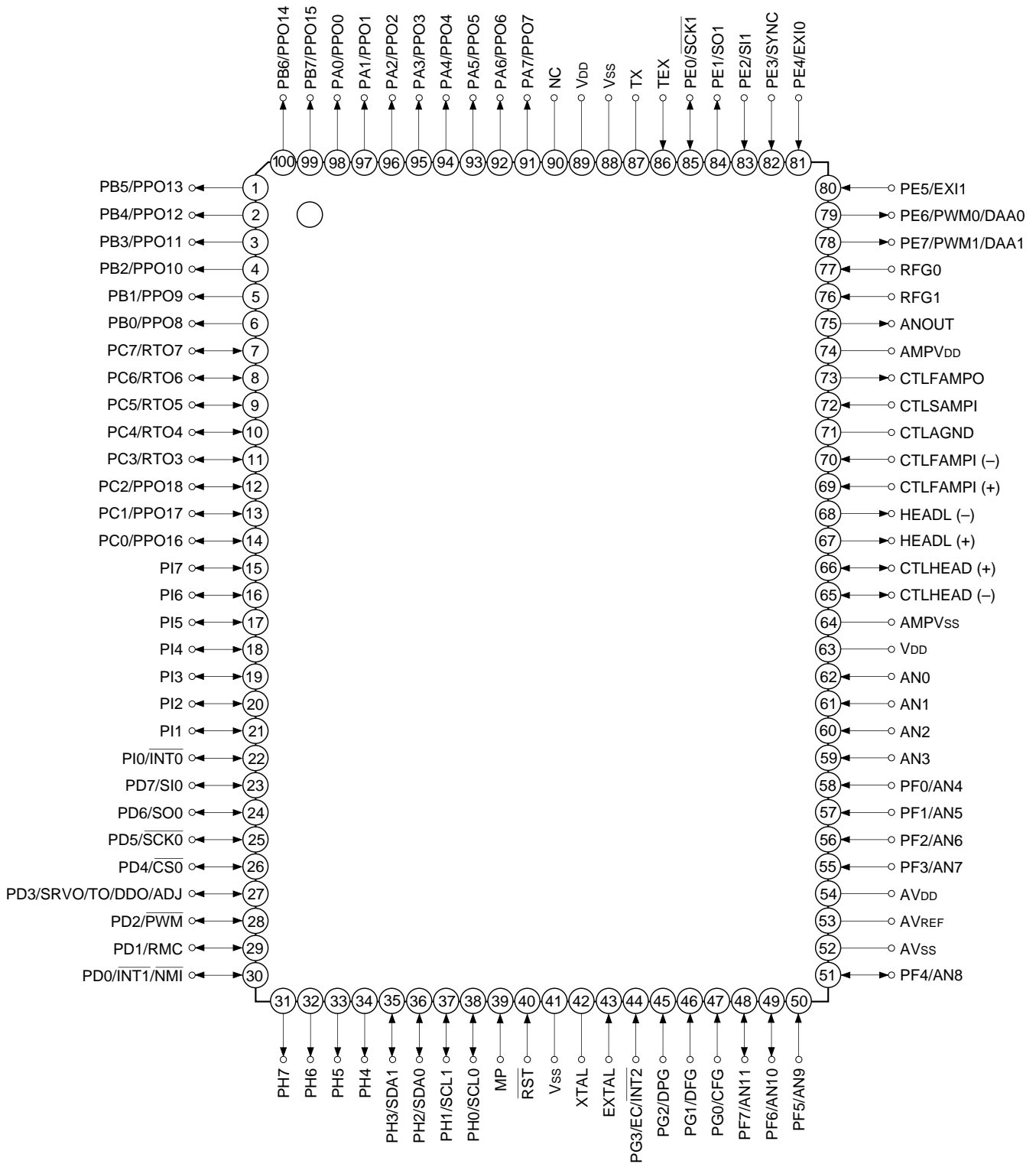


Block Diagram

Pin Assignment (Top View)



- Note)**
1. NC (Pin 90) is always connected to V<sub>DD</sub>.
  2. V<sub>DD</sub> (Pins 63 and 89) are both connected to V<sub>DD</sub>
  3. V<sub>SS</sub> (Pins 41 and 88) are both connected to GND.
  4. MP (Pin 39) is always connected to GND.

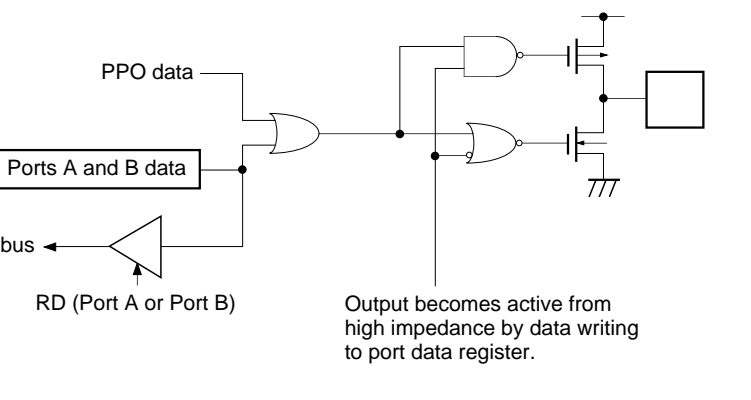
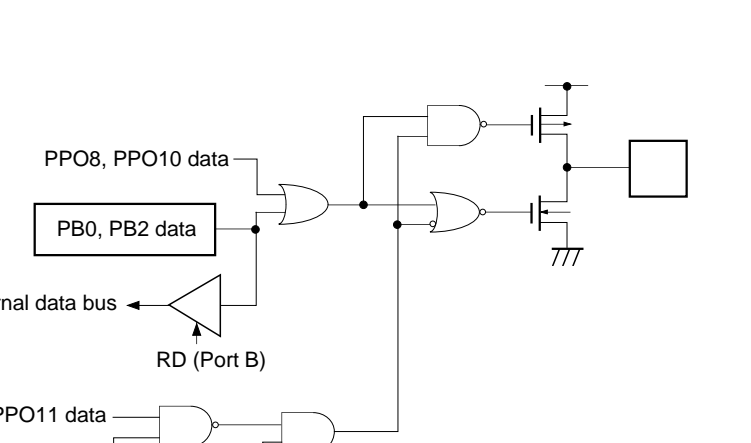
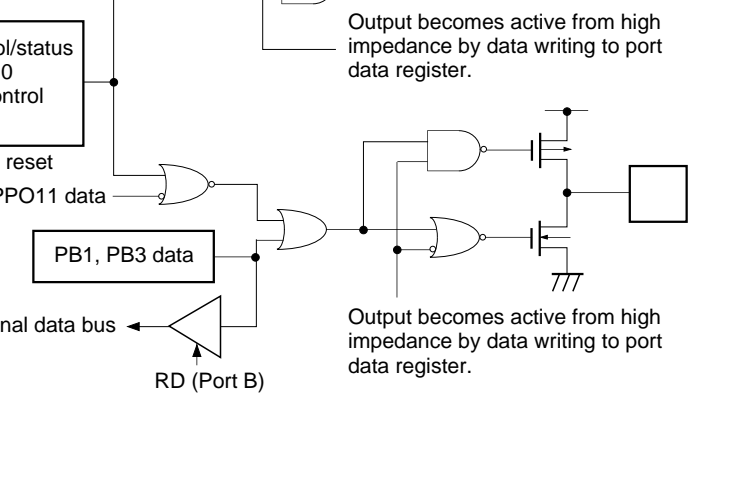
Pin Description

Symbol	I/O	Description	
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	<div style="border: 1px solid black; padding: 2px; display: inline-block;">Head switching output.</div> Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins) PB0 and PB2 can be tri-state controlled with PPG.
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. PC3 can be tri-state controlled with RTG. (5 pins)
PD0/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Input pin to request external interruption and non-maskable interruption.
PD1/RMC	I/O/Input		Remote control receiving circuit input pin.
PD2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PD3/TO DDO/ADJ SRVO	I/O/Output/Output/ Output/Output		Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.
PD4/ $\overline{\text{CS0}}$	I/O/Input		Serial chip select (CH0) input pin.
PD5/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O pin.
PD6/SO0	I/O/Output		Serial data (CH0) output pin.
PD7/SI0	I/O/Input		Serial data (CH0) input pin.
PE0/ $\overline{\text{SCK1}}$	Output/I/O		Serial clock (CH1) I/O pin.
PE1/SO1	Output/Output	Serial data (CH1) output pin.	
PE2/SI1	Input/Input	Serial data (CH1) input pin.	
PE3/SYNC	Input/Input	Composite sync signal input pin.	
PE4/EXI0	Input/Input	External input pin for FRC capture unit. (2 pins)	
PE5/EXI1	Input/Input		
PE6/PWM0/ DAA0	Output/Output	PWM output pin. (2 pins)	DA gate pulse output pin. (2 pins)
PE7/PWM1/ DAA1	Output/Output		

Description	I/O	Description	
AN0 to AN3	Input		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits also serve as standby release input pins. (8 pins)	Analog input pin to A/D converter. (12 pins)
PF4/AN8 to PF7/AN11	Output/Input		
PG0/CFG	Input/Input	(Port G) 4-bit input port. (4 pins)	Capstan FG input pin.
PG1/DFG			Drum FG input pin.
PG2/DPG			Drum PG input pin.
PG3/ $\overline{\text{EC}}$ / INT2	Input/Input/Input		External event input pin for timer/counter. Input pin to request external interruption. Active when falling edge.
PH0/SCL0 PH1/SCL1	I/O/I/O	(Port H) 8-bit I/O port. Upper four bits are for outputs. I/O can be set in a unit of single bits for lower four bits. Lower four bits are N-ch open drain outputs and which can drive 12mA sink current. Upper four bits are for outputs; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	Serial clock (CH2) I/O pin.
PH2/SDA0 PH3/SDA1			Serial data (CH2) I/O pin.
PH4 to PH7	Output		
PI0/ $\overline{\text{INT0}}$	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins)	Input pin to request external interruption. Active when falling edge.
PI1 to PI7	I/O		
RFG0, RFG1	Input	Input ports. (2 pins)	Reel FG input pin.
ANOUT	Output	Output port. (1 pin)	Internal waveform output pin analog circuit.
CTLFAMPO	Output	Output port. (1 pin)	PBCTL signal 1st amplifier output.
CTLSAMPI	Input	Input port. (1 pin)	PBCTL signal 2nd amplifier input.
CTLAGND	Output	Output port. (1 pin)	Smoothing capacitor connecting pin.
CTLFAMPI (-) CTLFAMPI (+)	Input	Input ports. (2 pins)	Input PBCTL signal with capacitor coupled.
HEADL (-) HEADL (+)	Output	Output ports. (2 pins)	During playback, connect to CTLHEAD (-) and CTLHEAD (+) with internal signal.
CTLHEAD (-) CTLHEAD (+)	I/O	I/O ports. (2 pins)	During playback, input pin of PBCTL signal; during recording, output pin of PBCTL signal.
AMPV <sub>SS</sub>		Analog signal input circuit GND pin.	
AMPV <sub>DD</sub>		Analog signal input circuit power supply pin.	

Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (In this time, feedback resistor is not removed.)
TX	Output	
$\overline{\text{RST}}$	Input	System reset pin; active at low level.
NC		NC pin. Connect this pin to $V_{DD}$ for normal operation.
MP	Input	Test mode input pin. Always connect to GND.
$AV_{DD}$		Positive power supply pin of A/D converter.
$AV_{REF}$	Input	Reference voltage input pin of A/D converter.
$AV_{SS}$		GND pin of A/D converter.
$V_{DD}$		Positive power supply pin.
$V_{SS}$		GND pin. Connect both $V_{SS}$ pins to GND.

Input/Output Circuit Formats for Pins

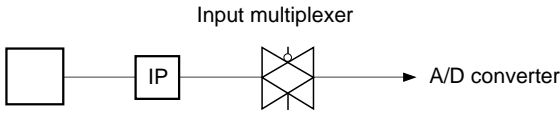
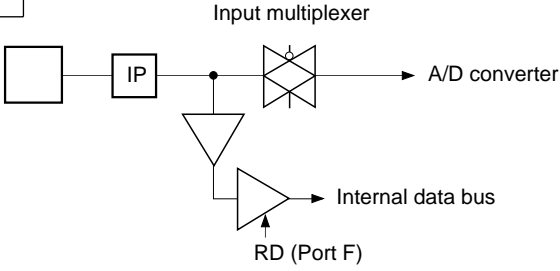
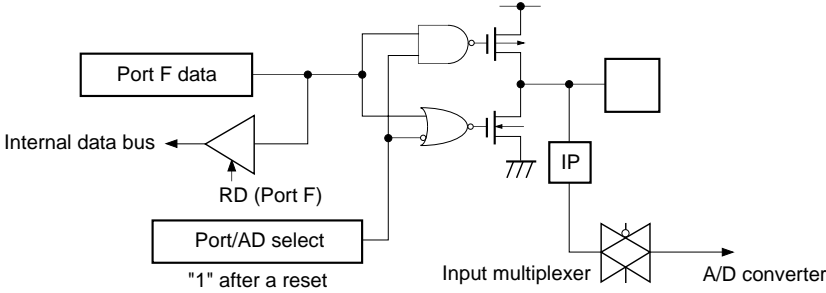
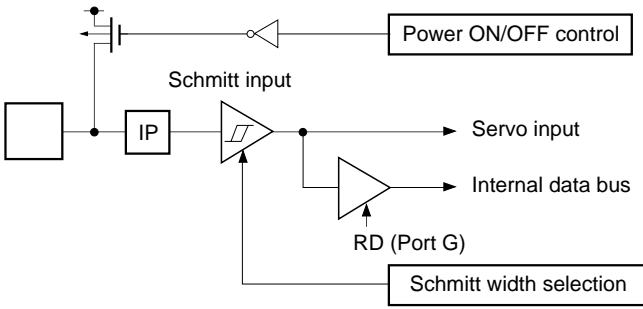
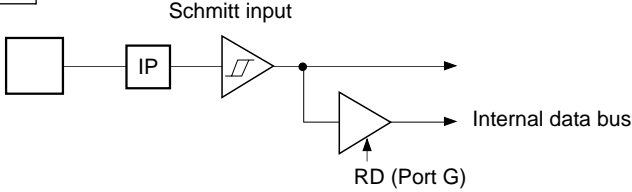
Pin	Circuit format		After a reset
<p>PA0/PPO0 to PA7/PPO7</p> <p>PB4/PPO12 to PB7/PPO15</p> <p>12 pins</p>	<p>Port A</p> <p>Port B</p>	 <p>PPO data</p> <p>Ports A and B data</p> <p>Internal data bus</p> <p>RD (Port A or Port B)</p> <p>Output becomes active from high impedance by data writing to port data register.</p>	<p>Hi-Z</p>
<p>PB0/PPO8</p> <p>PB2/PPO10</p> <p>2 pins</p>	<p>Port B</p>	 <p>PPO8, PPO10 data</p> <p>PB0, PB2 data</p> <p>Internal data bus</p> <p>RD (Port B)</p> <p>Output becomes active from high impedance by data writing to port data register.</p>	<p>Hi-Z</p>
<p>PB1/PPO9</p> <p>PB3/PPO11</p> <p>2 pins</p>		 <p>PPG control/status register bit 0 Tri-state control selection</p> <p>"0" after a reset</p> <p>PPO9, PPO11 data</p> <p>PB1, PB3 data</p> <p>Internal data bus</p> <p>RD (Port B)</p> <p>Output becomes active from high impedance by data writing to port data register.</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PC0/PPO16 to PC2/PPO18</p> <p>PC5/RTO5 to PC7/RTO7</p> <p>6 pins</p>	<p>Port C</p> <p>PPO, RTO data</p> <p>Port C data</p> <p>Port C direction</p> <p>"0" after a reset</p> <p>Internal data bus</p> <p>RD (Port C)</p> <p>Internal data bus</p> <p>RD (Port C direction)</p> <p>Input protection circuit</p> <p>IP</p> <p>777</p>	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pin</p>	<p>Port C</p> <p>RTO3 data</p> <p>PC3 data</p> <p>PC3 direction</p> <p>"0" after a reset</p> <p>Internal data bus</p> <p>RD (Port C)</p> <p>Internal data bus</p> <p>RD (Port C direction)</p> <p>RTO4 data</p> <p>RTG interruption control register bit 7 Tri-state control selection</p> <p>"0" after a reset</p> <p>IP</p> <p>777</p>	<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pin</p>	<p>PC4 data</p> <p>PC4 direction</p> <p>"0" after a reset</p> <p>Internal data bus</p> <p>RD (Port C)</p> <p>Internal data bus</p> <p>RD (Port C direction)</p> <p>IP</p> <p>777</p>	<p>Hi-Z</p>



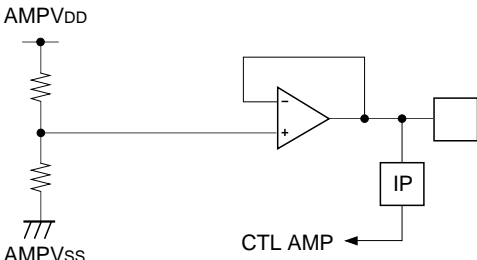
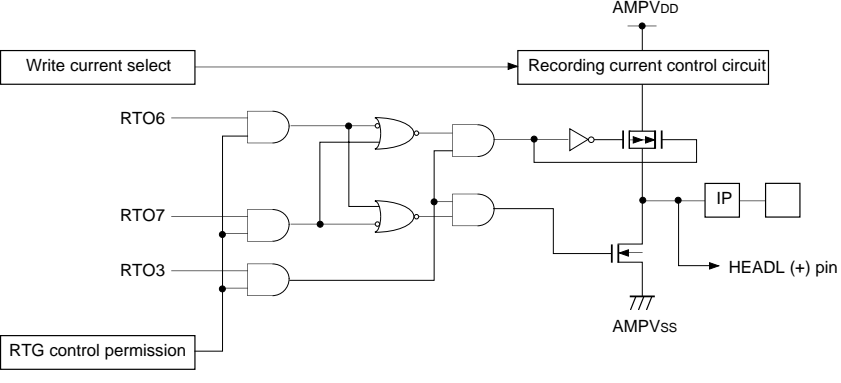
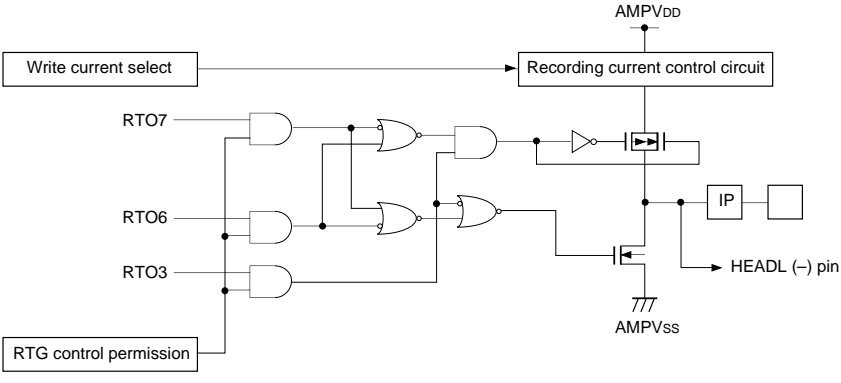
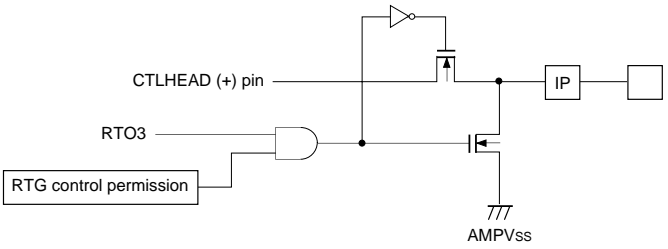
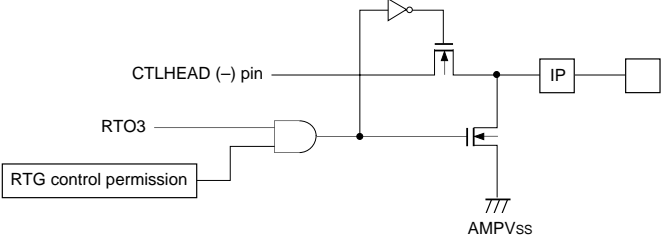
Pin	Circuit format	After a reset
<p>PD0/<math>\overline{\text{INT1}}/\overline{\text{NMI}}</math>            PD1/<math>\overline{\text{RMC}}</math>            PD4/<math>\overline{\text{CS0}}</math>            PD7/<math>\overline{\text{SI0}}</math></p> <p>4 pins</p>	<p>Port D</p> <p>Port D data</p> <p>Port D direction "0" after a reset</p> <p>Internal data bus ← RD (Port D)</p> <p>Internal data bus ← RD (Port D direction)</p> <p>Schmitt input</p> <p>IP</p> <p>( PD1: Remote control circuit            PD0: Interruption circuit            PD4, PD7: Serial CH0</p>	<p>Hi-Z</p>
<p>PD2/<math>\overline{\text{PWM}}</math>            PD3/<math>\overline{\text{SRVO}}/\overline{\text{TO}}/\overline{\text{DDO}}/\overline{\text{ADJ}}</math></p> <p>2 pins</p>	<p>Port D</p> <p>Port D function select "0" after a reset</p> <p>( PD2: 14-bit PWM            Timer/counter,            CTL duty detection circuit,            PD3: 32kHz timer,            amplifier circuit</p> <p>Port D data</p> <p>Port D direction "0" after a reset</p> <p>Internal data bus ← RD (Port D)</p> <p>Internal data bus ← RD (Port D direction)</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>
<p>PD5/<math>\overline{\text{SCK0}}</math>            PD6/<math>\overline{\text{SO0}}</math></p> <p>2 pins</p>	<p>Port D</p> <p>Port D function select "0" after a reset SIO CH0</p> <p>Port D data</p> <p>Port D direction "0" after a reset</p> <p>Internal data bus ← RD (Port D)</p> <p>SIO CH0</p> <p>Note)            ( PD5 is schmitt input            PD6 is inverter input )</p> <p>MPX</p> <p>MPX</p> <p>IP</p>	<p>Hi-Z</p>

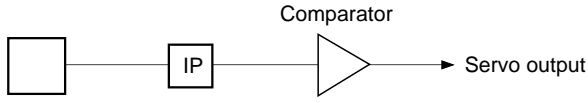
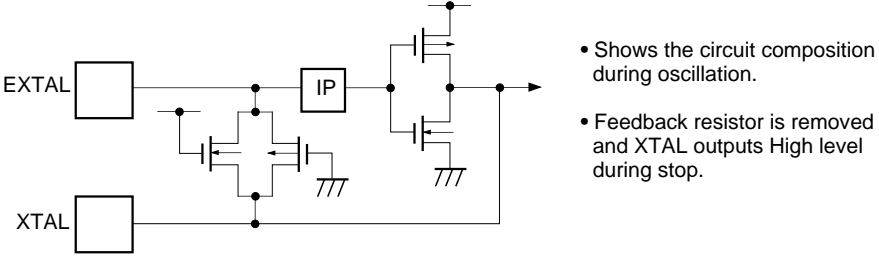
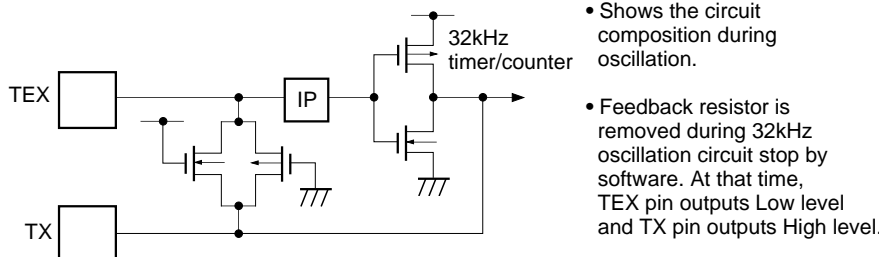
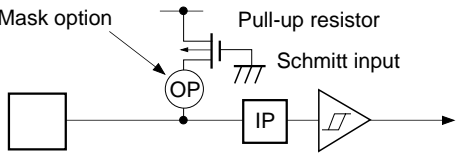
Pin	Circuit format	After a reset
<p>PE0/SCK<math>\bar{1}</math></p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE1/SO1</p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE2/SI1 PE3/SYNC PE4/EXI0 PE5/EXI1</p> <p>4 pins</p>	<p>Port E</p> <p>Note) For PE3/SYNC, CMOS schmitt input or TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PE6/PWM0/ DAA0 PE7/PWM1/ DAA1</p> <p>2 pins</p>	<p>Port E</p>	<p>High level</p>

Pin	Circuit format	After a reset
AN0 to AN3 3 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins		Hi-Z
PF4/AN8 to PF7/AN11 4 pins		Hi-Z
PG0/CFG PG1/DFG PG2/DPG 3 pins		Hi-Z
PG3/EC/INT2 1 pin		Hi-Z

Pin	Circuit format	After a reset
<p>PH0/SCL0 PH1/SCL1 PH2/SDA0 PH3/SDA1</p> <p>4 pins</p>	<p>Port H</p> <p>SCL, SDA I<sup>2</sup>C output enable Port H data Port H direction "0" after a reset Internal data bus ← RD (Port H) Internal data bus ← RD (Port H direction) SCL, SDA (Serial interface (CH2) circuit) Schmitt input IP Other serial interface (CH2) pin</p>	<p>Hi-Z</p>
<p>PH4 to PH7</p> <p>4 pins</p>	<p>Port H</p> <p>Port H data Internal data bus ← RD (Port H) * * 12V drive voltage, large current 12mA</p>	<p>Hi-Z</p>
<p>PI0/<math>\overline{\text{INT0}}</math></p> <p>1 pin</p>	<p>Port I</p> <p>Pull-up resistor "0" after a reset PI0 data PI0 direction "0" after a reset Internal data bus ← RD (Port I) Internal data bus ← RD (Port I direction) Internal data bus ← RD (pull-up resistor) Edge detection Standby release Interruption circuit * Pull-up transistors approx. 100k<math>\Omega</math></p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PI1 to PI7</p> <p>7 pins</p>	<p>Port I</p> <p>Pull-up resistor "0" after a reset</p> <p>Port I data</p> <p>Port I direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port I)</p> <p>Internal data bus</p> <p>RD (Port I direction)</p> <p>Internal data bus</p> <p>RD (pull-up resistor)</p> <p>Edge detection</p> <p>Standby release</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>CTLFAMPI (+) CTLFAMPI (-) CTLFAMPO</p> <p>3 pins</p>	<p>CTLAGND</p> <p>CTLFAMPI (+)</p> <p>IP</p> <p>CTLFAMPI (-)</p> <p>IP</p> <p>Input pin charge control</p> <p>CTLFAMPO</p>	<p>1/2AMPV<sub>DD</sub></p>
<p>CTLSAMPI</p> <p>1 pin</p>	<p>Input pin charge control</p> <p>IP</p> <p>CTLAGND</p> <p>LPF circuit</p>	<p>1/2AMPV<sub>DD</sub></p>

Pin	Circuit format	After a reset
<p>CTLAGND</p> <p>1 pin</p>		<p><math>1/2AMPV_{DD}</math></p>
<p>CTLHEAD (+)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>CTLHEAD (-)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>HEADL (+)</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>HEADL (-)</p> <p>1 pin</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>RFG0 RFG1</p> <p>2 pins</p>		<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed and XTAL outputs High level during stop.</li> </ul>	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during 32kHz oscillation circuit stop by software. At that time, TEX pin outputs Low level and TX pin outputs High level.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>		<p>Low level (during a reset)</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	−0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	−0.3 to +0.3	V	
	AMPV <sub>DD</sub>	AMPV <sub>SS</sub> to +7.0* <sup>2</sup>	V	
	AMPV <sub>SS</sub>	−0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	−0.3 to +7.0* <sup>3</sup>	V	
Output voltage	V <sub>OUT</sub>	−0.3 to +7.0* <sup>3</sup>	V	
Medium drive output voltage	V <sub>OUTP</sub>	−0.3 to +15.0	V	Port H (PH7 to PH4) pin
High level output current	I <sub>OH</sub>	−5	mA	
High level total output current	∑I <sub>OH</sub>	−50	mA	Total of output pins
Low level output current	I <sub>OL</sub>	15	mA	Other than large current output ports (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output port* <sup>4</sup> (value per pin)
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of output pins
Operating temperature	T <sub>opr</sub>	−20 to +75	°C	
Storage temperature	T <sub>stg</sub>	−55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP package type

\*1 AV<sub>DD</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*2 AMPV<sub>DD</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*3 V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*4 The large current output port is port H (PH7 to PH4).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.



## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during sleep mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during stop
Analog supply voltage	AV <sub>DD</sub>	4.5	5.5	V	*1
	AMPV <sub>DD</sub>	4.5	5.5	V	*2
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*3
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS schmitt input*4
	V <sub>IHTS</sub>	2.2	V <sub>DD</sub>	V	TTL schmitt input*5
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*6 TEX pin*7
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*3
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS schmitt input*4
	V <sub>ILTS</sub>	0	0.8	V	TTL schmitt input*5
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*6 TEX pin*7
Operating temperature	Topr	-20	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*2 AMPV<sub>DD</sub> and V<sub>DD</sub> should be set to the same voltage.

\*3 Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PI1 to PI7 and PH0 to PH3), MP pin

\*4 Each pin of  $\overline{RST}$ , PD0/ $\overline{INT1}$ / $\overline{NMI}$ , PD1/ $\overline{RMC}$ , PD4/ $\overline{CS0}$ , PD5/ $\overline{SCK0}$ , PD7/SI0, PE0/ $\overline{SCK1}$ , PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/ $\overline{INT0}$ , PG3/ $\overline{EC}$ / $\overline{INT2}$  (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

\*5 PE3/SYNC (when TTL schmitt input is selected with mask option.)

\*6 Specifies only during external clock input.

\*7 Specifies only during external event input.

**Electrical Characteristics**

**DC Characteristics** ( $V_{DD} = 4.5$  to  $5.5V$ )

( $T_a = -20$  to  $+75^\circ C$ ,  $V_{SS} = 0V$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	$V_{OH}$	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (VOL only)	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	$V_{OL}$	PI	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
Input current	$I_{IHE}$	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	$\mu A$
	$I_{ILE}$		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	$\mu A$
	$I_{IHT}$	TEX	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	$\mu A$
	$I_{ILT}$		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	$\mu A$
	$I_{ILR}$		$\overline{RST}^{*1}$	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	$I_{IZ}$	PA to PF, PG3, PI, MP, AN0 to AN3, $\overline{RST}^{*1}$	$V_{DD} = 5.5V, V_I = 0, 5.5V$			$\pm 10$	$\mu A$
Open drain output leakage current (N-CH Tr off state)	$I_{LOH}$	PH4 to PH7	$V_{DD} = 5.5V, V_{OH} = 12V$			50	$\mu A$
		PH0 to PH3	$V_{DD} = 5.5V, V_{OH} = 5.5V$			10	$\mu A$
Supply current*2	$I_{DD1}$	$V_{DD}, V_{SS}$	16MHz crystal oscillation ( $C_1 = C_2 = 15pF$ )		37	50	mA
			$V_{DD} = 5.5V^{*3}$				
	$I_{DDS1}$		Sleep mode		2.1	8	mA
			$V_{DD} = 5.5V$				
	$I_{DD2}$		32kHz crystal oscillation ( $C_1 = C_2 = 47pF$ )		58	100	$\mu A$
			$V_{DD} = 3.3V$				
	$I_{DDS2}$		Sleep mode		9	35	$\mu A$
			$V_{DD} = 3V \pm 0.3V$				
$I_{DDS3}$	Stop mode (EXTAL and TEX pins oscillation stop)			10	$\mu A$		
	$V_{DD} = 5V \pm 0.5V$						

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C <sub>IN</sub>	PC, PD, PE0, PE2 to PE5, PF, PG, PI, CTLHEAD (+), CTLHEAD (-), CTLFAMPI (+), CTLFAMPI (-), CTLSAMPI, RFG, XTAL, TEX	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1  $\overline{\text{RST}}$  pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistor is selected.

\*2 When entire output pins are left open.

\*3 When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FEh) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	$t_{XL}$ , $t_{XH}$	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	$t_{CR}$ , $t_{CF}$	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	$t_{EH}$ , $t_{EL}$	$\overline{\text{EC}}$	Fig. 3	$t_{\text{sys}} + 200^{*1}$			ns
Event count clock input rise and fall times	$t_{ER}$ , $t_{EF}$	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	$f_c$	TEX TX	$V_{DD} = 2.7$ to $5.5\text{V}$ Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	$t_{TL}$ , $t_{TH}$	TEX	Fig. 3	10			$\mu\text{s}$
Event count clock input rise and fall times	$t_{TR}$ , $t_{TF}$	TEX	Fig. 3			20	ms

\*1  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (CLC; 00FEh) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

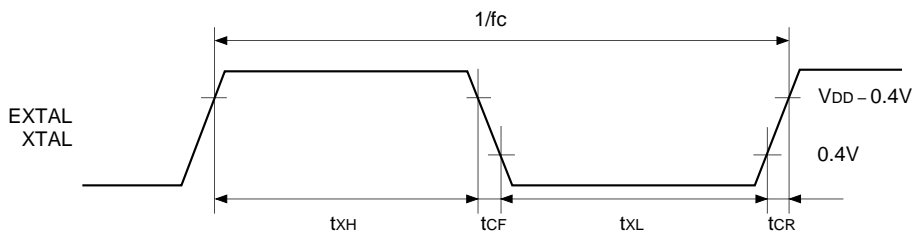


Fig. 1. Clock timing

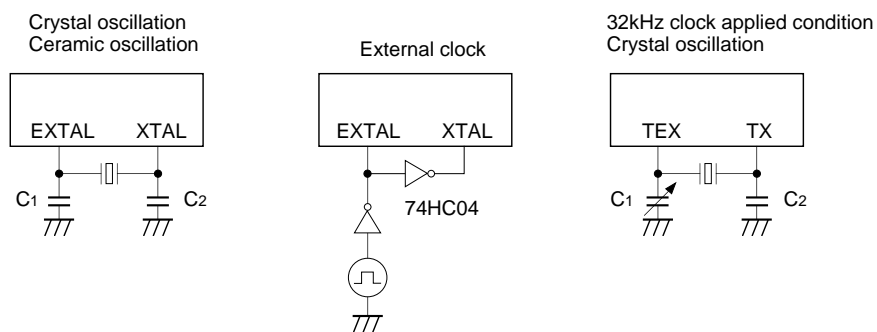


Fig. 2. Clock applied condition

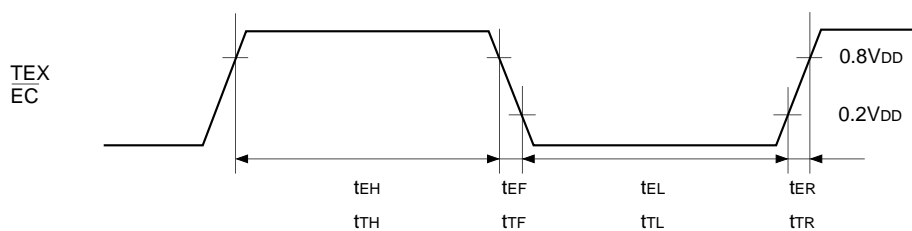


Fig. 3. Event count clock timing

## (2) Serial transfer (CH0)

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t <sub>DCSK</sub>	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t <sub>DCSKF</sub>	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t <sub>DCSOF</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}}$ high level width	t <sub>WHCS</sub>	$\overline{\text{CS0}}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY</sub>	$\overline{\text{SCK0}}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ high and low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{\text{SCK0}}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 100		ns
SI0 input set-up time (against $\overline{\text{SCK0}} \uparrow$ )	t <sub>SIK</sub>	SI0	$\overline{\text{SCK0}}$ input mode	-t <sub>sys</sub> + 100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$ )	t <sub>KSI</sub>	SI0	$\overline{\text{SCK0}}$ input mode	2t <sub>sys</sub> + 100		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t <sub>KSO</sub>	SO0	$\overline{\text{SCK0}}$ input mode		2t <sub>sys</sub> + 100	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

**Note 1** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC; 00FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

**Note 2** The load of  $\overline{\text{SCK0}}$  output mode and SO0 output delay time is 50pF + 1TTL.

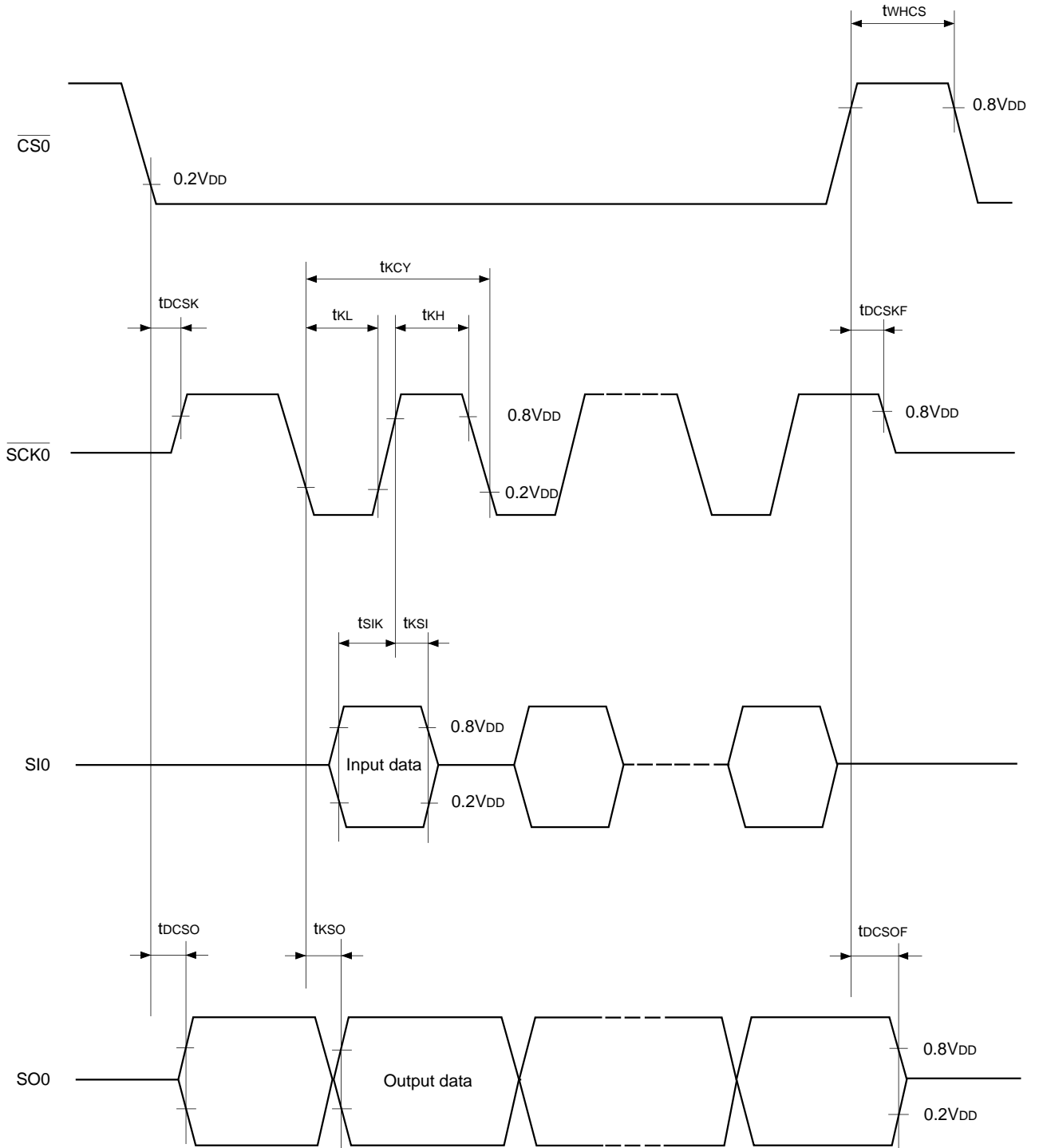


Fig. 4. Serial transfer timing (CH0)

**Serial transfer (CH1) (SIO mode)**

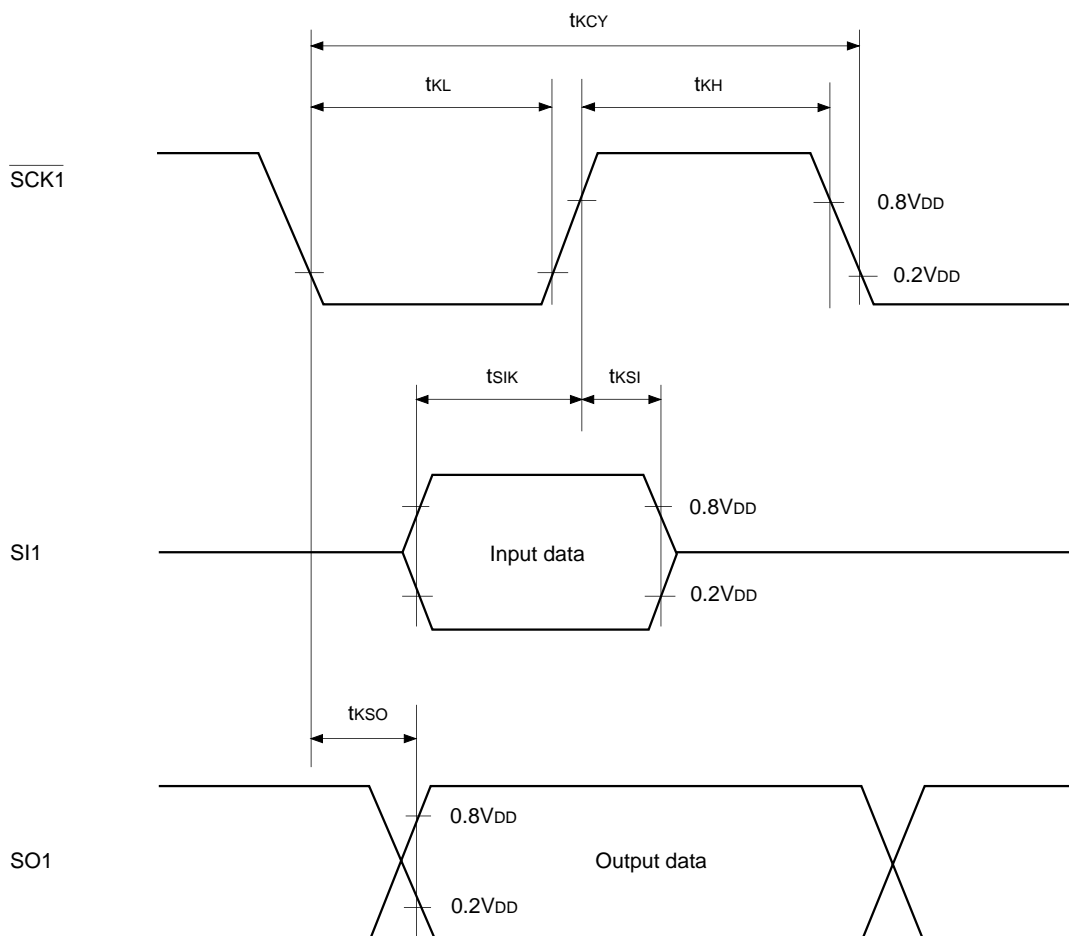
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/f_c \text{ (Upper 2 bits = "00")}, 4000/f_c \text{ (Upper 2 bits = "01")}, 16000/f_c \text{ (Upper 2 bits = "11")}$$

**Note 2)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .



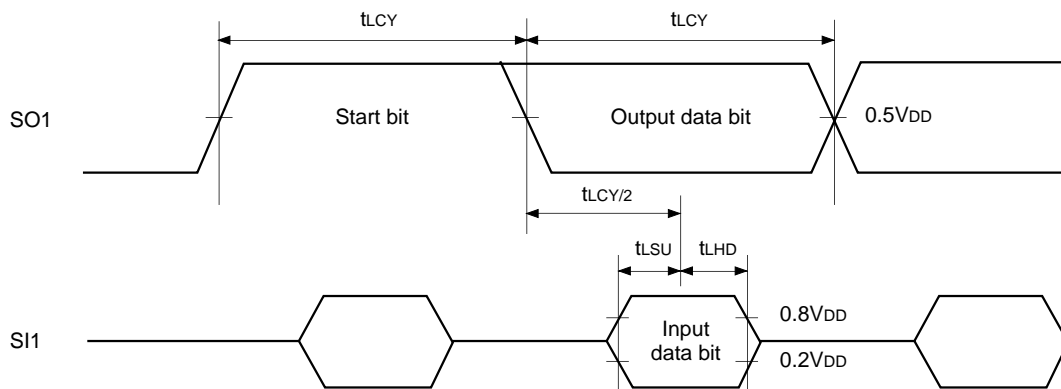
**Fig. 5. Serial transfer CH1 timing (SIO mode)**

**Serial transfer (CH1) (Special mode)** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}$	SO1 SI1	*1		104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

\*1  $t_{LCY}$  is specified only when serial mode register (CH1) (SIOM1: 05F2h) lower 2 bits (SO1 clock selection) are set at  $104\mu\text{s}$ .

**Note)** The load of SO1 pin is  $50\text{pF} + 1\text{TTL}$ .



**Fig. 6. Serial transfer CH1 timing (Special mode)**

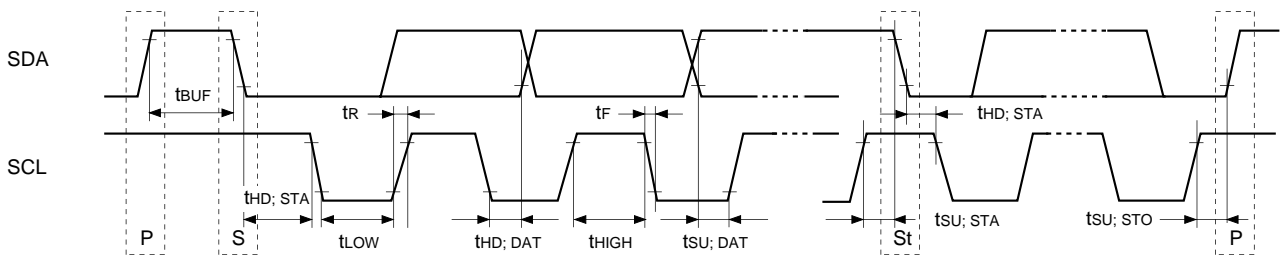


**Serial transfer (CH2)**

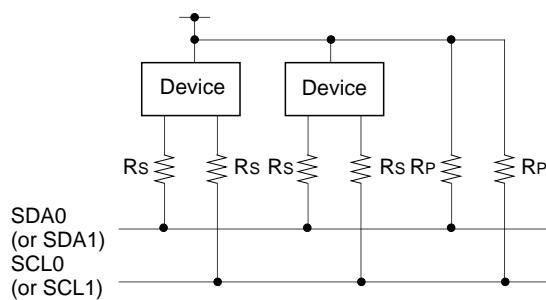
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	$f_{SCL}$	SCL			400	kHz
Bus-free time before starting transfer	$t_{BUF}$	SDA, SCL		2.6		$\mu\text{s}$
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		1.0		$\mu\text{s}$
Clock low level width	$t_{LOW}$	SCL		1.0		$\mu\text{s}$
Clock high level width	$t_{HIGH}$	SCL		1.0		$\mu\text{s}$
Setup time for repeated transfers	$t_{SU; STA}$	SDA, SCL		1.0		$\mu\text{s}$
Data hold time	$t_{HD; DAT}$	SDA, SCL		0*1		$\mu\text{s}$
Data set-up time	$t_{SU; DAT}$	SDA, SCL		100		ns
SDA, SCL rise time	$t_R$	SDA, SCL			300	ns
SDA, SCL fall time	$t_F$	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU; STO}$	SDA, SCL		1.6		$\mu\text{s}$

\*1 The SCL fall time (300ns Max.) is not included in the data hold time.



**Fig. 7. Serial transfer timing (CH2)**



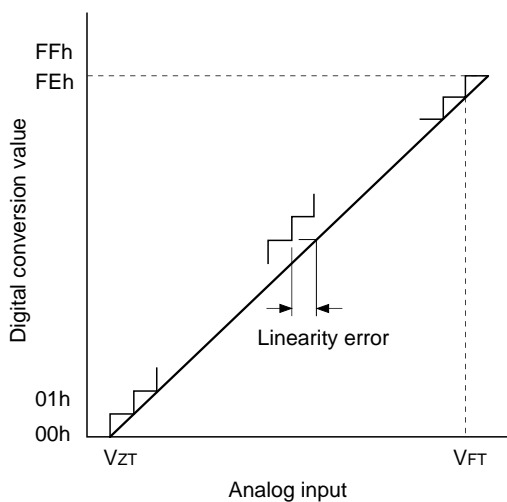
**Fig. 8. Device recommended circuit**

- A pull-up resistor ( $R_P$ ) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance ( $R_s = 300\Omega$  or less) can be used to reduce the spike noise caused by CRT flashover.

**(4) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 1$	LSB
Absolute error						$\pm 2$	LSB
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*1}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*1}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$		$AV_{DD} - 0.5$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	AN0 to AN7		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operating mode		0.6	1.0	mA
			Sleep mode Stop mode 32kHz operating mode			10	$\mu\text{A}$



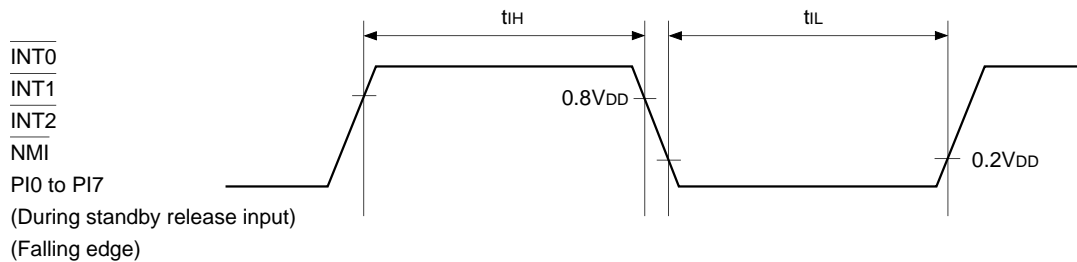
\*1  $f_{ADC}$  indicates the below values due to the peripheral clock control register (PCC: 05F8h) bit 3 and clock control register (CLC: 00FEh) upper 2 bits.

PCK1, PCK0	ADCCK	
	0 ( $\phi/2$ selection)	1 ( $\phi$ selection)
00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

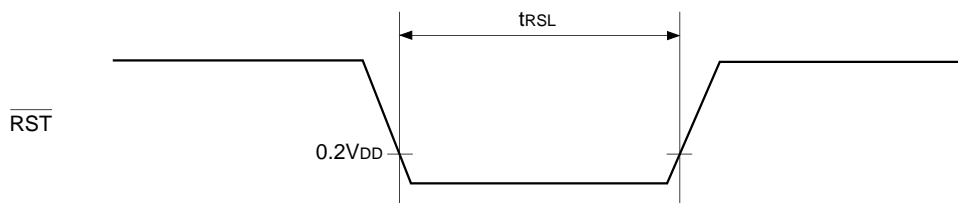
**Fig. 9. Definitions of A/D converter terms**

**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PI0 to PI7		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs



**Fig. 10. Interruption input timing**



**Fig. 11. Reset input timing**

**(5) Others** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t <sub>CFH</sub> t <sub> CFL</sub>	CFG		24t <sub>FRC</sub> + 200		ns
DFG input high and low level widths	t <sub>DFH</sub> t <sub> DFL</sub>	DFG		16t <sub>FRC</sub> + 200		ns
DPG minimum pulse width	t <sub>DPW</sub>	DPG		8t <sub>FRC</sub> + 200		ns
DPG minimum removal time	t <sub>rem</sub>	DPG		16t <sub>FRC</sub> + 200		ns
EXI input high and low level widths	t <sub>EIH</sub> t <sub> EIL</sub>	EXI0 EXI1	t <sub>sys</sub> = 2000/fc	8t <sub>FRC</sub> + 200 + t <sub>sys</sub>		ns

**Note 1)** t<sub>FRC</sub> = 1000/fc [ns]

**Note 2)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

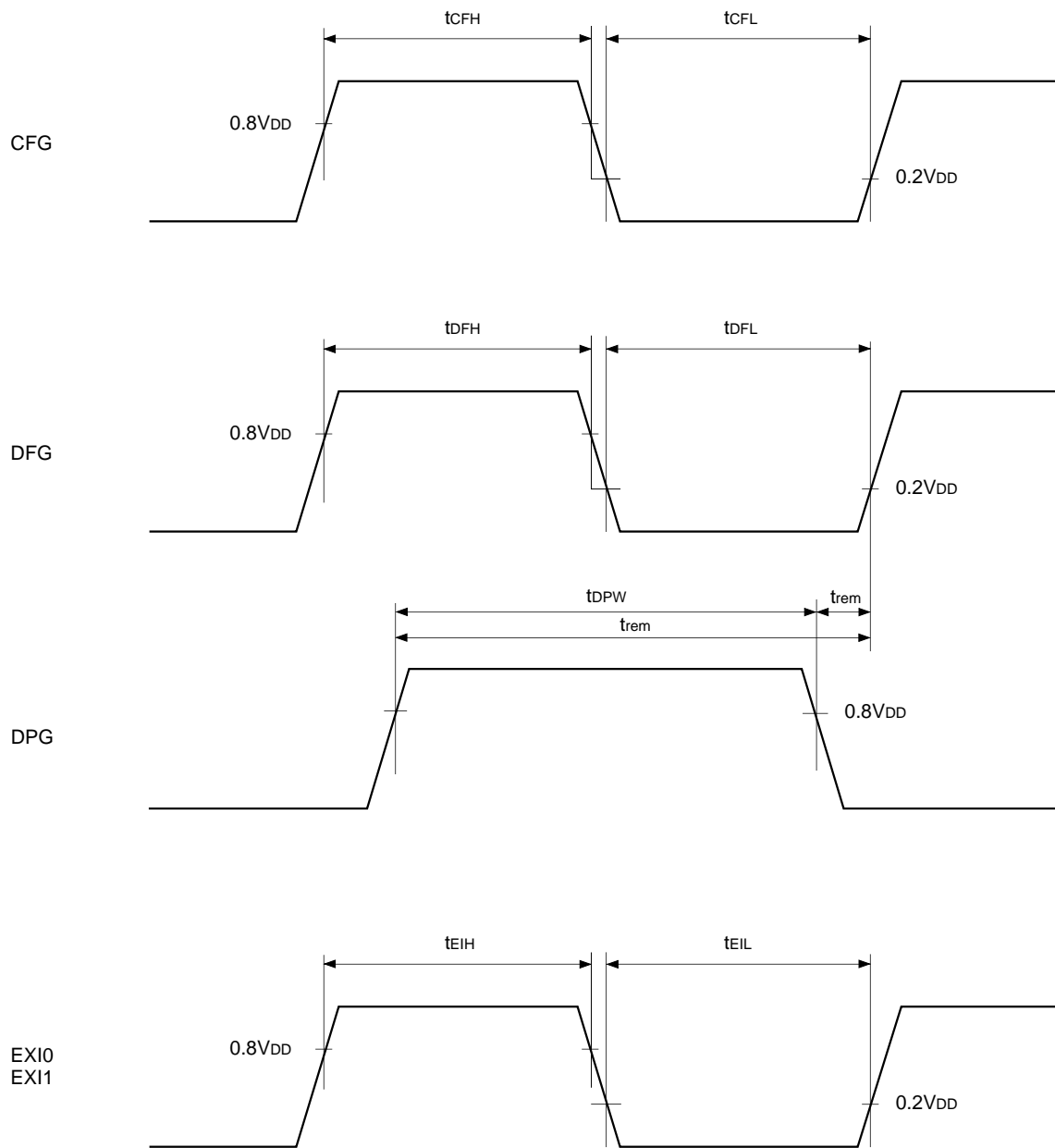


Fig. 12. Other timings

## Analog Circuit Characteristics

**(1) Amplifier circuit reference voltage characteristics** (AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V <sub>OR</sub>	CTLAGND		2.20	2.45	2.75	V

**(2) CTL 1st amplifier characteristics** (AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A <sub>VCTL1</sub>	CTLFAMPI (-) CTLFAMPI (+)	CTLFAMPI (-) = 0V, Gain = 16dB	13.5	15.5	17.5	dB
			CTLFAMPI (-) = 0V, Gain = 34dB	31.8	33.8	35.8	
			CTLFAMPI (-) = 0V, Gain = 49dB	46.5	48.5	50.5	
			CTLFAMPI (-) = 0V, Gain = 55dB	52.5	54.5	56.5	
Output offset voltage	V <sub>OSCTL1</sub>	CTLFAMPI (-) CTLFAMPI (+)	CTLFAMPI (-), CTLFAMPI (+) = open, Gain = 16dB	-25	0	+25	mV

\*1 The result after monitoring CTLFAMPO pin when the electrolytic capacitor (10μF) is connected to CTLFAMP (-) and CTLFAMP (+).

**(3) CTL 2nd amplifier characteristics** (AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*1	A <sub>VCTL2</sub>	CTLSAMPI	Gain = 5dB	3.5	5.5	7.5	dB
			Gain = 8dB	6.2	8.2	10.2	
			Gain = 11dB	9.0	11.0	13.0	
			Gain = 14dB	12.0	14.0	16.0	
			Gain = 17dB	15.0	17.0	19.0	
			Gain = 20dB	18.0	20.0	22.0	
Output offset voltage	V <sub>OSCTL2</sub>	CTLSAMPI	CTLSAMPI = open, Gain = 5dB	-30	0	+30	mV
LPF cut-off frequency	F <sub>CCTL</sub>	CTLSAMPI	12kHz, f <sub>DC</sub> - 3dB	8	12	24	kHz
			20kHz, f <sub>DC</sub> - 3dB	12	20	42	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Comparator level*2	V <sub>CCTL</sub>	CTLSAMPI	Comparator level = +100mV <sub>0-p</sub>	80	110	140	mV
			Comparator level = +150mV <sub>0-p</sub>	110	150	190	
			Comparator level = +200mV <sub>0-p</sub>	160	200	240	
			Comparator level = +250mV <sub>0-p</sub>	210	250	290	
			Comparator level = +300mV <sub>0-p</sub>	250	290	330	
			Comparator level = +400mV <sub>0-p</sub>	340	380	420	
			Comparator level = +500mV <sub>0-p</sub>	420	470	520	
			Comparator level = +600mV <sub>0-p</sub>	530	570	610	
			Comparator level = +1000mV <sub>0-p</sub>	850	920	990	
			Comparator level = -100mV <sub>0-p</sub>	-90	-120	-150	
			Comparator level = -150mV <sub>0-p</sub>	-110	-130	-190	
			Comparator level = -200mV <sub>0-p</sub>	-150	-190	-230	
			Comparator level = -250mV <sub>0-p</sub>	-200	-240	-280	
			Comparator level = -300mV <sub>0-p</sub>	-240	-280	-320	
			Comparator level = -400mV <sub>0-p</sub>	-340	-380	-420	
			Comparator level = -500mV <sub>0-p</sub>	-430	-480	-530	
			Comparator level = -600mV <sub>0-p</sub>	-540	-580	-620	
Comparator level = -1000mV <sub>0-p</sub>	-870	-970	-1070				

\*1 The result after monitoring ANOUT pin when the electrolytic capacitor (10μF) is connected to CTLSAMPI.

\*2 The reference value of the comparator level is CTLAGND.

**(4) CTL amplifier characteristics (CTL1stAMP + CTL2ndAMP)**

(AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain*3	A <sub>VCTL</sub>	CTLHEAD (-) CTLHEAD (+)	CTLHEAD (-) = 0V, Gain = (16dB + 5dB)	17.0	20.5	23.5	dB
			CTLHEAD (-) = 0V, Gain = (55dB + 20dB)	70.5	74.5	77.0	
Input sensitivity	V <sub>SCTL</sub>	CTLHEAD (-) CTLHEAD (+)	CTLHEAD (-) = 0V, Gain = (55dB + 20dB) Comparator = ±150mV <sub>0-p</sub>	60	70	140	μVp-p

\*3 The result when waveform is input from CTLHEAD (+) pin and ANOUT pin is monitored after performing coupling electrolytic capacitor (10μF) of CTLHEAD (-) and CTLHEAD (+), and coupling electrolytic capacitor (10μF) of HEADL (-) and HEADL (+), CTLFAMPI (-) and CTLFAMPI (+), and CTLFAMPO and CTLSAMPI. Gain is maximum -1.5dB lowered when waveform is input from CTLHEAD (+) pin.

**(5) RECCTL write circuit characteristics** (AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Write current*1	IOREC	CTLHEAD (-) CTLHEAD (+)	Write current 2.0mA <sub>p-p</sub>	0.8	1.8	3.6	mA
			Write current 3.0mA <sub>p-p</sub>	1.4	2.8	5.0	
			Write current 4.0mA <sub>p-p</sub>	2.0	3.8	7.0	
			Write current 5.0mA <sub>p-p</sub>	2.4	4.8	8.5	
			Write current 6.0mA <sub>p-p</sub>	3.0	6.0	10.0	
			Write current 7.0mA <sub>p-p</sub>	3.5	6.8	11.5	
			Write current 8.0mA <sub>p-p</sub>	4.5	7.8	13.0	
			Write current 9.0mA <sub>p-p</sub>	5.0	8.8	15.0	
			Write current 10.0mA <sub>p-p</sub>	5.5	7.7	17.0	

\*1 The current which flows when CTLHEAD (-) and CTLHEAD (+) shorts.

**(6) Auto threshold control circuit (ATC) characteristics**

(AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
ATC peak hold circuit initialize voltage value*2	V <sub>ATCINIT</sub>		Voltage = -150mV <sub>0-P</sub>	-110	-150	-190	mV
			Voltage = -400mV <sub>0-P</sub>	-350	-400	-450	
ATC comparator level offset voltage*3	V <sub>ATCOFF</sub>		Gain = 1/6 (16.7%)		-70	-160	mV
			Gain = 1/5 (20%)		-90	-210	
			Gain = 1/4 (25%)		-90	-210	
			Gain = 1/3 (33.3%)		-70	-160	
			Gain = 2/5 (40%)		-90	-210	
			Gain = 1/2 (50%)		-70	-160	
			Gain = 3/5 (60%)		-90	-210	

\*2 Reference is CTLAGND.

\*3 Reference is CTLAGND.

When comparator level is generated using ATC, actual comparator level is as follows by the offset voltage inside of ATC.

$$V_{in} \times \text{gain} + |\text{offset voltage}|$$

**Example:** Gain = 1/2

$$V_{in} \times 1/2 + 160$$

**(7) Schmitt characteristics**

(AMPV<sub>DD</sub> = V<sub>DD</sub> = 5.0V, AMPV<sub>SS</sub> = V<sub>SS</sub> = 0V, Ta = -20 to +75°C)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
RTG schmitt width	S <sub>RFG</sub>	RFG0, RFG1	Schmitt width 1V <sub>p-p</sub>	820	920	1020	mV
CFG/DFG/DPG	S <sub>CFG</sub> S <sub>DFG</sub> S <sub>DPG</sub>	CFG, DFG, DPG	Schmitt width 410mV <sub>p-p</sub>	180	300	420	mV
			Schmitt width 1V <sub>p-p</sub>	700	900	1100	

Appendix



Fig. 13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

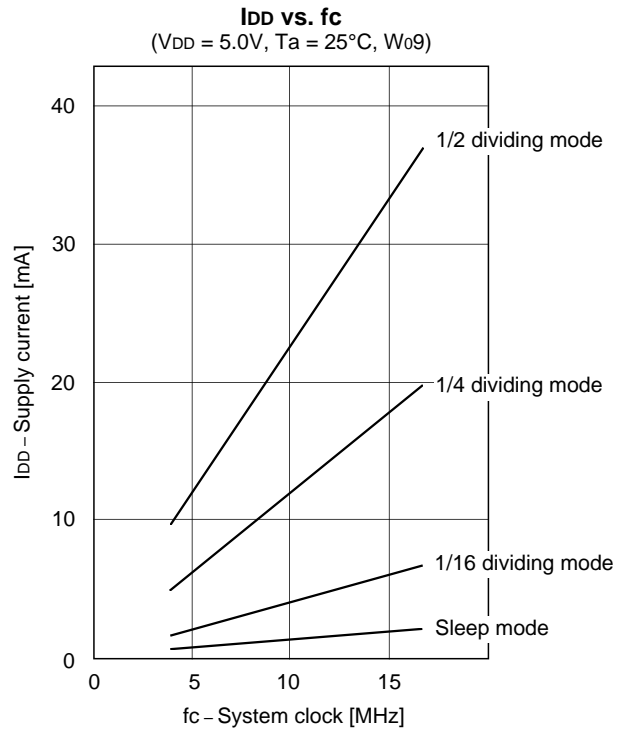
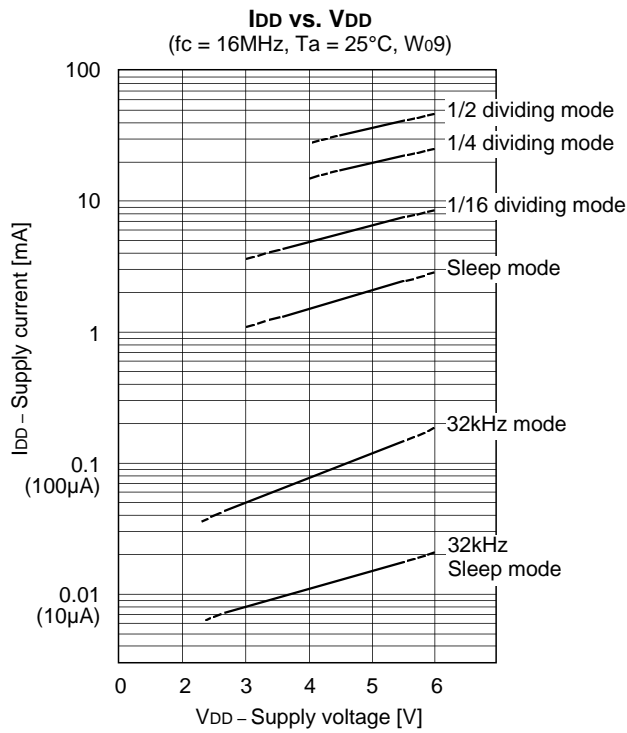
Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format*1	CMOS schmitt	TTL schmitt

\*1 The input circuit format can be selected for PE3/SYNC pin.

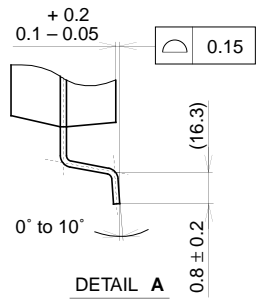
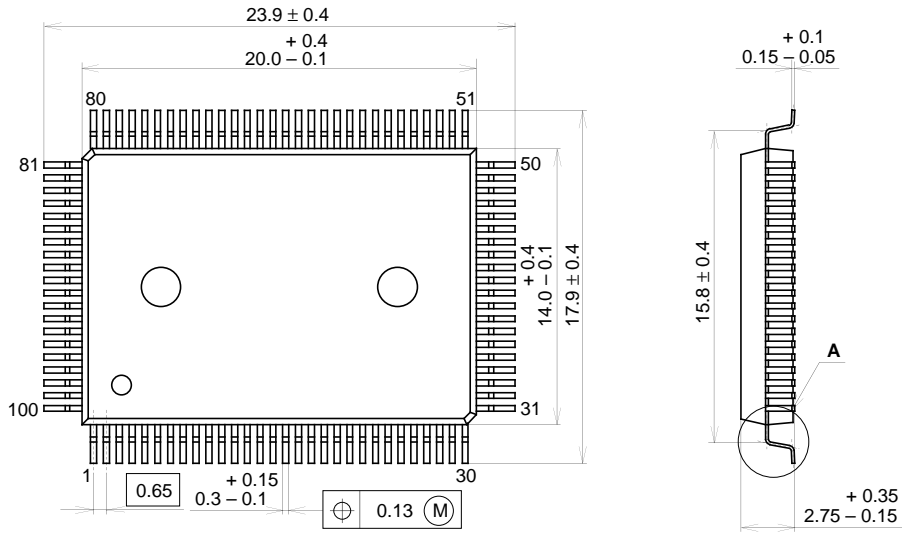


Characteristics Curve



Package Outline Unit: mm

100PIN QFP (PLASTIC)



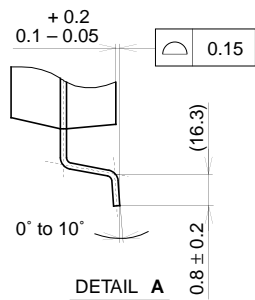
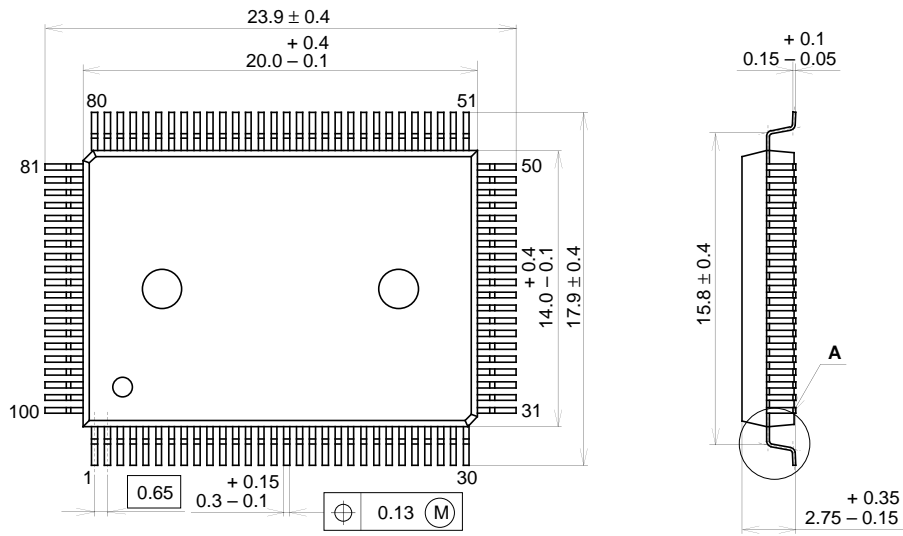
PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

Package Outline Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm