Ordering number : ENN*7143

CMOS IC

LC72311W, 72312W, 72313W

Low-Voltage ETR-Controller

Preliminary

Overview

The LC72311W, LC72312W, and LC72313W are low-voltage single-chip FM/AM electronic tuning microcontrollers that include a built-in PLL circuit for frequencies up to 230 MHz, a 1/4 duty 1/2 bias LCD controller, and a small EEPROM. These microcontroller also provide a low-power standby mode that reduces power consumption by switching the system clock frequency. Furthermore, since these devices include a low-pass filter amplifier required for the electronic tuning system and a tuning voltage generator circuit, they can contribute to reduced end product costs through lower parts counts.
These ICs are optimal for use in low-voltage portable audio equipment that includes a radio receiver.

Functions

- Program memory (ROM):
  — 8192 × 16 bits (16 KB) LC72311W
  — 16,384 × 16 bits (32 KB) LC72312W
  — 24,576 × 16 bits (48 KB) LC72313W
- Data memory (RAM):
  — 512 × 4 bits (RAM)
  — 512 × 4 bits (EEPROM)
- Cycle time:
  0.71 µs (at 4.2336 MHz) (All 1-word instructions)
  40 µs (at 75 kHz) (All 1-word instructions)
- Stack: 8 levels
- LCD driver:
  48 to 96 segments (1/4 duty 1/2 bias drive)
- Interrupts:
  Two external interrupt systems
  Internal timer interrupts: two systems (1, 5, 10, and 50 ms)
  Serial I/O interrupt (SIO0 only)
- A/D converter:
  Four-input 8-bit converter
- Input ports:
  9 or 10 ports (Ports PA, PF, and HCTR)
  The PF port is shared with the A/D converter, and HCTR is shared with the IF counter.
- Output ports:
  8 ports (Ports PB and PE)
  PE3 is shared with the BEEP pin, PE0 to PE2 are open-drain ports, and the PB port can be switched to function as an open-drain port.

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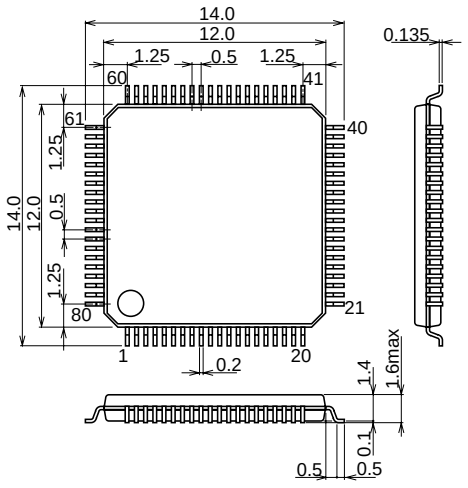
Package Dimensions

unit: mm

3220-SQFP80

[LC72311W, 72312W, 72313W]



SANYO: SQFP80

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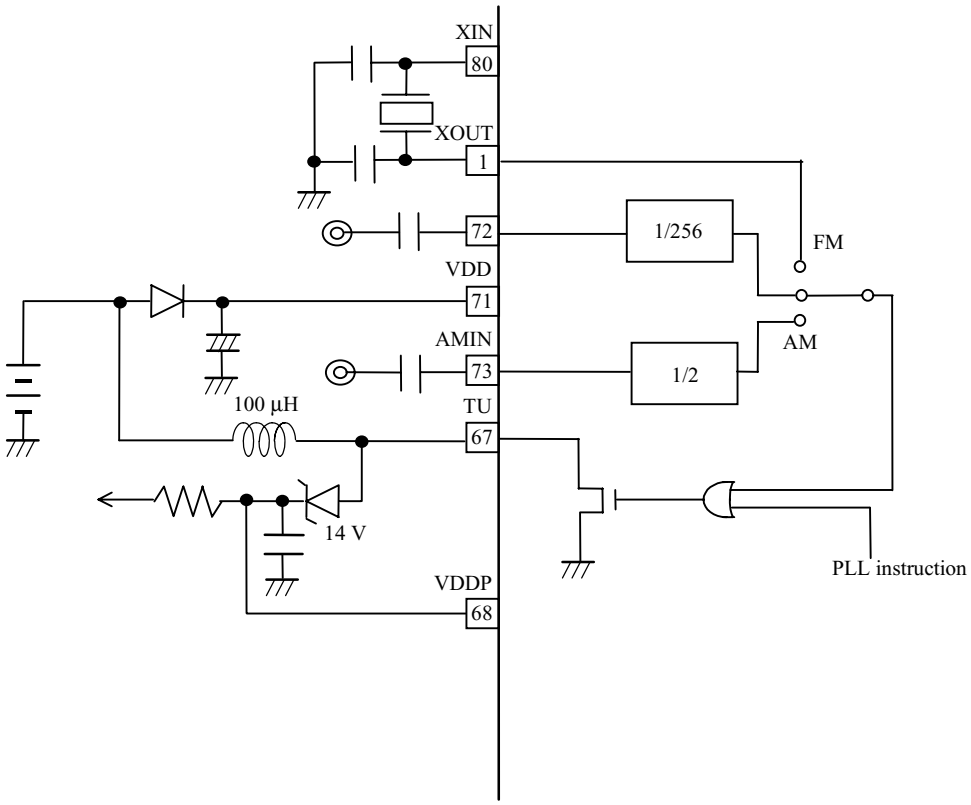
- I/O ports:
  22 ports (Ports PC, PD, PL, PI, PG, and PH)
  Port PD is shared with the interrupt function, ports PC and PK are shared with the serial I/O function, and ports PI, PG, and PH are shared with the LCD segment driver function.
- PLL:
  Provides dead band control (4 settings)
  Reference frequencies: 1, 3, 3.125, 5, 6.25, 12.5, and 25 kHz
- Input frequencies:
  FM band: 10 to 230 MHz
  AM band: 0.5 to 10 MHz
- Input sensitivity:
  FM band: 35 mVrms (130 MHz to 50 mVrms)
  AM band: 35 mVrms
- HCTR:
  IF counter (0.4 to 15 MHz)
- External reset pin:
  Starts the PC from address 0 during CPU and PLL operation.
- Built-in power-on reset circuit:
  Starts the PC from address 0 at power on.
- Halt mode:
  Temporarily slows the microcontroller operating clock and reduces power consumption.
- Backup mode:
  Stops the crystal oscillator circuit.
- Static power on:
  Backup mode can be cleared with the PF port.
- BEEP:
  Seven alarm tones: 0.75, 1.25, 1.5, 2.08, 2.5, 3.125, and 6.25 kHz.
- Serial I/O:
  Two channels (These functions use the PC and PK port pins.)
  The internal serial transfer clock provides three frequencies: 12.5, 25, and 75 kHz.
- On-chip low-pass filter amplifier:
  Reduces end product parts counts and costs.
- Tuning voltage generator circuit:
  Obviates the need for an external tuning power supply circuit for reduced end product parts counts and costs.
- Memory retention voltage:
  Over 0.9 V.
- VDD voltage:
  PLL circuit: 1.8 to 3.6 V
  CPU and A/D converter:
  1.6 to 3.6 V (For a 40 μs instruction cycle)
  2.4 to 3.6 V (For a 0.71 μs instruction cycle)
- Option selections:
  PH0 to PH3/S13 to S16
  PG0 to PG3/S17 to S20
  PI0 to PI3/S21 to S24
  Vsense circuit present/absent
- Package:
  SQFP80 (0.5 mm lead pitch)

Tuning Voltage Generator Circuit



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +4.0	V
	VDDPmax		–0.3 to +16.0	V
Input voltage	V_{IN}	All input pins	–0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	AOUT, PE0 to 2, TU	–0.3 to +15	V
	$V_{OUT}2$	All output pins other than $V_{OUT}1$	–0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	PC, PD, PE3, PG, PH, PI, PK, PL, EO	0 to 3	mA
	$I_{OUT}2$	PB	0 to 1	mA
	$I_{OUT}3$	AOUT, PE0 to 2, TU	0 to 2	mA
	$I_{OUT}4$	S1 to S24	300	μA
	$I_{OUT}5$	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –20 to +70°C	300	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –20 to +70°C, V_{DD} = 1.8 to 3.6 V

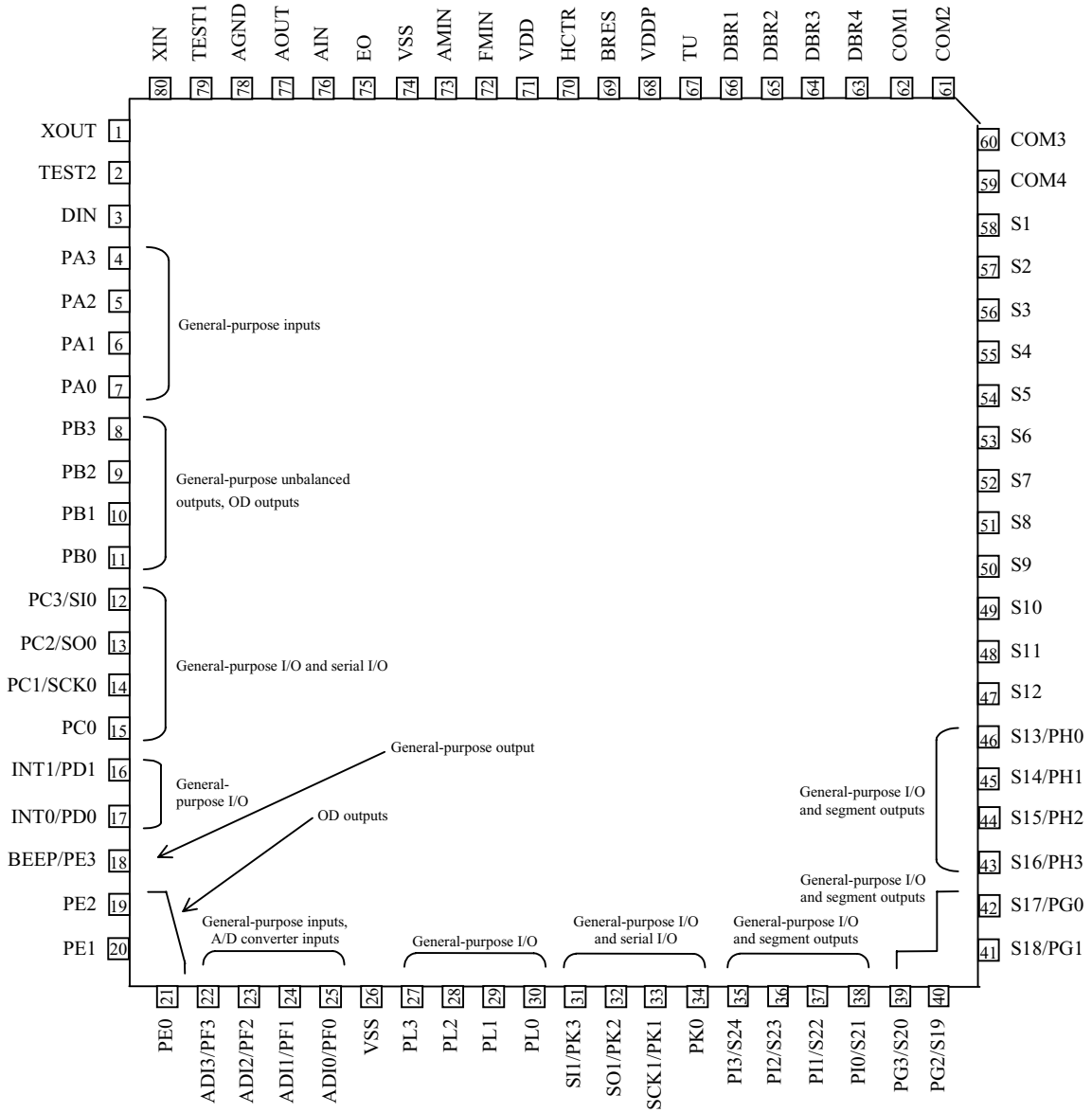
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	PLL operating voltage	1.8	3.0	3.6	V
	$V_{DD}2$	Memory retention voltage	1.0			
	$V_{DD}3$	CPU operating voltage	1.6	3.0	3.6	
	$V_{DD}4$	A/D converter operating voltage	1.6	3.0	3.6	
	VDDP1	Voltage applied to the VDDP pin	13	14	15	
High-level input voltage	$V_{IH}1$	Input ports other than $V_{IH}2$, $V_{IH}3$, AMIN, FMIN, HCTR, XIN, and DIN (with amplifier circuit)	0.7 V_{DD}		V_{DD}	V
	$V_{IH}2$	BRES	0.8 V_{DD}		V_{DD}	V
	$V_{IH}3$	The PF port	0.6 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Input ports other than $V_{IL}2$, $V_{IL}3$, AMIN, FMIN, HCTR, XIN, and DIN (with amplifier circuit)	0		0.3 V_{DD}	V
	$V_{IL}2$	BRES	0		0.2 V_{DD}	V
	$V_{IL}3$	The PF port	0		0.2 V_{DD}	V
Input amplitude	$V_{IN}1$	XIN	0.5		0.6	Vrms
	$V_{IN}2$	FMIN,AMIN	0.035		0.35	Vrms
	$V_{IN}3$	FMIN	0.05		0.35	Vrms
	$V_{IN}4$	HCTR and DIN (with amplifier circuit)	0.035		0.35	Vrms
Input voltage range	$V_{IN}6$	ADI0, ADI1, ADI2, ADI3	0		V_{DD}	V
Input frequency	$F_{IN}1$	XIN CI ≤ 35 kΩ	70	75	80	kHz
	$F_{IN}2$	FMIN: $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$F_{IN}3$	FMIN: $V_{IN}3$, $V_{DD}1$	130		230	MHz
	$F_{IN}4$	AMIN (H): $V_{IN}2$, $V_{DD}1$	2		40	MHz
	$F_{IN}5$	AMIN (L): $V_{IN}2$, $V_{DD}1$	0.5		10	MHz
	$F_{IN}6$	HCTR: $V_{IN}4$, $V_{DD}1$	0.4		12	MHz
	$F_{IN}7$	DIN (with amplifier circuit): $V_{IN}4$, $V_{DD}1$	2		18	MHz
	$F_{IN}8$	DIN (without amplifier circuit): $V_{IH}1$, $V_{DD}1$	2		18	MHz

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	$I_{IH}1$	XIN: VI = V_{DD} = 3.0 V			3	µA
	$I_{IH}2$	FMIN, AMIN, HCTR, DIN (with amplifier circuit): VI = V_{DD} = 3.0 V	3	8	20	µA
	$I_{IH}3$	The PA/PF (without pull-down resistors), PC, PD, PG, PH, PI, PK, and PL ports, BRES, and DIN (without amplifier circuit): VI = V_{DD} = 3.0 V			3	µA
Low-level input current	$I_{IL}1$	XIN: VI = V_{DD} = V_{SS}			–3	µA
	$I_{IL}12$	FMIN, AMIN, HCTR, DIN (with amplifier circuit): VI = V_{DD} = V_{SS}	–3	-8	–20	µA
	$I_{IL}13$	The PA/PF (without pull-down resistors), PC, PD, PG, PH, PI, PK, and PL ports, BRES, and DIN (without amplifier circuit): VI = V_{DD} = 3.0 V			–3	µA
Input floating voltage	V_{IF}	The PA and PF ports with pull-down resistors			0.05 V_{DD}	V
Pull-down resistors	$R_{PD}1$	The PA and PF ports with pull-down resistors: V_{DD} = 3.0 V	75	100	200	kΩ
	$R_{PD}2$	The TEST1 and TEST2 resistor		10		kΩ
Hysteresis	V_H	BRES	0.1 V_{DD}	0.2 V_{DD}		V
Voltage doubler reference voltage	DBR4	V_{DD} reference C (3) = 0.47 µF, Ta = 25°C (Note 1)	1.3	1.5	1.7	V
Voltage doubler step-up voltage	DBR1, 2, 3	C (1) = 0.47µF C (2) = 0.47µF No output load, Ta = 25°C (Note 1)	2.7	3.0	3.3	V
High-level output voltage	$V_{OH}1$	PB:IO = –1 mA	V_{DD} – 0.7 V_{DD}		V_{DD} – 0.3 V_{DD}	V
	$V_{OH}2$	PC, PD, PG, PH,PI, PK, PL:IO = –1 mA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}3$	EO: IO = –500 µA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}4$	XOUT: IO = –200 µA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}5$	S1 to S24: IO = –20 µA ∗1	2.0			V
	$V_{OH}6$	COM1, COM2, COM3, COM4: IO = –100µA ∗1	2.0			V
Low-level output voltage	$V_{OL}1$	PB: IO = –50 µA	0.3 V_{DD}		0.7 V_{DD}	V
	$V_{OL}2$	PC, PD, PE3, PG, PH, PI, PK, PL:IO = –1 mA			0.3 V_{DD}	V
	$V_{OL}3$	EO: IO = –500 µA			0.3 V_{DD}	V
	$V_{OL}4$	XOUT: IO = –200 µA			0.3 V_{DD}	V
	$V_{OL}5$	S1 to S24: IO = –20 µA ∗1			1.0	V
	$V_{OL}6$	COM1, COM2, COM3, COM4: IO = –100µA ∗1			1.0	V
	$V_{OL}7$	PE0 to 2: IO = 2 mA			1.0	V
	$V_{OL}8$	AOUT, TU: IO = 1 mA AIN = 1.3 V V_{DD} = 3 V			0.5	V
Output off leakage current	$I_{OFF}1$	Ports PB, PC, PD, PE3, PG, PH, PI, PK, PL, and EO	–3		+3	µA
	$I_{OFF}2$	AOUT, TU, and PE0 to PE2	–100		+100	nA
A/D converter error		ADI0, ADI1, ADI2, ADI3	–3/2		+3/2	LSB
Voltage drop detection voltage	$V_{SENSE}1$	Ta = 25°C ∗2	1.6	1.75	1.9	V
Voltage rise detection voltage	$V_{SENSE}2$	Ta = 25°C ∗2	(1) min +0.1		(1) max +0.2	V
Current drain	$I_{DD}1$	V_{DD}1: FIN (2) 130 MHz Ta = 25°C		10		mA
	$I_{DD}2$	V_{DD}2: Halt mode, Ta = 25°C ∗3		0.1		mA
	$I_{DD}3$	V_{DD} = 3.6 V, with the oscillator stopped,Ta = 25°C ∗4		1		µA
	$I_{DD}4$	V_{DD} = 2.4 V, with the oscillator stopped,Ta = 25°C ∗4		0.5		µA

With the halt mode current, this IC can execute 20 instruction steps every 125 ms.

Pin Assignment



Pin Functions

Pin No.	Pin	I/O	Function
80 1	XIN XOUT	I O	Connections for a 75 kHz crystal oscillator
79 2	TEST1 TEST2	I I	IC testing. These pins must be tied to ground.
4 5 6 7	PA3 PA2 PA1 PA0	I	General-purpose inputs with built-in pull-down resistors. The pull-down resistors are selected using the IOS instruction (IOS 2, b1). Note that the pull-down resistors cannot be selected individually for each pin. When these inputs are used in conjunction with port PB (unbalanced outputs) to form a key matrix circuit, multiple key presses of up to up to 3 keys can be detected.
8 9 10 11	PB3 PB2 PB1 PB0	O	The IOS instruction (IOS 2, b0, b2, b3) is used to select between the unbalanced output and open drain output circuit types. When the unbalanced type output circuit is selected, these outputs can be used in conjunction with port PA to form a key matrix circuit that can detect multiple key presses. If the general-purpose output function is selected, care is required to prevent problems related to impedance. If the open-drain output circuit is selected, the maximum output voltage will be VDD, and pull-up resistors will be required.
12 13 14 15	PC3/SI0 PC2/SO0 PC1/SCK0 PC0	I/O	General-purpose I/O ports and serial I/O ports. The I/O direction of these general-purpose ports can be selected in 1-bit units with the IOS instruction (IOS 4, b0 to b3). The IOS instruction (IOS 3, b2) is used to switch between the general-purpose input and the serial I/O functions.
16 17	INT1/PD1 INT0/PD0	I/O I/O	The I/O directions of the PD port pins can be selected in 1-bit units with the IOS instruction (IOS 5, b1, b2). The PD port pins can be used as interrupt input pins. For this use, the pin I/O direction must be set to input.
18	BEEP/PE3	O	BEEP output and general-purpose output. The BEEP instruction is used to switch the pin function. The output circuit is a CMOS push-pull circuit.
19 20 21	PE2 PE1 PE0	O	N-channel open-drain port. These port pins require pull-up resistors.
22 23 24 25	ADI3/PF3 ADI2/PF2 ADI1/PF1 ADI0/PF0	I	General-purpose input/A/D converter input shared function port. The IOS instruction (IOS F, b0 to b3) is used to switch between the general-purpose input and A/D converter input functions. All of these ports can be used to recover from backup mode. The IOS instruction (IOS 0, b0 to b3) is used to select which ports are used for recovery from backup mode. The A/D converter is an 8-bit successive approximation A/D converter and VDD is the full-scale voltage.
27 28 29 30	PL3 PL2 PL1 PL0	I/O	PL0 is a general-purpose I/O port. The I/O direction of these general-purpose port pins can be selected in 1-bit units with the IOS instruction (IOS B, b0 to b3).
31 32 33 34	SI1/PK3 SO1/PK2 SCK1/PK1 PK0	I/O	General-purpose I/O ports. The I/O direction of these general-purpose port pins can be selected in 1-bit units with the IOS instruction (IOS C, b0 to b3). PK1 to PK3 are general-purpose input or serial I/O ports. The IOS instruction (IOS 3, b3) is used to switch between the general-purpose input and serial I/O port functions.
35 36 37 38 39 40 41 42 43 44 45 46	PI3/S24 PI2/S23 PI1/S22 PI0/S21 PG3/S20 PG2/S19 PG1/S18 PG0/S17 PH3/S16 PH2/S15 PH1/S14 PH0/S13	I/O	LCD driver segment output and general-purpose I/O shared function ports. The IOS instruction is used to set the I/O direction for these pins used as general-purpose I/O pins. Port PI: IOS 8, b0 to b3 Port PH: IOS 7, b0 to b3 Port PG: IOS 6, b0 to b3 A combination of mask options and the IOS instruction are used to select the segment output and general-purpose port functions. The function can be selected in 1-bit units. Port PI: IOS D, b0 to b3 Port PH: IOS C, b0 to b3 Port PG: IOS B, b0 to b3

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Pin No.	Pin	I/O	Function
47 to 58	S12 to S1	O	LCD driver segment outputs. This circuit implements a 1/4 duty 1/2 bias LCD drive technique. The frame frequency is 75 Hz. An output voltage of 3 V is maintained for VDD in the range 1.8 to 3.6 V.
59 60 61 62	COM4 COM3 COM2 COM1	O	LCD driver segment outputs. This circuit implements a 1/4 duty 1/2 bias LCD drive technique. The frame frequency is 75 Hz. An output voltage of 3 V is maintained for VDD in the range 1.8 to 3.6 V.
63 64 65 66	DBR4 DBR3 DBR2 DBR1		LCD power supply step-up voltage outputs
69	BRES	I	System reset. A system reset is applied if a low level is applied to this pin for at least 1 machine cycle in either CPU operating mode or halt mode. The PC is set to 0 and program execution is started. In backup mode, applying a low level to this pin clears backup mode.
67	TU	–	Tuning voltage generation circuit. This IC provides an internal transistor, and a circuit that generates the tuning voltage (12 to 14 V) can be formed on this pin with external coil, Zener diode, and capacitor components.
72	FMIN	I	FM VCO (local oscillator) input. This pin is selected with CW1 in the PLL instruction. The input must be capacitor coupled. The input frequency is 10 to 230 MHz.
73	AMIN	I	AM VCO (local oscillator) input. This pin is selected with CW1 in the PLL instruction. The input must be capacitor coupled. The input frequency is 0.5 to 10 MHz.
70	HCTR	I	IF counter input and general-purpose input shared function pin. The IOS instruction (IOS 1, b3) is used to switch between these functions. If the IF counter is used, use a capacitor-coupled input, and use the UCC instruction to start and stop the counter. The input frequency range is 0.4 to 12 MHz. If the general-purpose input function is used, use the INR instruction to acquire the input data.
75	EO	O	Main charge pump output. If the frequency created by dividing the local oscillator frequency by N is higher than the reference frequency, a high level is output. If that frequency is lower than the reference, a low level is output. If the frequencies match, this pin goes to the high-impedance state.
3	DIN	I	Clock input from a CD DSP or other IC. The input frequency can be switched between 1/1, 1/2, and 1/4. A frequency range of from 4 to 4.5 MHz is used for the internal clock frequency. This pin can be used to form a self-oscillating circuit by connecting a capacitor. These functions are all switched with the DIN instruction.
68	VDDP		The internal EEPROM power supply. If the EEPROM is used, apply a 14 V level to this pin. The TU pin output can be used for this 14 V level.
76 77 78	AIN AOUT AGND	–	Connections for the low-pass filter amplifier transistor. Connect AGND to ground.
71 26 74	V_{DD} V_{SS} V_{SS}	–	Power supply.