EPD Systems Engineering Technical Bulletin

JTAG Boundary Scan Initialization on the AMD 29K Family

The Am29030™ and Am29035™ microprocessors and the Am29200™, Am29240™, Am29245™ and Am29243™ microcontrollers incorporate a five-pin Joint Test Action Group (JTAG) Boundary Scan Interface and Test Access Port that provides a scan interface to testing and debug features of the processor core. Improper initialization of the JTAG interface can cause intermittent and unpredictable behavior. This bulletin describes design requirements for proper initialization of the interface on the 29K Family of products, and supersedes the Technical Bulletin with PID#18010A.

The Test Access (JTAG) port can access, affect and sample the processor inputs and outputs because a boundary scan register is incorporated into the design of the input and output cells. For correct processor initialization in all cases, the $\overline{\text{TRST}}$ signal *must* be asserted in conjunction with the $\overline{\text{RESET}}$ input, whether or not the JTAG port is used. What follows is a recommended method for insuring that this occurs.

Tie $\overline{\text{TRST}}$, the test reset input, to system RESET so that the JTAG logic is initialized at power-on.

If the JTAG port is not to be used, drive $\overline{\text{TCK}}$, $\overline{\text{TMS}}$ and $\overline{\text{TDI}}$ to known states, preferably through pull-up resistors. Although these signals have weak internal active pull-ups, tying them to a known signal level will eliminate any system noise from being coupled into the JTAG interface.

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