NBVSPA013

2.5 V, 212.00 MHz LVDS Voltage-Controlled Clock Oscillator (VCXO) PureEdge™ Product Series

The NBVSPA013 voltage−controlled crystal oscillator (VCXO) is designed to meet today's requirements for 2.5 V LVDS clock generation applications. These devices use a high Q fundamental mode crystal and Phase Locked Loop (PLL) multiplier to provide 212.00 MHz with a pullable range of ±100 ppm and a frequency stability of ±50 ppm. The silicon−based PureEdge™ products design provides users with exceptional frequency stability and reliability. They produce an ultra low jitter and phase noise LVDS differential output.

The NBVSPA013 is a member of ON Semiconductor's PureEdge clock family that provides accurate and precision clock generation solutions.

Available in the industry standard 5.0 x 7.0 x 1.8 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000 and 100.

Features

- LVDS Differential Output
- Uses High Q Fundamental Mode Crystal
- Ultra Low Jitter and Phase Noise − 0.5 ps (12 kHz − 20 MHz)
- Pullable Range Minimum of ±100 ppm
- Frequency Stability of ±50 ppm
- Control Voltage with Positive Slope
- Voltage Control Linearity of ±10%
- Hermetically Sealed Ceramic SMD Packages of size 5.0 x 7.0 x 1.8 mm
- Operating Range: 2.5 V ±5%
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Networking
- Networking Base Stations
- Broadcasting

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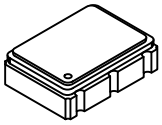
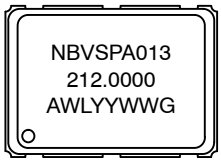


6 PIN CLCC
LN SUFFIX
CASE 848AB

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

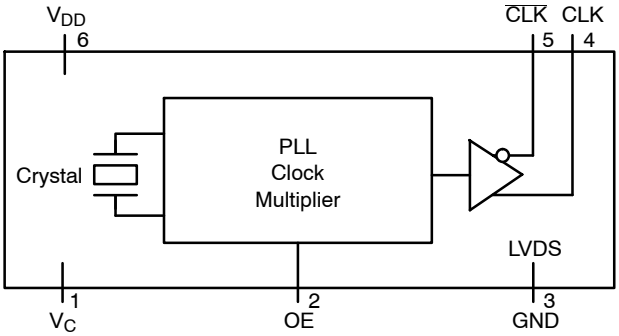


Figure 1. Simplified Logic Diagram

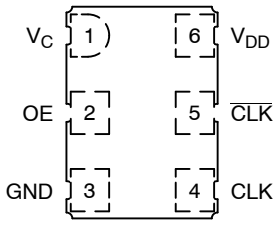


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_C (Note 1)	Analog Input	Analog control voltage input pin that adjusts output oscillation frequency. $f_0 = V_C$ = 1.25 V
2	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
3	GND	Power Supply	Ground at 0 V. Electrical and Case Ground.
4	CLK	LVDS Output	Non−Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	$\overline{CLK}$	LVDS Output	Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
6	V_{DD}	Power Supply	Positive Power Supply Voltage. Voltage should not exceed 2.5 V ±5%.

1. Control voltage has a positive slope with a typical linearity of ±10%; V_C = 1.25 V ± 1 V.

Table 2. OUTPUT ENABLE TRI−STATE FUNCTION

OE Pin	Output Pins
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. ATTRIBUTES

Characteristic		Value
Input Default State Resistor		170 kΩ
ESD Protection	Human Body Model Machine Model	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_{IN}	Control Input (V_C and OE)		$V_{IN} \le V_{DD}$ + 200 mV $V_{IN} \ge$ GND − 200 mV		V
I_{OSC}	Output Short Circuit Current CLK to $\overline{CLK}$ CLK or $\overline{CLK}$ to GND	Continuous Continuous		12 24	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−55 to +120	°C
T_{sol}	Wave Solder	See Figure 5		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS (V_{DD} = 2.5 V ±5%, GND = 0 V, T_A = −40°C to +85°C) (Note 2)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current			75	100	mA
V_{IH}	OE and FSEL Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	OE and FSEL Input LOW Voltage		GND − 300		800	mV
I_{IH}	Input HIGH Current OE		−100		+100	μA
I_{IL}	Input LOW Current OE		−100		+100	μA
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States	(Note 3)	0	1	25	mV
V_{OS}	Offset Voltage		1125		1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	(Note 3)	0	1	25	mV
V_{OH}	Output HIGH Voltage			1425	1600	mV
V_{OL}	Output LOW Voltage		900	1075		mV
V_{OD}	Differential Output Voltage		250		450	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 4.
3. Parameter guaranteed by design verification not tested in production.

Table 6. AC CHARACTERISTICS (V_{DD} = 2.5 ±5%, GND = 0 V, T_A = −40°C to +85°C) (Note 4)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Unit
f_{CLKOUT}	Output Clock Frequency	NBVSPA013		212.00		MHz
Δf	Frequency Stability	(Note 5)			±50	ppm
$t_{jit}(\phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.4	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		3	8	ps
	Cycle to Cycle, Peak−to−Peak	1000 Cycles		15	30	ps
	Period, RMS	10,000 Cycles		2	4	ps
	Period, Peak−to−Peak	10,000 Cycles		10	20	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
F_P	Crystal Pullability (Note 6)	$0 V \le V_C \le V_{DD}$	±100			ppm
$V_{C(bw)}$	Control Voltage Bandwidth	−3 dB	20			KHz
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		45	50	55	%
t_R	Output Rise Time (20% and 80%)			245	400	ps
t_F	Output Fall Time (80% and 20%)			245	400	ps
t_{start}	Start−up Time			1	5	ms
	Aging	1st Year			3	ppm
		Every Year After 1st			1	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 4.
5. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration and first year aging.
6. Gain transfer is positive with a rate of 130 ppm/V.

Table 7. PHASE NOISE PERFORMANCE FOR NBVSPA013

Parameter	Characteristic	Condition	212.00 MHZ	Unit
ϕ_{NOISE}	Output Phase−Noise Performance	100 Hz of Carrier	−82	dBc/Hz
		1 kHz of Carrier	−110	dBc/Hz
		10 kHz of Carrier	−122	dBc/Hz
		100 kHz of Carrier	−123	dBc/Hz
		1 MHz of Carrier	−132	dBc/Hz
		10 MHz of Carrier	−160	dBc/Hz

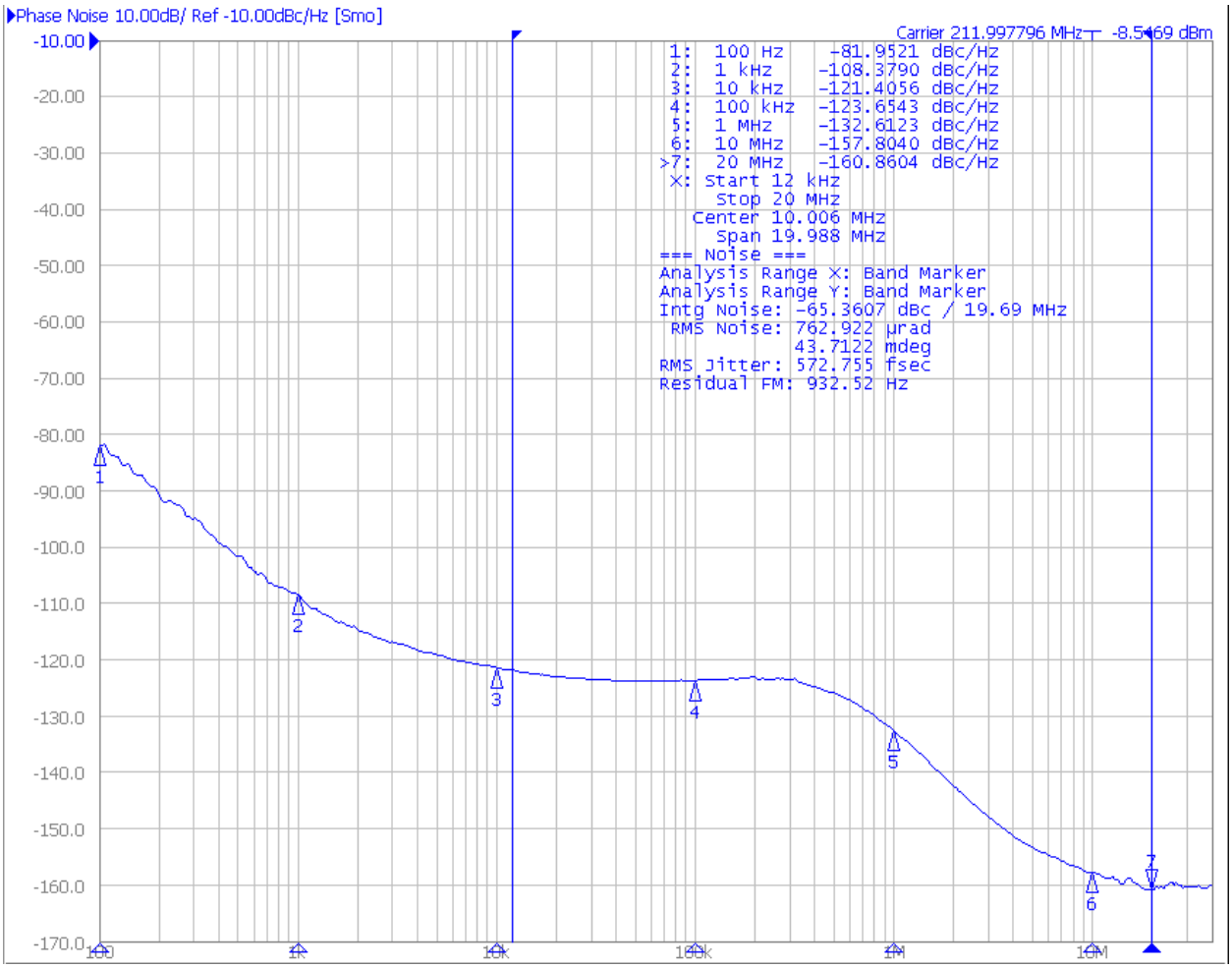


Figure 3. Typical Phase Noise Plot at 212.00 MHz

Table 8. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL−STD−833, Method 2002, Condition B
Solderability	Mechanical	MIL−STD−833, Method 2003
Vibration	Mechanical	MIL−STD−833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL−STD−202, Method 215
Thermal Shock	Environment	MIL−STD−833, Method 1011, Condition A
Moisture Level Sensitivity	Environment	MSL1 260°C per IPC/JEDEC J−STD−020D

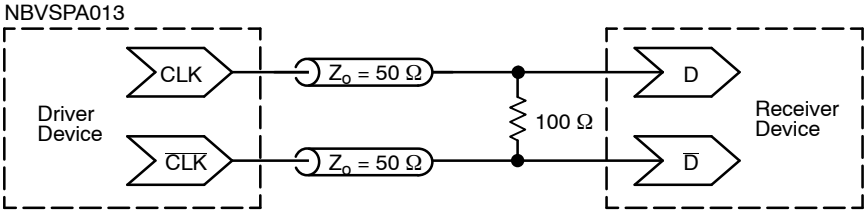


Figure 4. Typical Termination for Output Driver and Device Evaluation

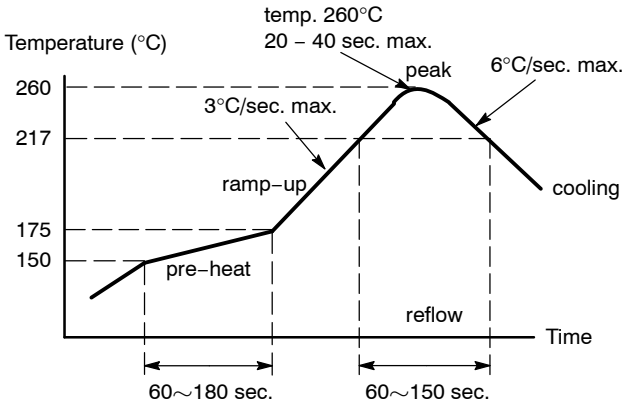


Figure 5. Recommended Reflow Soldering Profile

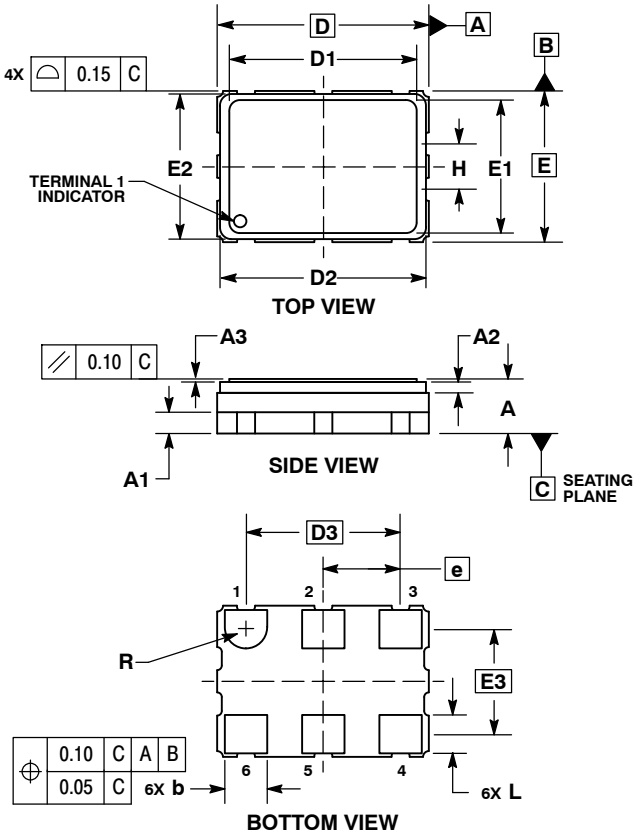
Table 9. ORDERING INFORMATION

Device	Output Frequency (MHz)	Package	Shipping†
5.0 x 7.0 x 1.8 mm			
NBVSPA013LN1TAG	212.0000	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSPA013LNHTAG	212.0000	CLCC−6, Pb−Free	100 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our tape and Reel Packaging Specification Brochure, BRD8011/D

PACKAGE DIMENSIONS

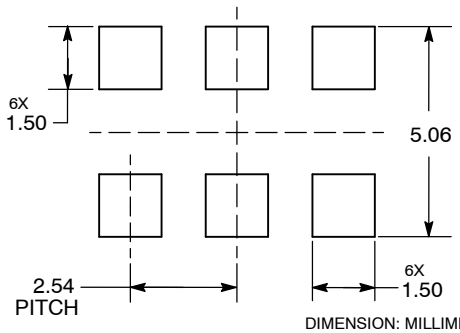
6 PIN CLCC, 7x5, 2.54P
CASE 848AB
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
H		1.80 REF	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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