

550V INTEGRATED HALF-BRIDGE DRIVER

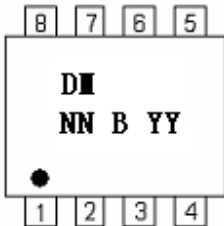
Description

The BL8003 is an integrated high-speed half bridge power MOSFET driver. Our proprietary DBiCMOS technologies provide stable operation under high dv/dt noise circumstances. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high side, which operates up to 550V. The logic input is compatible with standard CMOS or LSTTL, down to 3.3V logic. Cross conduction prevention logic and dead-times are built in to simplify the applications.

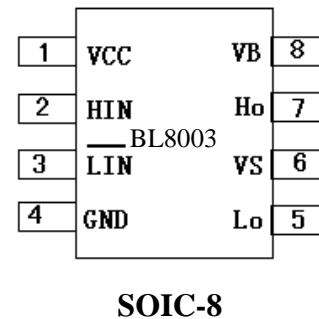
Features

- DBiCMOS technologies, low power dissipation and high output current
- Internal 5V LDO, CMOS and LSTTL logic (5V and 3.3V) compatible
- Under voltage lockout
- Cross conduction prevention logic
- Gate drive supply range from 10V to 16V
- Internal set deadtime
- High side output in phase with HIN input
- Low side output out of phase with LIN input.

Marking Information

Product Classification		BL8003CD8TR
Marking		
DM NN B YY	DM: Product Code	
	NN: LOT NO.	
	B: FAB Code	
	YY: Date Code	

Lead Assignments



Ordering Information

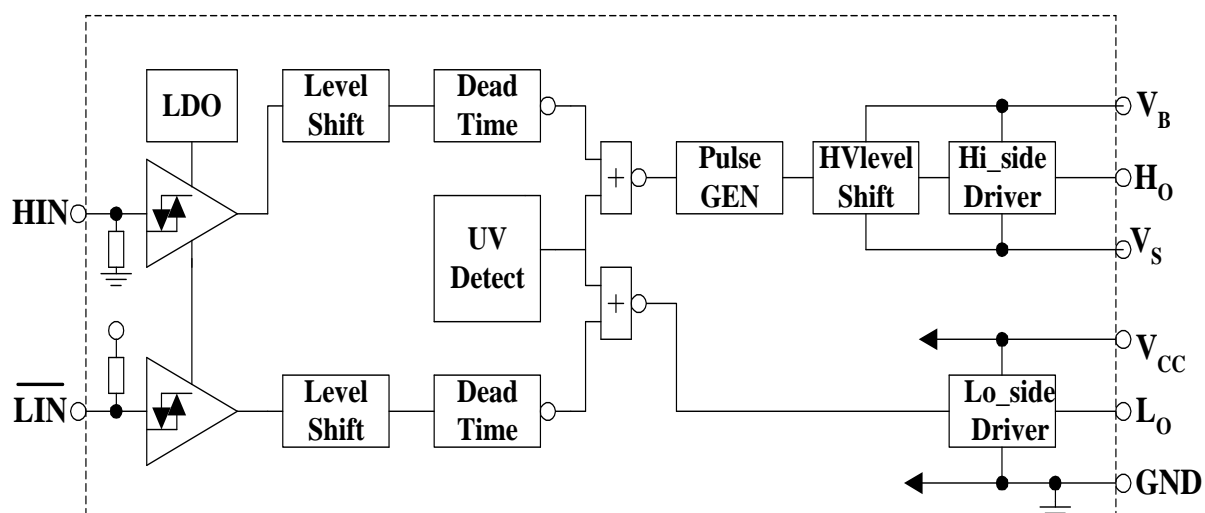
BL8003 1 2 3

Code	Description
1	Temperature&Rohs: C: -40~85°C ,Pb Free Rohs Std.
2	Package type: D8: SOIC-8
3	Packing type: TR: Tape&Reel (Standard)

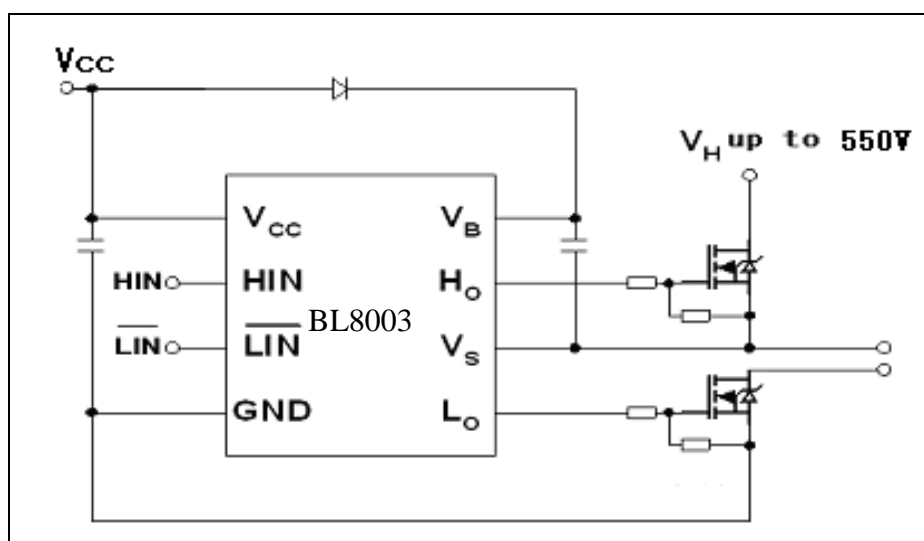
Pin Descriptions

Symbol	Description
HIN	Logic input for high side gate driver output (H _O), in phase
$\overline{\text{LIN}}$	Logic input for low side gate driver output (L _O), out of phase
V _B	High side floating supply
H _O	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
L _O	Low side gate drive output
GND	Low side return

Functional Block Diagram



Typical Connection



Absolute Maximum Ratings

Symbol	Definition	Min.	Max.	Unit
V _{CC}	Low side and logic fixed supply voltage	-0.3	16	V
V _B	High side floating absolute voltage	-0.3	550	V
V _S	High side floating supply offset voltage	V _B -16	V _B +0.3	V
P _D	Package power dissipation @ T _A ≤+25°C		0.625	W
R _{thJA}	Thermal resistance, junction to ambient		200	°C/W

Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Units
V _B	V _S +10	V _S +12	V _S +16	V
V _S	Note1		550	V
V _{HO}	V _S		V _B	V
V _{CC}	10	12	16	V
V _H			550	V
T _A	-40		125	°C

Note1: Logic operational for V_S of -5 to 550V.

Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=12V, unless specified noted.

Symbol	Definition	Min	Typ	Max	Unit	Test Conditions
V _{IH}	Logic "1" (HIN) & "0" (LIN) input voltage	3			V	V _{CC} =10 to 15V
V _{IL}	Logic "0" (HIN) & "1" (LIN) input voltage			1.5	V	V _{CC} =10 to 15V
V _{OH}	High level output voltage, V _{BIAS} -V _O			50	mV	I _O =0A
V _{OL}	Low level output Voltage, V _O			50	mV	I _O =0A
V _{CC_uv+}	V _{CC} supply undervoltage positive going threshold		9.1		V	
V _{CC_uv-}	V _{CC} supply undervoltage negative going threshold		8.3		V	
I _{QCC}	Quiescent V _{CC} supply current	1.3	1.5	1.8	mA	
I _{QBS}	Quiescent V _{BS} supply current	0	25	45	uA	
I _{LK}	V _S to GND leakage current	0	50	75	uA	V _S =550V
I _{O+}	Peak source output current	80	150		mA	V _O =0V, V _{IN} =V _{IH}
I _{O-}	Peak sink output current	150	200			V _O =12V, V _{IN} =V _{IL}
DT	Deadtime	650	700	750	nS	

Input/output True table

Hin	$\overline{\text{Lin}}$	Ho	Lo
0	0	0	1
0	1	0	0
1	0	0	0
1	1	1	0

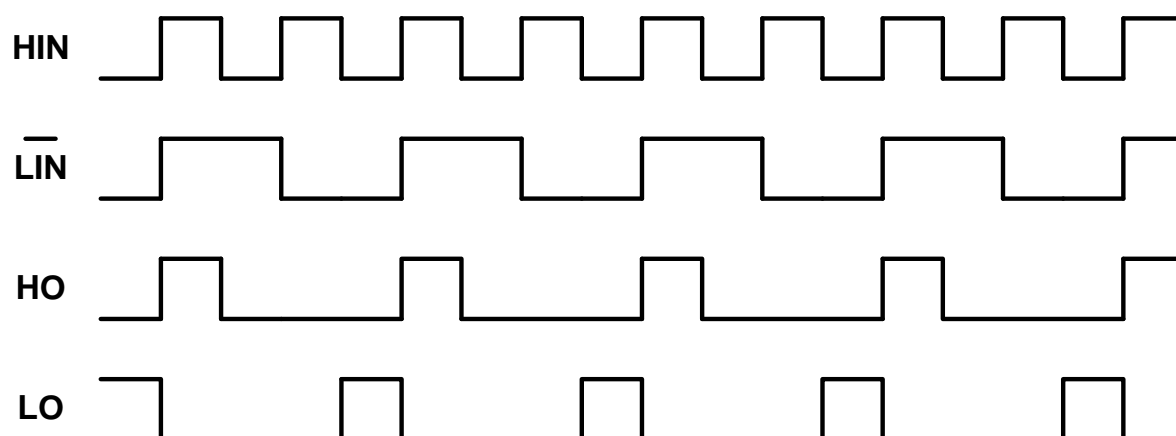


Figure 1: Input/output Timing Diagram

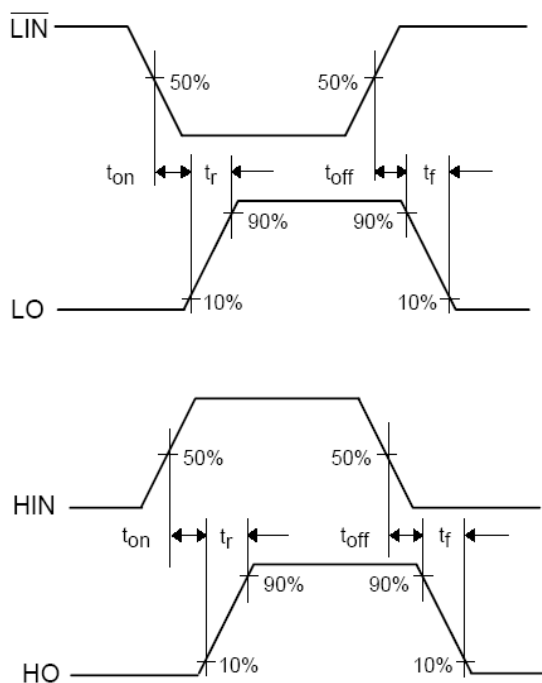


Figure 2: Switch Time Definition

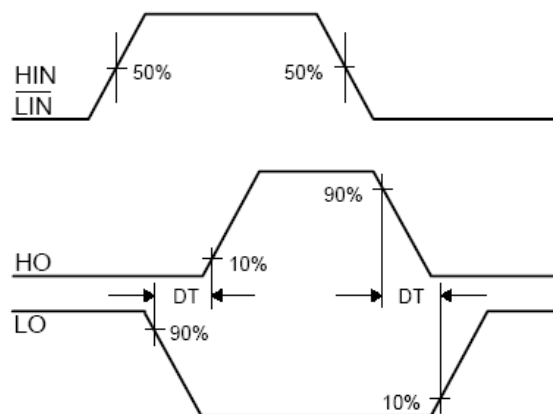
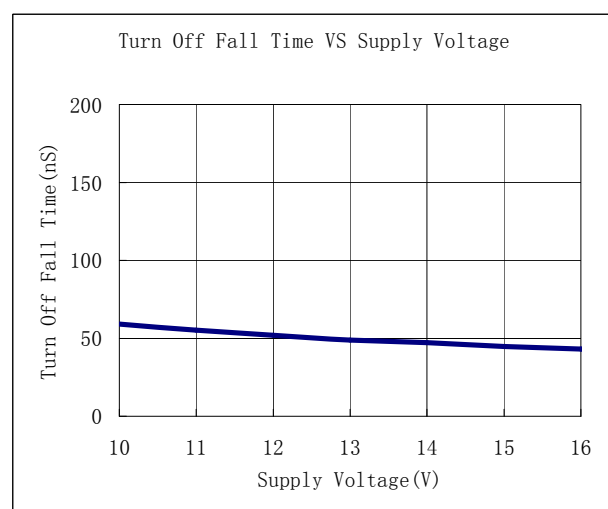
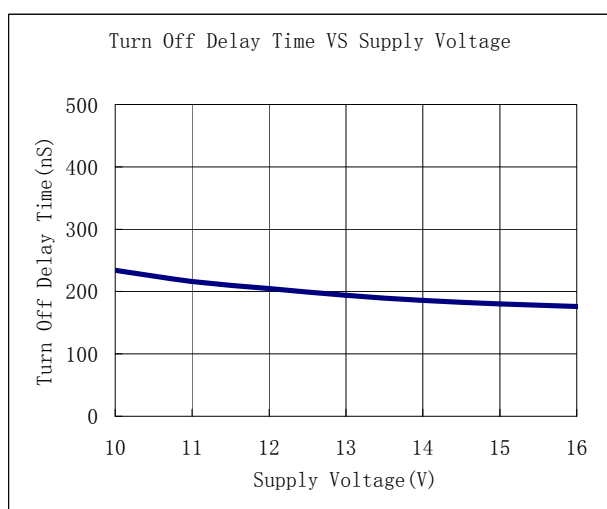
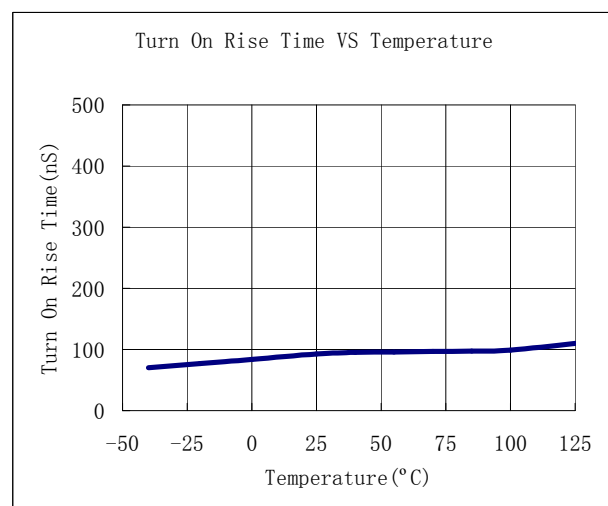
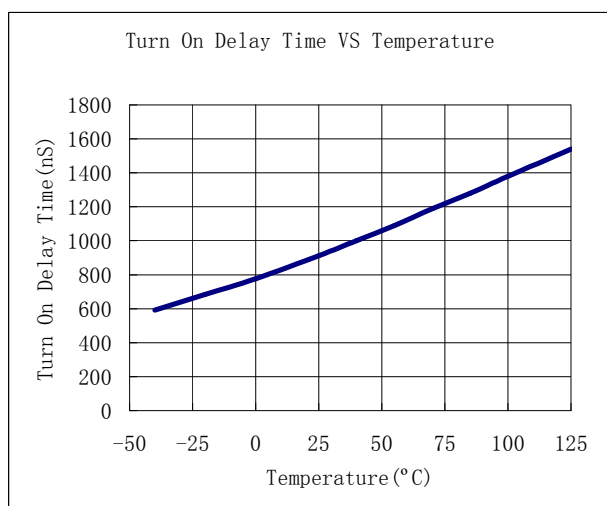
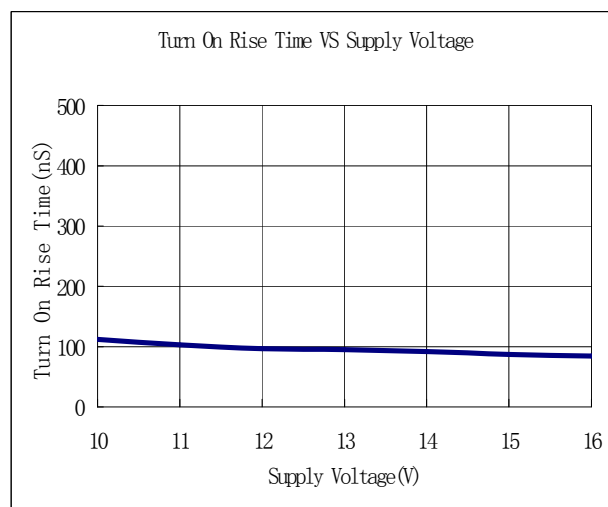
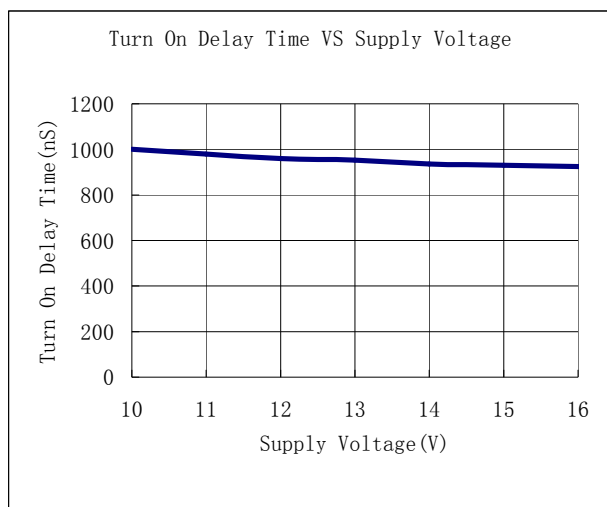
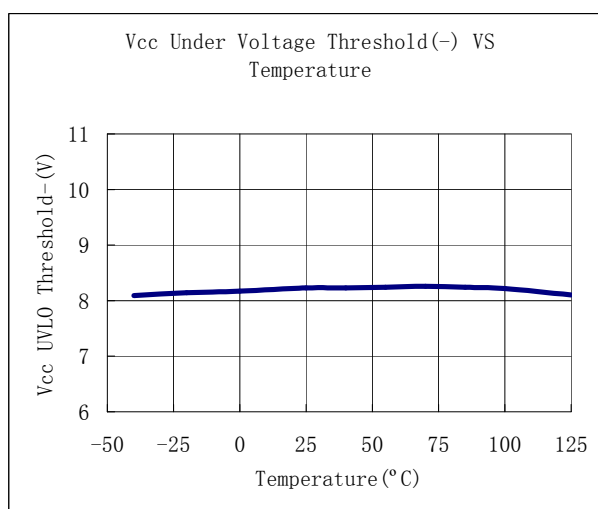
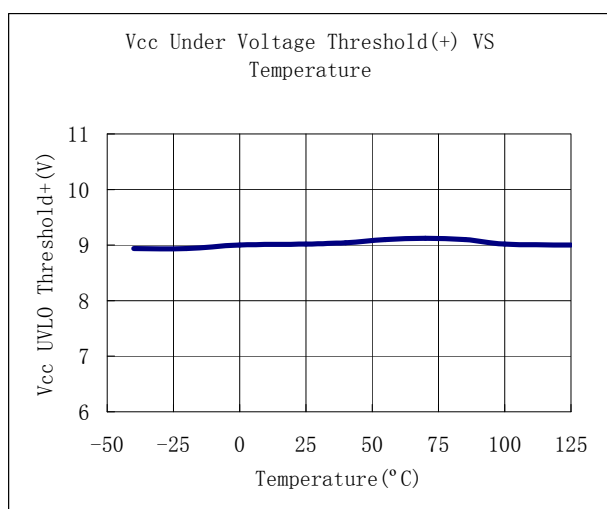
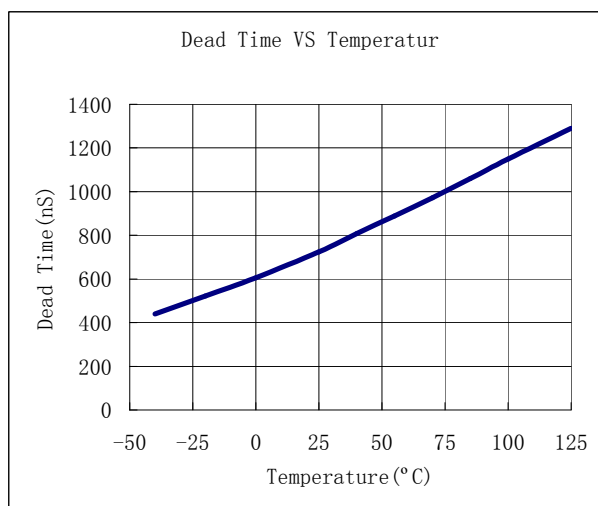
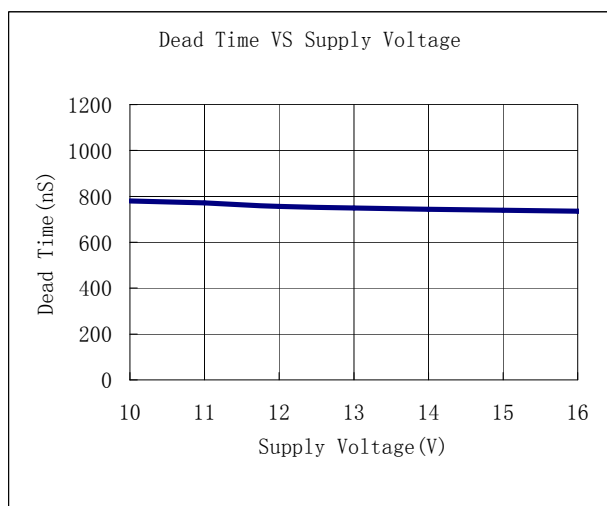
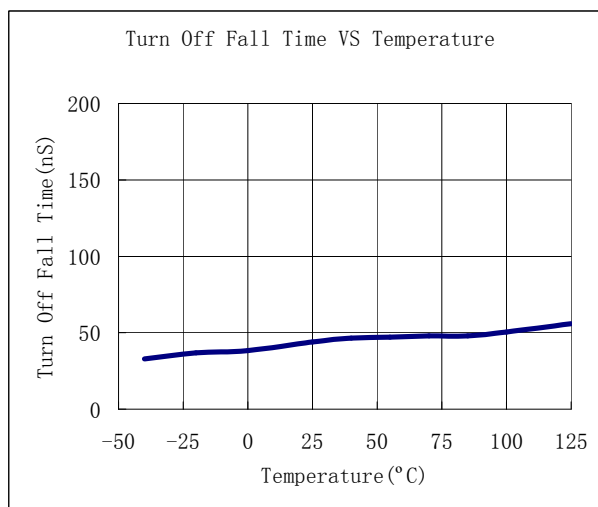
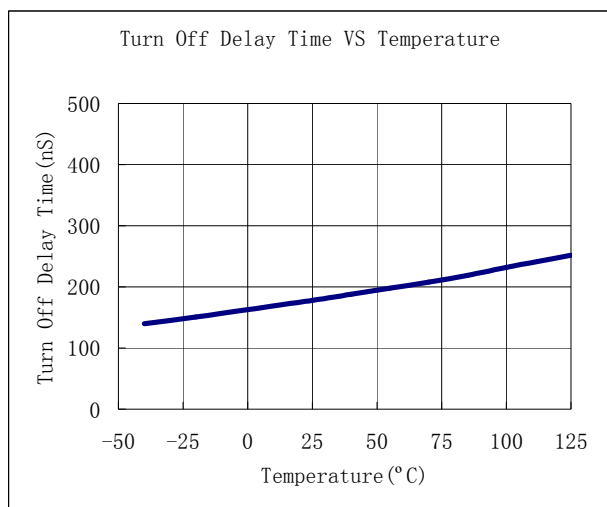


Figure 3: Dead Time Definition

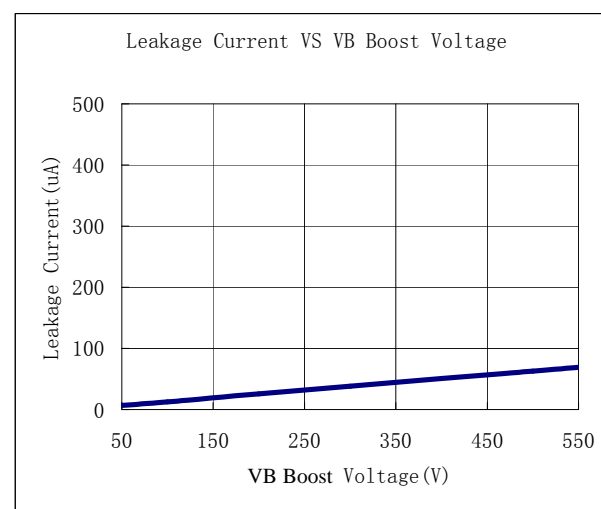
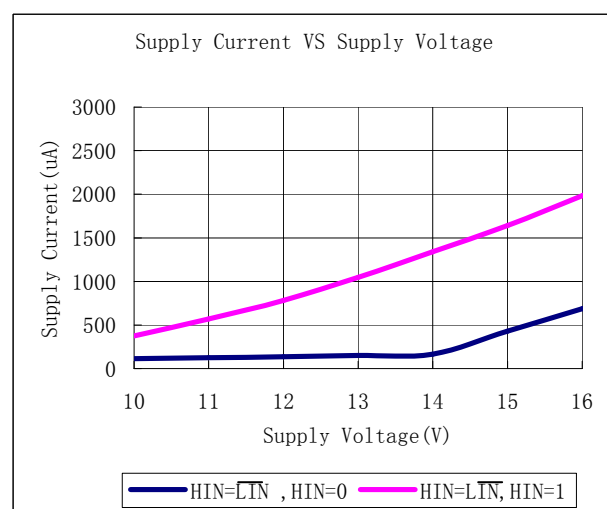
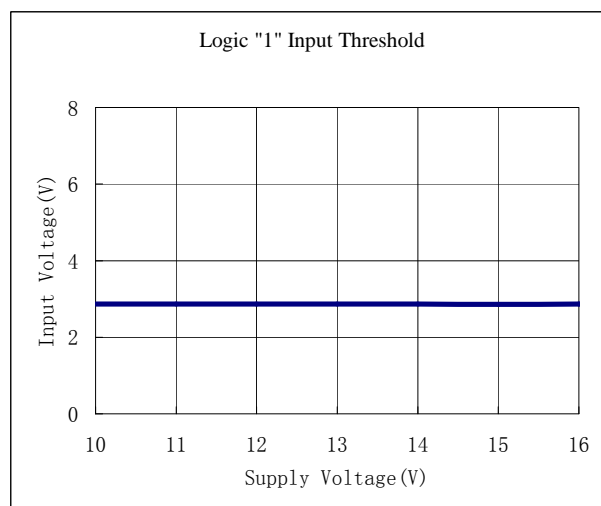
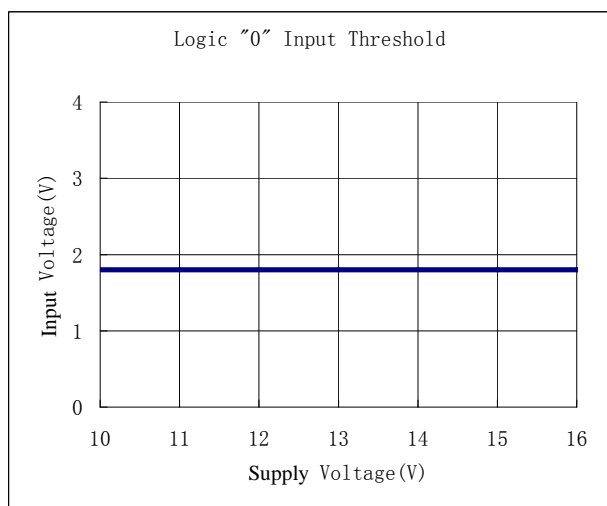
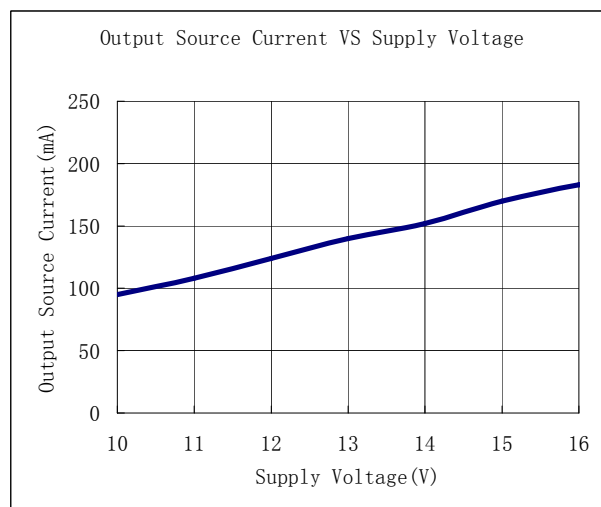
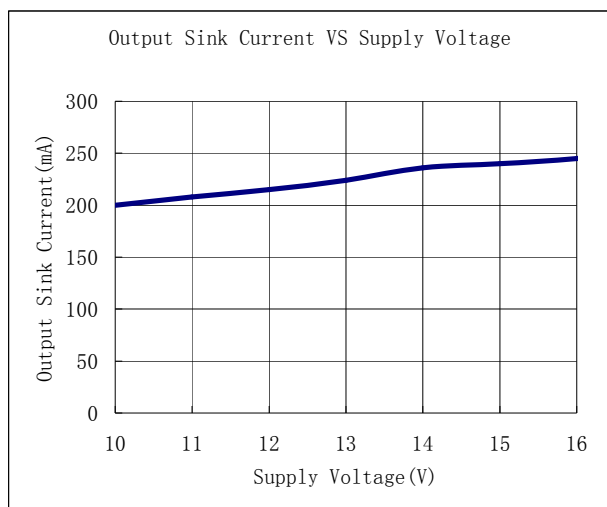
Typical Characteristics



Typical Characteristics (Continued)



Typical Characteristics (Continued)



Packaging Information

Package	SOIC-8	Devices per reel	2500Pcs	Unit	mm
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Package specification:

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	—	8°

SECTION B-B