AO4354

30V N-Channel AlphaMOS

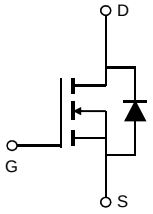
General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Features

V_{DS}	30V
I_D (at V_{GS}=10V)	23A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 3.7mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 5.3mΩ

Green Product



Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	23	A
	T_A=100℃		14	
Pulsed Drain Current [C]		I_{DM}	174	
Avalanche Current [C]		I_{AS}	37	A
Avalanche energy L=0.1mH [C]		E_{AS}	68	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	V
Power Dissipation [B]	T_A=25℃	P_D	3.1	W
	T_A=100℃		1.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.2	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		3	3.7	mΩ
		T_J=125℃		4.1	5	
		V_{GS}=4.5V, I_D=20A		4.1	5.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		105		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2010		pF
C_{oss}	Output Capacitance			898		pF
C_{rss}	Reverse Transfer Capacitance			124		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		36	49	nC
Q_g(4.5V)	Total Gate Charge			17	23	nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.5		ns
t_r	Turn-On Rise Time			4.0		ns
$t_{D(off)}$	Turn-Off DelayTime			37.0		ns
t_f	Turn-Off Fall Time			7.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		14		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		20.3		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

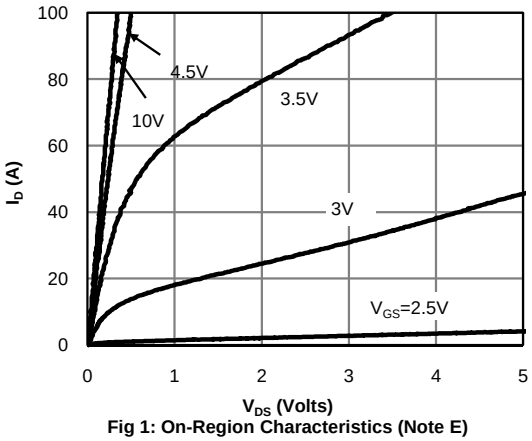


Fig 1: On-Region Characteristics (Note E)

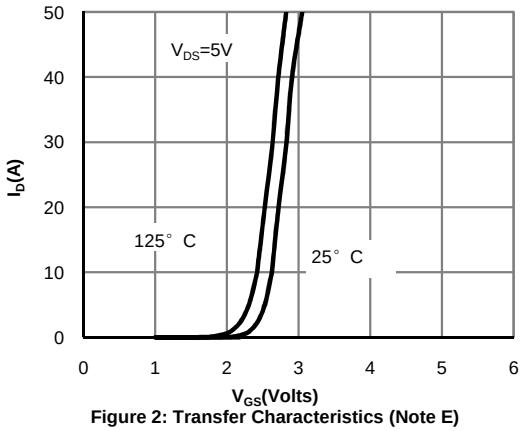


Figure 2: Transfer Characteristics (Note E)

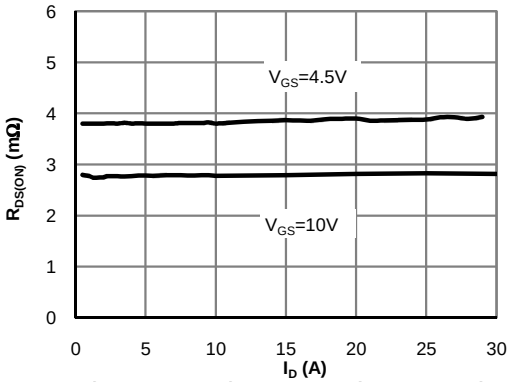


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

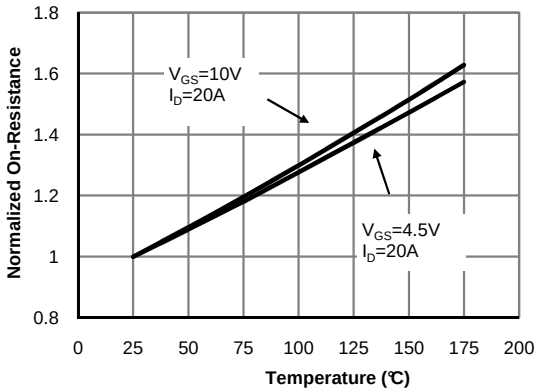


Figure 4: On-Resistance vs. Junction Temperature (Note E)

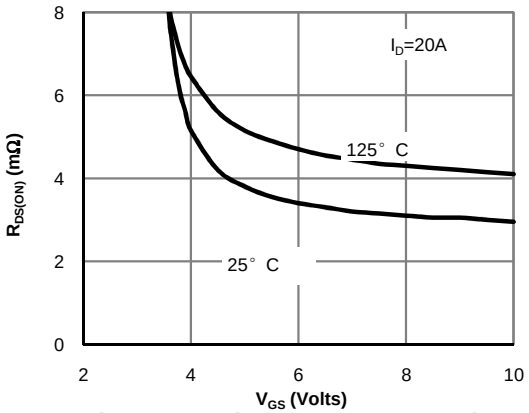


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

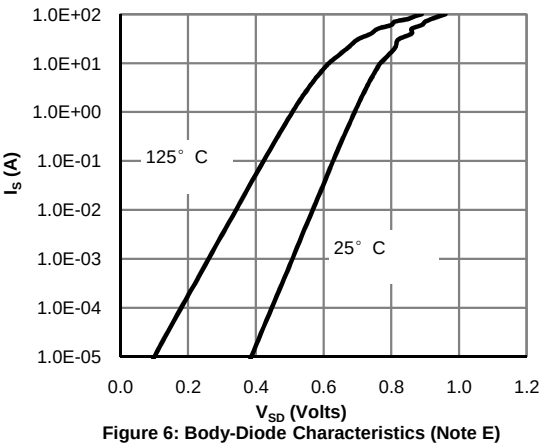


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

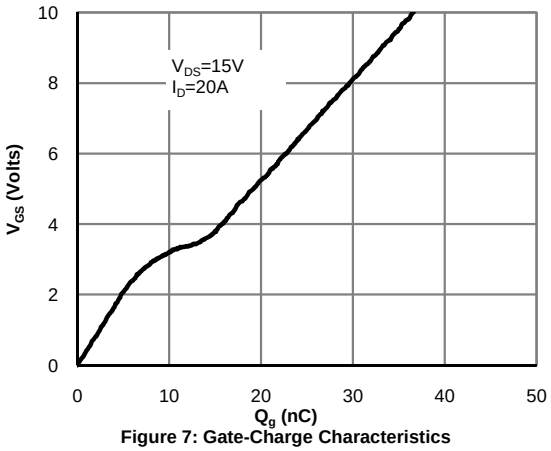


Figure 7: Gate-Charge Characteristics

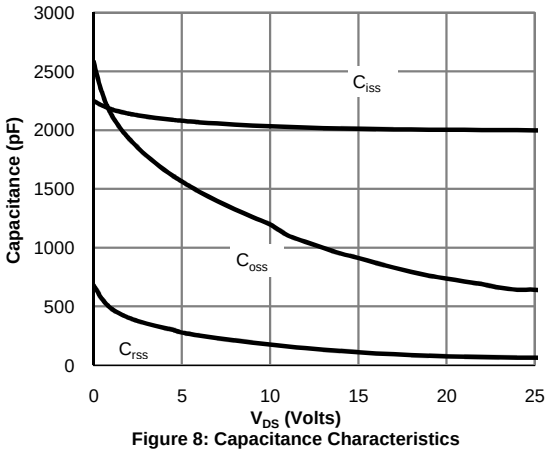


Figure 8: Capacitance Characteristics

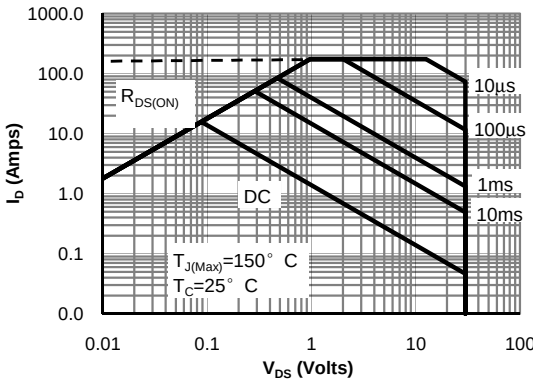
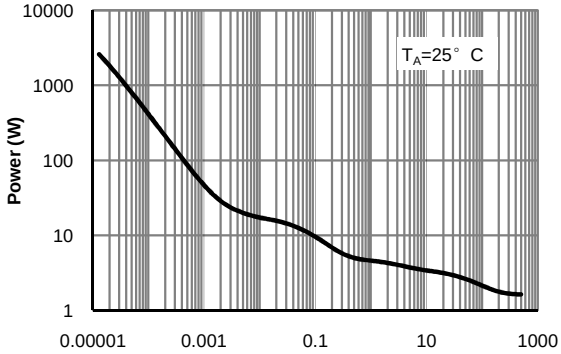
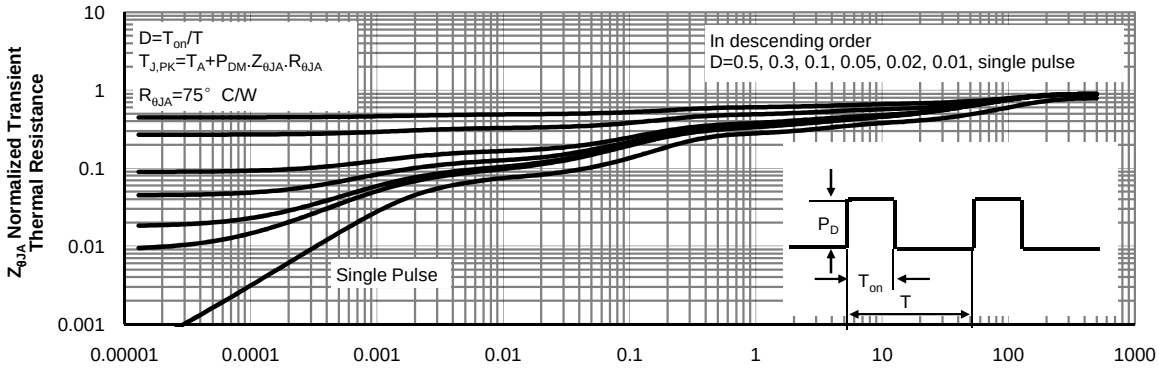


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)



Pulse Width (s)

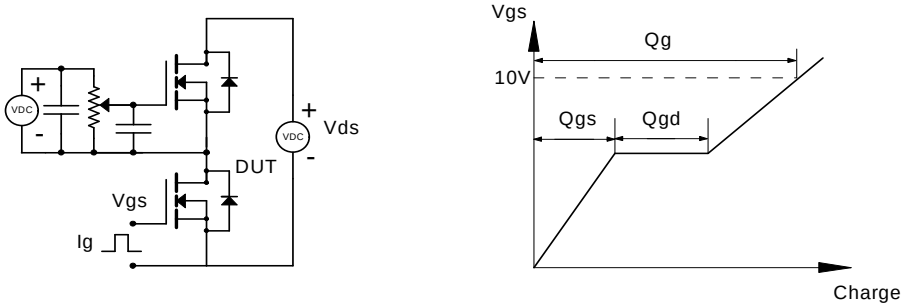
Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note F)



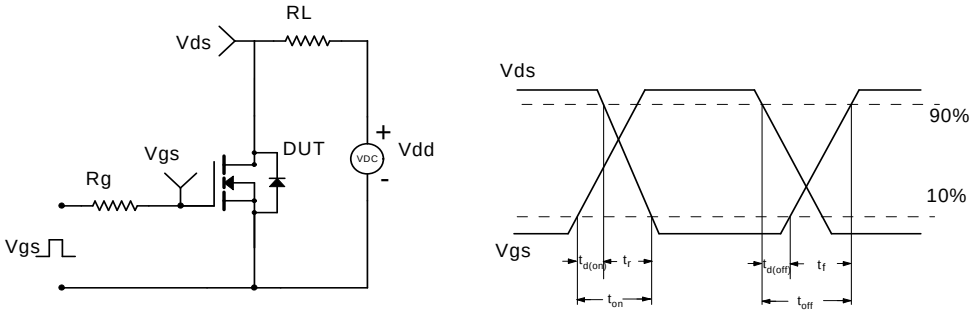
Pulse Width (s)

Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

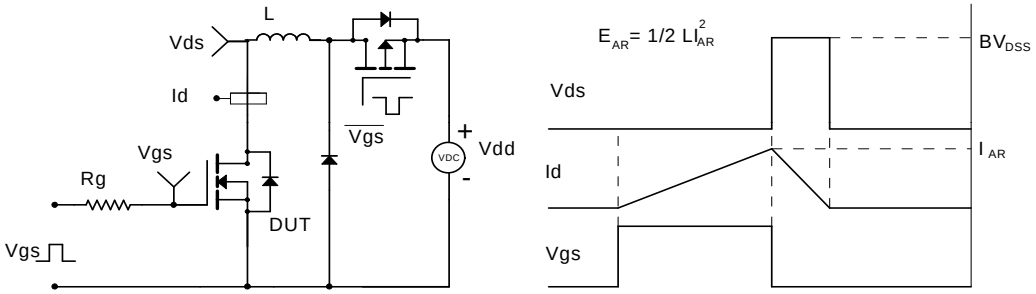
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms