

FDMS039N08B

N-Channel PowerTrench® MOSFET

80V, 100A, 3.9mΩ

Features

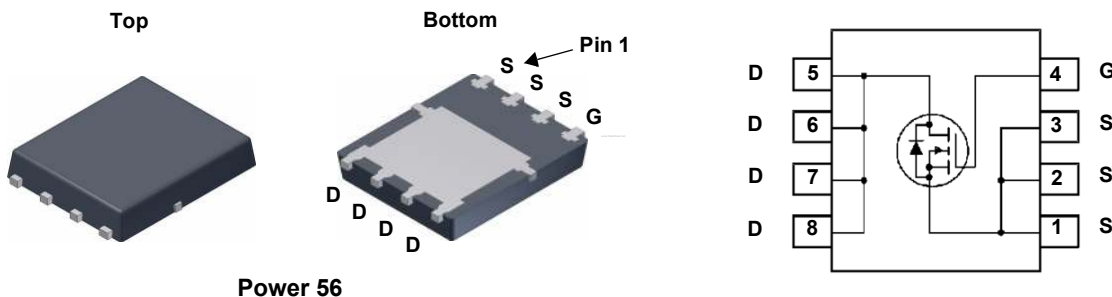
- $R_{DS(on)} = 3.2m\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 50A$
- Low FOM $R_{DS(on)} \cdot Q_G$
- Low reverse recovery charge, Q_{rr}
- Soft reverse recovery body diode
- Enables highly efficiency in synchronous rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- Synchronous Rectification for Server / Telecom PSU
- Battery Charger and Battery Protection circuit
- DC motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted*

Symbol	Parameter	Conditions	Ratings	Units
V_{DSS}	Drain to Source Voltage		80	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$)	100	A
		- Continuous ($T_A = 25^\circ C$) (Note 1)	19.4	
I_{DM}	Drain Current	- Pulsed (Note 2)	400	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 3)	240	mJ
P_D	Power Dissipation	($T_C = 25^\circ C$)	104	W
		($T_A = 25^\circ C$) (Note 1)	2.5	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Conditions	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS039N08B	FDMS039N08B	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.04	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	-	3.2	3.9	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 50\text{A}$ (Note 4)	-	100	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5715	7600	pF
C_{oss}	Output Capacitance		-	881	1170	pF
C_{rss}	Reverse Transfer Capacitance		-	15	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	1646	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40\text{V}, I_D = 50\text{A}$ $V_{GS} = 0\text{V}$ to 10V	-	77	100	nC
Q_{gs}	Gate to Source Gate Charge		-	34	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	13	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4,5)	-	16	-

Switching Characteristics

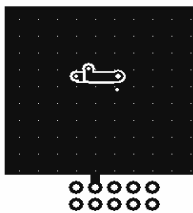
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	42	94	ns
t_r	Turn-On Rise Time		-	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		-	48	106	ns
t_f	Turn-Off Fall Time		(Note 4,5)	-	17	44
ESR	Equivalent Series Resistance	Drain Open, $f = 1\text{MHz}$	-	1.2	-	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	100	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	400	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 50\text{A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 50\text{A}, V_{DD} = 40\text{V}$	-	68	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	80	-	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper.



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $L = 0.3\text{mH}, I_{AS} = 40\text{A}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty cycle $\leq 2.0\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

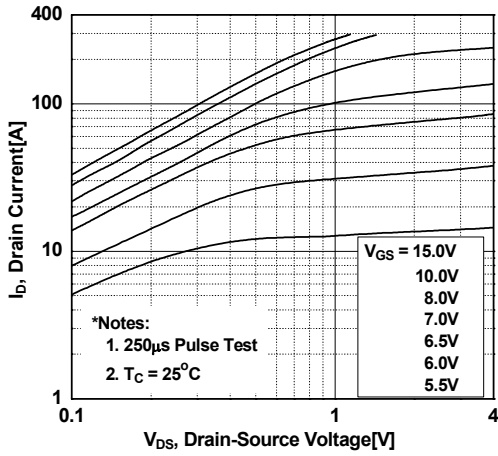


Figure 2. Transfer Characteristics

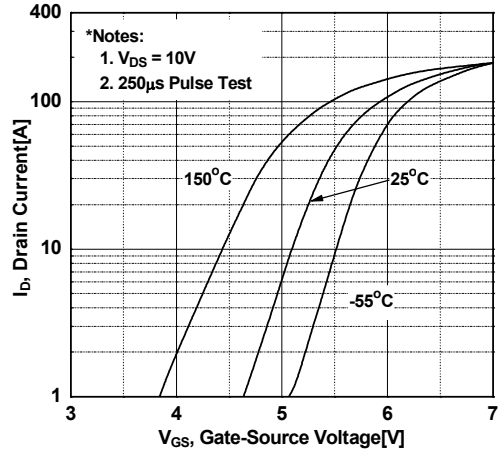


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

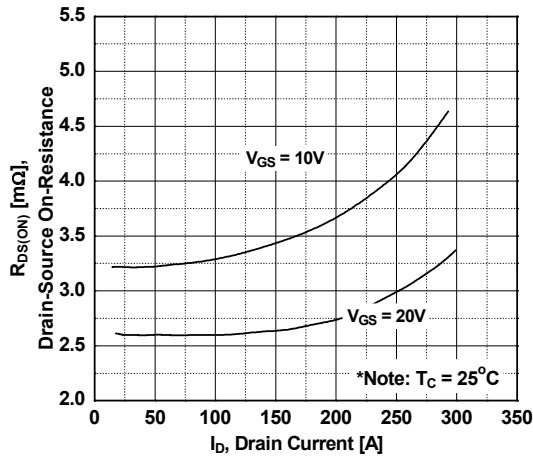


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

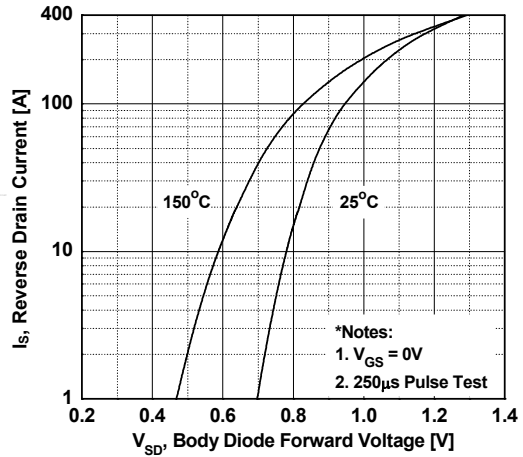


Figure 5. Capacitance Characteristics

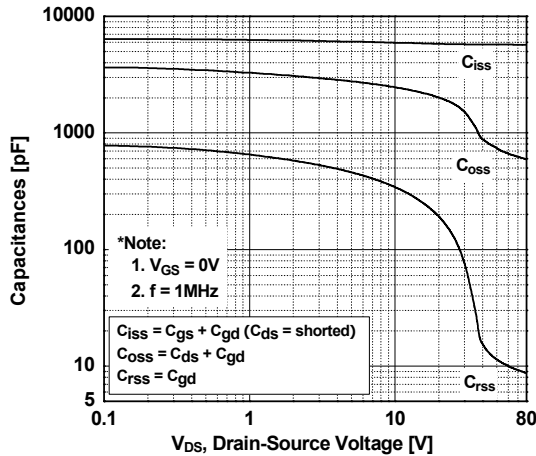
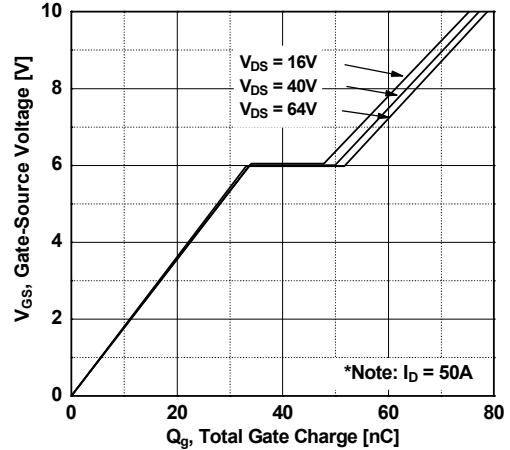


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

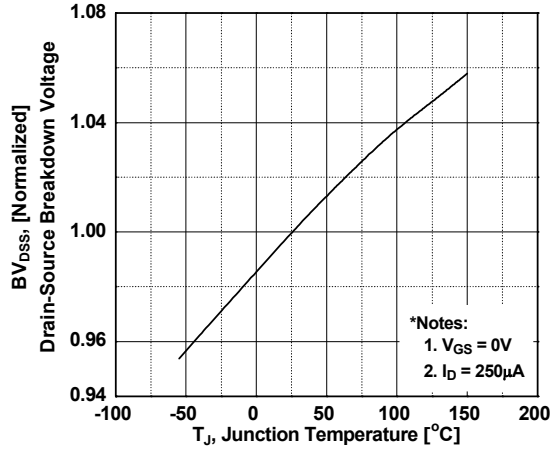


Figure 8. On-Resistance Variation vs. Temperature

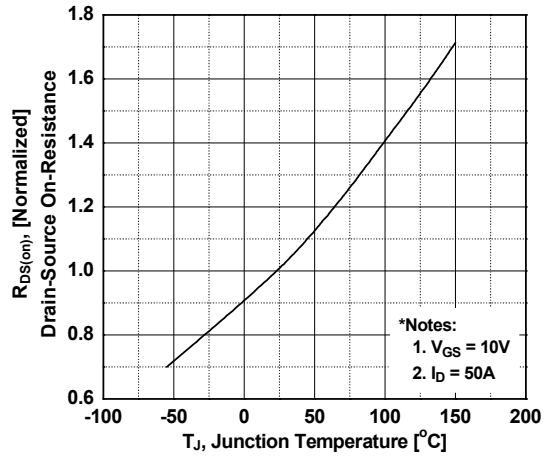


Figure 9. Maximum Safe Operating Area vs. Ambient Temperature

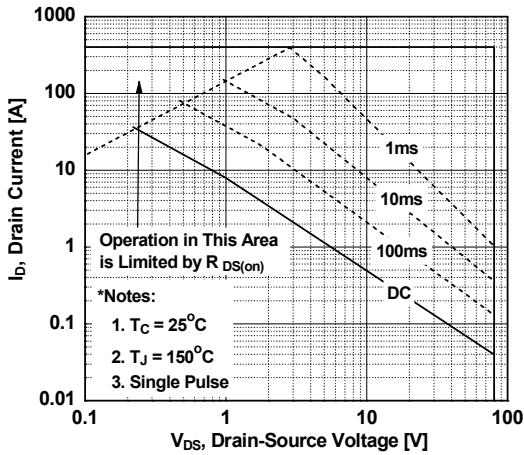


Figure 10. Maximum Drain Current

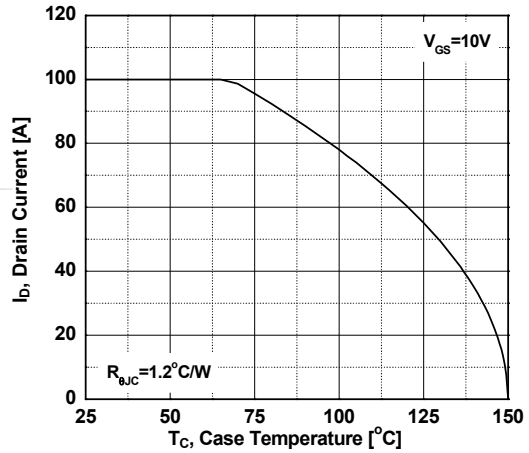


Figure 11. Unclamped Inductive Switching Capability

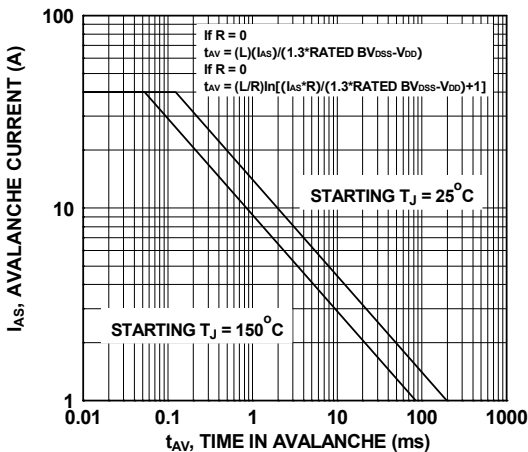
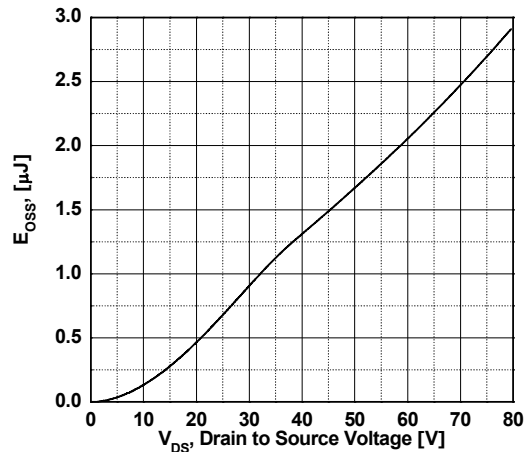
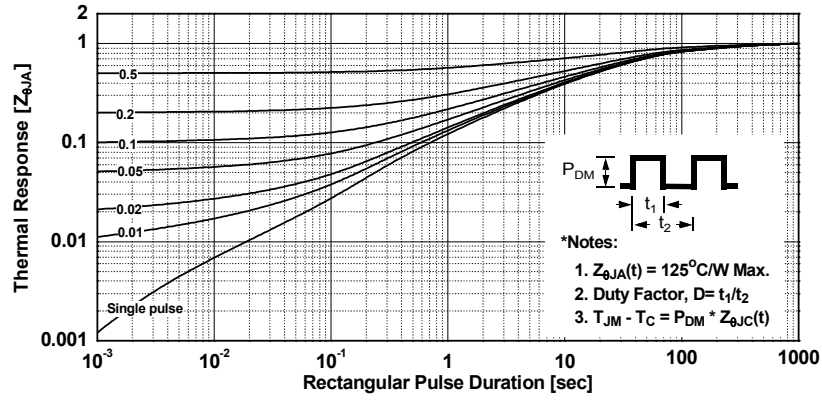


Figure 12. Eoss vs. Drain to Source Voltage

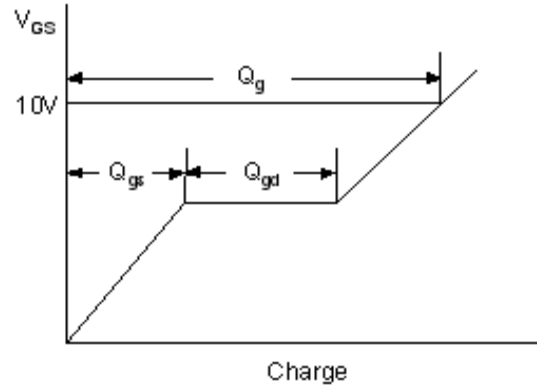
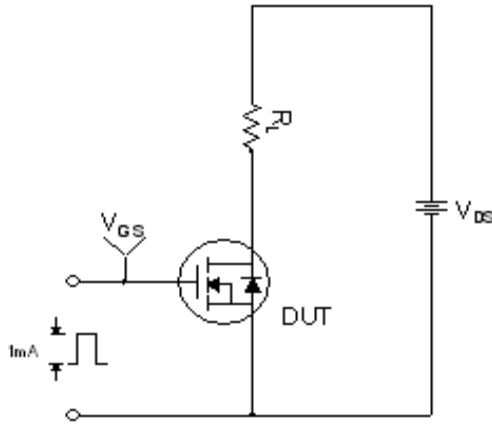


Typical Performance Characteristics (Continued)

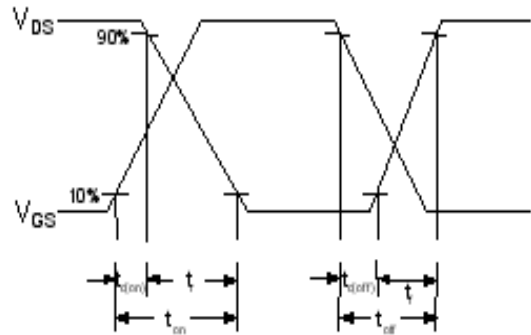
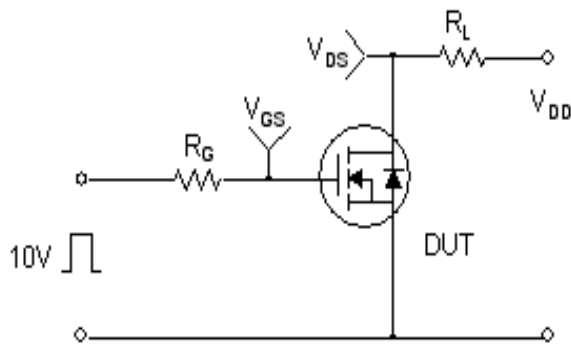
Figure 13. Transient Thermal Response Curve



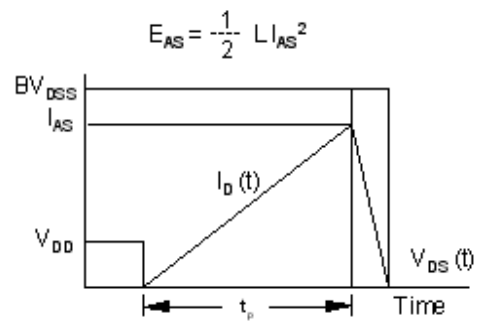
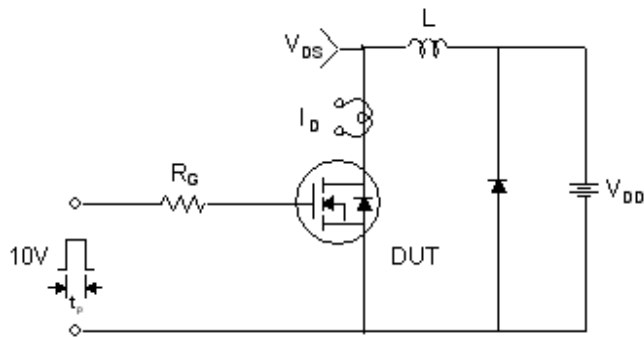
Gate Charge Test Circuit & Waveform



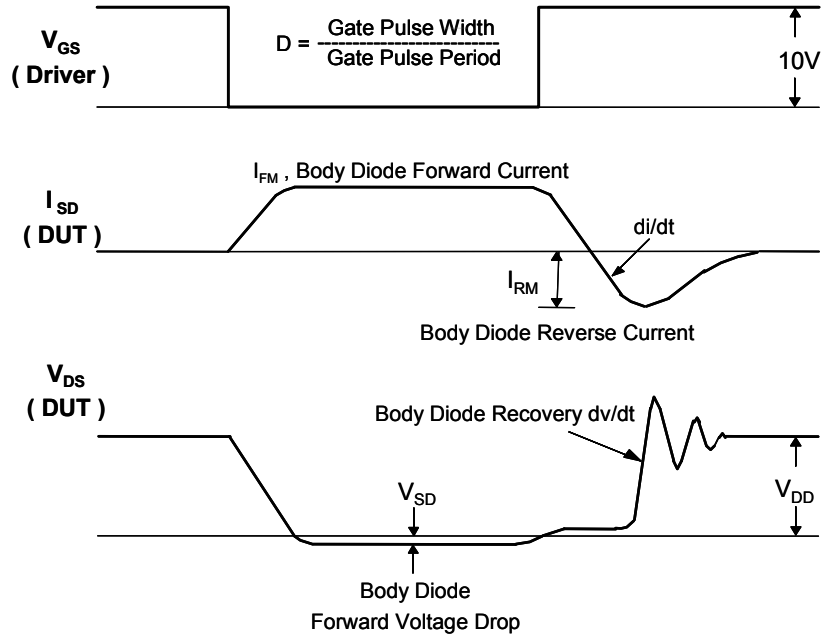
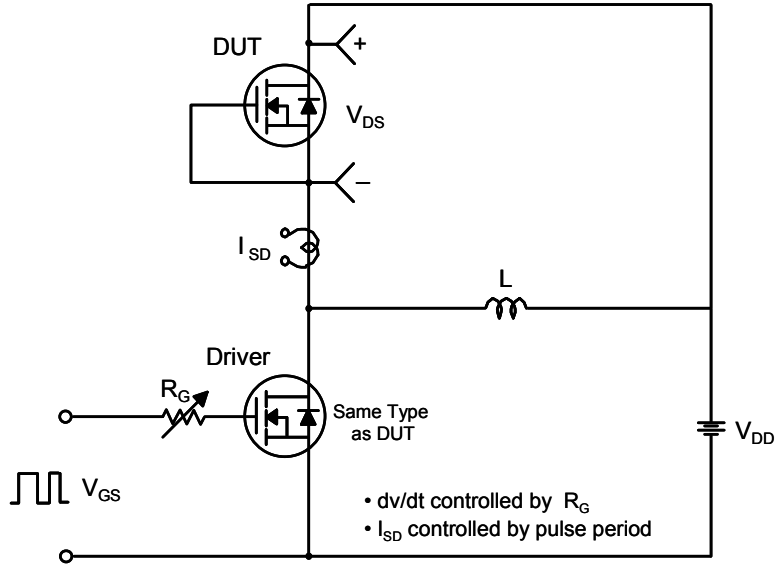
Resistive Switching Test Circuit & Waveforms



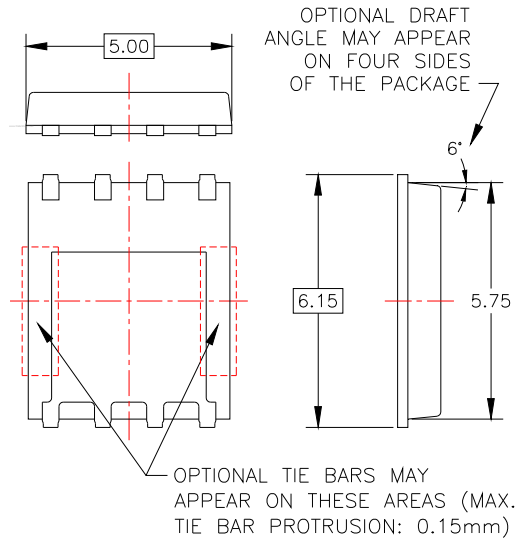
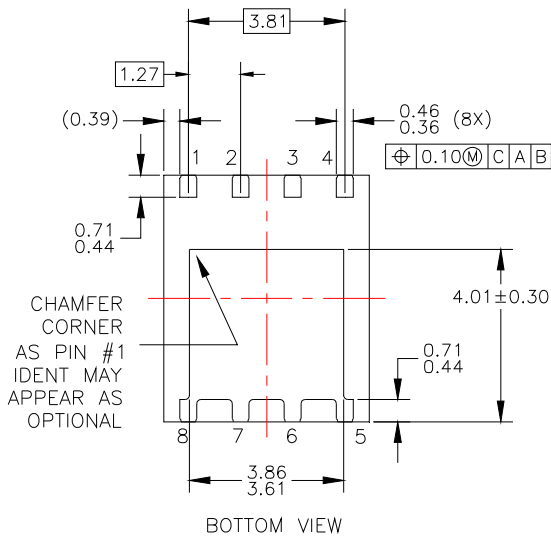
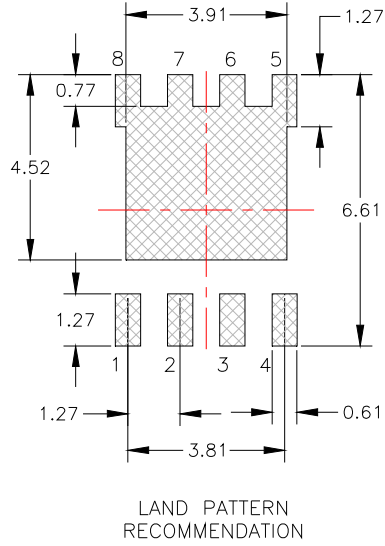
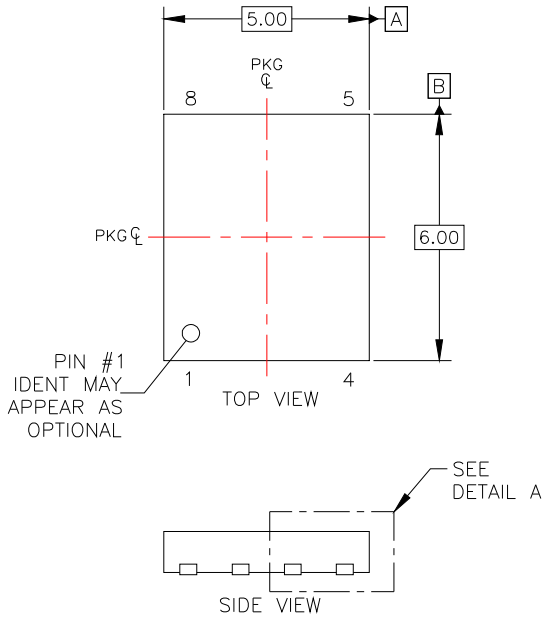
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

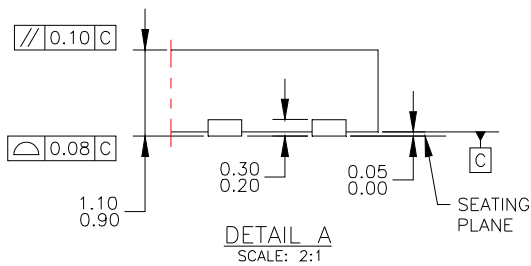


Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED


- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4





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