



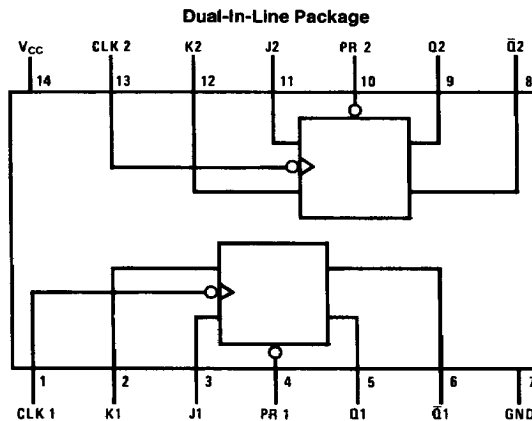
## DM54S113/DM74S113 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs

### General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the

negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set the outputs regardless of the logic levels of the other inputs.

### Connection Diagram



Order Number DM54S113J or DM74S113N  
See NS Package Number J14A or N14A

TL/F/6460-1

### Function Table

Inputs				Outputs	
PR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	$Q_0$	$\bar{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

$Q_0$  = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	-55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S113			DM74S113			Units
			Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage		2			2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8			0.8	V
I <sub>OH</sub>	High Level Output Current				-1			-1	mA
I <sub>OL</sub>	Low Level Output Current				20			20	mA
f <sub>CLK</sub>	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f <sub>CLK</sub>	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t <sub>w</sub>	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Preset Low	8			8			
t <sub>w</sub>	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Preset Low	10			10			
t <sub>SU</sub>	Setup Time (Notes 1 & 4)		7 ↓			7 ↓			ns
t <sub>H</sub>	Input Hold Time (Notes 1 & 4)		0 ↓			0 ↓			ns
T <sub>A</sub>	Free Air Operating Temperature		-55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: C<sub>L</sub> = 15 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 3: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 4: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54 DM74	2.5 2.7	3.4 3.4	V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.5	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7 \text{ V}$	J, K Preset Clock		50 100 100	$\mu\text{A}$
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.5 \text{ V}$	J, K Preset Clock		-1.6 -7 -4	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54 DM74	-40 -40	-100 -100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max},$ (Note 3)		30	50	mA

Note 1: All typicals are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## Switching Characteristics

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		80		60		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Preset to $\bar{Q}$		7		12	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Q or $\bar{Q}$		7		9	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Q or $\bar{Q}$		7		12	ns