1.2V 8BIT 2MSPS DAC DAC1353X

GENERAL DESCRIPTION

The DAC1353X is a CMOS 8-bit D/A converter for general applications. This digital to analog converter has a R-string structure.
The maximum conversion rate of DAC1353X is 2MSPS and supply voltage is 1.2V single.

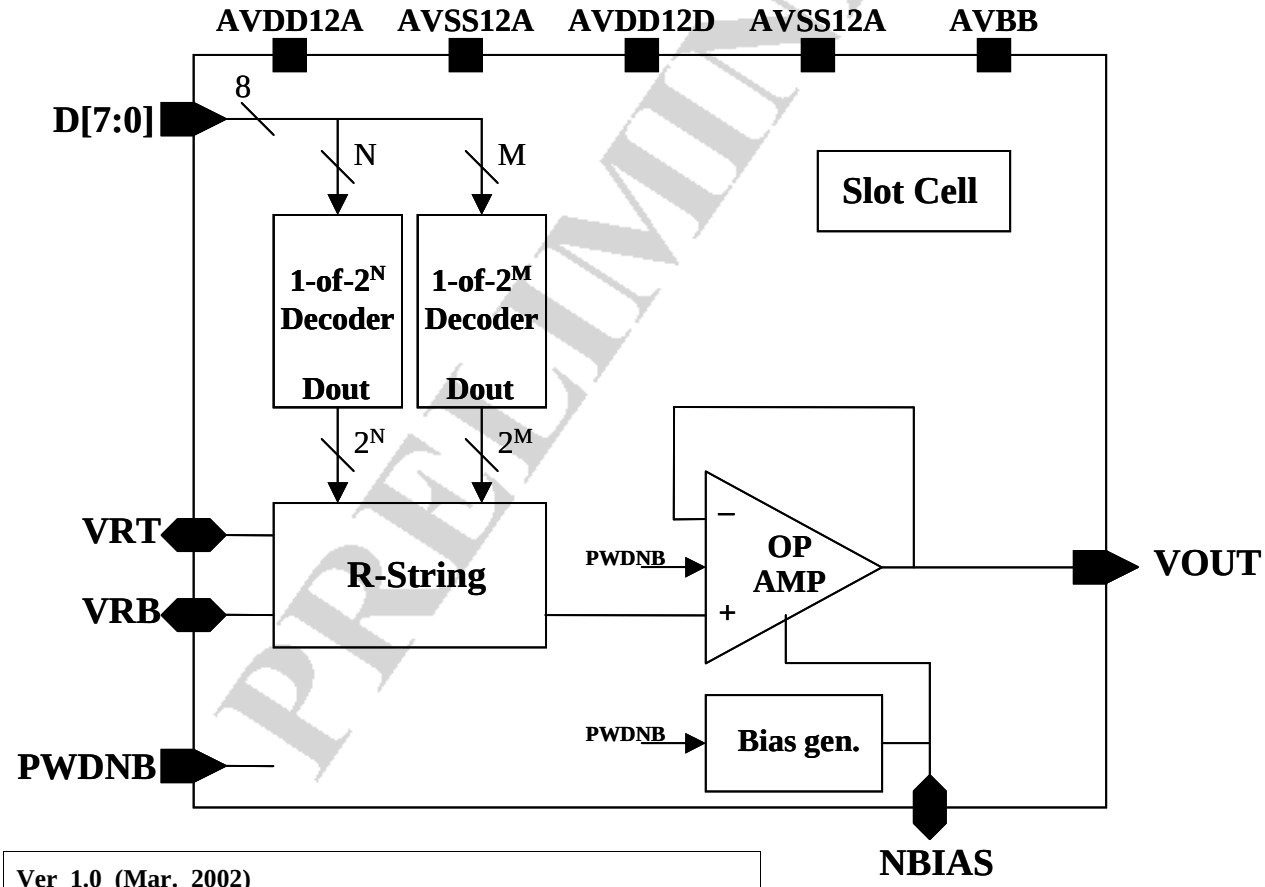
TYPICAL APPLICATIONS

- Hard Disk Drive (HDD)
- Battery Operated Instruments
- Motor Control Systems
- General Applications

FEATURES

- **Resolution : 8Bit**
- **Differential Linearity Error : ± 1.0 LSB**
- **Integral Linearity Error : ± 1.0 LSB**
- **Maximum Conversion Rate : 2MSPS**
- **Low Power Consumption : 3.6mW**
- **Power Down Mode**
- **Operation Temperature Range : 0° C ~ 70° C**
- **Power Supply : 1.2V Single**

FUNCTIONAL BLOCK DIAGRAM



Ver 1.0 (Mar. 2002)
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CORE PIN DESCRIPTION

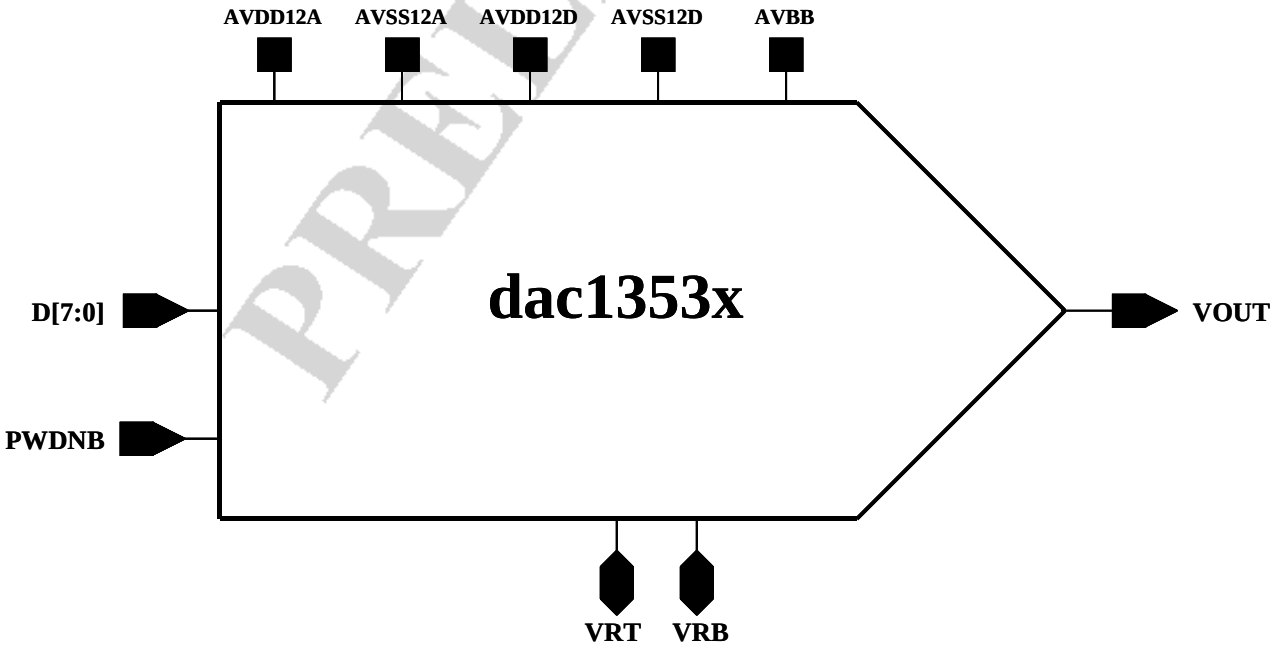
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
D[7:0]	DI	picc_abb	Digital Input Data (8BIT) D[7] : MSB , D[0] : LSB
PWDNB	DI	picc_abb	Power Down (Active Low)
VRT	AB	pia_abb	Voltage Reference Top
VRB	AB	pia_abb	Voltage Reference Bottom
NBIAS	AB	pia_abb	Bias Generator Output Voltage
VOUT	AO	poa_abb	Analog Voltage Output
AVDD12A	AP	vdd12t_abb	Analog Power (+1.2V)
AVSS12A	AG	vsst_abb	Analog Ground (0.0V)
AVDD12D	DP	vdd12t_abb	Digital Power (+1.2V)
AVSS12D	DG	vsst_abb	Digital Ground (0.0V)
AVBB	AG	vbb_abb	Analog Sub Bias (0.0V)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD (AVDD12A,AVDD12D)	1.2	V
Analog Output Voltage	VOUT	0.05 to 1.15	V
Digital Input Voltage	D[7:0]	VSS to VDD	V
Reference Voltage	VRT VRB	1.15 0.05	V
Operating Temperature Range	Topr	0 to 70	°C

NOTES :

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(AVSS12A or AVSS12D or AVBB) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD12A - AVSS12A AVDD12D - AVSS12D	1.08	1.2	1.32	V
Supply Voltage Difference	AVDD12A - AVDD12D	-0.1	0.0	0.1	V
Reference Voltage	VRT VRB	- 0.05	- -	1.15 -	V
Digital Input 'Low' Voltage Digital Input 'High' Voltage	VIL VIH	- 0.7×VDD	- -	0.3×VDD -	V
Operating Temperature	Topr	0	-	70	°C

NOTE :

It is strongly recommended that to avoid power latch-up all the supply pins(AVDD12A,AVDD12D) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD12A=AVDD12D=1.2V, AVSS12A=AVSS12D=AVBB=0V, PWDNB=High, Top=25°C, VRT=1.2V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	-	-	8	Bits	-
Differential Linearity Error	DLE	-	1.0	-	LSB	-
Integral Linearity Error	ILE	-	1.0	-	LSB	-
Zero Scale Error[1]	V_{ZSE}	-	10	-	mV	VRT=1.15V , VRB=0.05V
Full Scale Voltage Error[2]	V_{FSE}	-	10	-	mV	
Maximum Output Voltage	Vo_{MAX}	-	1.146	-	V	Vo_{MAX} = VOUT(D[7:0]=High)
LSB Size	V_{LSB}	-	4.49	-	mV	V_{LSB} = Vo_{MAX} / 255

NOTE 1 : V_{ZSE}=VOUT(D[7:0]=Low) - VRB

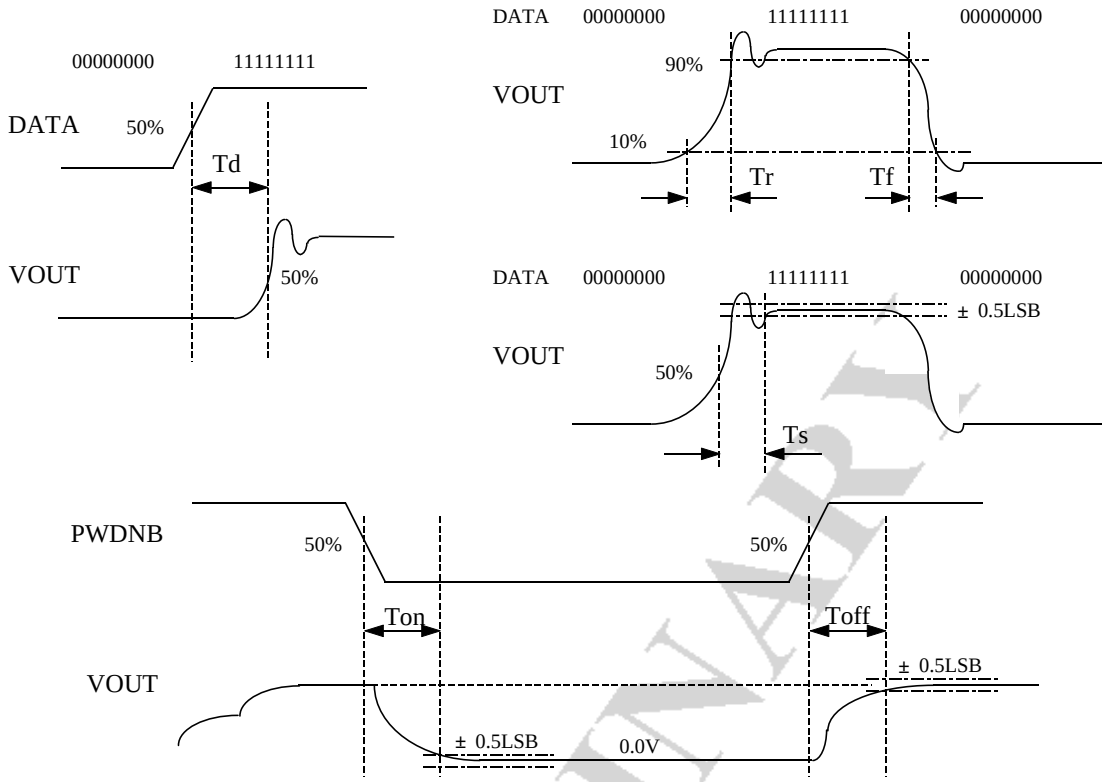
2 : V_{FSE}=VOUT(D[7:0]=High) - {(VRT-VRB) × 255/256 + VRB}

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD12A=AVDD12D=1.2V, AVSS12A=AVSS12D=AVBB=0V, load cap=20pF, Resistive load=100k Top=25°C, VRT=1.2V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Maximum Conversion Rate	f_C	-	-	2	MSPS	Data Rate = 2MHz
Dynamic Supply Current	Ivdd1	-	3	-	mA	Ivdd1 = $I_{AVDD12A}$ + I_{VRT} + $I_{AVDD12D}$ Data Rate = 2MHz
Dynamic Supply Current (Power Down Mode)	Ivdd2	-	-	10	uA	Ivdd2 = $I_{AVDD12A}$ + $I_{AVDD12D}$ Data Rate = 2MHz PWDNB=LOW
Analog Output Delay	Td	-	120	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Rise Time	Tr	-	90	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Fall Time	Tf	-	130	-	ns	Data Rate = 2MHz Data : All HIGH → All LOW
Analog Output Settling Time	Ts	-	430	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH VRT = VDD/2
Power Down On Time	Ton	-	60	-	ns	PWDNB : HIGH → LOW
Power Down Off Time	Toff	-	900	-	ns	PWDNB : LOW → HIGH

TIMING DIAGRAM



1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1/2 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

FUNCTIONAL DESCRIPTION

1. The DAC1353X has a R-string Block for 10bit and an Opamp Block for driving Output.

2. The digital outputs of two decoders decide the voltage level of R-string block.

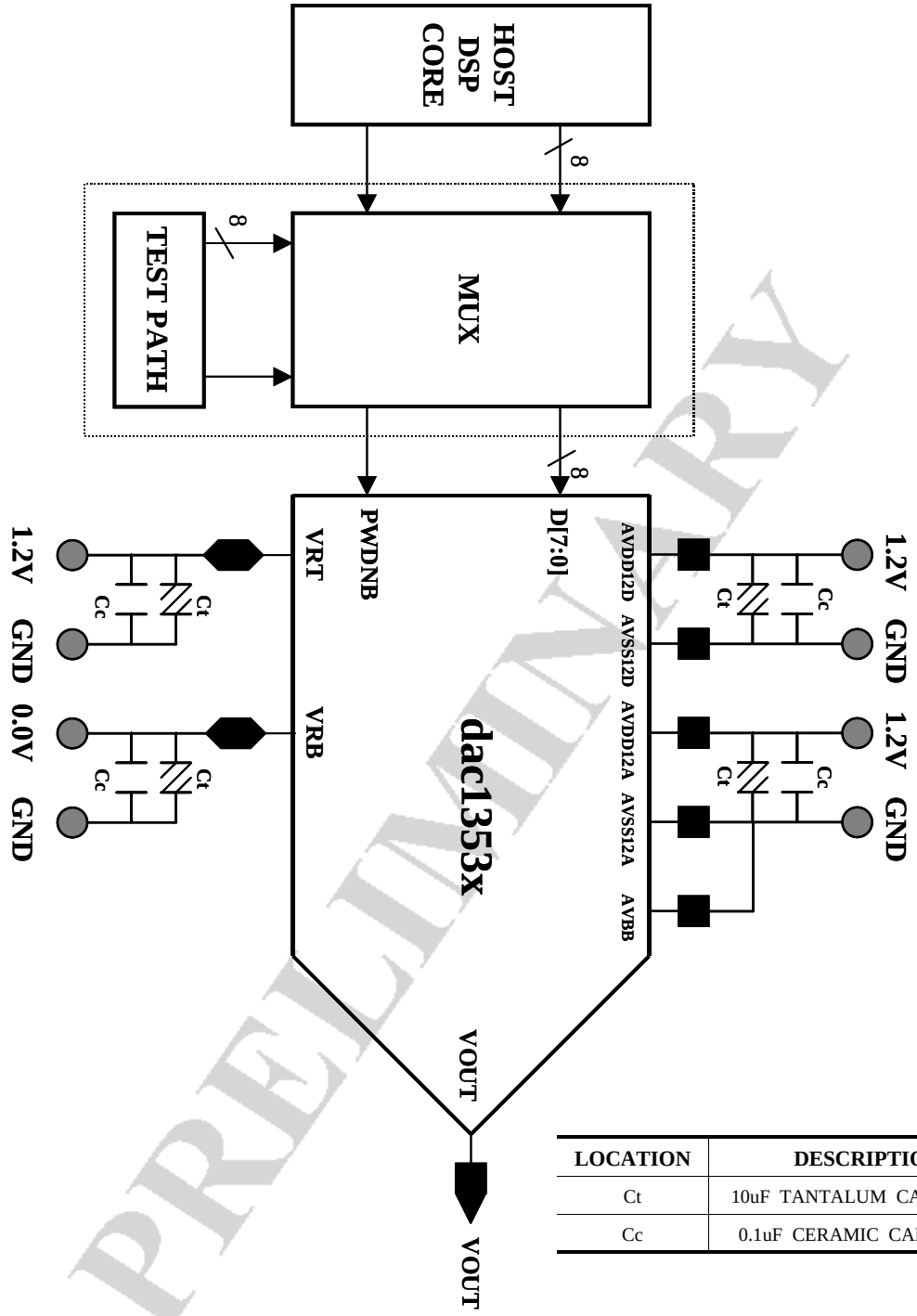
$$V_{Rstring} = \frac{VRT - VRB}{2^8} \sum_{n=0}^{7} (2^n * Dn) + VRB$$

3. Output of the R-string Block is driven by OPamp.

4. Bias gen. consists of simple current source to provide constant current independent of supply voltage and temperature.

5. In power down mode, only analog current($I_{AVDD12A}$) is reduced.

CORE EVALUATION GUIDE

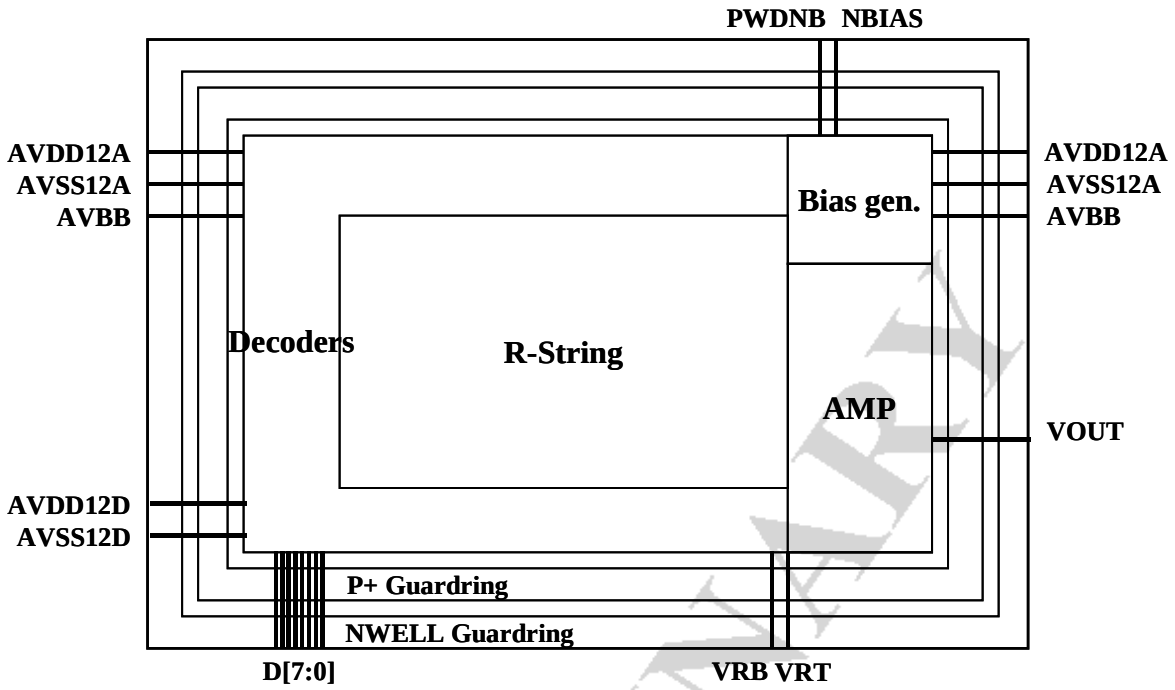


LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[7:0]).
See above figure. Only if it is, you can check the main function. (Linearity)
Normal Test Condition : VRT=1.15V , VRB=0.05V , PWDNB=High

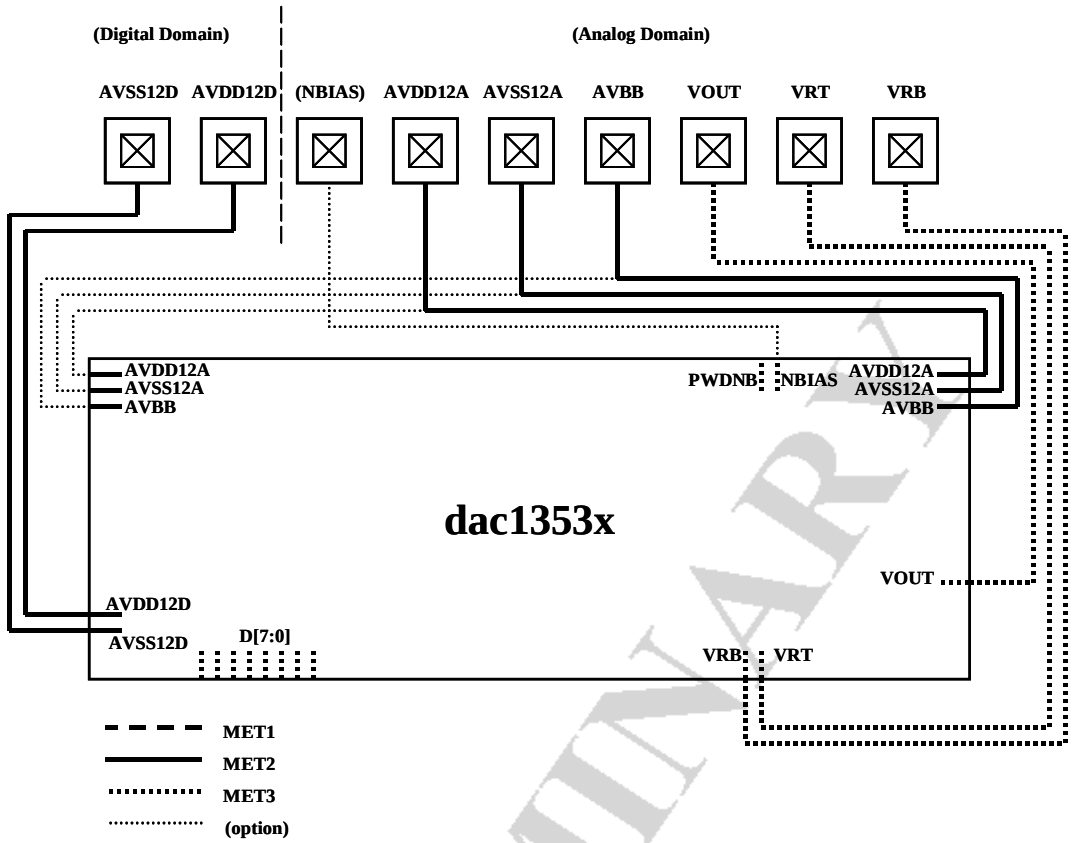
CORE LAYOUT GUIDE



Pin Name	Property	Pin Usage	Pin Layout Guide
D[7:0]	DI	Internal / External	1. Digital Input Signal lines must have same length to reduce propagation delay.
PWDNB	DI	Internal / External	
VRT	AB	External	1. Voltage reference lines (VRT and VRB) must be wide metal to reduce voltage drop of metal lines. 2. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
VRB	AB	External	
NBIAS	AB	Internal / External	
VOUT	AO	Internal / External	
AVDD12A	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used. 3. Each analog power / ground (AVDD12A, AVSS12A and AVBB) pin have two ports and you may connect just one of them, because they are connected internally.
AVSS12A	AG	External	
AVDD12D	DP	External	
AVSS12D	DG	External	
AVBB	AG	External	

1. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
2. The Bulk power is used to reduce the influence of substrate noise.

LAYOUT GUIDE WITH PADS



(1) It is recommended that you use thick analog power metal. When connecting to PAD, the path should be kept as short as possible, and use branch metal to connect to the center of analog switch block.
(ex. If analog supply current is 30mA, then analog power metal width should be kept over than 30um)

(2) Digital power and analog power should be used separately.

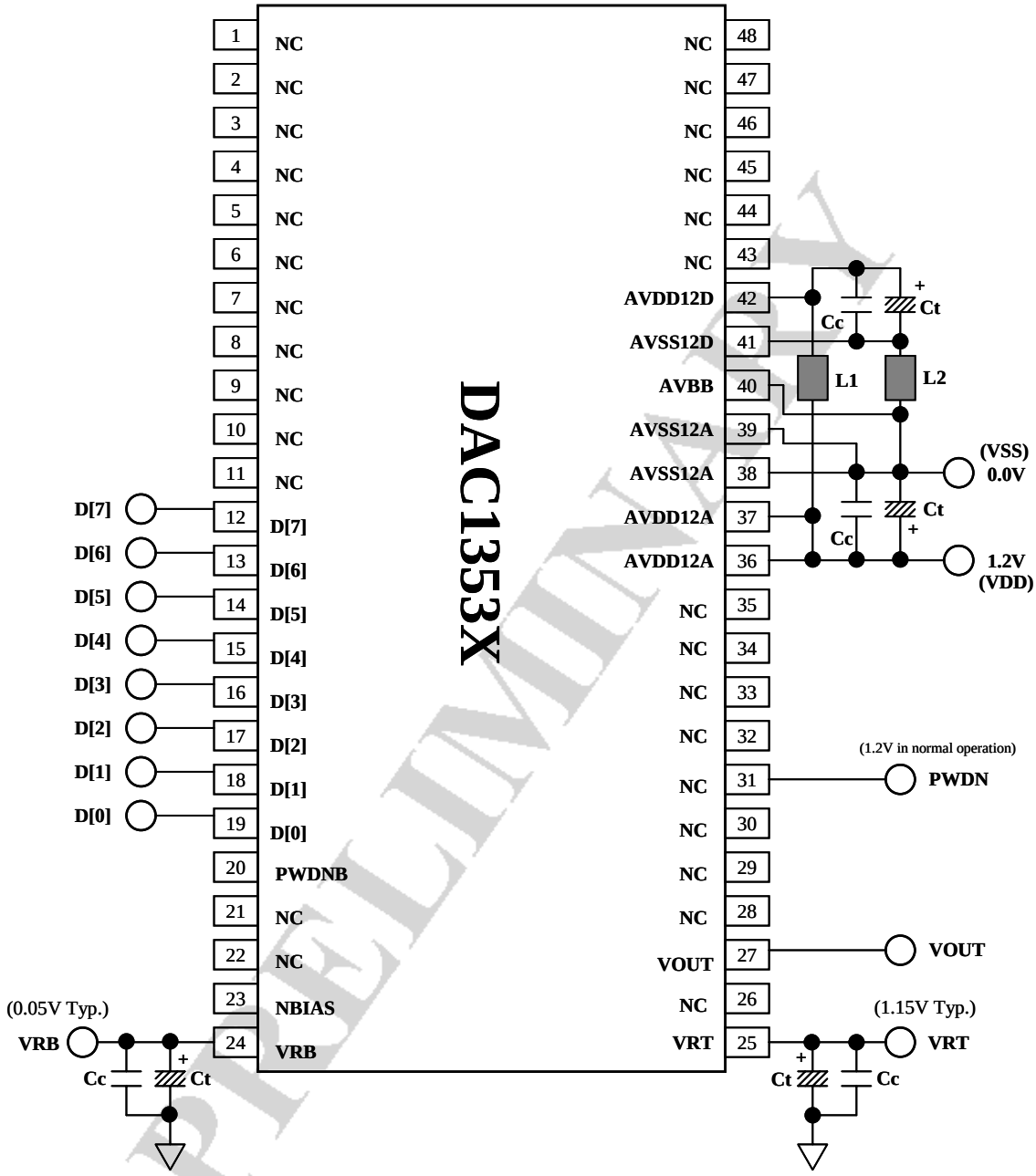
(3) The analog core should be placed near PAD as close as possible
.

(4) Bulk power is used to reduce the influence of substrate noise.

(5) VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.

(6) If you want to control the analog current, NBIAS pin should be connected to I/O PAD.

PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR
L1~L3	FERRITE BEAD (0.1mh)

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
AVDD12D	1,2	DP	Digital Power (1.8V)
AVSS12D	3,4	DG	Digital Ground (0.0V)
D[7:0]	10~17	DI	Digital Input Data
VRB	23,24	AB	Voltage Reference Bottom (0.0V)
VRT	25,26	AB	Voltage Reference Top (1.8V)
VOUT	29,30	AO	Analog Voltage Output
PWDNB	31	DI	Power Down Mode (Low Active)
AVDD12A	36,37	AP	Analog Power (1.8V)
AVSS12A	38,39	AG	Analog Ground (0.0V)
NBIAS	45	AB	Bias Generator Output Voltage
AVBB	47,48	AG	Analog Sub Bias (0.0V)
NC	5,6,7,8,9,18,19 20,21,22,27,28, 32,33,34,35,40, 41,42,f43,44,46	AO	No Connection

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

PC BOARD LAYOUT CONSIDERATION

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (AVDD12A, AVDD12D) and VSS (AVSS12A, AVSS12D) pins should be as short as possible so as to minimize inductive ringing.

2. Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor.
The digital power plane(AVDD12D) and analog power plane(AVDD12A) are connected through a ferrite bead, and also the digital ground plane(AVSS12D) and the analog ground plane(AVSS12A). This ferrite bead should be located within 3inches of the DAC1353X. The analog power plane supplies power to the DAC1353X of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in out products.
If you have further questions, please specify in the attached form.
Thank you very much.

DC / AC ELECTRICAL CHARACTERISTIC

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				kΩ	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC

Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC

Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				W	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Internal Reference Voltage(BGR)?
- Which do you want to Serial Input TYPE or parallel Input TYPE?
- Do you need 3.3V and 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0	01.01.30	Preliminary Version All pictures and texts are modified with DAC1326X datasheet. The format ant fonts of datasheet are same with DAC1326X's datasheet.	Reference datasheet DAC1236X dac1264x_ra DAC1326X