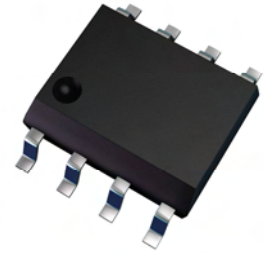


# ZXMC10A816N8

## 100V SO8 Complementary Dual enhancement mode MOSFET

### Summary

Device	$V_{(BR)DSS}$ (V)	$Q_G$ (nC)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) $T_A = 25^\circ\text{C}$
Q1	100	9.2	0.230 @ $V_{GS} = 10\text{V}$	2.1
			0.300 @ $V_{GS} = 4.5\text{V}$	1.9
Q2	-100	16.5	0.235 @ $V_{GS} = -10\text{V}$	-2.2
			0.320 @ $V_{GS} = -4.5\text{V}$	-1.9

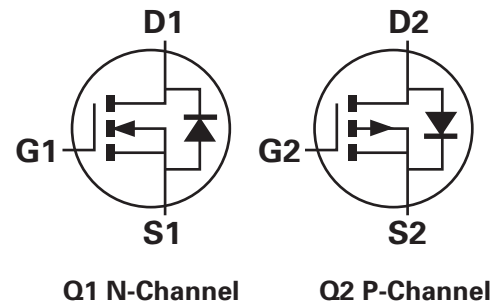


### Description

This new generation complementary dual MOSFET features low on-resistance achievable with low gate drive.

### Features

- 100 V Complementary in SOIC package
- Low on-resistance
- Fast switching speed
- Low voltage ( $V_{GS} = 4.5\text{ V}$ ) gate drive

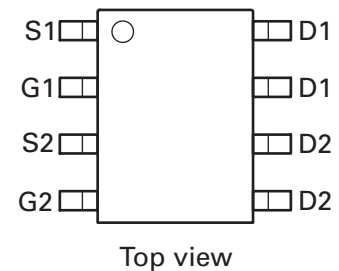


### Applications

- DC motor control
- Backlighting
- Class D Audio Output Stages (<100W)

### Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC10A816N8TC	13	12	2,500



### Device marking

ZXMC  
10A816

**Absolute maximum ratings**

Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source voltage	$V_{DSS}$	100	-100	V
Gate-Source voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain current @ $V_{GS}=10V$ ; $T_A=25^\circ C$ (b)(d) @ $V_{GS}=10V$ ; $T_A=70^\circ C$ (b)(d) @ $V_{GS}=10V$ ; $T_A=25^\circ C$ (a)(d) @ $V_{GS}=10V$ ; $T_A=25^\circ C$ (a)(e) @ $V_{GS}=10V$ ; $T_L=25^\circ C$ (f)(d)	$I_D$	2.1 1.7 1.7 2.0 2.3	-2.2 -1.8 -1.7 -2.0 -2.4	A
Pulsed Drain current @ $V_{GS}=10V$ ; $T_A=25^\circ C$ (c)(d)	$I_{DM}$	9.4	-10.5	A
Continuous Source current (Body diode) at $T_A=25^\circ C$ (b)(d)	$I_S$	3.0	-3.1	A
Pulsed Source current (Body diode) at $T_A=25^\circ C$ (c)(d)	$I_{SM}$	9.4	-10.5	A
Power dissipation at $T_A=25^\circ C$ (a)(d) Linear derating factor	$P_D$	1.3 10.0		W mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ (a)(e) Linear derating factor	$P_D$	1.8 14.2		W mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ (b)(d) Linear derating factor	$P_D$	2.1 16.7		W mW/ $^\circ C$
Power dissipation at $T_L=25^\circ C$ (f)(d) Linear derating factor	$P_D$	2.4 18.9	2.6 20.4	W mW/ $^\circ C$
Operating and storage temperature range	$T_j, T_{stg}$	-55 to 150		$^\circ C$

**Thermal resistance**

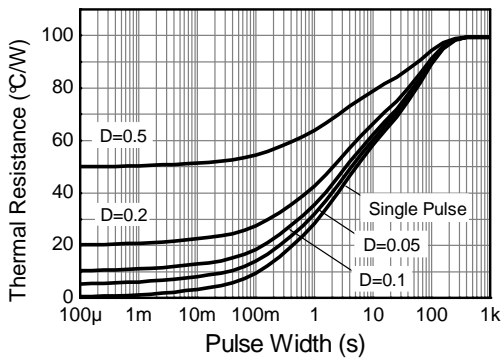
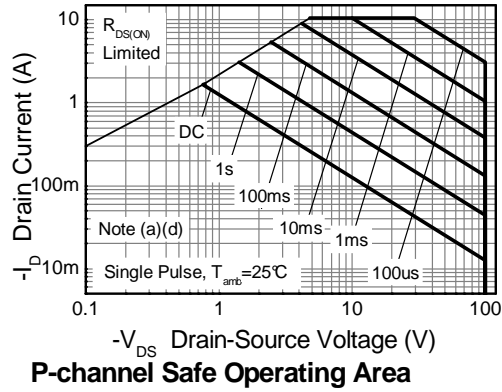
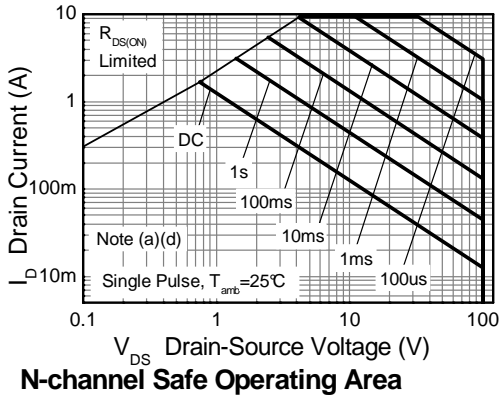
Parameter	Symbol	Value		Unit
Junction to ambient (a)(d)	$R_{\theta JA}$	100		$^\circ C/W$
Junction to ambient (a)(e)	$R_{\theta JA}$	70		$^\circ C/W$
Junction to ambient (b)(d)	$R_{\theta JA}$	60		$^\circ C/W$
Junction to lead (f)(d)	$R_{\theta JL}$	53	49	$^\circ C/W$

**NOTES:**

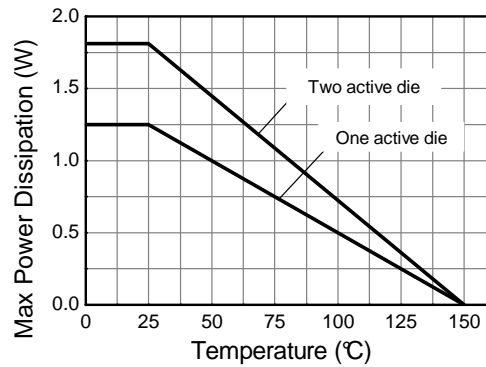
- (a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- (b) Same as note (a), except the device is measured at  $t \leq 10$  sec.
- (c) Same as note (a), except the device is pulsed with  $D=0.02$  and pulse width 300  $\mu s$ . The pulse current is limited by the maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition.

# ZXMC10A816N8

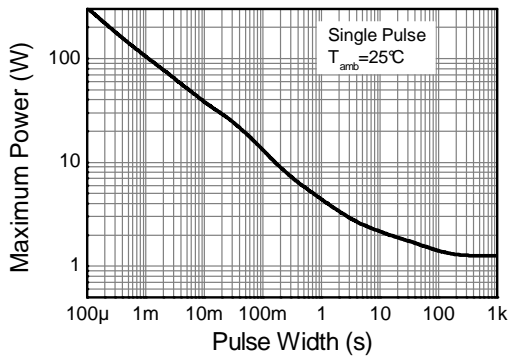
## Thermal characteristics



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

**ZXMC10A816N8****Q1 (N-channel) electrical characteristics (at  $T_{amb} = 25^{\circ}\text{C}$  unless otherwise stated)**

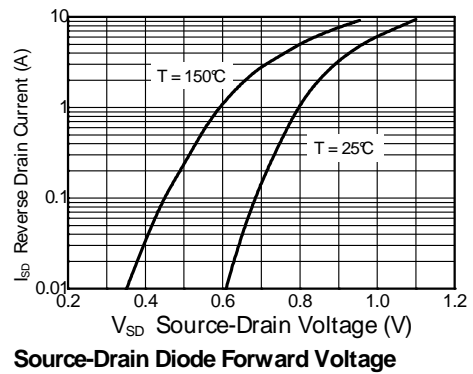
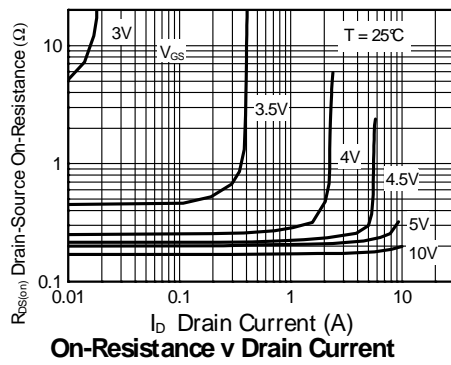
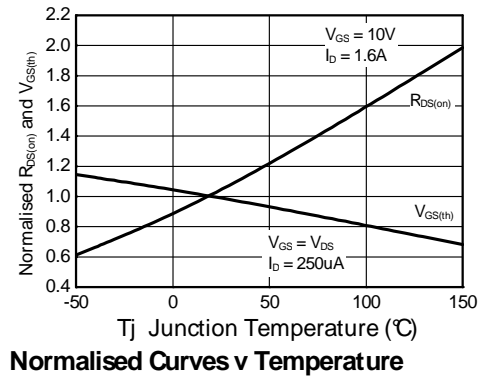
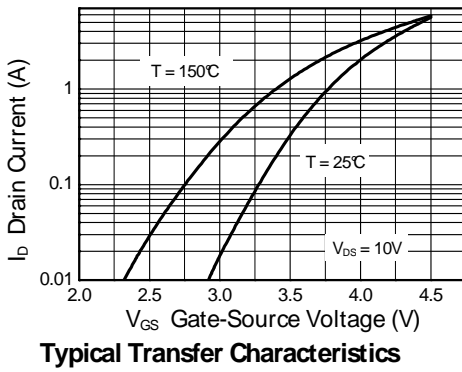
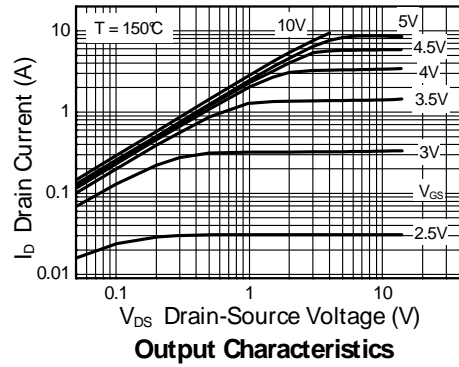
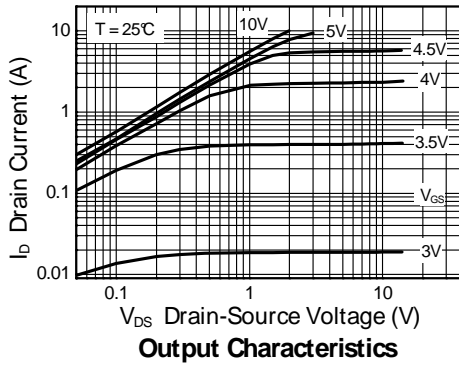
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Static</b>						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	100			V	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	$I_{DSS}$			0.5	$\mu\text{A}$	$V_{DS} = 100\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Body leakage	$I_{GSS}$			100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	$I_D = 250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance <sup>(a)</sup>	$R_{DS(on)}$		0.170 0.210	0.230 0.300	$\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 1.0\text{A}$ $V_{GS} = 4.5\text{V}$ , $I_D = 0.5\text{A}$
Forward Transconductance <sup>(a) (c)</sup>	$g_{fs}$		4.8		S	$V_{DS} = 15\text{V}$ , $I_D = 1.6\text{A}$
<b>Dynamic</b>						
<b>Capacitance</b> <sup>(c)</sup>						
Input capacitance	$C_{iss}$		497		pF	$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	$C_{oss}$		29		pF	
Reverse transfer capacitance	$C_{rss}$		18		pF	
<b>Switching</b> <sup>(b) (c)</sup>						
Turn-on-delay time	$t_{d(on)}$		2.9		ns	$V_{DD} = 50\text{V}$ , $V_{GS} = 10\text{V}$ $I_D = 1.0\text{A}$ $R_G \cong 6.0\Omega$ ,
Rise time	$t_r$		2.1		ns	
Turn-off delay time	$t_{d(off)}$		12.1		ns	
Fall time	$t_f$		5.0		ns	
<b>Gate charge</b> <sup>(c)</sup>						
Total Gate charge	$Q_g$		9.2		nC	$V_{DS} = 50\text{V}$ , $V_{GS} = 10\text{V}$ $I_D = 1.6\text{A}$
Gate-Source charge	$Q_{gs}$		1.7		nC	
Gate-Drain charge	$Q_{gd}$		2.5		nC	
<b>Source-Drain diode</b>						
Diode forward voltage <sup>(a)</sup>	$V_{SD}$		0.85	0.95	V	$I_S = 1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time <sup>(c)</sup>	$t_{rr}$		32		ns	$I_S = 1.7\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge <sup>(c)</sup>	$Q_{rr}$		40		nC	

**NOTES:**

- (a) Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
(b) Switching characteristics are independent of operating junction temperature.  
(c) For design aid only, not subject to production testing

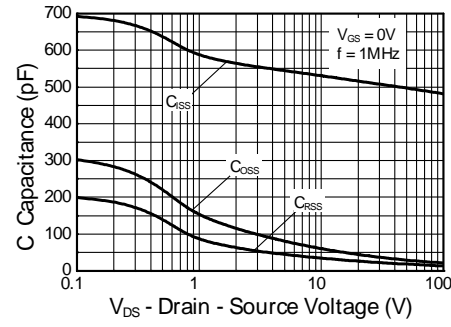
# ZXMC10A816N8

## Q1 (N-channel) typical characteristics

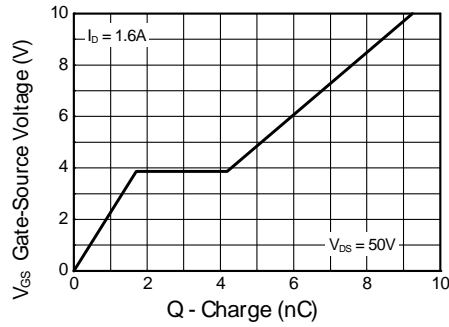


# ZXMC10A816N8

## Q1 (N-channel) typical characteristics –continued

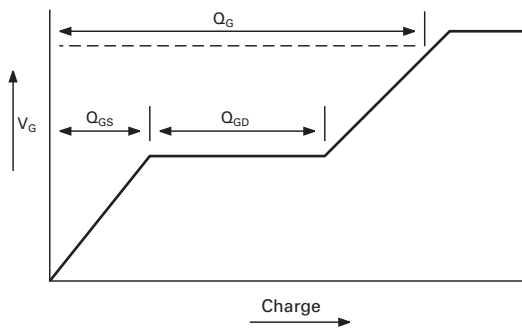


Capacitance v Drain-Source Voltage

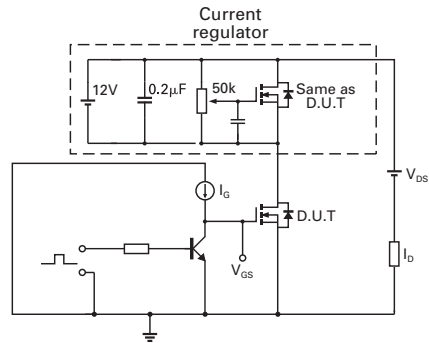


Gate-Source Voltage v Gate Charge

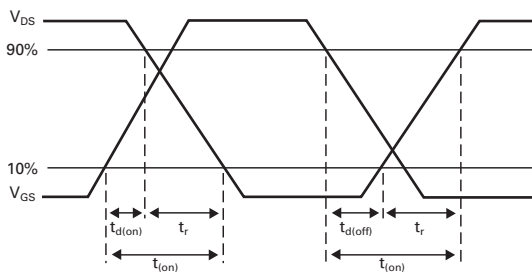
## Test circuits



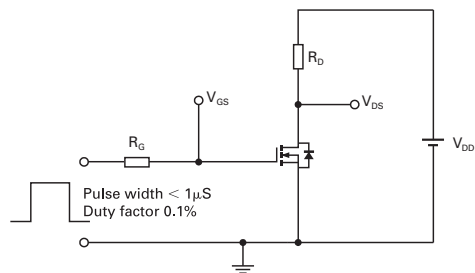
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

**ZXMC10A816N8****Q1 (P-channel) electrical characteristics (at  $T_{amb} = 25^{\circ}\text{C}$  unless otherwise stated)**

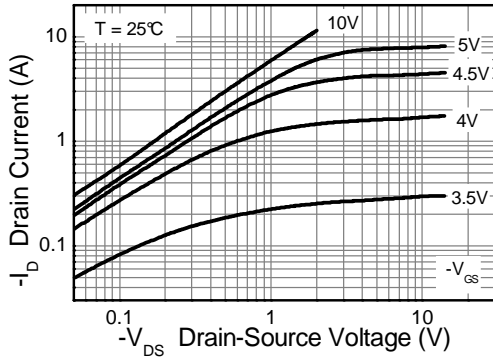
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Static</b>						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-100			V	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	$I_{DSS}$			-0.5	$\mu\text{A}$	$V_{DS} = -100\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Body leakage	$I_{GSS}$			100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	-2.0		-4.0	V	$I_D = -250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance <sup>(a)</sup>	$R_{DS(on)}$		0.170 0.250	0.235 0.320	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -1.0\text{A}$ $V_{GS} = -4.5\text{V}$ , $I_D = -0.5\text{A}$
Forward Transconductance <sup>(a) (c)</sup>	$g_{fs}$		4.7		S	$V_{DS} = -15\text{V}$ , $I_D = -2.1\text{A}$
<b>Dynamic</b>						
<b>Capacitance</b> <sup>(c)</sup>						
Input capacitance	$C_{iss}$		717		pF	$V_{DS} = -50\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	$C_{oss}$		55		pF	
Reverse transfer capacitance	$C_{rss}$		46		pF	
<b>Switching</b> <sup>(b) (c)</sup>						
Turn-on-delay time	$t_{d(on)}$		4.3		ns	$V_{DD} = -50\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ $R_G \cong 6.0\Omega$ ,
Rise time	$t_r$		5.2		ns	
Turn-off delay time	$t_{d(off)}$		20		ns	
Fall time	$t_f$		12		ns	
<b>Gate charge</b> <sup>(c)</sup>						
Total Gate charge	$Q_g$		16.5		nC	$V_{DS} = -50\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -2.1\text{A}$
Gate-Source charge	$Q_{gs}$		2.5		nC	
Gate-Drain charge	$Q_{gd}$		5.4		nC	
<b>Source-Drain diode</b>						
Diode forward voltage <sup>(a)</sup>	$V_{SD}$		-0.85	-0.95	V	$I_S = -1.7\text{A}$ , $V_{GS} = 0\text{V}$
Reverse recovery time <sup>(c)</sup>	$t_{rr}$		43		ns	$I_S = -1.7\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge <sup>(c)</sup>	$Q_{rr}$		77		nC	

**NOTES:**

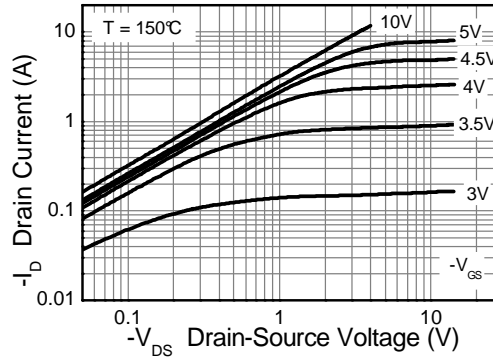
- (a) Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
(b) Switching characteristics are independent of operating junction temperature.  
(c) For design aid only, not subject to production testing

# ZXMC10A816N8

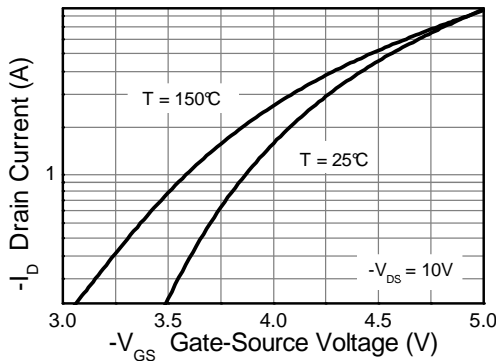
## Q2 (P-channel) typical characteristics



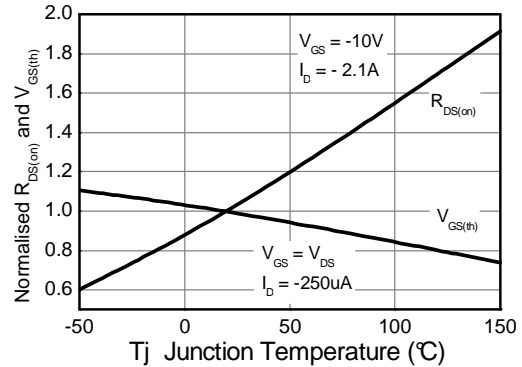
**Output Characteristics**



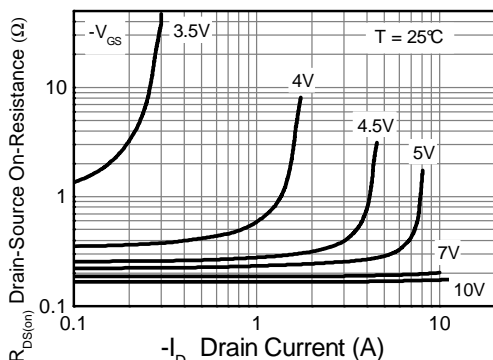
**Output Characteristics**



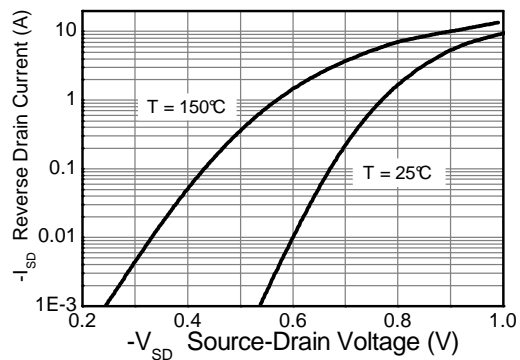
**Typical Transfer Characteristics**



**Normalised Curves v Temperature**



**On-Resistance v Drain Current**

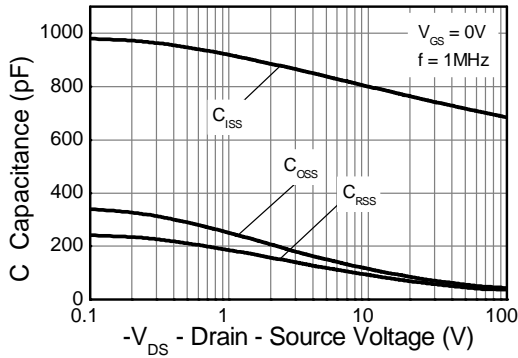


**Source-Drain Diode Forward Voltage**

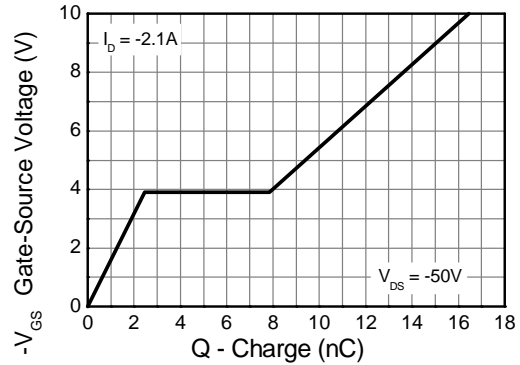


# ZXMC10A816N8

## Q2 (P-channel) typical characteristics –continued

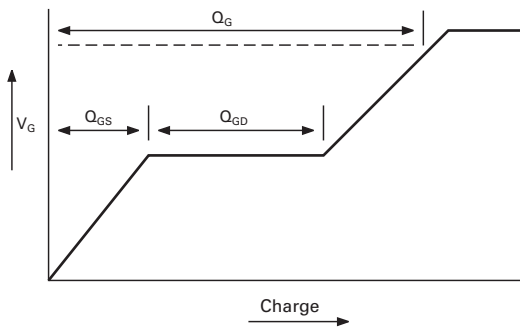


Capacitance v Drain-Source Voltage

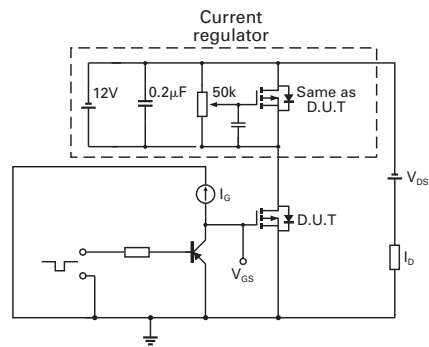


Gate-Source Voltage v Gate Charge

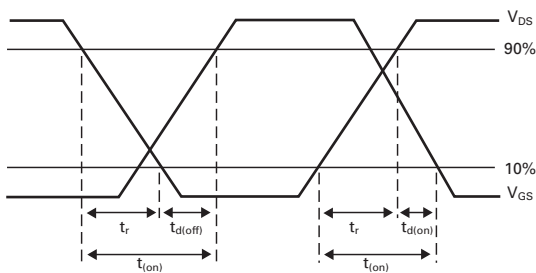
### Test circuits



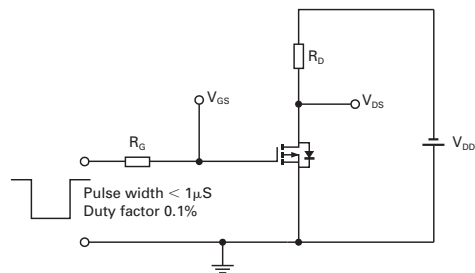
Basic gate charge waveform



Gate charge test circuit



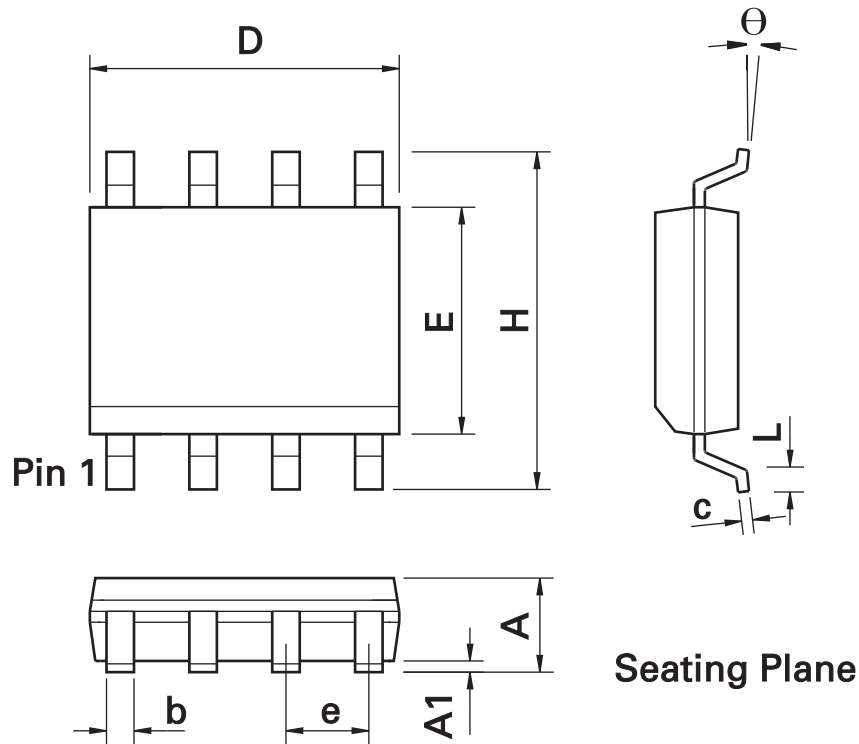
Switching time waveforms



Switching time test circuit

# ZXMC10A816N8

## Packaging details - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	$\theta$	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	-	-	-	-	-
L	0.016	0.050	0.40	1.27	-	-	-	-	-

**Note:** Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

## ZXMC10A816N8

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