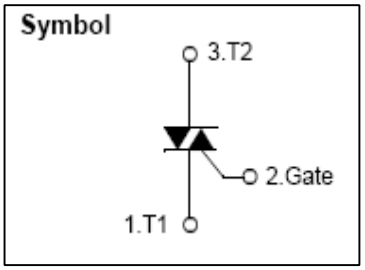
STN1A60S

Logic Level
Bi-Directional Triode Thyristor

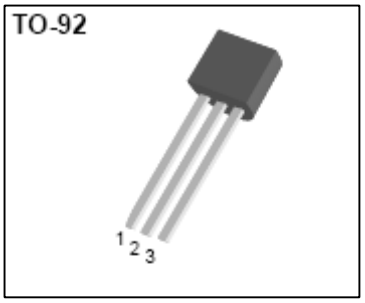
Features

- Repetitive Peak off-State Voltage: 600V
- R.M.S On-State Current($I_{T(RMS)}$=1A
- Low on-state voltage: V_{TM}=1.2(typ.)@ I_{TM}
- Low reverse and forward blocking current: I_{DRM}=500uA@TC=125℃
- Low holding current: I_H=4mA (typ.)
- High Commutation dV/dt.



General Description

General purpose switching and phase control applications. These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.



Absolute Maximum Ratings (T_J=25℃ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DRM}	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	600	V
$T_{(RMS)}$	Forward Current RMS (All Conduction Angles, T_L=50℃)	1	A
I_{TSM}	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	9.1/10	A
I^2t	Circuit Fusing Considerations (tp= 10 ms)	0.41	A^2s
P_{GM}	Peak Gate Power — Forward, (Tc = 58°C,Pulse with≤1.0us)	5	W
$P_{G(AV)}$	Average Gate Power — Forward, (Over any 20ms period)	0.1	W
dI/dt	Critical rate of rise of on-state current I_{TM} = 1.5A; I_G = 200mA; dI_G/dt = 200mA/μs T_J=125℃	50	A/μs
I_{FGM}	Peak Gate Current — Forward, Tj = 125°C (20 μs, 120 PPS)	0.5	A
V_{RGM}	Peak Gate Voltage — Reverse, Tj = 125°C (20 μs, 120 PPS)	6	V
$T_{J,}$	Junction Temperature	-40~125	℃
T_{stg}	Storage Temperature	-40~150	℃
	mass	2	g

Note1: .Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on-state. The rate of rise of current should not exceed 3A/us.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	60	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	120	℃/W

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Characteristics		Min	Typ.	Max	Unit
I_{DRM}	Peak Forward or Reverse Blocking Current (V_D= V_{DRM}/V_{RRM},gate open)	T_J=25℃ T_J=125℃	- -	- -	5 500	μA
V_{TM}	Forward "On" Voltage (I_{TM} = 1.5 A)	(Note2)	-	1.2	1.5	V
I_{GT}	Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, RL = 33 Ω)	T2+G+ T2+G- T2-G- T2-G+	- - - -	0.4 1.3 3 3.8	5 5 5 7	mA
V_{GT}	Gate Trigger Voltage (Continuous dc) (V_D =12 Vdc, RL = 33 Ω)	T2+G+ T2+G- T2-G- T2-G+	- - - -	- - - -	1.2 1.2 1.2 1.5	V
V_{GD}	Gate threshold voltage(T_J=125℃, V_D=V_{DRM},R_L=3.3KΩ)		0.2	-	-	V
dV/dt	Critical rate of rise of commutation Voltage (V_D=0.67V_{DRM},gate open)		10	20	-	V/μs
I_H	Holding Current (V_D =12 V, I_{GT} = 100 mA)		-	1.3	5	mA
I_L	latching current (V_D = 12 V; I_{GT} = 100 mA)	T2+G+ T2+G- T2-G- T2-G+	- - - -	1.2 4.0 1.0 2.5	5 8 5 8	mA
R_d	Dynamic resistance (T_J=125℃)		-	-	420	mΩ

Note 2. Forward current applied for 1 ms maximum duration, duty cycle

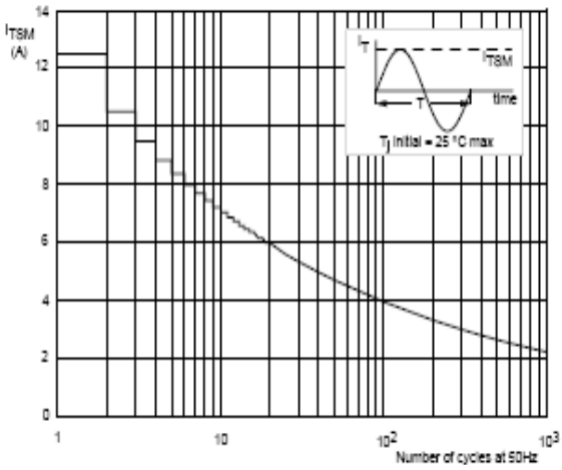


Fig.1 *Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

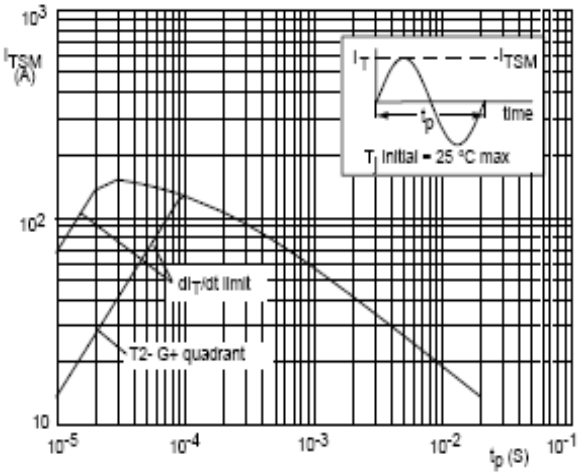


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

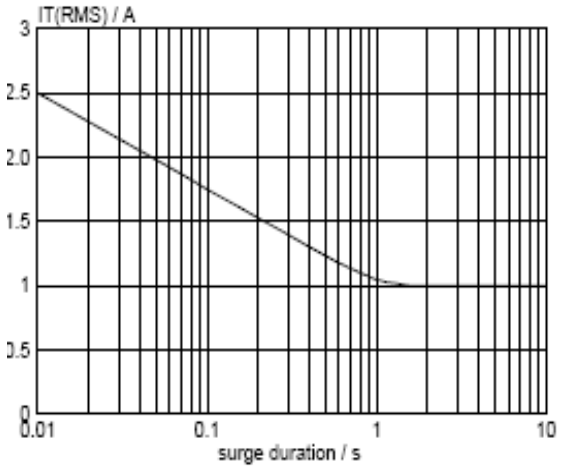


Fig.3 *Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 66°C$.*

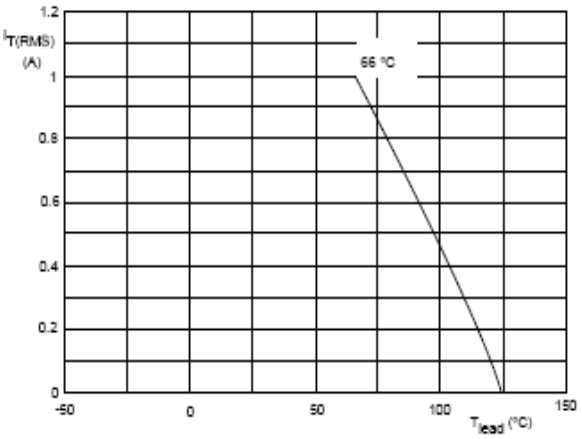


Fig.4 *Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead}.*

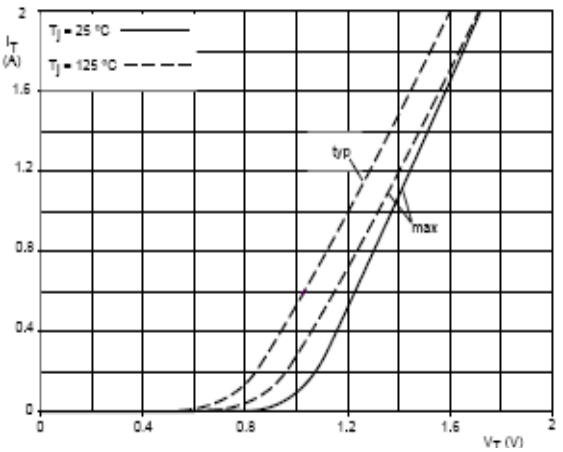


Fig.5 *Typical and maximum on-state characteristic.*

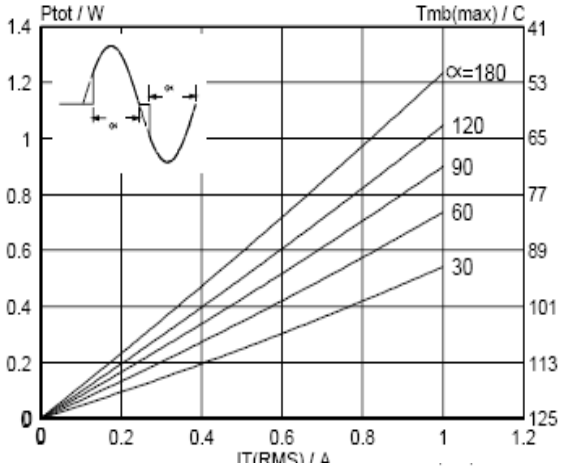


Fig.6 *Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

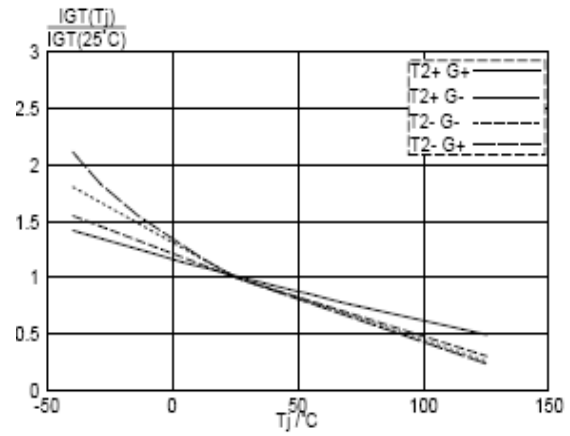


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature T_j.

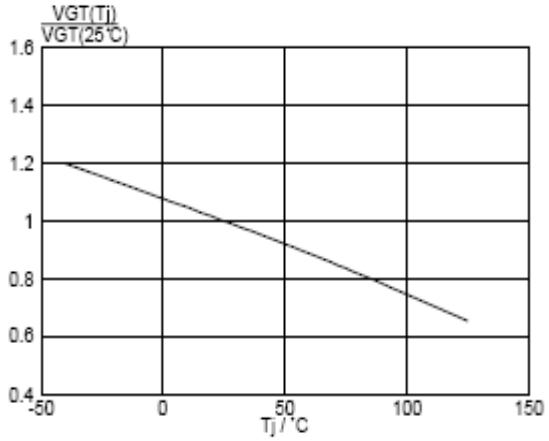


Fig.8 Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

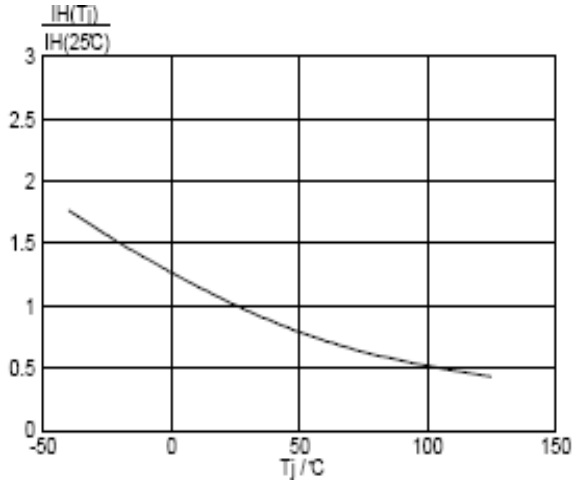


Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature T_j.

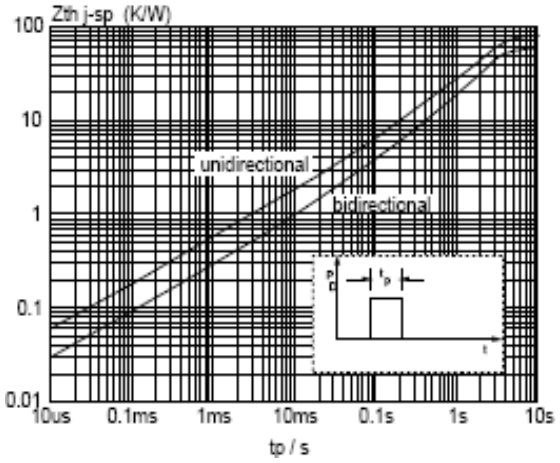


Fig.10 Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

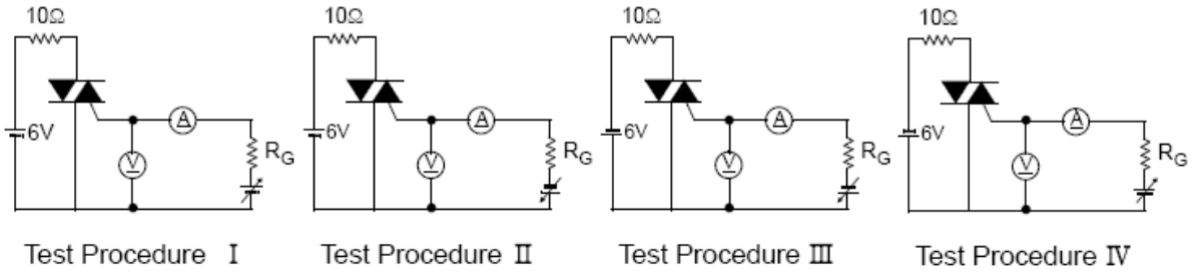


Fig.11 Gate Trigger Characteristics Test Circuit

TO-92 Package Dimension

Unit:mm