

# Am2805/2806/2807/2808

## 512- and 1024-Bit Dynamic Shift Registers

### Distinctive Characteristics

- Am2805 Plug-in Replacement Intel 1405A and Signetics 2505
- Am2806 Plug-in Replacement Signetics 2512
- Am2807 Plug-in Replacement Signetics 2524
- Am2808 Plug-in Replacement Signetics 2525

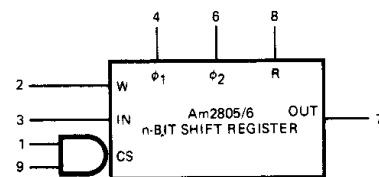
- On chip recirculate and chip select controls
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL and DTL compatible
- Full military temperature range devices available

### FUNCTIONAL DESCRIPTION

The Am2805 and Am2807 are 512-bit dynamic shift registers with recirculate logic on chip. The Am2806 and Am2808 are 1024-bit dynamic shift registers which also have built-in recirculate logic. When the write input is HIGH, data on the data input enters the first bit of the register during the  $\phi_2$  clock time. If the write input is LOW, then the output of the register is written into the first bit instead. Data in the last bit of the register appears on the data output during the  $\phi_1$  clock time if the read line is HIGH. If the read line is LOW, the output is OFF (high impedance state). The outputs of all four devices are open drains; they pull the output to  $V_{CC}$  when ON and exhibit a very high impedance when OFF. An external pull-down resistor to ground or  $V_{DD}$  must be used to establish the LOW logic level.

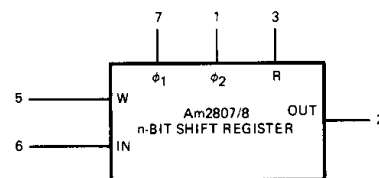
The Am2805 and Am2806 also have two chip select inputs,  $CS_1$  and  $CS_2$ . If either of these inputs is LOW, the register recirculates and the output remains OFF, regardless of the state of the read and write lines. All inputs except the clocks are TTL/DTL compatible. A TTL input may be driven by the output if a 3k pull-down resistor to  $V_{DD}$  is used. The register outputs can be wire-ORed for expansion. The devices are guaranteed to operate at speeds up to 3MHz.

### LOGIC SYMBOLS



Am2805 n = 512  
Am2806 n = 1024

$V_{CC}$  = Pin 5  
 $V_{DD}$  = Pin 10

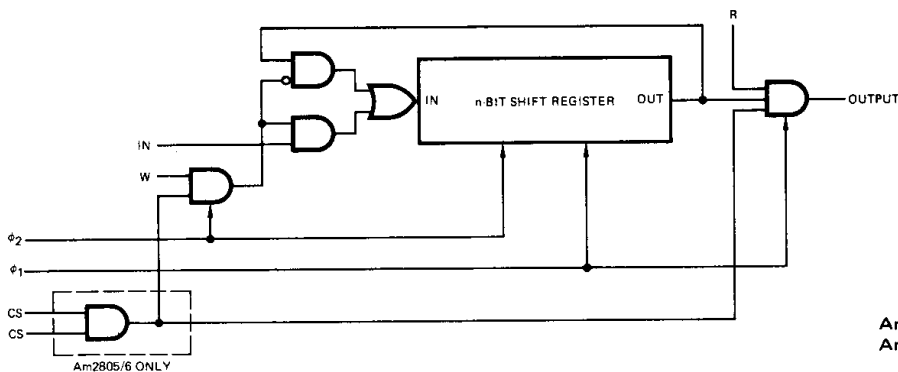


Am2807 n = 512  
Am2808 n = 1024

$V_{CC}$  = Pin 8  
 $V_{DD}$  = Pin 4

MOS-494

### LOGIC DIAGRAM



Am2805/7 n = 512  
Am2806/8 n = 1024

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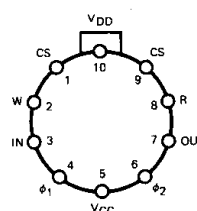
### ORDERING INFORMATION

Ambient Temperature	Package Type	Length	
		512 Bits	1024 Bits
$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	Molded DIP (8 Pin)	AM2807PC	AM2808PC
	TO-100 (10 Pin)	AM2805HC	AM2806HC
$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	TO-100 (10 Pin)	AM2805HM	AM2806HM

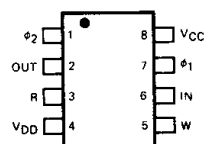
### CONNECTION DIAGRAMS

#### Top View

Am2805/6



Am2807/8



Note: PIN 1 is marked for orientation.

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**MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
DC Input Voltage with Respect to V <sub>CC</sub>	-20V to +0.3V

**ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (Unless Otherwise Noted)V<sub>DD</sub> = -5V ±5%, V<sub>CC</sub> = 5.0V ±5%Am280XXM T<sub>A</sub> = -55°C to +125°CAm280XXC T<sub>A</sub> = 0°C to +70°C

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units	
V <sub>OH</sub>	Output HIGH Voltage (Notes 2 & 3)	V <sub>CC</sub> = MIN. I <sub>OH</sub> = 1.6mA, (R <sub>L</sub> = 5.6kΩ) I <sub>OH</sub> = 2.6mA, (R <sub>L</sub> = 3kΩ)	3.6	4.0		Volts	
			2.4	3.5			
I <sub>OL</sub>	Output Leakage Current	V <sub>O</sub> = -5.5V, V <sub>φ1</sub> = V <sub>φ2</sub> = -12V		10	1000	nA	
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs except clocks	Am1405	V <sub>CC</sub> -2.0	V <sub>CC</sub> +0.3	Volts	
			Am2505/12/24/25	V <sub>CC</sub> -1.8	V <sub>CC</sub> +0.3		
			Am2805/6/7/8	V <sub>CC</sub> -1.0	V <sub>CC</sub> +0.3		
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs except clocks	V <sub>CC</sub> -10		V <sub>CC</sub> -4.2	Volts	
I <sub>I</sub>	Input Leakage Current	V <sub>IN</sub> = -5.5V, T <sub>A</sub> = 25°C		10	500	nA	
I <sub>φ</sub>	Clock Input Leakage Current	V <sub>φ</sub> = -12V, T <sub>A</sub> = 25°C		10	1000	nA	
V <sub>φH</sub>	Clock HIGH Level		V <sub>CC</sub> -1.0		V <sub>CC</sub> +0.3	V	
V <sub>φL</sub>	Clock LOW Level		V <sub>CC</sub> -17		V <sub>CC</sub> -14.5	V	
I <sub>DD</sub>	Power Supply Current (Note 4)	f = 1MHz, T <sub>A</sub> = 25°C Output Open V <sub>DD</sub> = -5.5V, t <sub>φL</sub> = 150ns	Am2805/7		7	12	mA
			Am2806/8		10	20	

Notes: 1. Typical Limits are at V<sub>CC</sub> = 5.0V, V<sub>DD</sub> = -5.0V, 25°C Ambient and maximum loading.2. Variations in V<sub>CC</sub> will be tracked directly by V<sub>OH</sub> and input thresholds.3. The output is open drain and the logic LOW level must be defined by an external pull-down resistor. A 3k resistor to V<sub>DD</sub> provides TTL compatibility.

4. The power supply current flows only while one clock is LOW. Average power is therefore directly proportional to clock duty cycle (ratio of clock LOW time to total clock period.) See curves next page.

**SWITCHING CHARACTERISTICS** (T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5.0V ±5%, V<sub>DD</sub> = -5.0V ±5%, V<sub>φL</sub> = -11V)

Parameters	Definition	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
f <sub>max</sub>	Maximum Clock and Data Rate	0°C to +70°C	4.0	7.0		MHz
		Am280XXM -55°C to +125°C	3.0			
t <sub>φd</sub>	Delay Between clocks		5.0		Note 5	ns
t <sub>φpw</sub>	Clock LOW Time		0.070		Note 8	μs
t <sub>r</sub> , t <sub>f</sub>	Clock Rise and Fall Times	10% to 90%			1.0	μs
t <sub>s(D)</sub>	Set-up Time, Data Input (see definitions)	t <sub>r</sub> = t <sub>f</sub> = 50ns			150	ns
t <sub>h(D)</sub>	Hold Time, Data Input (see definitions)	t <sub>r</sub> = t <sub>f</sub> = 50ns			0	ns
t <sub>s(C)</sub>	Set-up Time, Read, Write and Recirculate Controls (see definitions)	t <sub>r</sub> = t <sub>f</sub> = 50ns	135			ns
t <sub>h(C)</sub>	Hold Time, Read, Write and Recirculate Controls (see definitions)	t <sub>r</sub> = t <sub>f</sub> = 50ns	0			ns
t <sub>pd</sub>	Delay, Clock to Data Out	R = HIGH	0°C to +70°C		100	ns
			-55°C to +125°C		150	
C <sub>in</sub> , C <sub>out</sub>	Capacitance, Any Input and Output (Note 6)	f = 1MHz, V <sub>IN</sub> = V <sub>CC</sub>			5.0	pF
C <sub>φ</sub>	Clock Input Capacitance (Note 6)	f = 1MHz, V <sub>IN</sub> = V <sub>CC</sub>	Am2805/7		50	pF
			Am2806/8		100	

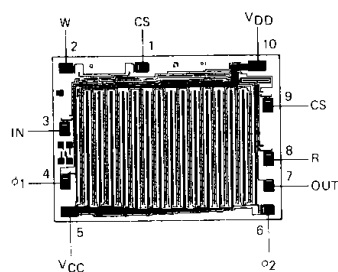
Notes: 5. The maximum delay between clocks (φ<sub>1</sub> and φ<sub>2</sub> both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency.

6. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

7. For some reason known only to God and Intel, the convention for φ<sub>1</sub> and φ<sub>2</sub> for this device are reversed from the normal. φ<sub>1</sub> is the output clock and φ<sub>2</sub> is the input clock.

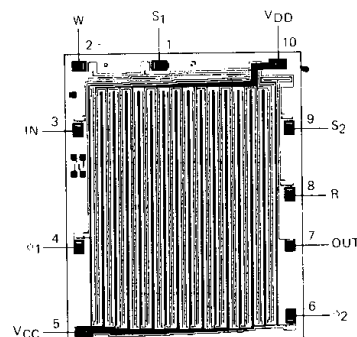
8. 100μsec or 50% duty cycle, whichever is less.

**Metallization and Pad Layout  
Am2805/7**



106 x 78 Mils

**Metallization and Pad Layout  
Am2806/8**



106 x 131 Mils

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

$\phi_1, \phi_2$  The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at  $V_{SS}$  or  $V_{CC}$ . Data is accepted into the master of each bit during  $\phi_2$  and is transferred to the slave of each bit during  $\phi_1$ .

$f_{max}$  The maximum frequency at which the register will operate. This is the data rate through the register and also the frequency of each clock signal.

$t_{\phi d}$  Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During  $t_{\phi d}$  both clocks are HIGH and all data is stored on capacitive nodes.

$t_{\phi pw}$  Clock pulse width. The LOW time of each clock signal. During  $t_{\phi pw}$  one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

$t_r, t_f$  Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occurring.

$t_s(D)$  Data set-up time. The time prior to the LOW-to-HIGH transition of  $\phi_2$  during which the data on the data input must be steady to be correctly written into the memory.

$t_h(D)$  Data hold time. The time following the LOW-to-HIGH transition of  $\phi_2$  during which the data must be steady. To correctly write data into the register, the data must be applied by  $t_s(D)$  before this transition and must not be changed until  $t_h(D)$  after this transition.

$t_s(C), t_h(C)$  The set-up and hold times for the Read, Write, and Chip Select controls, relative to the LOW-to-HIGH transition of the appropriate clock phase.

$t_{pd}$  The delay from the start of a read cycle to correct data present at the register output. A read cycle is begun when  $\phi_1$  is LOW AND Read is HIGH.

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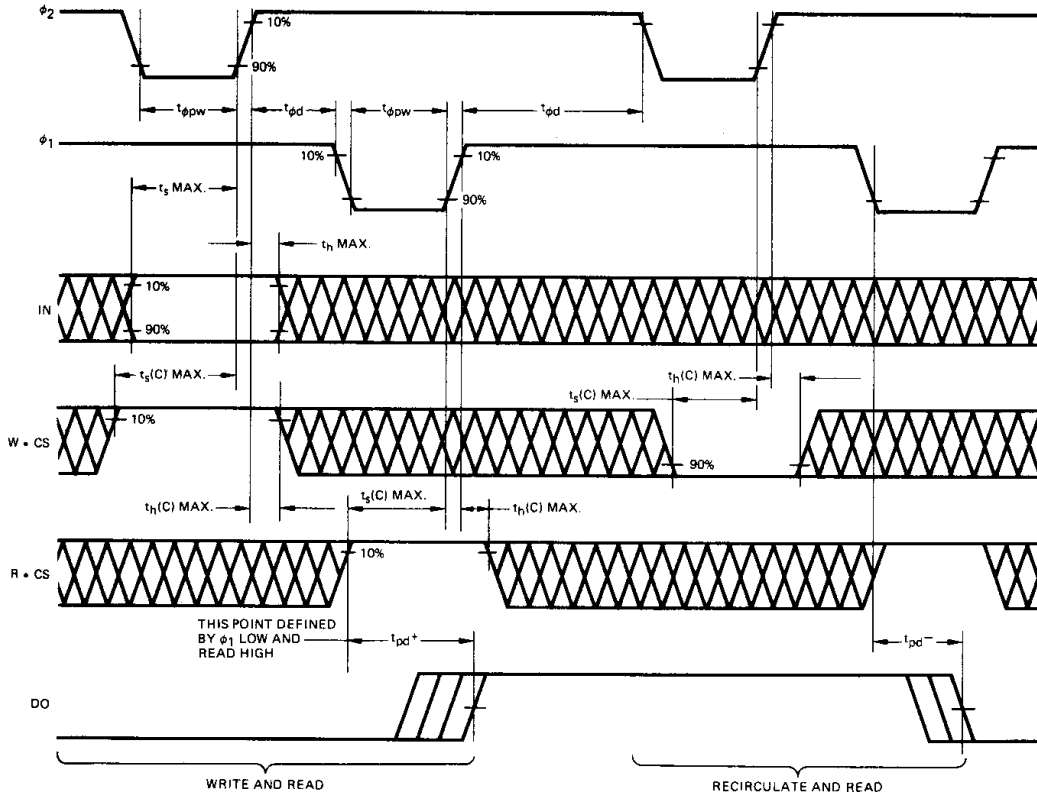
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SWITCHING WAVEFORMS



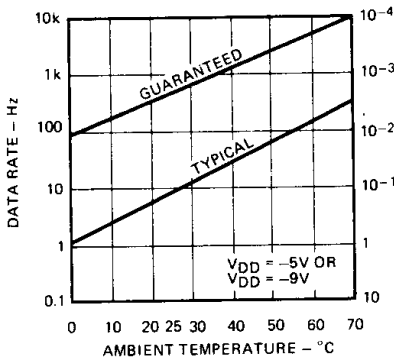
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KEY TO TIMING DIAGRAM

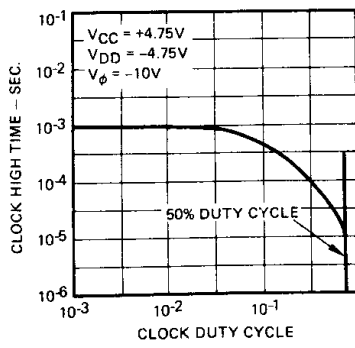
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

OPERATING CHARACTERISTICS

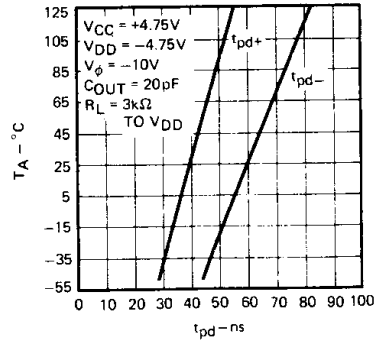
Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature



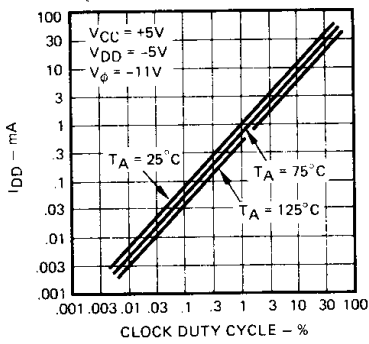
Maximum Clock High Time Versus Clock Duty Cycle



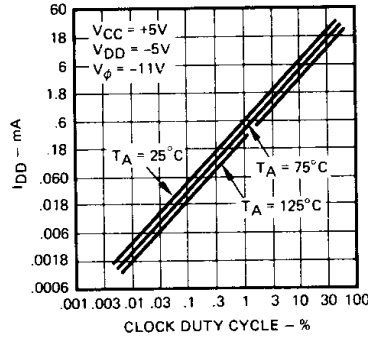
Propagation Delay Versus Ambient Temperature



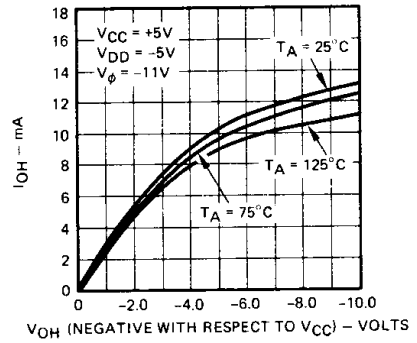
Am2806/8  
IDD Current Versus Clock Duty Cycle



Am2805/7  
IDD Current Versus Clock Duty Cycle



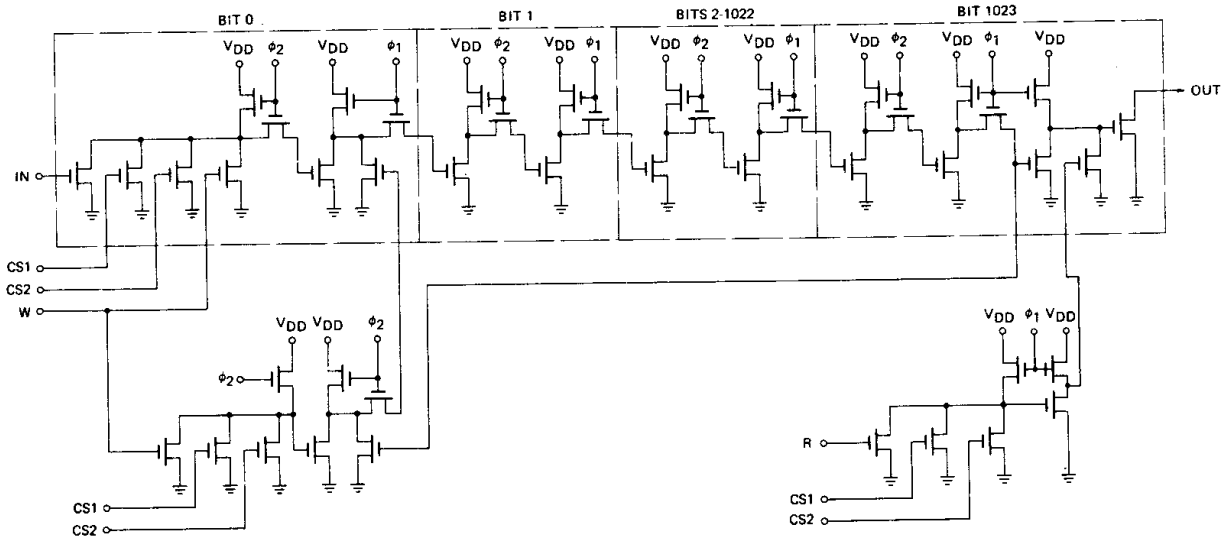
VOH Versus IOH



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SCHEMATIC DIAGRAM



Note: No CS inputs on Am2807/8

$\text{⏏} = V_{CC}$

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### APPLICATIONS

#### Multiplexed 2048-Bit Recirculating Register $f_{max} = 6\text{MHz}$

