KS0094

34 COM / 80 SEG DRIVER & CONTROLLER FOR STN LCD

Nov.1999.

Ver. 0.4

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KS0094 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Apr.1999
0.1	CGROM font table added at table 5 COM data shift direction changed at table 9 Read data instruction separation according to RE bit at table 10 Symbol register is changed to ICONRAM at table 12 IDD1 is changed at table 18, 19	May.1999
0.2	IDD1 is changed at table 18, 19	Jun.1999
0.3	Pad location added at table 1 and 2	July.1999
0.4	VDD change (2.4V~5.5V -> 2.4V~3.6V)	Nov.1999

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INTRODUCTION

The KS0094 is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 2, 3 or 4 lines of 16 characters with 5 x 8 dots format. It is capable of interfacing various microprocessors, supporting the 4-bit, 8-bit parallel modes and the clock synchronized serial mode. Voltage converter, oscillator, voltage regulator, voltage follower and bias circuit are built in the IC. The double height character mode and line vertical scroll functions are supported.

FEATURES

Driver Outputs

- Common outputs: 34 common
- Segment outputs: 80 segment

Applicable Panel Size

Font	Display	Duty	Contents of outputs
5 x 8	2-line x 16 characters	1 / 18	2 x 16 characters + 160 icons
	3-line x 16 characters	1 / 26	3 x 16 characters + 160 icons
	4-line x 16 characters	1 / 34	4 x 16 characters + 160 icons

Internal Memory

- Character Generator ROM (CGROM): 21,760 bits (544 characters x 5 x 8 dots)
- Character Generator RAM (CGRAM): 240 bits (6 characters x 5 x 8 dots)
- Display Data RAM (DDRAM): 640 bits (16 characters x 5 lines)
- Segment Icon RAM (ICONRAM): 160 bits (160 icons)

MPU Interface

- No busy MPU interface (no busy check or no execution waiting time)
- 8-bit parallel interface mode: 68-series and 80-series are available
- 4-bit parallel interface mode: 68-series and 80-series are available
- Serial interface mode: 4-pin clock synchronized serial interface

Function Set

- Various instructions set: display control, power save, power control, etc.
- COM / SEG bi-directional (4-type LCD application available)
- H/W reset (RESETB)

Built-in Analog Circuit

- Internal RC oscillator circuit or external clock
- Electronic volume for contrast control (32 steps)
- Voltage converter / voltage regulator / voltage follower & bias circuit

Low Power Operation

- Sleep mode operation (5uA Max.)
- Normal mode operation (TBD)

Operating Voltage Range

- Power supply voltage (V_{DD}): 2.2V – 3.6V
- LCD driving voltage (VLCD = V0 - V_{SS}): 7.0V Max.

Package Type

- Gold bumped chip

BLOCK DIAGRAM

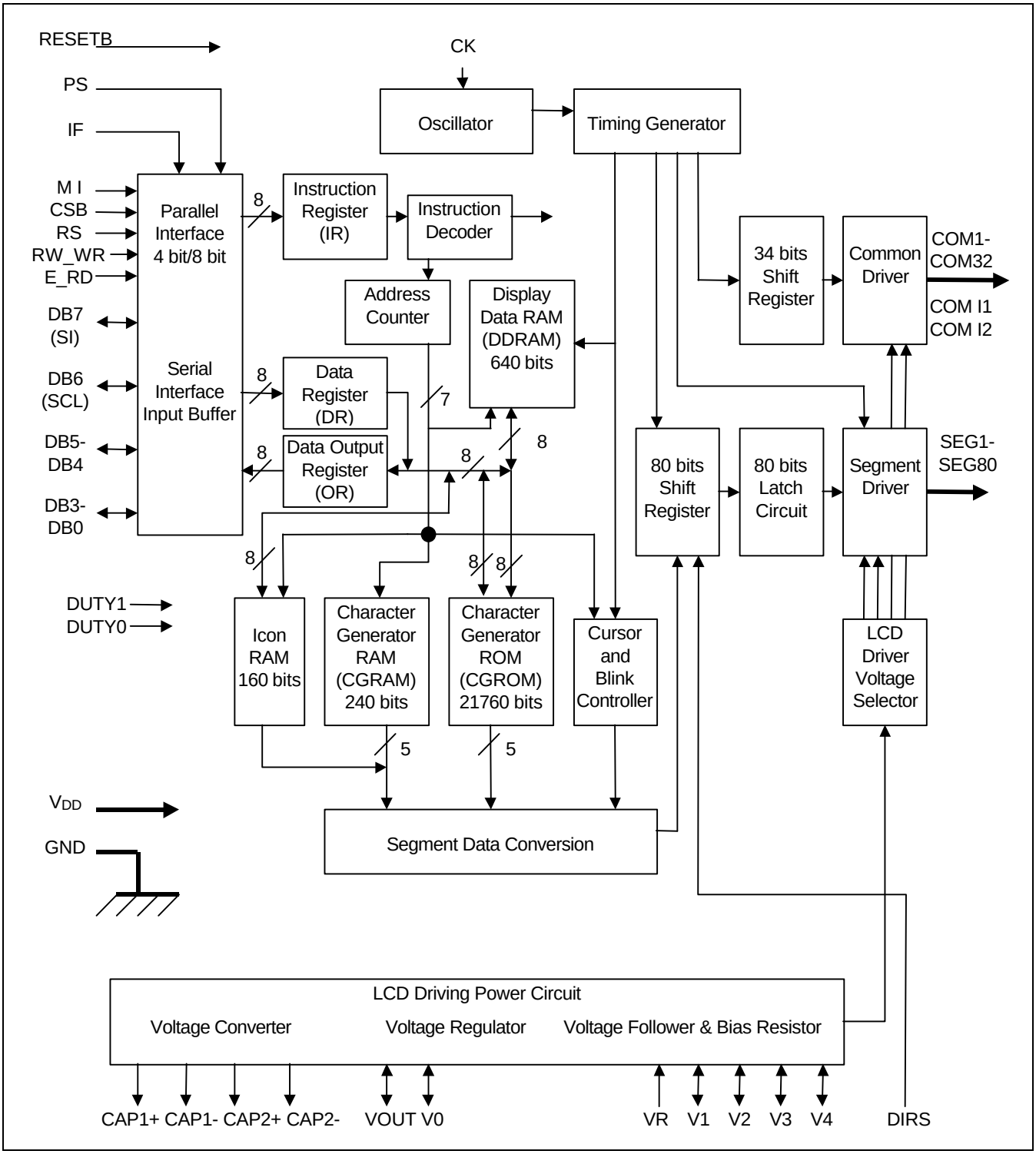


Figure 1. Block Diagram

PAD CONFIGURATION (NOT FIXED)

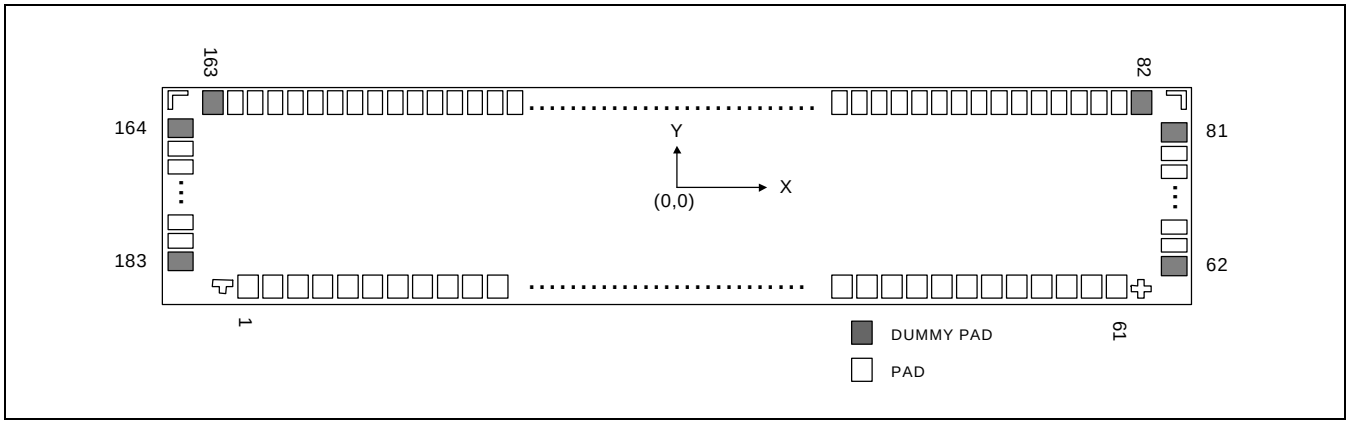
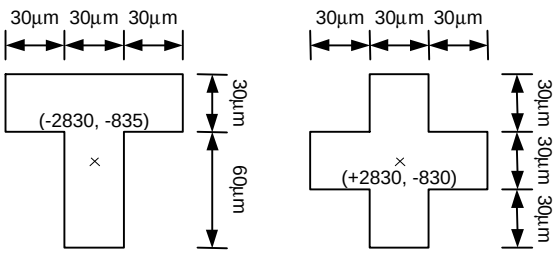


Figure 2. Pad Configuration

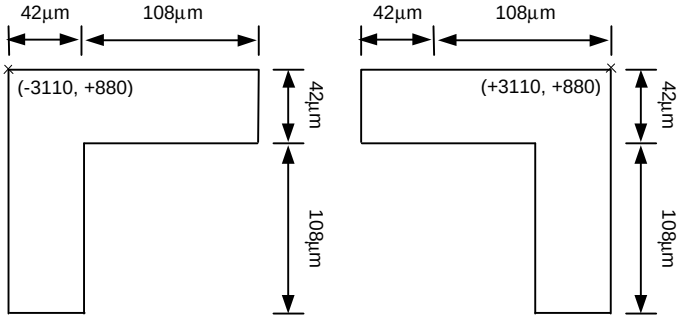
Table 1. KS0094 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	6320	1860	μm
Pad pitch	1 – 66	90		
	63~80,83~162,165~182	70		
	62,81,82,163,164,183	90		
Bumped pad size	1~61	60	100	
	63~80	100	50	
	83~162	50	100	
	165~182	100	50	
	62,81	100	60	
	82,163	60	100	
	164,183	100	60	
Bumped pad height	All pad	17 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate



SAMSUNG ELECTRONICS

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates [Unit: µm]

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	RS	-2700	-820	62	DUMMY	3050	-700	123	SEG41	-35	820
2	VSS	-2610	-820	63	COMI1	3050	-620	124	SEG42	-105	820
3	RW_WR	-2520	-820	64	COM1	3050	-550	125	SEG43	-175	820
4	VDD	-2430	-820	65	COM2	3050	-480	126	SEG44	-245	820
5	E_RD	-2340	-820	66	COM3	3050	-410	127	SEG45	-315	820
6	VSS	-2250	-820	67	COM4	3050	-340	128	SEG46	-385	820
7	CSB	-2160	-820	68	COM5	3050	-270	129	SEG47	-455	820
8	DB7	-2070	-820	69	COM6	3050	-200	130	SEG48	-525	820
9	DB6	-1980	-820	70	COM7	3050	-130	131	SEG49	-595	820
10	DB5	-1890	-820	71	COM8	3050	-60	132	SEG50	-665	820
11	DB4	-1800	-820	72	COM9	3050	10	133	SEG51	-735	820
12	DB3	-1710	-820	73	COM10	3050	80	134	SEG52	-805	820
13	DB2	-1620	-820	74	COM11	3050	150	135	SEG53	-875	820
14	DB1	-1530	-820	75	COM12	3050	220	136	SEG54	-945	820
15	DB0	-1440	-820	76	COM13	3050	290	137	SEG55	-1015	820
16	VDD	-1350	-820	77	COM14	3050	360	138	SEG56	-1085	820
17	VDD	-1260	-820	78	COM15	3050	430	139	SEG57	-1155	820
18	VSS	-1170	-820	79	COM16	3050	500	140	SEG58	-1225	820
19	VSS	-1080	-820	80	COMI1	3050	570	141	SEG59	-1295	820
20	V4	-990	-820	81	DUMMY	3050	650	142	SEG60	-1365	820
21	V4	-900	-820	82	DUMMY	2845	820	143	SEG61	-1435	820
22	V3	-810	-820	83	SEG1	2765	820	144	SEG62	-1505	820
23	V3	-720	-820	84	SEG2	2695	820	145	SEG63	-1575	820
24	V2	-630	-820	85	SEG3	2625	820	146	SEG64	-1645	820
25	V2	-540	-820	86	SEG4	2555	820	147	SEG65	-1715	820
26	V1	-450	-820	87	SEG5	2485	820	148	SEG66	-1785	820
27	V1	-360	-820	88	SEG6	2415	820	149	SEG67	-1855	820
28	V0	-270	-820	89	SEG7	2345	820	150	SEG68	-1925	820
29	V0	-180	-820	90	SEG8	2275	820	151	SEG69	-1995	820
30	V0	-90	-820	91	SEG9	2205	820	152	SEG70	-2065	820
31	V0	0	-820	92	SEG10	2135	820	153	SEG71	-2135	820
32	VR	90	-820	93	SEG11	2065	820	154	SEG72	-2205	820
33	VR	180	-820	94	SEG12	1995	820	155	SEG73	-2275	820
34	VSS	270	-820	95	SEG13	1925	820	156	SEG74	-2345	820
35	DUTY1	360	-820	96	SEG14	1855	820	157	SEG75	-2415	820
36	VDD	450	-820	97	SEG15	1785	820	158	SEG76	-2485	820
37	DUTY0	540	-820	98	SEG16	1715	820	159	SEG77	-2555	820
38	VSS	630	-820	99	SEG17	1645	820	160	SEG78	-2625	820
39	VOUT	720	-820	100	SEG18	1575	820	161	SEG79	-2695	820
40	VOUT	810	-820	101	SEG19	1505	820	162	SEG80	-2765	820
41	CAP2-	900	-820	102	SEG20	1435	820	163	DUMMY	-2845	820
42	CAP2-	990	-820	103	SEG21	1365	820	164	DUMMY	-3050	650
43	CAP2+	1080	-820	104	SEG22	1295	820	165	COMI2	-3050	570
44	CAP2+	1170	-820	105	SEG23	1225	820	166	COM32	-3050	500
45	CAP1-	1260	-820	106	SEG24	1155	820	167	COM31	-3050	430
46	CAP1-	1350	-820	107	SEG25	1085	820	168	COM30	-3050	360
47	CAP1+	1440	-820	108	SEG26	1015	820	169	COM29	-3050	290
48	CAP1+	1530	-820	109	SEG27	945	820	170	COM28	-3050	220
49	VSS	1620	-820	110	SEG28	875	820	171	COM27	-3050	150
50	DIRS	1710	-820	111	SEG29	805	820	172	COM26	-3050	80
51	VDD	1800	-820	112	SEG30	735	820	173	COM25	-3050	10
52	CK	1890	-820	113	SEG31	665	820	174	COM24	-3050	-60
53	VSS	1980	-820	114	SEG32	595	820	175	COM23	-3050	-130
54	PS	2070	-820	115	SEG33	525	820	176	COM22	-3050	-200
55	VDD	2160	-820	116	SEG34	455	820	177	COM21	-3050	-270
56	IF	2250	-820	117	SEG35	385	820	178	COM20	-3050	-340
57	VSS	2340	-820	118	SEG36	315	820	179	COM19	-3050	-410
58	MI	2430	-820	119	SEG37	245	820	180	COM18	-3050	-480
59	VDD	2520	-820	120	SEG38	175	820	181	COM17	-3050	-550
60	RESETB	2610	-820	121	SEG39	105	820	182	COMI2	-3050	-620
61	TEST	2700	-820	122	SEG40	35	820	183	DUMMY	-3050	-700

PIN DESCRIPTION

POWER SUPPLY

Table 3. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td rowspan="2">Power</td><td>Power supply
Connect to MPU power supply pin</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>Bias voltage level for LCD driving
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the built-in power circuit is active and internal 1/5 bias resistors are used.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table>
When the built-in power circuit is active and internal 1/4 bias resistors are used.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/4 bias</td><td>(3/4) x V0</td><td colspan="2">(2/4) x V0</td><td>(1/4) x V0</td></tr>
</table>
</td></tr>
</table>

LCD DRIVER SUPPLY

Table 3. Pin Description (Continued)

Name	I/O	Description
CAP1+	O	Capacitor + connecting pin for the internal voltage converter
CAP1-	O	Capacitor - connecting pin for the internal voltage converter
CAP2+	O	Capacitor + connecting pin for the internal voltage converter
CAP2-	O	Capacitor - connecting pin for the internal voltage converter
VOUT	I/O	DC/DC voltage converter output
VR	I	Voltage adjust pin This pin gives a voltage between V0 and VSS by resistance-division of voltage.

SYSTEM CONTROL

Table 3. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CK</td><td>I</td><td>External clock input
It must be fixed to "High" or "Low" when the internal oscillation circuit is used. In case of the external clock mode, CK is used as the clock and OS bit should be OFF.</td></tr>
<tr><td>MI</td><td>I</td><td>MPU interface selection input
MI = "Low": 80 series MPU
MI = "High": 68 series MPU</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / Serial selection input
When PS = "Low": Serial mode
When PS = "High": 4-bit/8-bit bus mode</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length selection pin for parallel data input
When PS = "Low"
IF = "Low" or "High": serial interface mode
When PS = “High”
IF = "Low": 4-bit bus mode
IF = "High": 8-bit bus mode</td></tr>
<tr><td>DIRS</td><td>I</td><td>SEG direction selection input
When DIRS = "Low”
SEG1 → SEG2 → SEG79 → SEG80
When DIRS = "High”
SEG80 → SEG79 → SEG2 → SEG1</td></tr>
<tr><td>DUTY1
DUTY0</td><td>I</td><td>Display line mode selection input
<table>
<tr><th>DUTY1</th><th>DUTY0</th><th>Mode</th><th>Duty</th></tr>
<tr><td>0</td><td>0</td><td>2-line</td><td>1/18</td></tr>
<tr><td>0</td><td>1</td><td>3-line</td><td>1/26</td></tr>
<tr><td>1</td><td>0/1</td><td>4-line</td><td>1/34</td></tr>
</table></td></tr>
</table>

MPU INTERFACE

Table 3. Pin Description (Continued)

Name	I/O	Description
RESETB	I	Reset input KS0094 is initialized while RESETB is low.
CSB	I	Chip selection input KS0094 is selected while CSB is low.
RS	I	Register selection input When RS = "Low", instruction register When RS = "High", data register
RW_WR	I	In 80-series MPU interface mode This pin is connected to WR pin of MPU and is an active low write signal. In 68-series MPU interface mode This pin is connected to R/W pin of MPU. When RW_WR = "Low", write mode When RW_WR = "High", read mode
E_RD	I	In 80-series MPU interface mode This pin is connected to RD pin of MPU and is a active low read signal. In 68-series MPU interface mode This pin is connected to E pin of MPU and enable read or write command according to RW_WR signal.
DB0 - DB3 DB4 - DB5 DB6 (SCL), DB7 (SI)	I/O	When 8-bit bus mode, used as bi-directional data bus DB0 - DB7. During 4-bit bus mode, only DB4 - DB7 are used. In this case DB0 - DB3 pins are not used. When serial mode, DB6 (SCL) is used as serial clock input pin and DB7 (SI) is used as serial data input pin.

LCD DRIVER OUTPUTS

Name	I/O	Description
COM1 – COM32	O	Common signal output for driving LCD
COMI1, COMI2	O	Common signal output for icon display
SEG1 – SEG80	O	Segment signal output for driving LCD

TEST

Name	I/O	Description
TEST	I	Test pin This pin is not used for normal operation. Open at normal operation mode

NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0094 has two kinds of interface type with MPU: bus mode, serial mode. Serial or bus mode is selected by PS pin. In bus mode, 4-bit bus or 8-bit bus is selected by IF pin, and 68 series MPU or 80 series MPU is selected by MI pin.

Table 4. Various Kinds of MPU Interface according to PS, MI and IF

PS	MI	IF	CSB	RS	RW_WR	E_RD	DB0~DB3	DB4~DB5	DB6	DB7
Bus mode (H)	68 series (H)	8 bit (H)	CSB	RS	R/$\overline{W}$	E	DB0~DB3	DB4~DB5	DB6	DB7
		4 bit (L)	CSB	RS	R/$\overline{W}$	E	*(1)	DB4~DB5	DB6	DB7
	80 series (L)	8 bit (H)	CSB	RS	$\overline{WR}$	$\overline{RD}$	DB0~DB3	DB4~DB5	DB6	DB7
		4 bit (L)	CSB	RS	$\overline{WR}$	$\overline{RD}$	*	DB4~DB5	DB6	DB7
Serial mode (L)	(H)/(L)(2)	(H)/(L)	CSB	RS	(H)/(L)	(H)/(L)	*	*	SCL	SI

NOTES:
1. ' * ': Don't care (High, Low or Open)
2. ' (H)/(L) ': Fixed High (V_{DD}) or Low (V_{SS})

PS: "High" = bus mode, "Low" = serial mode
MI: "High" = 68-series MPU, "Low" = 80-series MPU
IF: "High" = 8-bit mode, "Low" = 4-bit mode (PS: "High")
CSB: "High" = chip is not selected, "Low" = chip is selected
RS: "High" = data register, "Low" = instruction register
RW_WR: read / write indicating signal in 68 mode or active low signal for enabling write in 80 mode.
E_RD: active high signal for enabling command is 68 mode or active low signal for enabling read in 80 mode.
SCL (DB6): serial clock input
SI (DB7): serial data input

Interface with MPU in Parallel Mode (PS = "High")

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR), are used. The data register (DR) is used as temporary data storage place for being written into DDRAM / CGRAM / ICONRAM and one of these RAM is selected by RAM address setting instruction. The Instruction register (IR) is used only to store instruction code transferred from MPU. To select DR or IR register, RS input pin is used.

During reading operation, 8-bit register, output data register (OR) is used. The output data register (OR) is used as temporary data storage place for being read from DDRAM / CGRAM / ICONRAM and one of these RAM is selected by RAM address setting instruction. After RAM address setting, first reading is a dummy cycle in 8-bit bus mode (figure 3, 4). The valid data comes from second reading. In 4-bit bus mode, after RAM address setting, first and second reading are dummy cycles (figure 5, 6). The valid data comes from third reading. The dummy read make the address counter (AC) increased by 1. So it is recommended to set address again before writing. The instruction read cycle is not supported and it is regarded as a no operation cycle.

In 4-bit bus mode, it is needed to transfer 4-bit data (through DB7-DB4) by two times. The high order bits (for 8-bit mode DB7-DB4) are written before the low order bits (for 8-bit mode DB3-DB0) in write and low order bits (for 8-bit mode DB3-DB0) are read before the high order bits (for 8-bit mode DB7-DB4) in read transaction. The DB0-DB3 pins are floated in this 4-bit bus mode. After RESETB resets, KS0094 considers first 4-bit data from MPU as the high order bits.

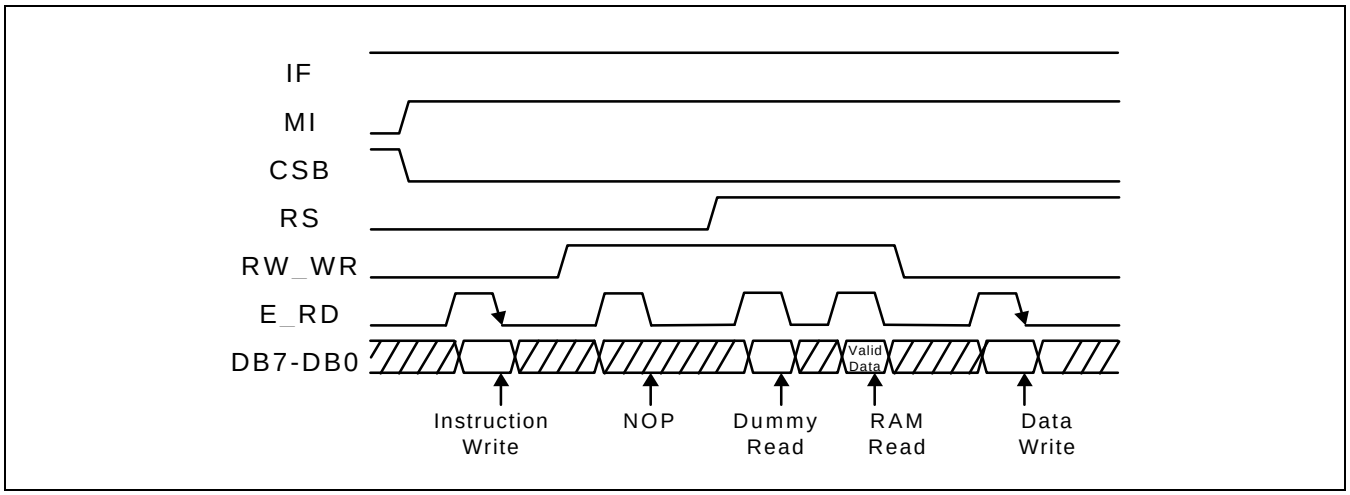


Figure 3. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

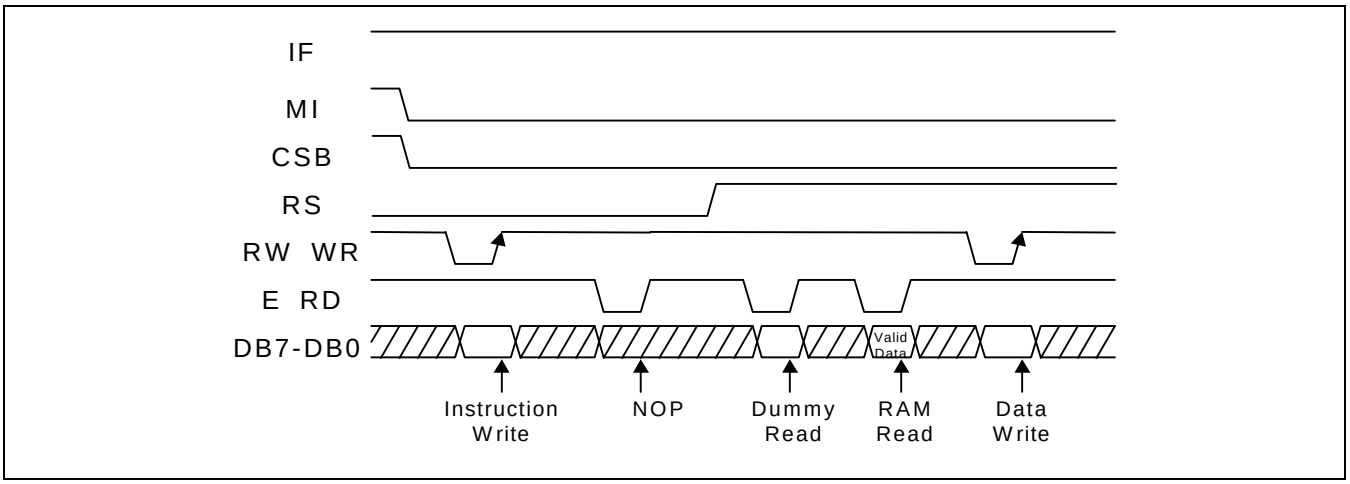


Figure 4. Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

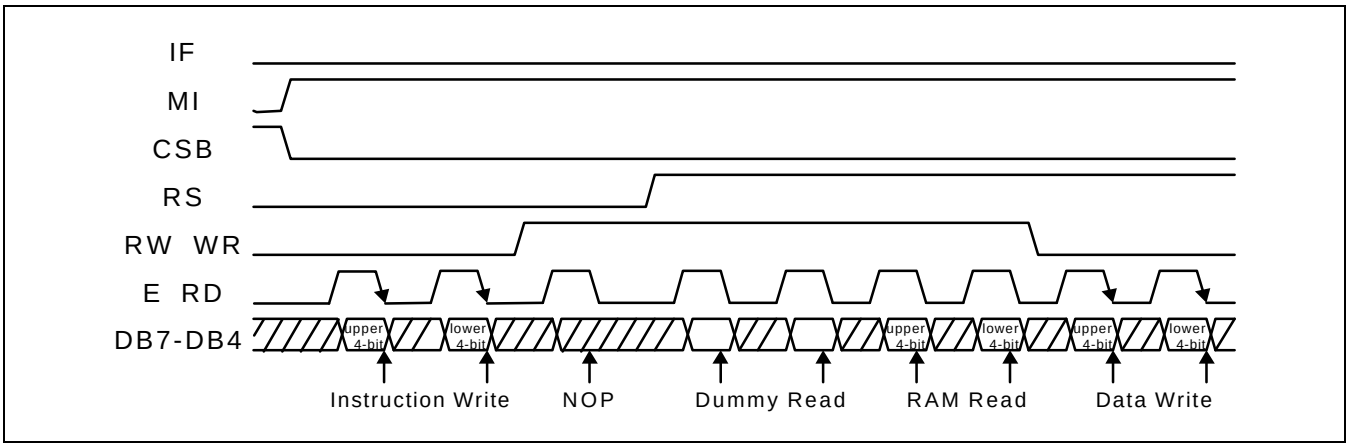


Figure 5. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

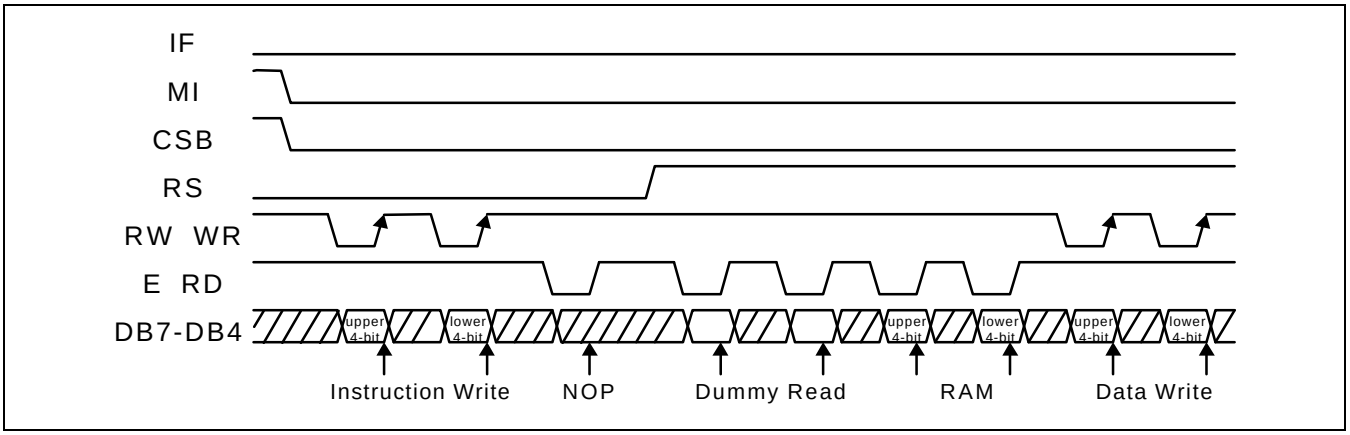


Figure 6. Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

Interface with MPU in Serial Mode (PS = "Low")

When PS input pin is "Low", clock synchronized serial interface mode is selected. At this time, four ports, SCL (DB6, synchronizing transfer clock), SI (DB7, serial input data), RS (register selection input) and CSB (chip selection input) are used.

By setting CSB to "Low", KS0094 can receive SCL input. If CSB is set to "High", KS0094 resets the internal 8-bit shift register and 3-bit counter. Serial data is input in the order of "D7, D6, D5, D4, D3, D2, D1, D0" from the serial data input pin (SI = DB7) at the rising edge of serial clock (SCL = DB6).

At the rising edge of the 8th serial clock, the serial data (D7-D0) is converted into 8 bit bus mode data. The RS input of the DR/IR selection is latched at the rising edge of the 8th serial clock (SCL).

In serial mode, the read is not possible.

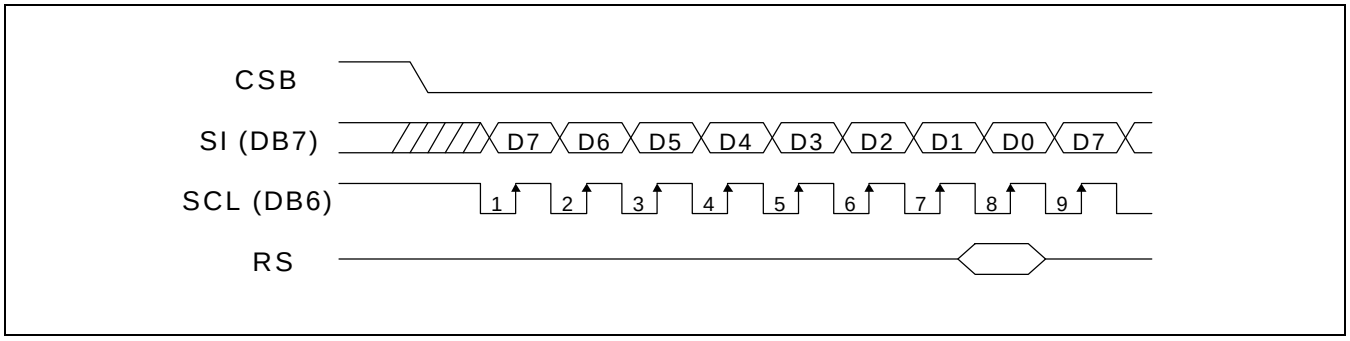


Figure 7. Timing Diagram of Serial Data Transfer

ADDRESS COUNTER (AC)

Address Counter (AC) in KS0094 stores DDRAM / CGRAM / ICONRAM address. After writing into or reading from DDRAM / CGRAM / ICONRAM, AC is automatically increased by 1. The address counter is only one and stores the address among DDRAM / CGRAM / ICONRAM.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (Max. 80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

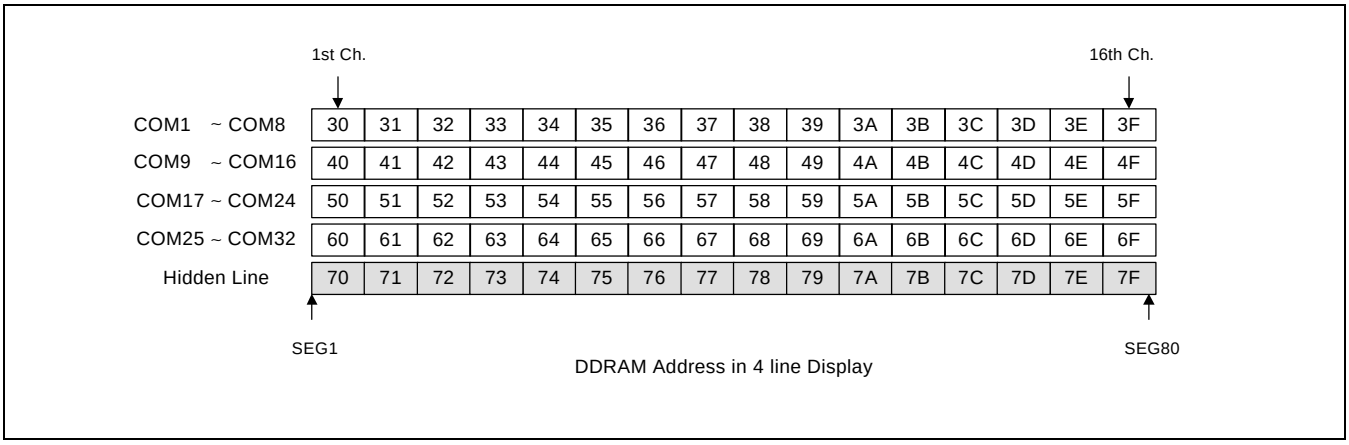


Figure 8. DDRAM Address

CHARACTER GENERATOR ROM (CGROM)

CGROM has one main ROM and four option ROM. The main CGROM has 160 characters and the option CGROMs have 96 characters each. The total CGROM has 5 x 8-dot 544 characters. The R1, R0 bits select an option CGROM between 4 option CGROM. If one of 4 CGROM is selected, the other CGROM font can not be used. The CG bit of the instruction table selects the 6 characters (00h ~ 05h) of CGROM or CGRAM.

Table 5. CGROM Character Code (Main ROM)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL																
LLLH																
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

Table 5. CGROM Character Code (Option ROM1) (Continued)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL																
LLLH																
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

Table 5. CGROM Character Code (Option ROM2) (Continued)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL																
LLLH																
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

Table 5. CGROM Character Code (Option ROM3) (Continued)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL																
LLLH																
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

Table 5. CGROM Character Code (Option ROM4) (Continued)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL																
LLLH																
LLHL																
LLHH																
LHLL																
LHLH																
LHHL																
LHHH																
HLLL																
HLLH																
HLHL																
HLHH																
HHLL																
HHLH																
HHHL																
HHHH																

CHARACTER GENERATOR RAM (CGRAM)

CGRAM has up to 5 x 8-dot 6 characters. By writing font data to CGRAM, user defined character can be used. CGRAM can be written regardless of CG bit.

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character code (DDRAM data)	CGRAM address		CGRAM data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	RE	A6 A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 0 0 0 (00h)	1	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0 1 0 1 0 0 0 0 1 1 0 0 0 0 0 1 1 1	- - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1 - - - 0 1 0 1 0 - - - 1 0 1 0 1	Pattern 1
0 0 0 0 0 0 0 1 (01h)	1	0 0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 0 1 0 1 0 0 0 0 1 0 1 1 0 0 0 1 1 0 0 0 0 0 1 1 0 1 0 0 0 1 1 1 0 0 0 0 1 1 1 1	- - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 1 1 1 1 1	Pattern 2
0 0 0 0 0 0 1 0 (02h)	1	0 0 1 0 0 0 0 0 0 1 0 0 0 1 0 0 1 0 0 1 0 0 0 1 0 0 1 1 0 0 1 0 1 0 0 0 0 1 0 1 0 1 0 0 1 0 1 1 0 0 0 1 0 1 1 1	- - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0 - - - 0 1 0 1 0	Pattern 3
0 0 0 0 0 0 1 1 (03h)	1	0 0 1 1 0 0 0 0 0 1 1 0 0 1 0 0 1 1 0 1 0 0 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 1 0 1 0 0 1 1 1 1 0 0 0 1 1 1 1 1	- - - 0 1 1 1 0 - - - 1 0 1 0 1 - - - 1 1 0 1 1 - - - 1 0 1 0 1 - - - 0 1 1 1 0 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1	Pattern 4

NOTE: ”-” - Don’t care

Table 6. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM) (continued)

Character code (DDRAM data)	CGRAM address		CGRAM data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	RE	A6 A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 1 0 0 (04h)	1	0 1 0 0 0 0 0 0 1 0 0 0 0 1 0 1 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 1 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1 0 0 1 0 0 1 1 1	- - - 1 1 0 1 1 - - - 1 0 0 0 1 - - - 0 0 0 0 0 - - - 1 0 0 0 1 - - - 1 1 0 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 1 1 1 1 1	Pattern 5
0 0 0 0 0 1 0 1 (05h)	1	0 1 0 1 0 0 0 0 1 0 1 0 0 1 0 1 0 1 0 1 0 0 1 0 1 0 1 1 0 1 0 1 1 0 0 0 1 0 1 1 0 1 0 1 0 1 1 1 0 0 1 0 1 1 1 1	- - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 0 0 0 0 0 - - - 1 1 1 1 1 - - - 1 1 1 1 1 - - - 0 0 0 0 0 - - - 0 0 0 0 0	Pattern 6

NOTE: ”-” - Don’t care

SEGMENT ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data. The number of icons is 160.

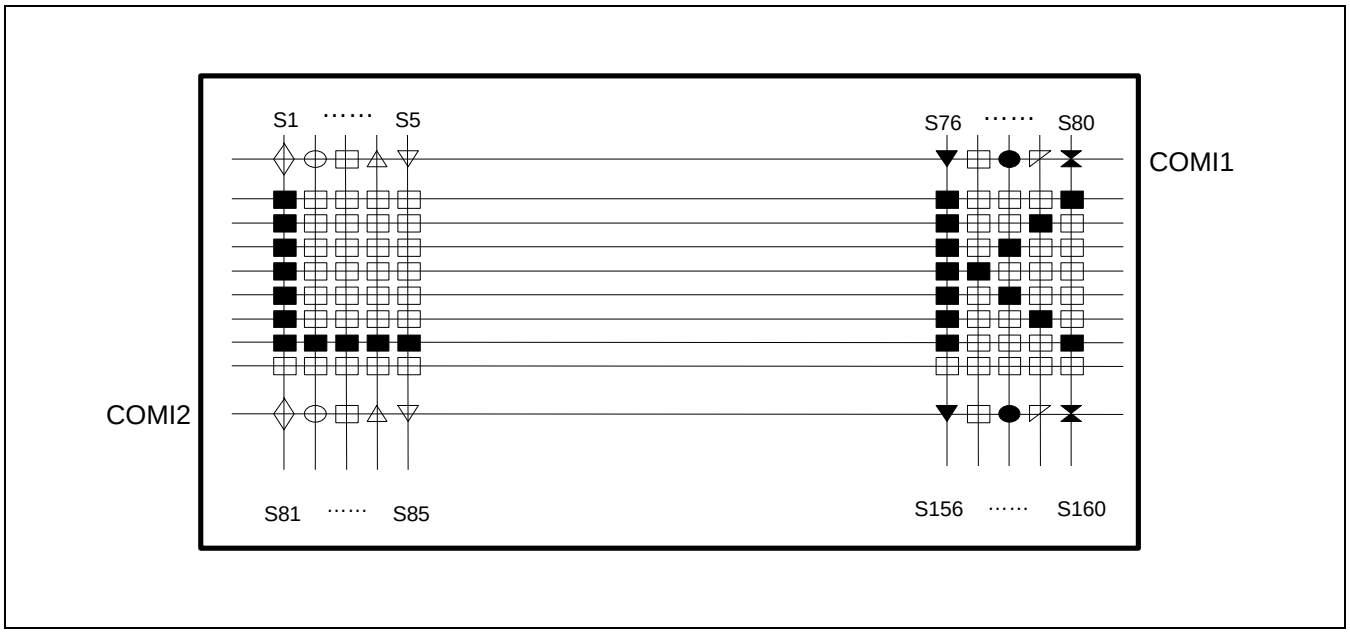


Figure 9. Relationship between ICONRAM and Icon Display

Table 7. Relationship between ICONRAM Address and Display Pattern

RE	ICONRAM address	ICONRAM bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	60h	-	-	-	S1	S2	S3	S4	S5
1	61h	-	-	-	S6	S7	S8	S9	S10
1	62h	-	-	-	S11	S12	S13	S14	S15
. .	. .	⋮	⋮	⋮		⋮			⋮
1	6Dh	-	-	-	S66	S67	S68	S69	S70
1	6Eh	-	-	-	S71	S72	S73	S74	S75
1	6Fh	-	-	-	S76	S77	S78	S79	S80
1	70h	-	-	-	S81	S82	S83	S84	S85
1	71h	-	-	-	S86	S87	S88	S89	S90
1	72h	-	-	-	S91	S92	S93	S94	S95
. .	. .	⋮	⋮	⋮		⋮			⋮
1	7Dh	-	-	-	S146	S147	S148	S149	S150
1	7Eh	-	-	-	S151	S152	S153	S154	S155
1	7Fh	-	-	-	S156	S157	S158	S159	S160

NOTE: ”-” - Don’t care

HIGH POWER MODE

The power circuit built-in the KS0094 is a low power consumption type (when the High Power mode is OFF). Accordingly, in the case of a large load liquid crystal or panel, the display quality may be degraded. In the case, the display quality can be improved by entering HPM = “1” by command. Before determining whether or not to use this mode. It is recommended to make a display check with real machine. In the case, the display quality cannot be improved satisfactorily though the power mode is set, a liquid crystal driver power must be supplied from the outside.

LOW POWER CONSUMPTION MODE

KS0094 provides with sleep mode for saving power consumption during standby period.

Sleep Mode (Power Save Bit ON, Oscillation Bit OFF)

To enter the Sleep mode, the power circuit and oscillation circuit should be turned off by using the power save command and the power control command. This mode helps to save power consumption by reducing current to reset level.

1. Liquid Crystal Display Output
   COM1 - COM32, COMI1, COMI2 : Vss level
   SEG1 - SEG80 : Vss level

2. Data written in DDRAM, CGRAM, ICONRAM and registers are remained as previous value.

3. Operation mode is retained the same as it was prior to execution of the sleep mode.
   All internal circuits are stopped.

4. Power Circuit and Oscillation Circuit
   The built-in power supply circuit and oscillation circuit are turned off by power save command and power control command.

LCD DRIVER CIRCUIT

LCD Driver circuit has 34 commons and 80 segments signals for driving LCD. Data from ICONRAM / CGRAM / CGROM are transferred to 80-bit segment register serially, and then they are stored to 80-bit shift latch. In case of 2-line display mode COM1 - COM16, COMI1 and COMI2 have 1/18 duty, in 3-line mode COM1 - COM24, COMI1 and COMI2 have 1/26 duty, and in 4-line mode COM1 - COM32, COMI1 and COMI2 have 1/34 duty ratio. SEG bi-directional function is selected by DIRS input pin, and COM shift direction is selected by function set instruction "SS" bit.

Table 8. SEG Data Shift Direction

DIRS pin	SEG data shift direction
Low	SEG1 → SEG2 → SEG3 ..... SEG78 → SEG79 → SEG80
High	SEG80 → SEG79 → SEG78 ..... SEG3 → SEG2 → SEG1

Table 9. COM Data Shift Direction

Line mode	CS	COM data shift direction
2-line mode	0 (left)	COM1 → COM2 ..... COM15 → COM16 → COMI1 → COMI2
	1 (right)	COM16 → COM15 ..... COM2 → COM1 → COMI1 → COMI2
3-line mode	0 (left)	COM1 → COM2 ..... COM23 → COM24 → COMI1 → COMI2
	1 (right)	COM24 → COM23 ..... COM2 → COM1 → COMI1 → COMI2
4-line mode	0 (left)	COM1 → COM2 ..... COM31 → COM32 → COMI1 → COMI2
	1 (right)	COM32 → COM31 ..... COM2 → COM1 → COMI1 → COMI2

INSTRUCTION DESCRIPTION

Table 10. Instruction Table

Instruction	RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Return home line shift	0	0	0	0	0	1	*	*	*	*	DDRAM address is set to 30h from AC and the cursor returns to home position The contents of DDRAM are not changed.
	1	0	0	0	0	1	*	*	LS1	LS0	Determination of the DDRAM line which is displayed at the first line at LCD LS1, LS0 = 00: DDRAM line 1 shows at the first line of LCD (default) 01: DDRAM line 2 shows at the first line of LCD 10: DDRAM line 3 shows at the first line of LCD 11: DDRAM line 4 shows at the first line of LCD
Line blink double height	0	0	0	0	1	0	LB4	LB3	LB2	LB1	Line blink mode LB4 = 0: DDRAM4 is normal display (default) 1: DDRAM4 is blink mode LB3 = 0: DDRAM3 is normal display (default) 1: DDRAM3 is blink mode LB2 = 0: DDRAM2 is normal display (default) 1: DDRAM2 is blink mode LB1 = 0: DDRAM1 is normal display (default) 1: DDRAM1 is blink mode
	1	0	0	0	1	0	DH4	DH3	DH2	DH1	Doubled height mode DH4 = 0: DDRAM4 is normal display (default) 1: DDRAM4 is double height DH3 = 0: DDRAM3 is normal display (default) 1: DDRAM3 is double height DH2 = 0: DDRAM2 is normal display (default) 1: DDRAM2 is double height DH1 = 0: DDRAM1 is normal display (default) 1: DDRAM1 is double height
Display control	0/1	0	0	0	1	1	C	B	RE	D	Cursor / blink / display ON / OFF C = 0: cursor OFF (default) 1: cursor ON B = 0: blink OFF (default) 1: blink ON RE=0: extension register OFF (default) 1: extension register ON D = 0: display OFF (default) 1: display ON
Power save	0/1	0	0	1	0	0	*	*	OS	PS	Power save / oscillation circuit ON / OFF OS = 0: oscillator OFF (default) 1: oscillator ON PS = 0: power save OFF (default) 1: power save ON

Table 10. Instruction Table (Continued)

Instruction	RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	1	0	1	HPM	VR	VF	VC	LCD power control HPM = 0: high power mode OFF (default) 1: High power mode ON VR = 0 : Voltage regulator OFF (default) 1 : Voltage regulator ON VF = 0 : Voltage follower OFF (default) 1 : Voltage follower ON VC = 0 : Voltage converter OFF (default) 1 : Voltage converter ON
	1	0	0	1	0	1	IRS	BS	IR1	IR0	Internal resistor select IRS = 0: external resistors are used for regulator (default) 1: internal resistors are used for regulator LCD bias select BS = 0: 1/5 bias (default) 1: 1/4 bias Internal resistor ratio select IR1, IR0 = 00: (1+Rb/Ra) = 2.81 01: (1+Rb/Ra) = 3.27 10: (1+Rb/Ra) = 3.50 11: (1+Rb/Ra) = 3.00
System set	0	0	0	1	1	0	R1	R0	CS	CG	Option CGROM select R1,R0 = 00: main ROM + option ROM1 (default) 01: main ROM + option ROM2 10: main ROM + option ROM3 11: main ROM + option ROM4 Shifting direction of COM CS = 0: COM1 → COM32 (default) 1: COM32 → COM1 Select CGRAM or CGROM CG = 0: CGROM (default), 1: CGRAM
	1	0	0	1	1	0	*	*	SS	*	Segment symmetry of each segment character SS = 0: normal character display (default) 1: symmetrical character display
DDRAM / CGRAM address set	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM or Electronic volume Address Range: 30h - 7Fh
	1	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	CGRAM or segment ICON RAM Address Range: 00h - 2Fh
Write data	0/1	1	D7	D6	D5	D4	D3	D2	D1	D0	Write DDRAM / CGRAM / ICONRAM/electronic volume RAM This is determined by the address set instruction executed immediately before writing data.
Read data	0/1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read DDRAM / CGRAM / ICONRAM This is determined by the address set instruction executed immediately before reading data.
NOP	0/1	0	0	0	0	0	0	0	0	0	Non-operation Instruction
Test	0/1	0	0	0	0	0	*	*	*	*	Don't use this Instruction

NOTES:
1. "-": Don't care
2. "*": Don't use

Return Home

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	*	*	*	*

*: Don't care

Return Home instruction field makes cursor return home. DDRAM address is set to 30h from address counter and the cursor returns to home position. The contents of DDRAM are not changed.

Line Shift Mode

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	*	*	LS2	LS1

*: Don't care

Line Shift mode instruction field selects the DDRAM to be displayed in first line.

LS1, LS0 = 00: scroll amount 0 line (default)
01: scroll 1 line upward (display line 1 from DDRAM line 2)
10: scroll 2 line upward (display line 2 from DDRAM line 3)
11: scroll 2 line upward (display line 3 from DDRAM line 4)

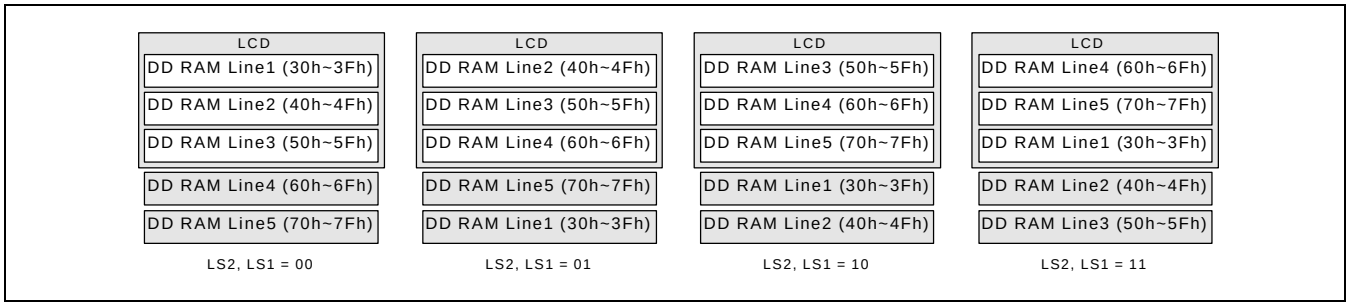


Figure 10. Line Shift Mode Display at 3-line LCD

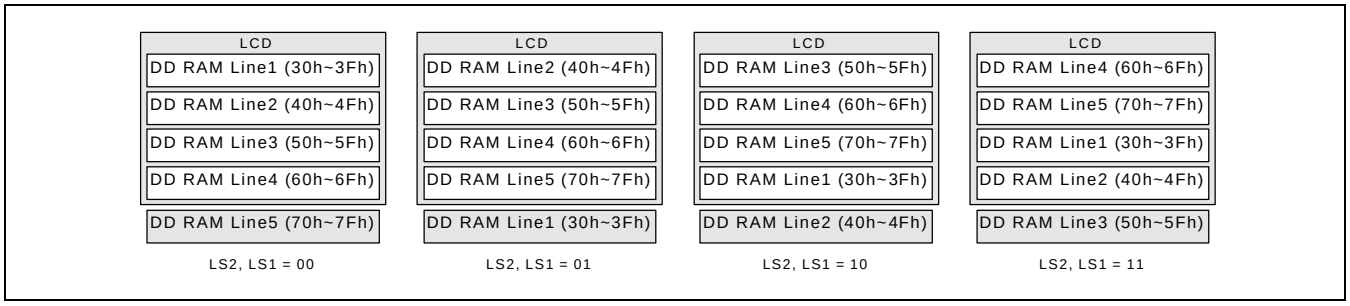


Figure 11. Line Shift Mode Display at 4-line LCD

Line Blink Display Control

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	LB4	LB3	LB2	LB1

Displays the specified line in black-and-white form. The specified line corresponds to the address line of DDRAM. Display the specified line of the DDRAM in black-and-white form by setting LB4 to LB1. Blinking is performed at the same frequency as cursor blink. If blinking is caused to occur at the same time, the cursor position will be hard to know.

LB4 = 0: displays the data for line 4 of the DDRAM in standard form (no blink)
(DDRAM 60H to 6FH)
= 1: displays the data for line 4 of the DDRAM in black-and-white reverse blink form
(DDRAM 60H to 6FH)

LB3 = 0: displays the data for line 3 of the DDRAM in standard form (no blink)
(DDRAM 50H to 5FH)
= 1: displays the data for line 3 of the DDRAM in black-and-white reverse blink form
(DDRAM 50H to 5FH)

LB2 = 0: displays the data for line 2 of the DDRAM in standard form (no blink)
(DDRAM 40H to 4FH)
= 1: displays the data for line 2 of the DDRAM in black-and-white reverse blink form
(DDRAM 40H to 4FH)

LB1 = 0: displays the data for line 1 of the DDRAM in standard form (no blink)
(DDRAM 30H to 3FH)
= 1: displays the data for line 1 of the DDRAM in black-and-white reverse blink form
(DDRAM 30H to 3FH)

Double Height Mode

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	0	DH4	DH3	DH2	DH1

Double Height mode instruction field selects double height line type.

DH4 = 0: displays the data for line 4 of the DDRAM in standard form
(DDRAM 60H to 6FH)
= 1: displays the data for line 4 of the DDRAM in vertical double size form
(DDRAM 60H to 6FH)

DH3 = 0: displays the data for line 3 of the DDRAM in standard form
(DDRAM 50H to 5FH)
= 1: displays the data for line 3 of the DDRAM in vertical double size form
(DDRAM 50H to 5FH)

DH2 = 0: displays the data for line 2 of the DDRAM in standard form
(DDRAM 40H to 4FH)
= 1: displays the data for line 2 of the DDRAM in vertical double size form
(DDRAM 40H to 4FH)

DH1 = 0: displays the data for line 1 of the DDRAM in standard form
(DDRAM 30H to 3FH)
= 1: displays the data for line 1 of the DDRAM in vertical double size form
(DDRAM 30H to 3FH)

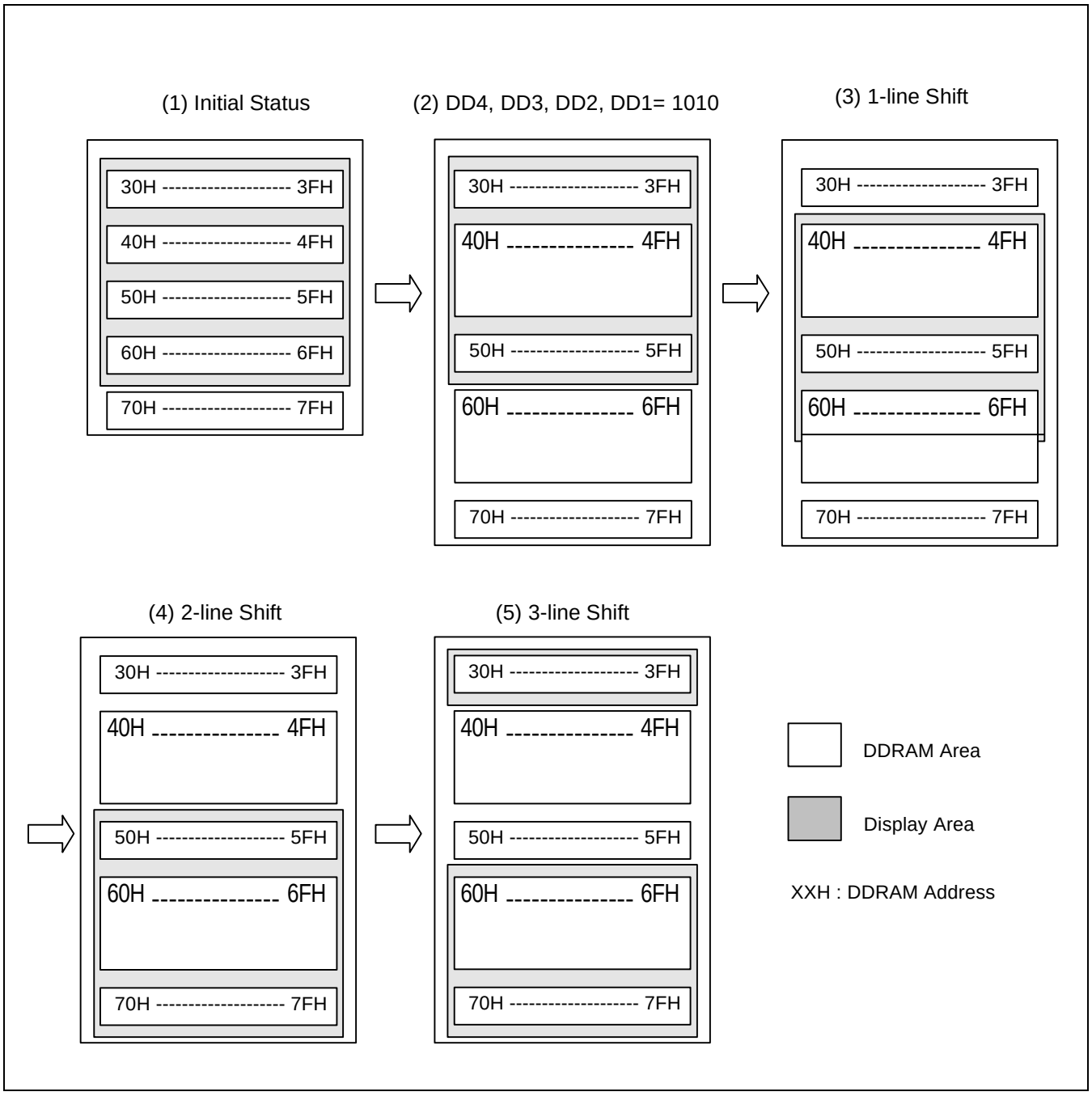


Figure 12. Line Double Height Mode Display

Display Control

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	0	0	0	1	0	C	B	RE	D

Display Control instruction field controls cursor / blink / display ON / OFF.

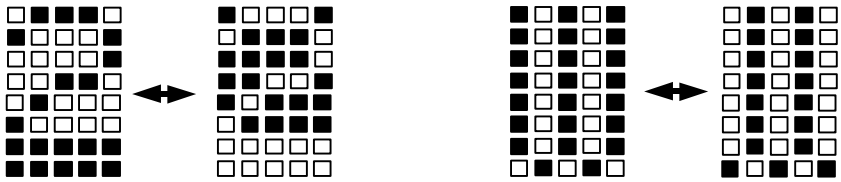
C: Cursor ON / OFF control bit
When C = "High", cursor is turned ON
When C = "Low", cursor is disappeared in current display (default).

B: Cursor blink ON / OFF control bit
When C = "High" and B = "High", KS0094 make LCD alternate between inverting display character and normal display character at the cursor position with about a half second. On the contrary, if C = "Low", only a normal character is displayed regardless of "B" flag.
When B = "Low", blink is OFF (default).

RE: Extended register access is specified by setting RE
When RE = “High”, extended register ON
When RE = “Low”, extended register OFF

D: Display ON / OFF control bit
When D = "High", entire display is turned ON.
When D = "Low", display is turned OFF, but display data are remained in DDRAM (default).

Table 11. Cursor Attributes

C, B	Display state
1, 0	
1, 1 (Blinking mode)	
0, 0 0, 1	

Power Save

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	0	0	1	0	0	*	*	OS	PS

*: Don't care

Power Save instruction field is used to control the oscillator and to set or to reset the power save mode.

OS: oscillator ON / OFF control bit
When OS = "High", internal oscillator is turned ON
When OS = "Low", internal oscillator is turned OFF (default)

PS: power save ON / OFF control bit
When PS = "High", power save mode is turned ON
When PS = "Low", power save mode is turned OFF (default)

Power Control (1)

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	HPM	VR	VF	VC

Power Control instruction field sets high power mode and voltage regulator / converter / follower ON / OFF.

HPM: high power mode control bit
When HPM = "High", high power mode is turned ON
When HPM = "Low", high power mode is turned OFF (default)

VR: voltage regulator circuit control bit
When VR = "High", voltage regulator is turned ON
When VR = "Low", voltage regulator is turned OFF (default)

VF: voltage follower circuit control bit
When VF = "High", voltage follower is turned ON
When VF = "Low", voltage follower is turned OFF (default)

VC: voltage converter circuit control bit
When VC = "High", voltage converter is turned ON
When VC = "Low", voltage converter is turned OFF (default)

NOTE: The oscillation circuit must be turned on for the voltage converter circuit to be active.

Power Control (2)

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	IRS	BS	IR1	IR0

IRS: initial resistors select
When IRS = "High", internal resistors are used for regulator
When IRS = "Low", external resistors are used for regulator (default)

BS: bias select
When BS = "High", it's 1/4 bias
When BS = "Low", it's 1/5 bias (default)

IR1, IR0: internal resistor ratio select
When IR1,IR0 = 00, (1 + Rb/Ra) = 2.81, V0 = 5.60V
When IR1,IR0 = 01, (1 + Rb/Ra) = 3.27, V0 = 6.54V
When IR1,IR0 = 10, (1 + Rb/Ra) = 3.50, V0 = 7.00V
When IR1,IR0 = 11, (1 + Rb/Ra) = 3.00, V0 = 6.00V

System Set (1)

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	R1	R0	CS	CG

R1, R0: selects an option ROM

When R1, R0 = 00, standard ROM (160 characters) + option ROM1 (96 characters)
When R1, R0 = 01, standard ROM (160 characters) + option ROM2 (96 characters)
When R1, R0 = 10, standard ROM (160 characters) + option ROM3 (96 characters)
When R1, R0 = 11, standard ROM (160 characters) + option ROM4 (96 characters)

CS: data shift direction of common

CS sets the shift direction of common display data
When CS = "High", COM right shift
When CS = "Low", COM left shift (default)
(refer to table 9 and figure 13)

CG: CGRAM enable bit

When CG = "High", CGRAM can be used and you can use this RAM for eight special character area. (00h - 05h=**CGRAM** font display)
When CG = "Low", CGRAM is disabled. CGROM (00h - 05h) can be used and the additional current consumption is saved by using this mode (default)
(00h - 05h=**CGROM** font display)

System Set (2)

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	1	0	*	*	SS	*

*: Don't care

SS: the normal / reverse character display of SEG is specified by setting SS.

When SS = "LOW", normal display of SEG
When SS = 'HIGH", reverse display of SEG

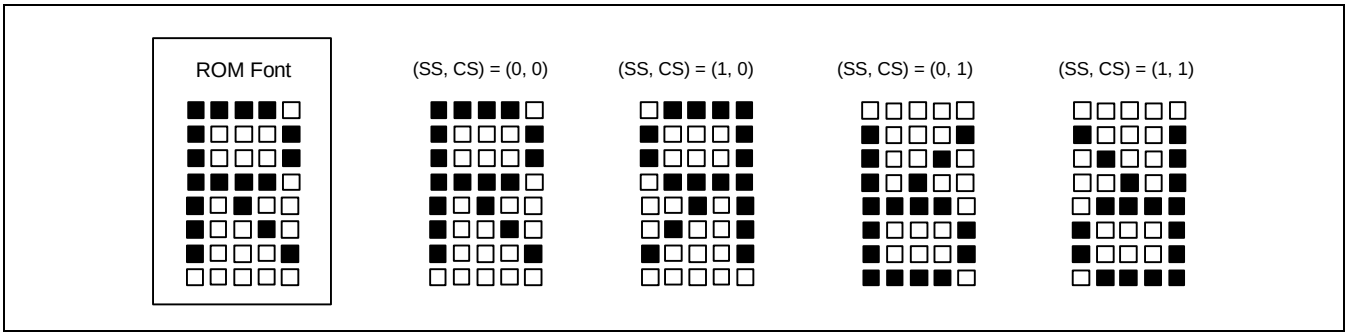


Figure 13. Example of Display according to SS and CS-bit

DDRAM Address Set

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Above RAM Address Set instruction field sets DDRAM and electronic volume register in the address counter.

Before writing / reading data into / from the DDRAM, set the address by DDRAM Address set instruction. Next, when data are written / read in succession, the address is automatically increased by 1. After accessing 7Fh, the address of AC is 00h. The read data from the unused address are unknown.

The address ranges are 00h - 7Fh.

Table 12. RAM Address Mapping (RE = 0)

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	Unused								EV	Test	Unused					
10h	Unused															
20h	Unused															
30h	DDRAM line-1															
40h	DDRAM line-2															
50h	DDRAM line-3															
60h	DDRAM line-4															
70h	DDRAM line-5															

EV: Electric volume RAM

TEST: Testing register, don' use it.

CGRAM Address Set

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Above RAM Address set instruction field sets CGRAM, segment icon RAM in the address counter.

Before writing / reading data into / from the CGRAM / ICONRAM, set the address by CGRAM Address Set instruction. Next, when data are written/read in succession, the address is automatically increased by 1. After accessing 7Fh, the address of AC is 00h. The read data from the unused address are unknown.

The address ranges are 00h - 7Fh.

Table 13. RAM Address Mapping (RE = 1)

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	CGRAM (00H)								CGRAM (01H)							
10h	CGRAM (02H)								CGRAM (03H)							
20h	CGRAM (04H)								CGRAM (05H)							
30h	Unused															
40h	Unused															
50h	Unused															
60h	ICONRAM (S1 - S80)															
70h	ICONRAM (S81 - S160)															

Write Data

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	1	D7	D6	D5	D4	D3	D2	D1	D0

This instruction field make KS0094 write binary 8-bit data to DDRAM / CGRAM / ICONRAM or register. The RAM address to be written into is determined by previous DD/CGRAM Address Set instruction. After writing operation, the address counter (AC) automatically increased by 1.

Read Data

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	1	D7	D6	D5	D4	D3	D2	D1	D0

DDRAM / CGRAM / ICONRAM data read instruction.

Each RAM is selected by address set instruction. And then you can read the RAM data. You can get correct RAM data from second read transaction. The first read data after setting RAM address is dummy data, so the correct RAM data come from the second read transaction. After reading operation, the address counter (AC) is increased by 1 automatically.

NOP

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	0	0	0	0	0	0	0	0	0

No operation command
It is recommended to add this command at each breakpoint of the program.

Test Mode

RE	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	0	0	0	0	0	*	*	*	*

*: Don't care

An IC test mode set command. Don't use it any case.

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

When RESETB pin = "Low", KS0094 can be initialized as the following state.

(1) Control Display ON / OFF Instruction
C = 0: cursor OFF
B = 0: blink OFF
RE = 0: extension register OFF
D = 0: display OFF

(2) Power Save Set Instruction
OS = 0: oscillator OFF
PS = 0: power save OFF

(3) Power Control Set Instruction
HPM = 0: high power mode OFF
VR = 0: voltage regulator OFF
VF = 0: voltage follower OFF
VC = 0: voltage converter OFF
IRS = 1: for built-in resistor
BS = 0: 1/5 bias
IR1, 0 = 00: Rb / Ra = 2.81

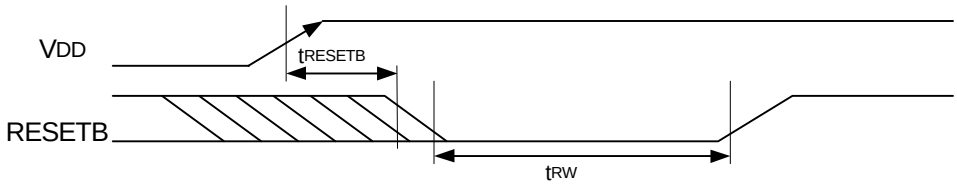
(4) System Set Instruction
R1, R0 = 00: main ROM + option ROM
CS = 0: COM left shift
SS = 0 : normal display character
CG = 0: CGRAM is not used

(5) Return Home
Address counter = 30h

(6) Electronic Contrast Control Register: address 10h = data (0, 0, 0, 0, 0)

(7) In Case of 4-bit Interface Mode Selection
KS0094 considers the first 4-bit data from MPU as the high order bits.

NOTE: If initialization is not done by the RESETB pin at application, unknown condition might result. Then you can initialize by instruction.

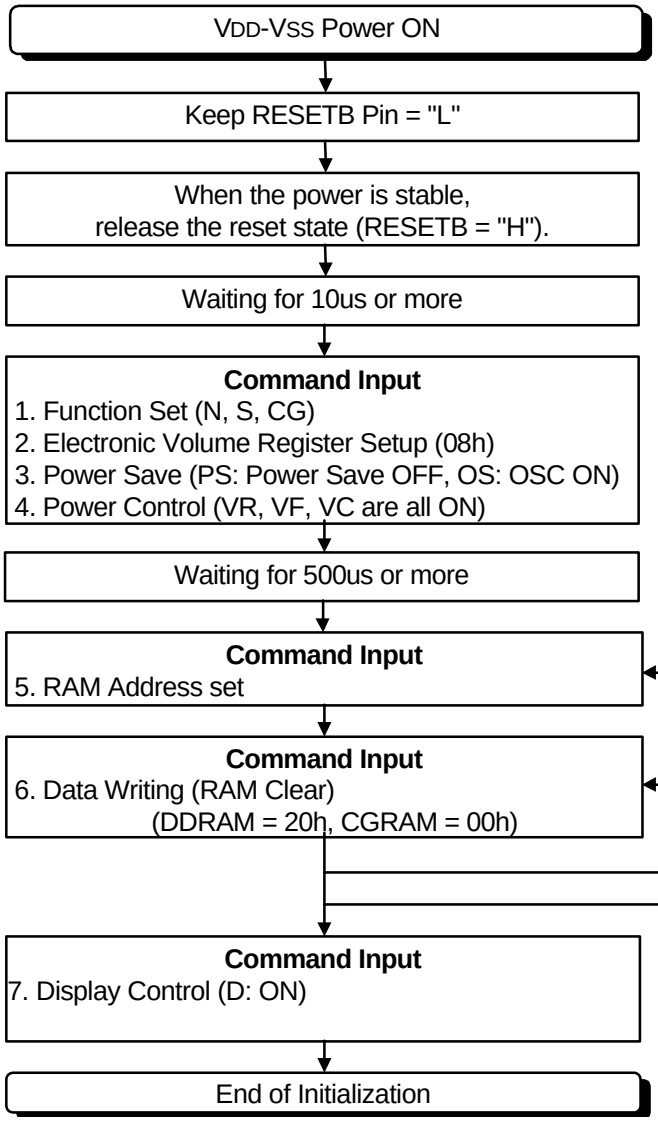


RESETB pulse width	t_{RW}	10μs
RESETB start time	t_{RESETB}	50ns

Figure 14. RESET Timing

INITIALIZING AND POWER SAVE SETUP

Initializing by Instruction



NOTE:

At command 5 and 6, the internal RAM should be cleared.

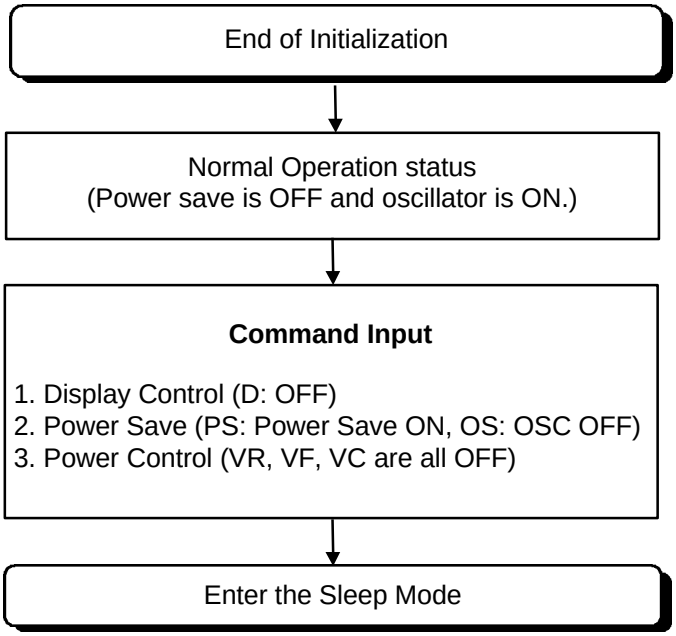
To clear DDRAM,
RE bit should be set 0,
set address at 30h (first DDRAM)
and then write 20h (space character code) 80 times

To clear CGRAM (RE=1),
RE bit should be set 1,
Set address at 00h (first CGRAM)
and then write 00h (null data) 48 times

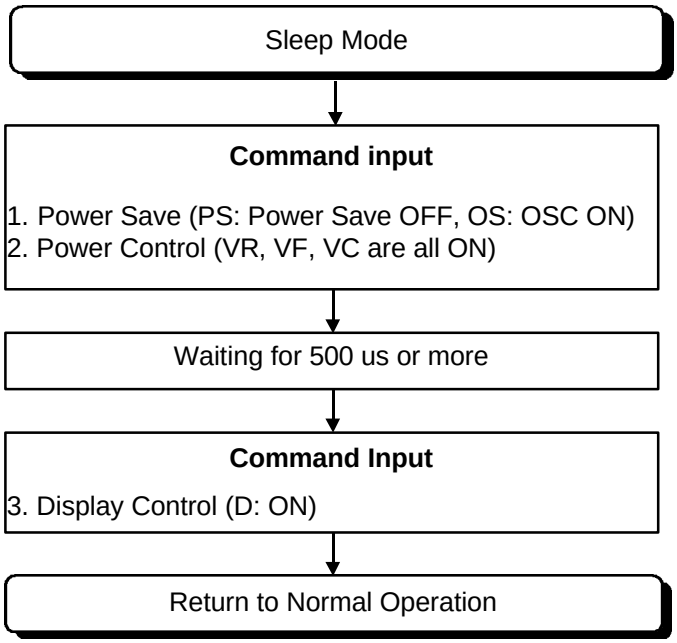
To clear ICONRAM (RE=1),
RE bit should be set 1,
set ICONRAM address at 60h (first ICONRAM) and then write 00h (null data) 32 times

Sleep Mode Set or Release by Instruction

a) Sleep Mode Set

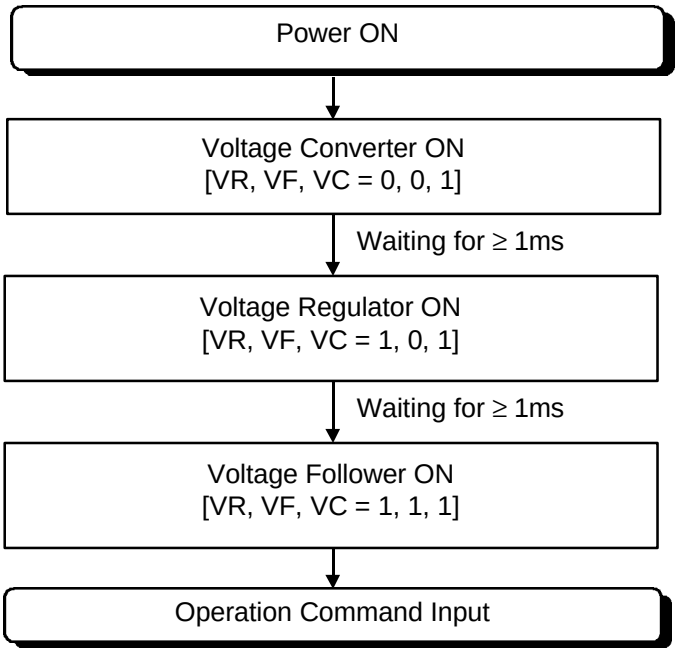


b) Sleep Mode Release

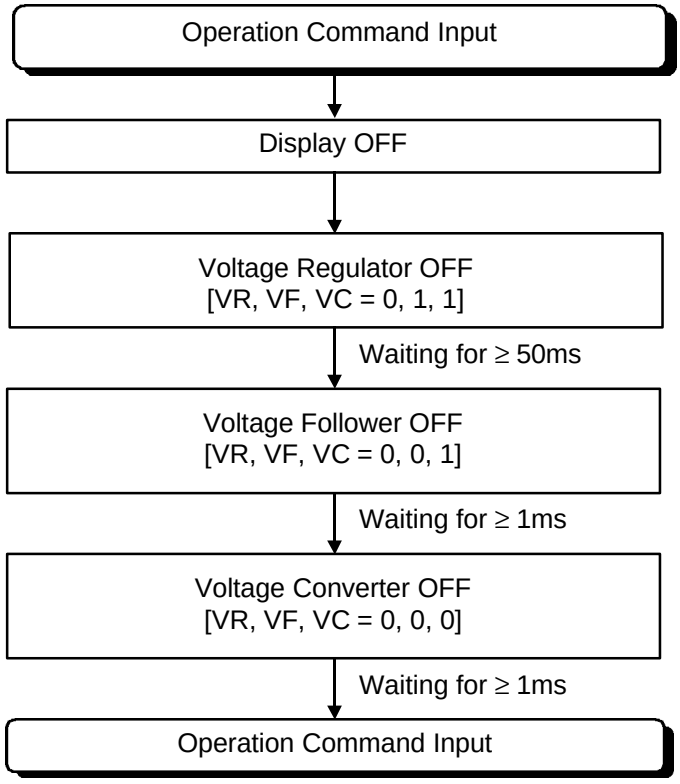


Recommendation of Power ON / OFF Sequence

a) Power ON Sequence



b) Power OFF Sequence



LCD DRIVING POWER SUPPLY CIRCUIT

The Power Supply circuit produces LCD panel driving voltage at low power consumption. The LCD driving Power Supply circuit consists of voltage converter, voltage regulator, and voltage follower. It is controlled by power control instruction. Table 14 shows how the LCD Driving Power Supply circuit works by power control instruction sets.

Table 14. Power Supply Control Mode Set

VR VF VC	Voltage regulator	Voltage follower	Voltage converter	VOUT pin	VR pin	V0, V1, V2, V3, V4 pin
1 1 1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
1 1 0	Enable	Enable	Disable	External voltage input	Used for voltage adjustment	Internal voltage output
0 1 0	Disable	Enable	Disable	Open	Open	V1~V4: Internal voltage output V0: External voltage input
0 0 0	Disable	Disable	Disable	Open	Open	V0~V4: External voltage input

NOTE: SEC recommendation is to use only the case listed above table.

VOLTAGE CONVERTER

The Voltage Converter circuit generates positive 4 times voltage of 2.0V that is generated internally. VOUT is generated from the Voltage Converter. And this conversion voltage is used in the built-in voltage regulator circuit. This application circuit is same as 3 times DC/DC converter.

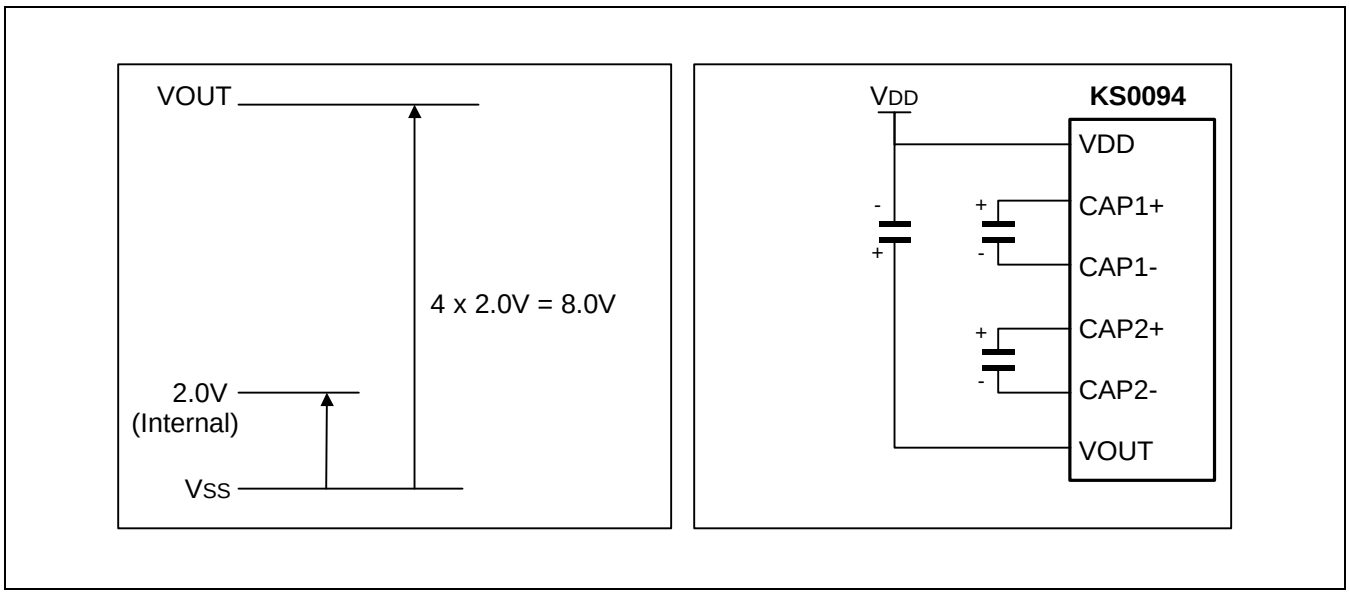


Figure 15. DC/DC Converter Output and Circuit

VOLTAGE REGULATOR

The Voltage Regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained by adjusting resistors Ra and Rb as shown in equation (1), and by setting electronic contrast control data bits, see equation (2).

The potential of V0 Pin can be adjusted within VOUT - V_{REF}. V_{REF} is the internal constant voltage source of the chip and this value is 2.0V in the condition $V_{DD} \geq 2.2V$

- Voltage regulation by adjusting resistors Ra, Rb

When REF is "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \quad \text{--- (1)}$$

The internal V_{REF} of voltage regulator has the temperature compensation function, and the temperature coefficient is approximately 0%

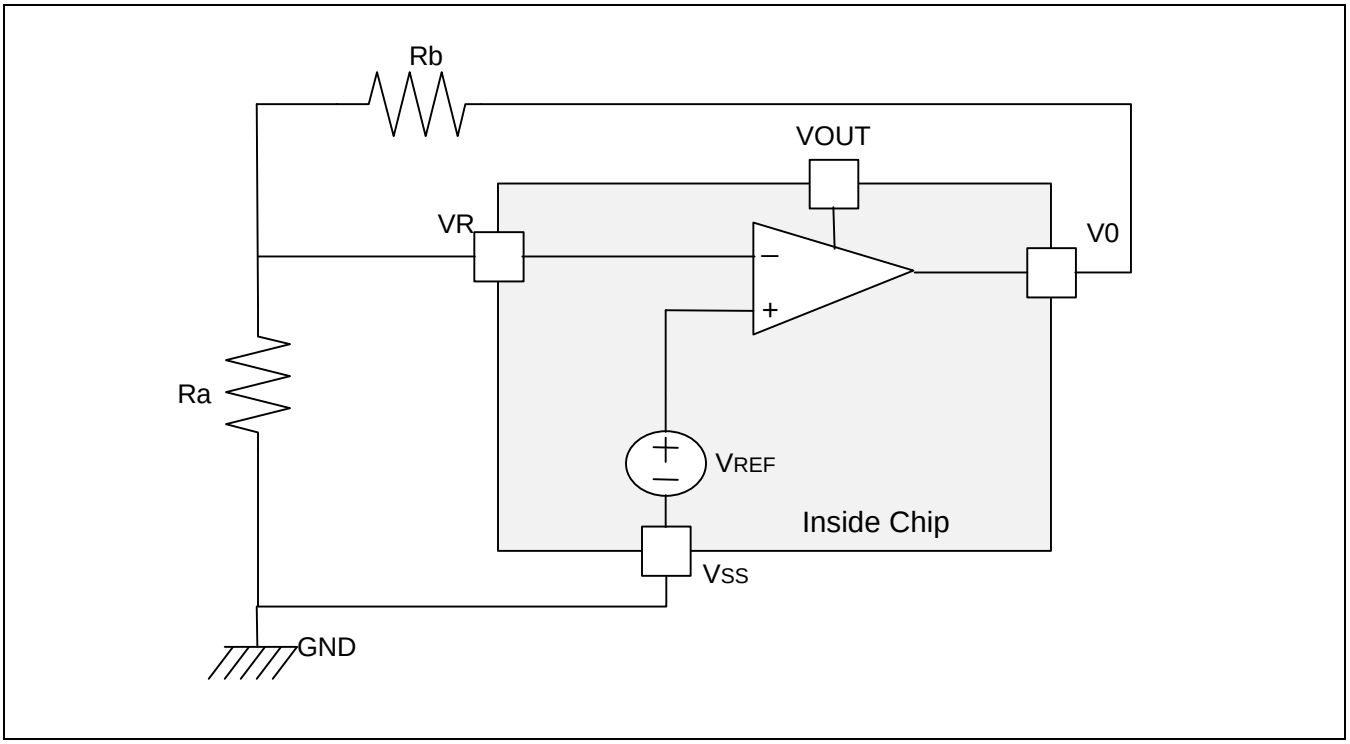


Figure 16. Voltage Regulator Circuit

ELECTRONIC CONTRAST CONTROL (32 STEPS)

Electronic Contrast Control data bits is 10h = (d4, d3, d2, d1, d0). Voltage regulation is adjusted as 32-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the Electronic Contrast Control register (RE = 0 address 08h). When using the Electronic Contrast Control function, you need to turn the voltage regulators on using power control instruction.

When REF = "Low"

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad \text{--- (2)}$$

$$V_{EV} = V_{REF} - n\alpha \quad (n = 0, 1, 2, \ldots 30, 31)$$

$$\alpha = V_{REF} / 150$$

Table 15. Electronic Contrast Control Register

No.	d7	d6	d5	d4	d3	d2	d1	d0	nα	V0	Contrast
1	-	-	-	0	0	0	0	0	0α (default)	Maximum	High
2	-	-	-	0	0	0	0	1	1α	.	.
3	-	-	-	0	0	0	1	0	2α	.	.
4	-	-	-	0	0	0	1	1	3α	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
31	-	-	-	1	1	1	1	0	30 α	.	.
32	-	-	-	1	1	1	1	1	31α	Minimum	Low

NOTE:
1. "-": Don't care

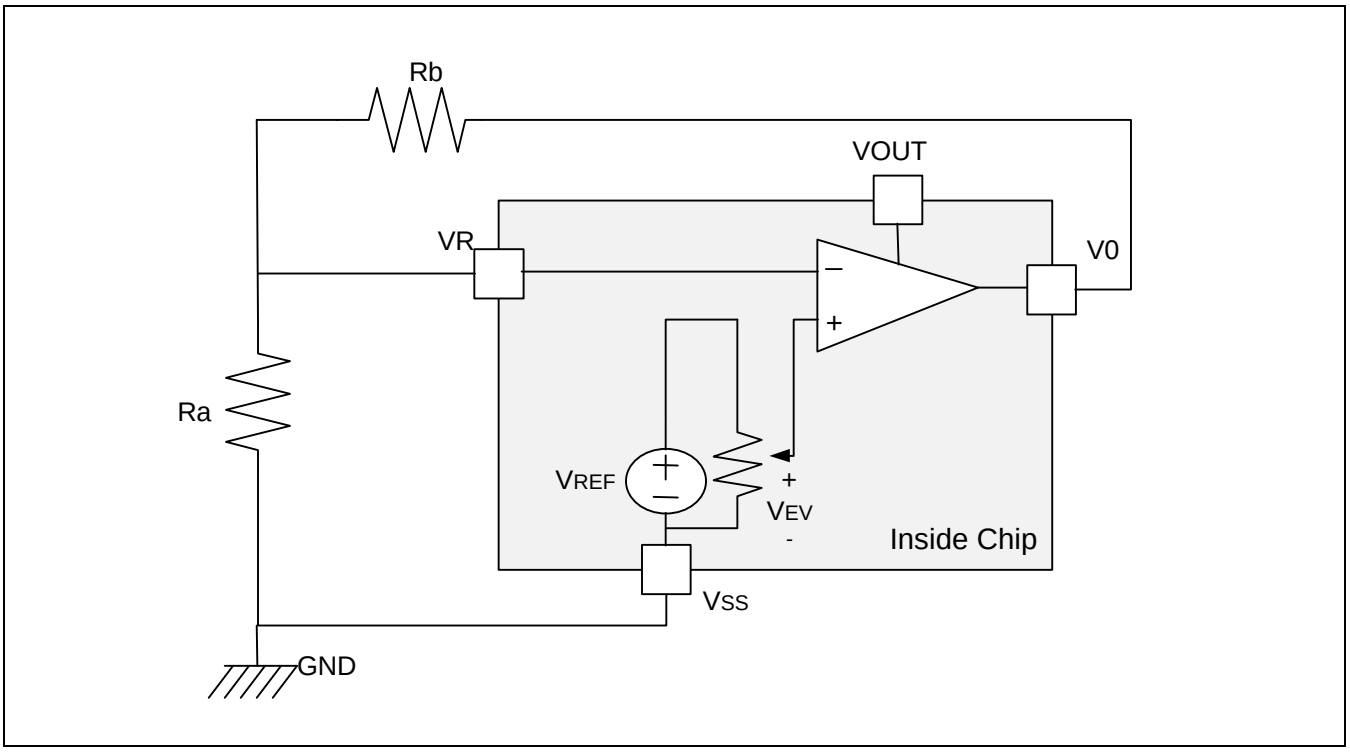


Figure 17. Electronic Contrast Control Circuit

The voltage rage of the V5 output can be adjusted by changing the built-in resister ratio (1 + Rb / Ra) by command. Reference values are shown in table 16.

Table 16. V0 Voltage Regulating Built-in Resister Ratio Set Values (Reference Values)

Command		(1+Rb / Ra)	V0
IR1	IR0		
0	0	2.81	5.60V
0	1	3.27	6.54V
1	0	3.50	7.00V
1	1	3.00	6.00V

VOLTAGE GENERATOR CIRCUIT

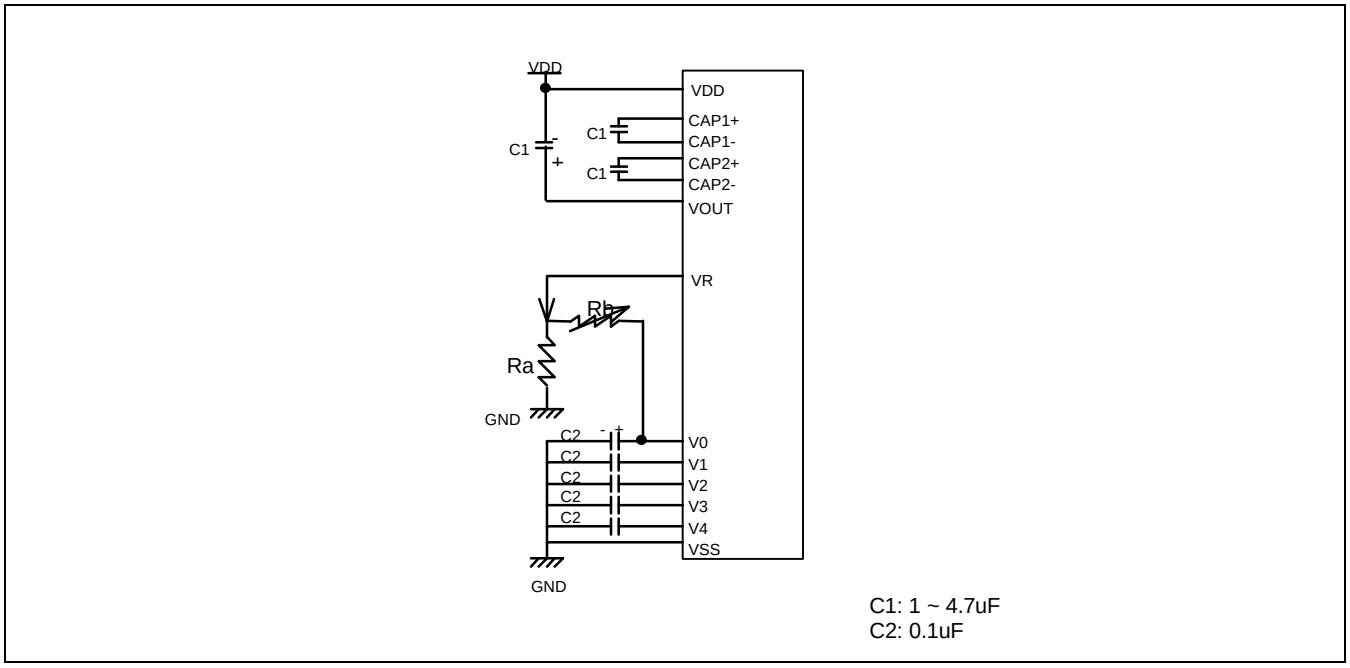


Figure 18. When Built-in Power Supply is used (VR, VF, VC = 1, 1, 1)

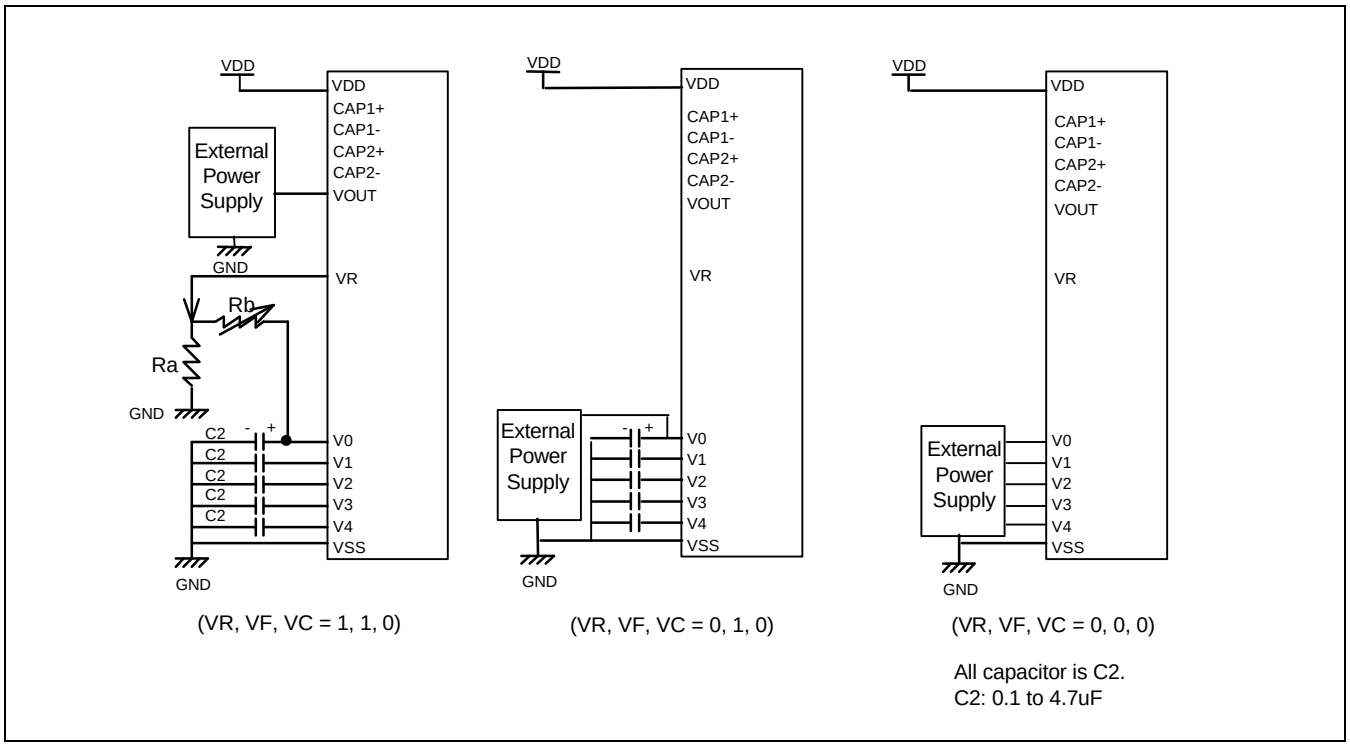


Figure 19. When External Power Supply is used

MPU INTERFACE

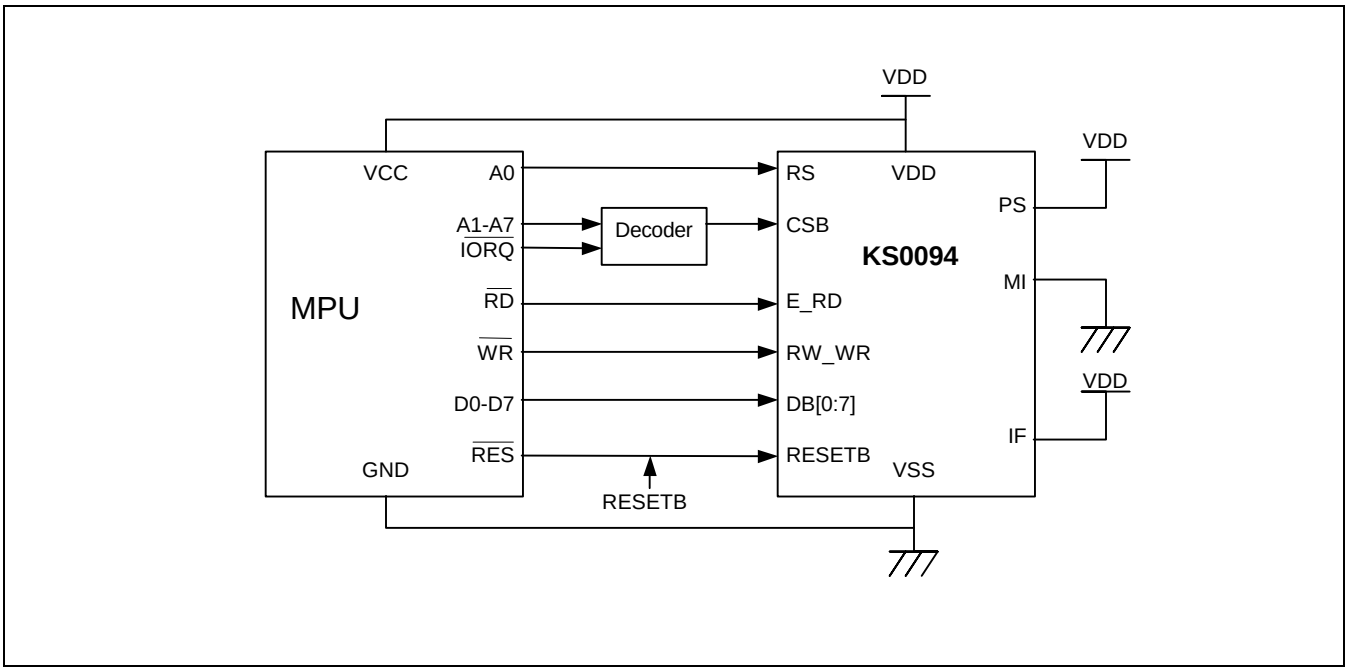


Figure 20. Parallel Interfacing with 8080-series Microprocessors

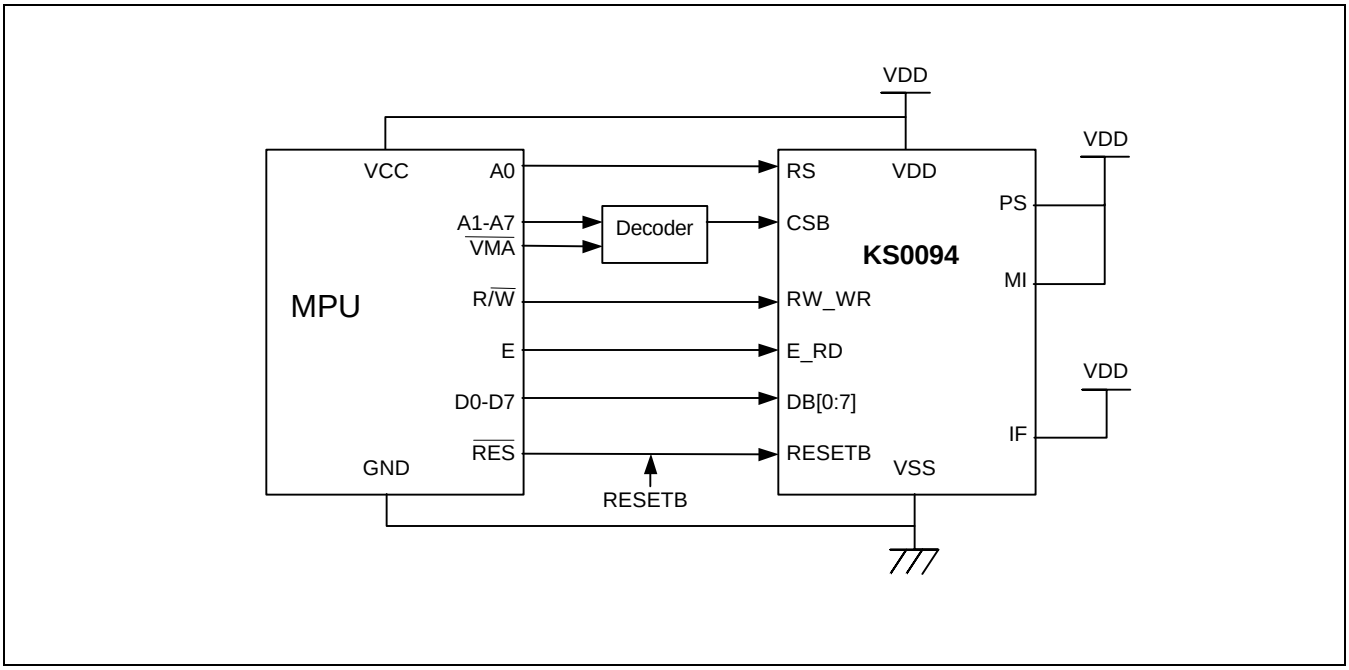


Figure 21. Parallel Interfacing with 6800-series Microprocessors

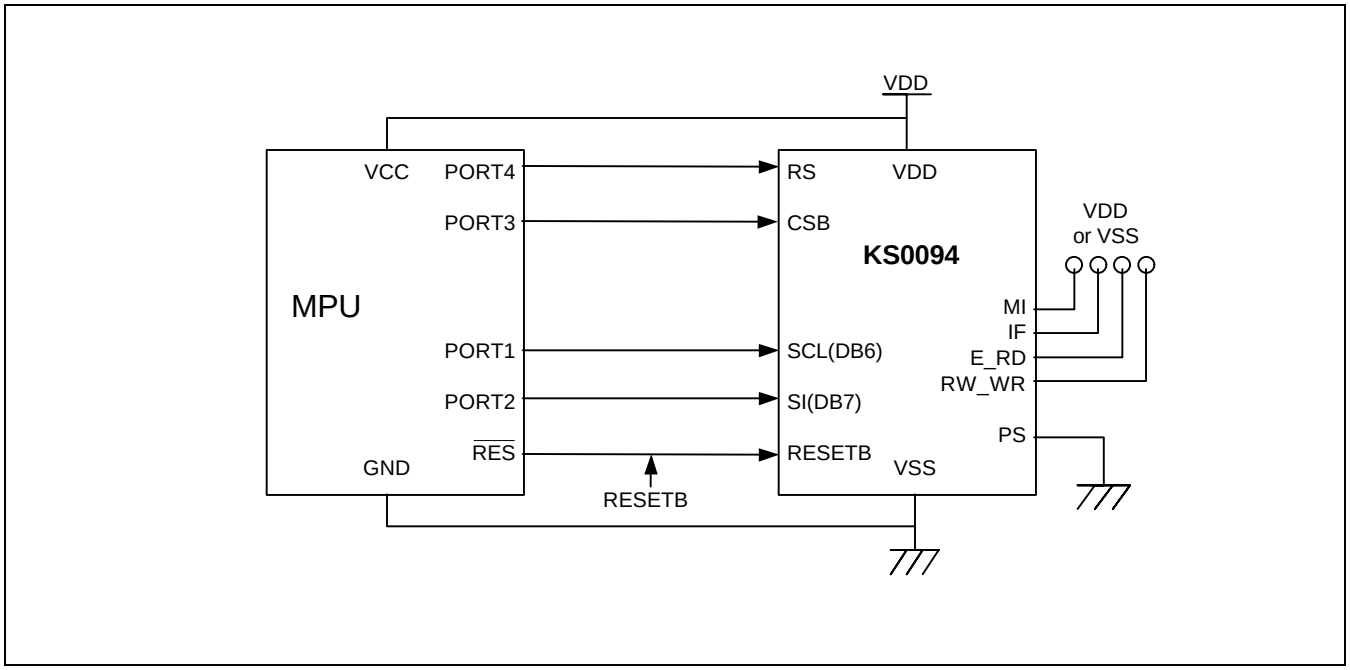


Figure 22. Clock Synchronized Serial Interfacing with any Microprocessors

APPLICATION INFORMATION FOR LCD PANEL

Chip Bottom & Lower View (CS bit = "0", DIRS = "0")

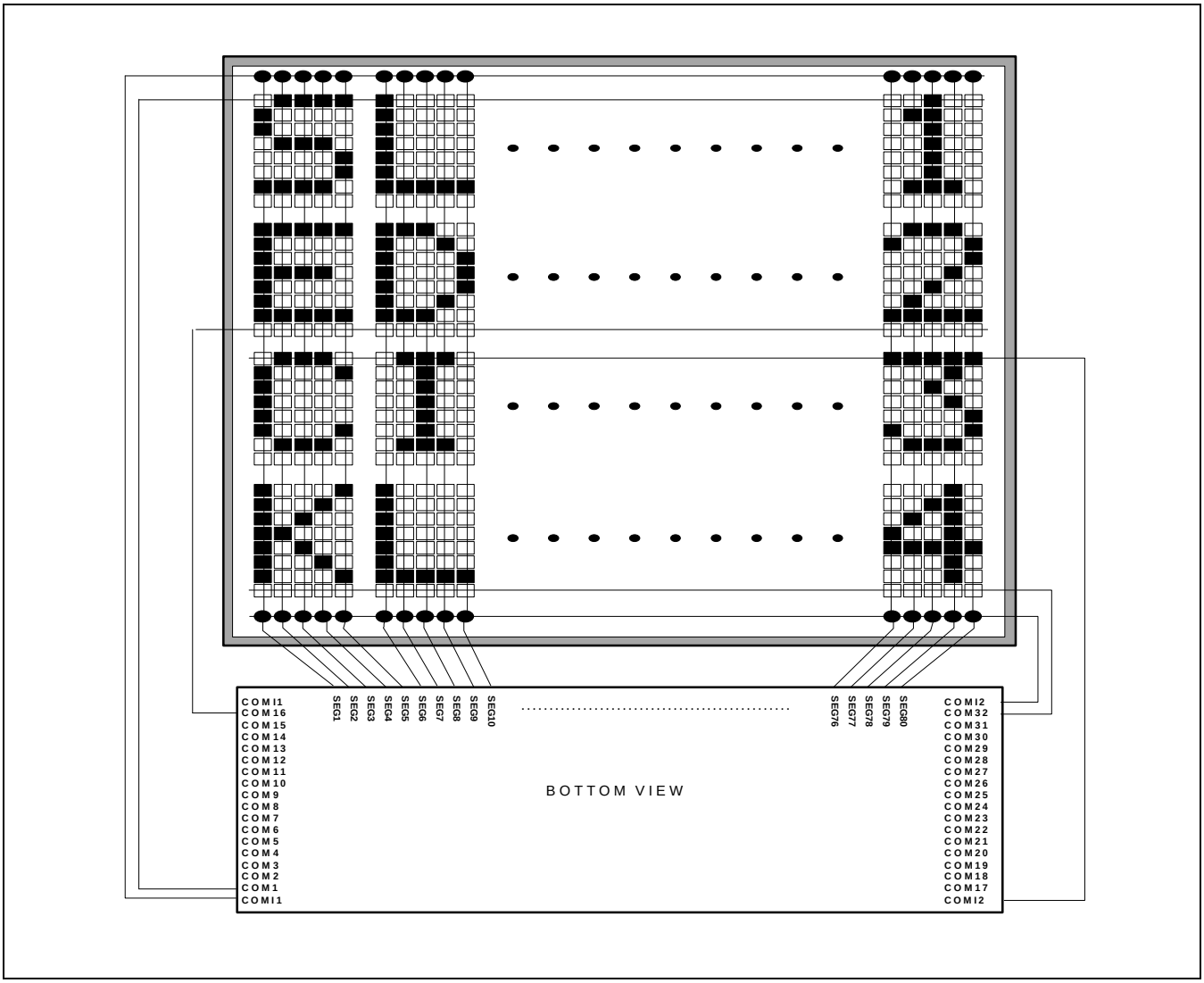


Figure 23. Chip Bottom & Lower View (CS bit = "0", DIRS = "0")

Chip Bottom & Upper View (CS bit = "1", DIRS = "1")

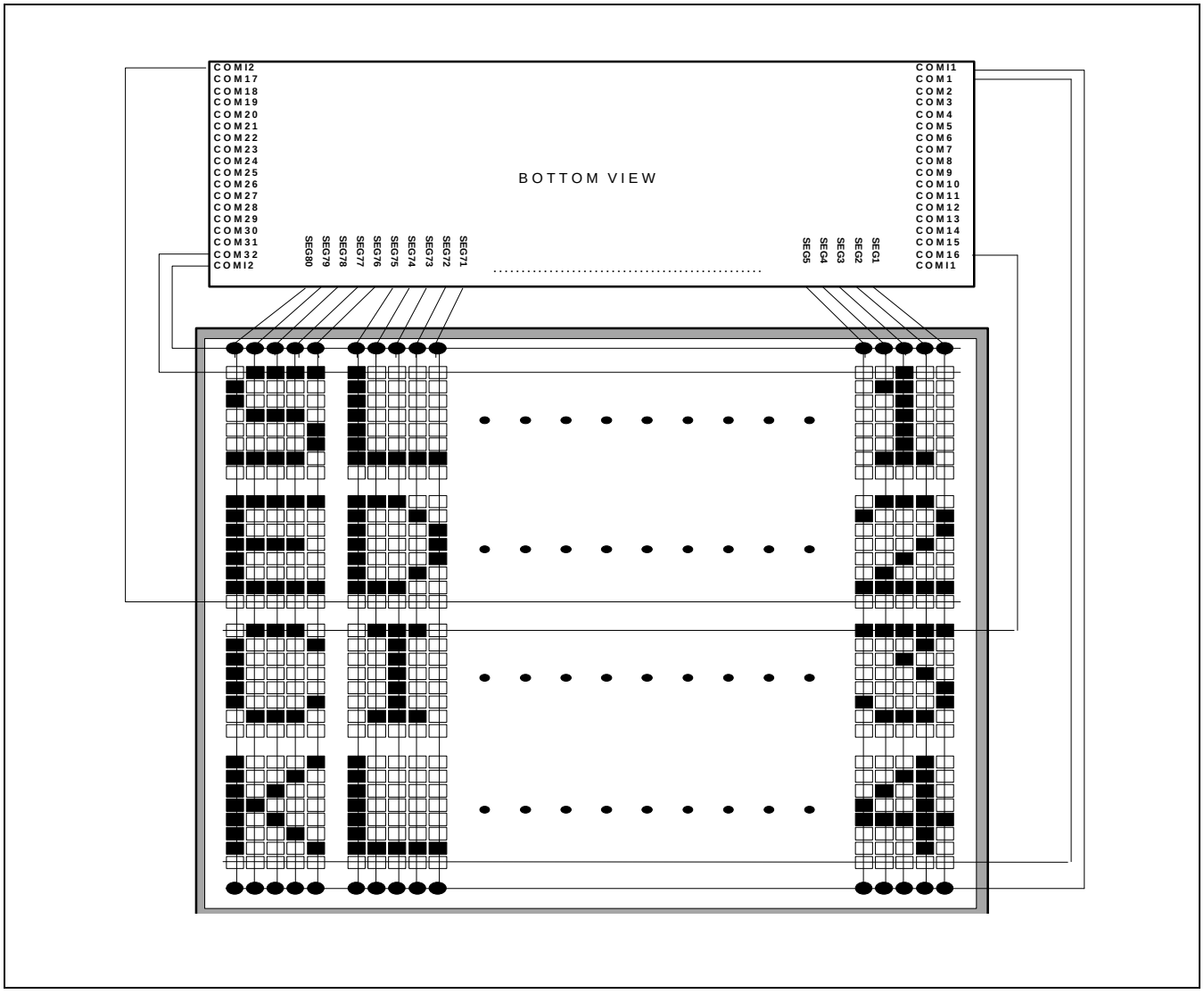


Figure 24. Chip Bottom & Upper View (CS bit = "1", DIRS = "1")

Chip Top & Lower View (CS bit = "0", DIRS = "1")

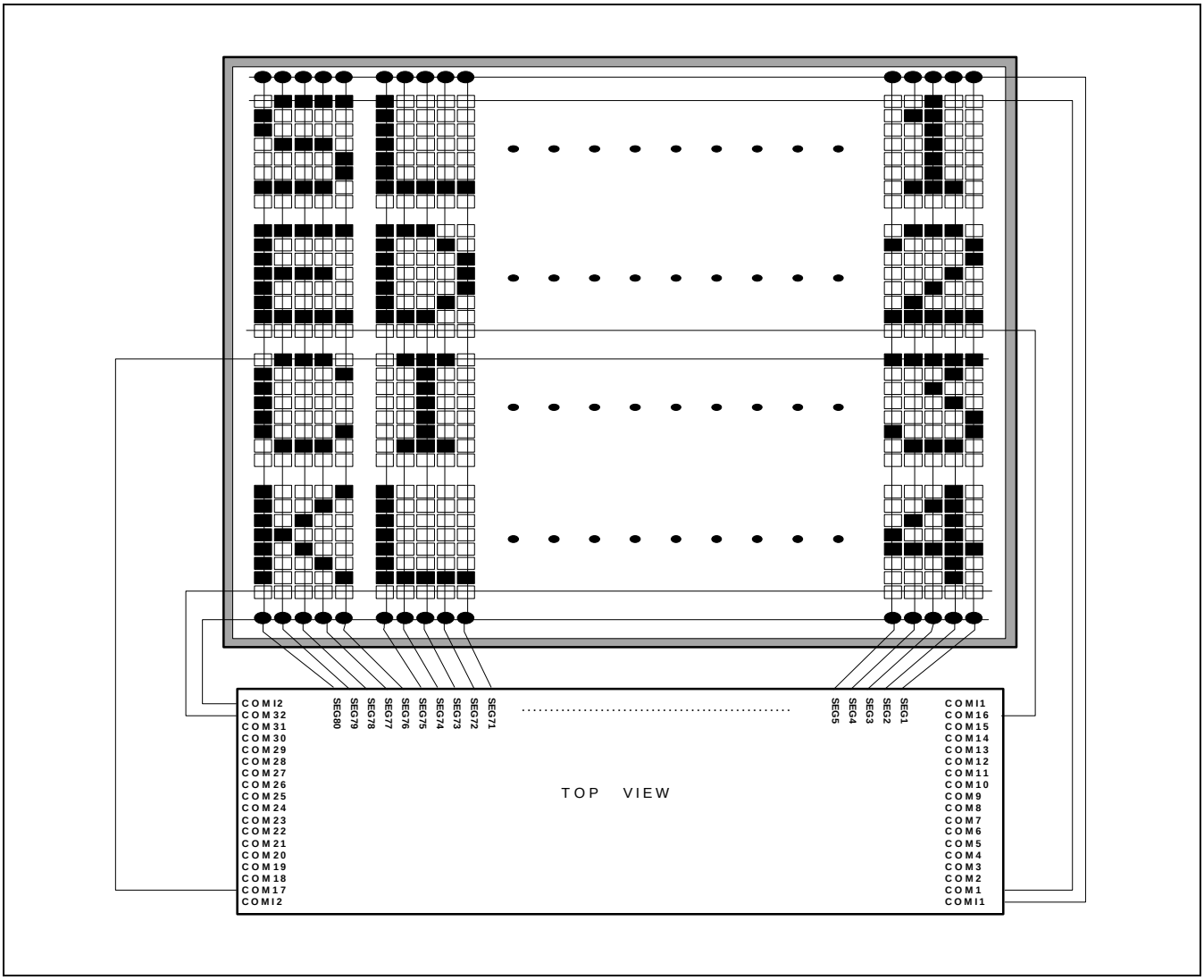


Figure 25. Chip Top & Lower View (CS bit = "0", DIRS = "1")

Chip Top & Upper View (CS bit = "1", DIRS = "0")

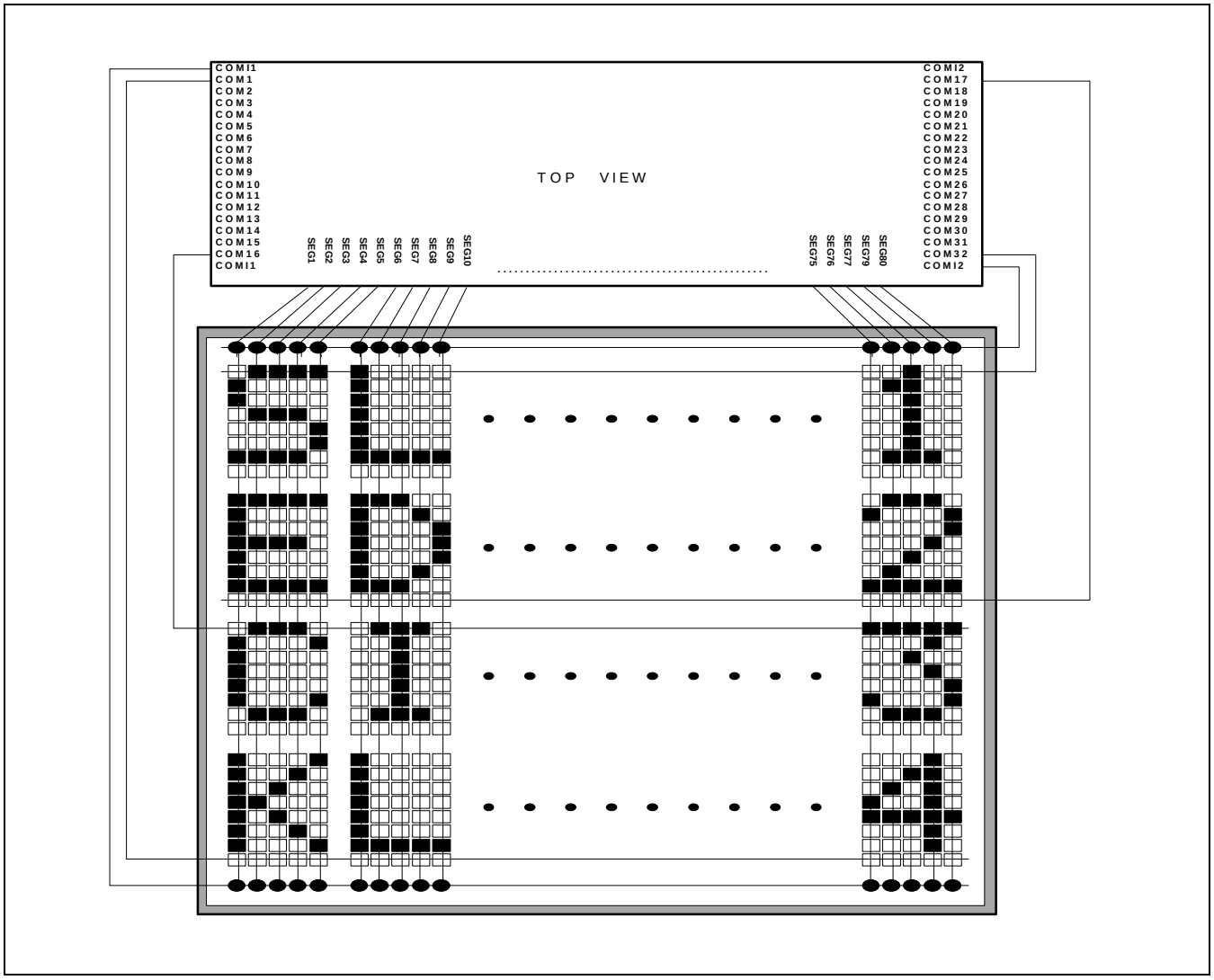
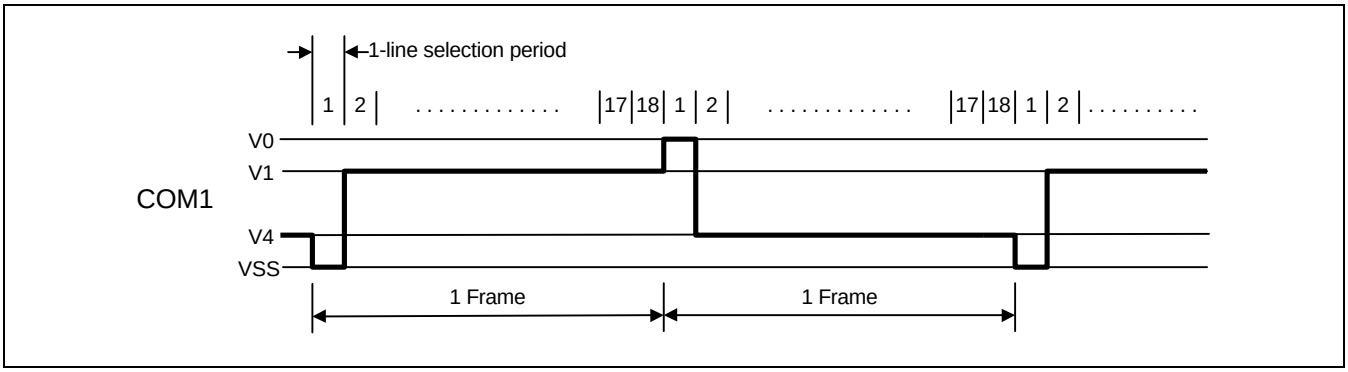


Figure 26. Chip Top & Upper View (CS bit = "0", DIRS = "1")

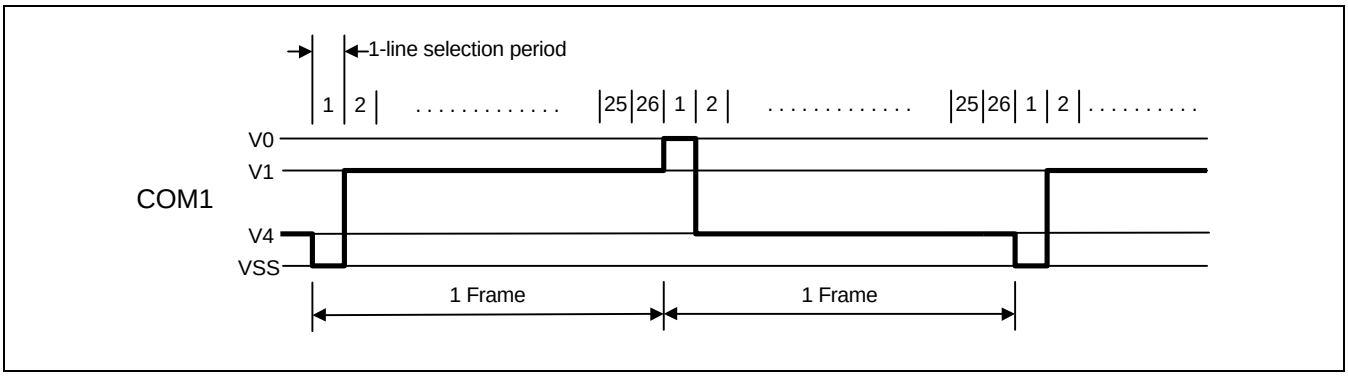
FRAME FREQUENCY

1/18 Duty (2-line Mode)



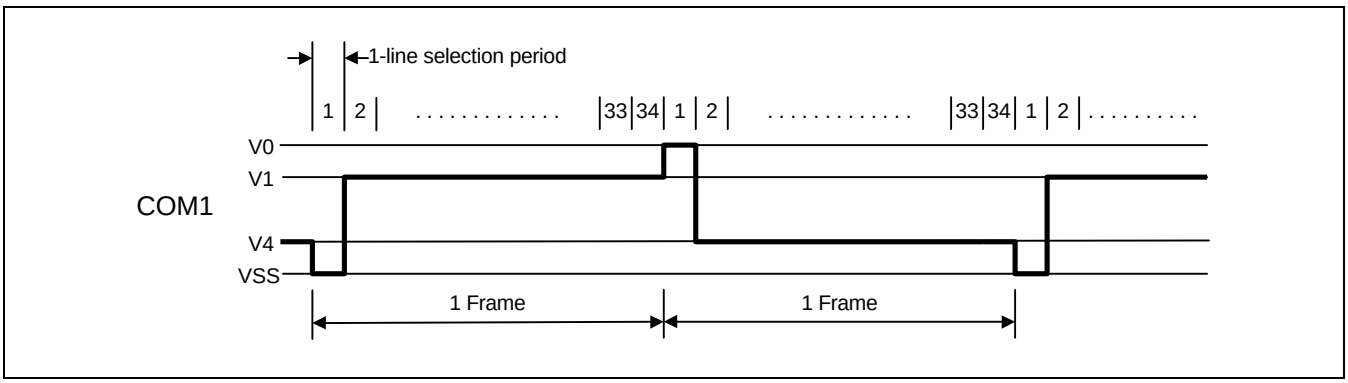
1-line Selection Period = 16 Clocks
One Frame = 16 x 18 x 44.44 us = 12.8 ms (1 Clock = 44.44 us at fOSC = 45 kHz)
Frame Frequency = 1 / 12.8 ms = 78.1 Hz

1/26 Duty (3-line Mode)



1-line Selection Period = 16 Clocks
One Frame = 16 x 26 x 29.63 us = 12.33 ms (1 Clock = 29.63 us at fOSC = 45 kHz)
Frame Frequency = 1 / 12.33 ms = 81.1 Hz

1/34 Duty (4-line Mode)



1-line Selection Period = 16 Clocks
One Frame = 16 x 34 x 22.2 us = 11.97 ms (1 Clock = 22.2 us at fOSC = 45 kHz)
Frame Frequency = 1 / 11.97 ms = 83 Hz

MAXIMUM ABSOLUTE RATINGS

Table 17. Maximum Absolute Ratings

Characteristic	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to + 7.0	V
Power supply voltage (2)	VOUT, V0	-0.3 to + 9.0	V
Power supply voltage (3)	V1, V2, V3, V4	-0.3 to V0	V
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating temperature	T_{OPR}	-30 to +85	^{o}C
Storage temperature	T_{STG}	-55 to +125	^{o}C

NOTE1: All the voltage levels are based on V_{SS} = 0V.

NOTE2: Voltage greater than above may damage the circuit
Voltage level : VOUT ≥ V0 ≥ V_{DD} ≥ V_{SS}
Voltage level : V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS}

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 18. DC Characteristics

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}	-	2.2	-	3.6	V
Supply current (V_{DD} = 3V, Ta = 25 °C)		I_{DD1}	Display operation V_{LCD}=6V without load No access from MPU	-	-	95	uA
		I_{DD2}	Access operation from MPU (Fcyc = 200kHZ)	-	-	500	
		I_{DDS1}	Sleep operation without load oscillator OFF, power save ON	-	-	5	
Input voltage		V_{IH}	-	0.8V_{DD}		V_{DD}	V
		V_{IL}	-	Vss		0.2V_{DD}	
Output voltage		V_{OH}	I_{OH} = -1mA, V_{DD} =2.4V	V_{DD}-0.4			V
		V_{OL}	I_{OL} = 1mA, V_{DD} =2.4V			0.4	
Input leakage current		I_{IZ}	V_{IN} = 0V to V_{DD}	-1	-	1	uA
Output leakage current		I_{OZ}	V_{IN} = 0V to V_{DD}	-3		3	uA
R_{ON} resistance		R_{COM}	Io = ±50uA	-	-	5	kΩ
		R_{SEG}	Io = ±50uA	-	-	10	
Frame frequency (Internal OSC)		f_{FR}	V_{DD} = 3V, Ta = 25 °C (4-line mode)	70	85	100	Hz
Voltage converter	Conversion efficiency	V_{EF}	RL = ∞	95	99	-	%
	Output voltage	V_{OUT}	Ta = 25 °C, C = 1uF	7.5	8.0	8.5	V
Voltage regulator reference voltage		V_{REF}	Ta = 25 °C	1.94	2.0	2.06	V
LCD driving voltage		V_{LCD}	V_{LCD} = V0 - Vss	3.0	-	7.0	

AC CHARACTERISTICS

Parallel Write Interface (68 Mode)

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	450	-	-	
E_RD pulse width low	t_{WL}	150	-	-	
RS and CSB setup time	t_{SU1}	60	-	-	
RS and CSB hold time	t_{H1}	30	-	-	
DB setup time	t_{SU2}	100	-	-	
DB hold time	t_{H2}	50	-	-	

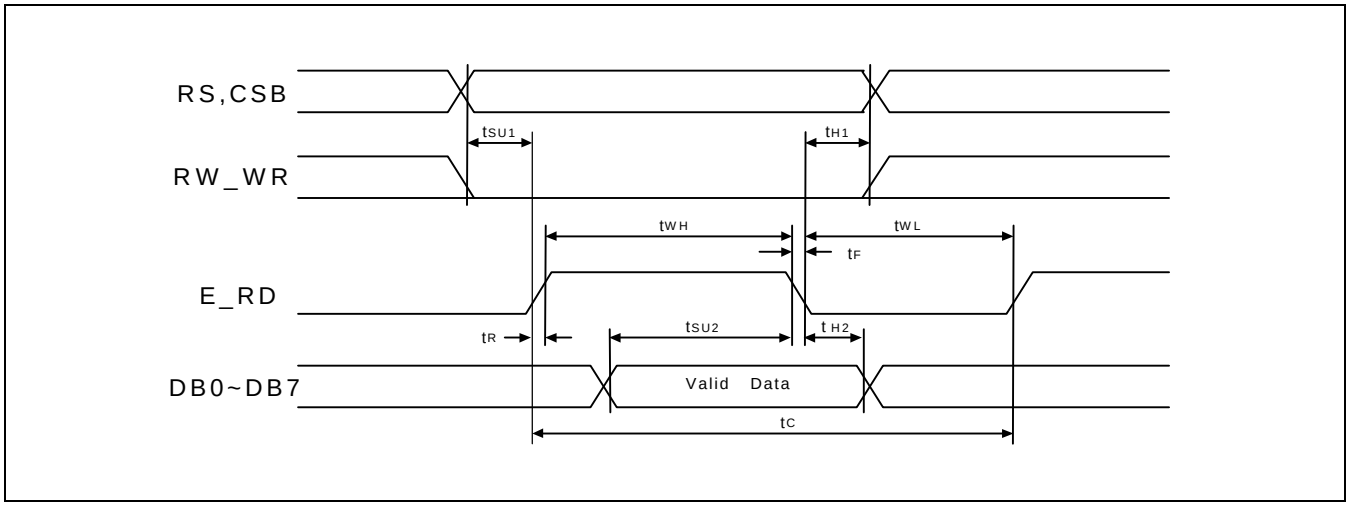


Figure 27. Write Timing Diagram (68-series)

Parallel Read Interface (68 Mode)

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	450	-	-	
E_RD pulse width low	t_{WL}	150	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

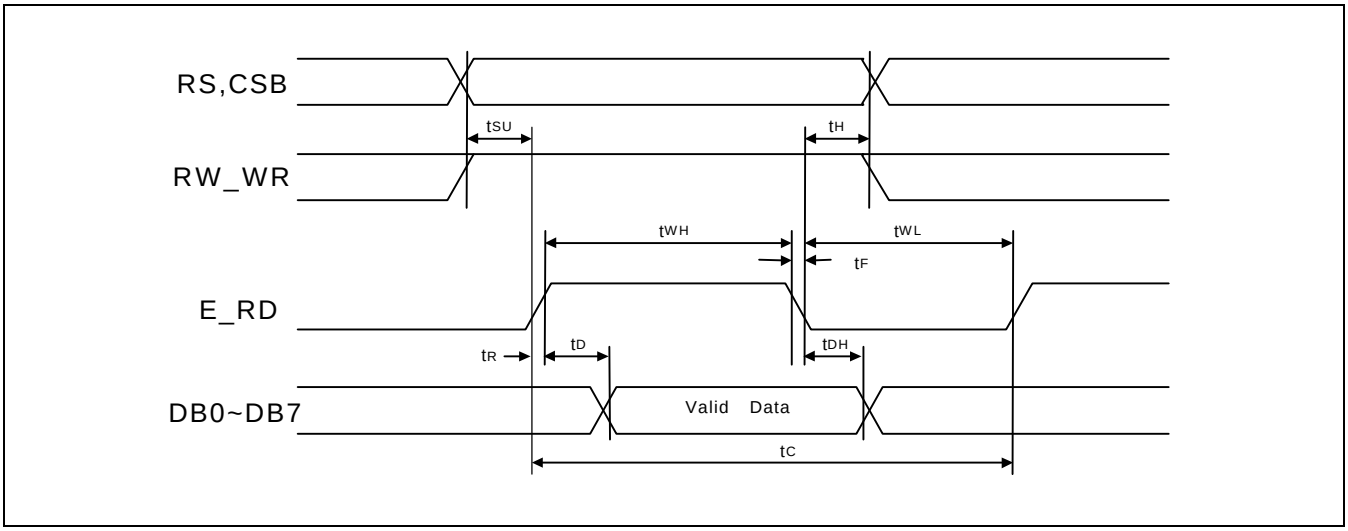


Figure 28. Read Timing Diagram (68-series)

Parallel Write Interface (80 Mode)

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
RW_WR cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
RW_WR pulse width high	t_{WH}	150	-	-	
RW_WR pulse width low	t_{WL}	450	-	-	
RS and CSB setup time	t_{SU1}	60	-	-	
RS and CSB hold time	t_{H1}	30	-	-	
DB setup time	t_{SU2}	100	-	-	
DB hold time	t_{H2}	50	-	-	

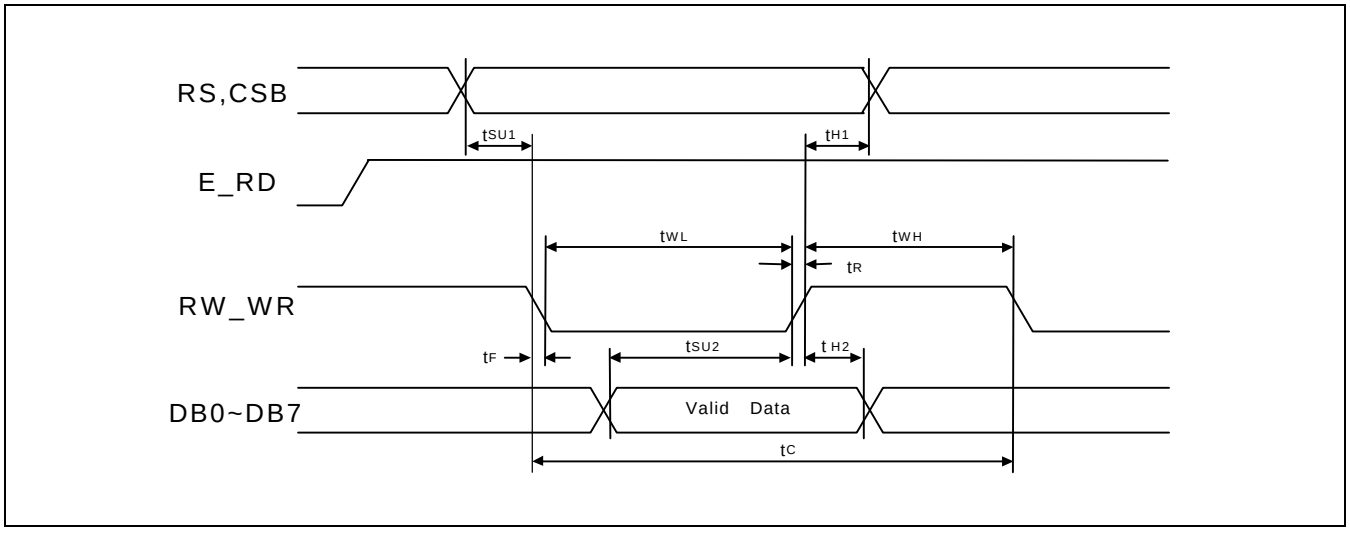


Figure 29. Write Timing Diagram (80-series)

Parallel Read Interface (80 Mode)

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
E_RD cycle time	t_C	650	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
E_RD pulse width high	t_{WH}	150	-	-	
E_RD pulse width low	t_{WL}	450	-	-	
RS and CSB setup time	t_{SU}	60	-	-	
RS and CSB hold time	t_H	30	-	-	
DB output delay time	t_D	100	-	-	
DB output hold time	t_{DH}	50	-	-	

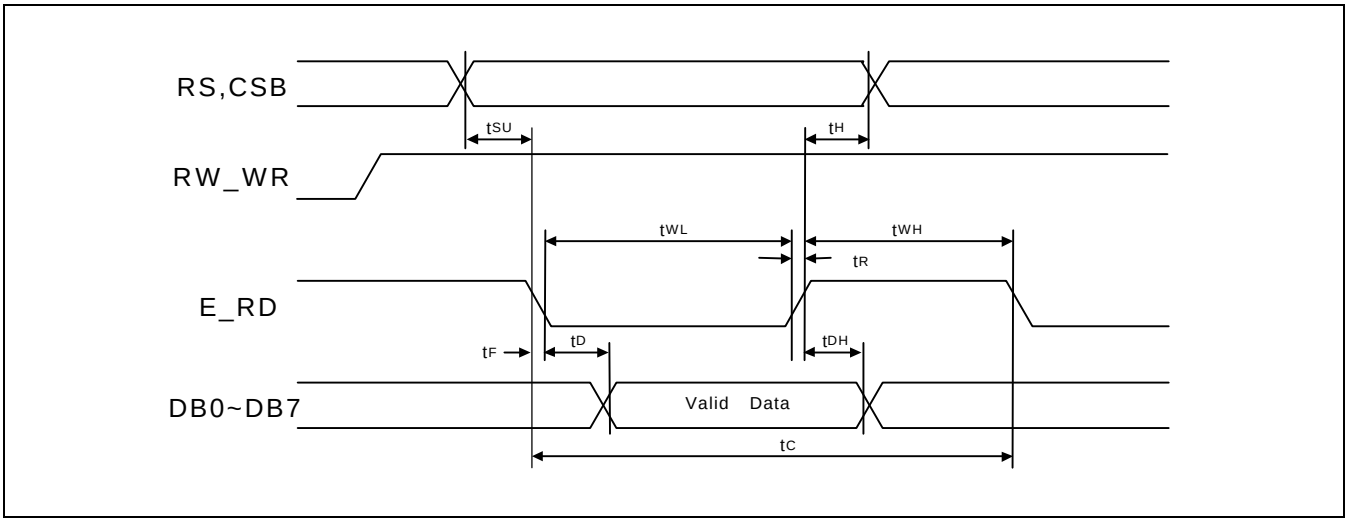


Figure 30. Read Timing Diagram (80-series)

Clock Synchronized Serial Mode

(V_{DD} = 2.2V to 3.6V, Ta = -30 to +85 °C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time	t_C	1000	-	-	ns
Pulse rise / fall time	t_R,t_F	-	-	25	
SCL clock width (high, low)	t_W	300	-	-	
CSB setup time	t_{SU1}	150	-	-	
CSB hold time	t_{H1}	700	-	-	
RS data setup time	t_{SU2}	50	-	-	
RS data hold time	t_{H2}	300	-	-	
SI data setup time	t_{SU3}	50	-	-	
SI data hold time	t_{H3}	50			

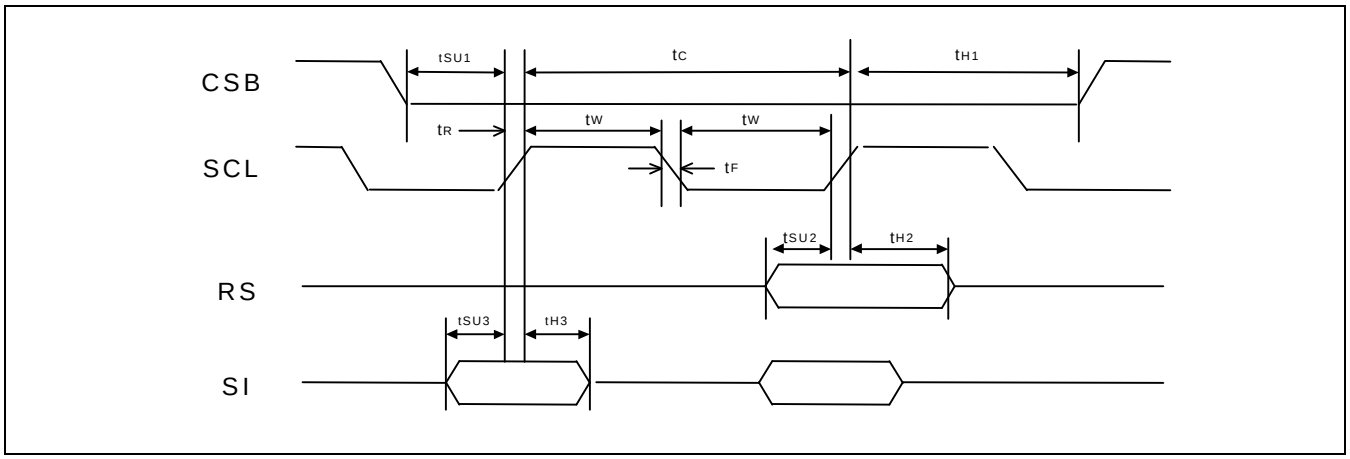


Figure 31. Clock Synchronized Serial Interface Mode Timing Diagram