Application Notes

An Examination of Recovery Time of an Integrated Limiter/LNA

■ Jim Looney, David Conway, and Inder Bahl

GaAs monolithic microwave integrated circuits (MMICs) are widely used in commercial and military microwave systems. Due to the fine geometry used in MMIC transistors, these circuits are susceptible to damage from high-power spurious electromagnetic (EM) radiation, either from microwave transmitters or nuclear electromagnetic pulse. Especially, low noise amplifiers (LNAs) in the front-end of microwave systems need high power protection because these amplifiers can sustain only low input power levels in the range of 10–20 dBm continuous wave (CW). To protect these circuits and maintain low noise figure, a high power and low loss limiter is required.

The purpose of this application note is to document the test methodology employed and test results achieved measuring the small-signal gain recovery time of a balanced LNA with an integrated Schottky diode limiter and high power load.

Device Under Test

The circuit selected for this investigation was the commercially available M/A-COM limiter/LNA MMIC [1]. This limiter/LNA has an operating bandwidth of 8.5 to 12 GHz, a nominal gain of 16 dB, a noise figure (NF) < 3 dB, and an input third-order intercept (TOI) of 13 dBm. Operating bias voltages and currents are 5 V, 130 mA nominal, –5 V, 4 mA nominal for the drain and gate, respectively. The active device employed in this IC is the low noise multifunction self-aligned (MSAG) metal-semiconductor field-effect transistor (MESFET). Salient features of this circuit are:

- single chip, no extra components and assembly, low cost solution
- balanced configuration, built-in couplers
- high-power termination resistor on the chip
- limiter parasitic capacitance part of the LNA's input match, improved noise figure with respect to discrete solutions
- high-output, third-order intercept point
- uses standard, reliable and high performance MSAG MESFET technology.

A block diagram of the high power limiter/LNA MMIC is shown in Figure 1. Figure 2 shows the photograph of the two-stage balanced limiter/LNA. The chip measures 4.6 ×3.1 mm. The design of integrated high power limiter/LNA has been described in [2].

Test Methodology

The limiter recovery time was measured by pulsing the input RF signal from a small signal level to a high power state

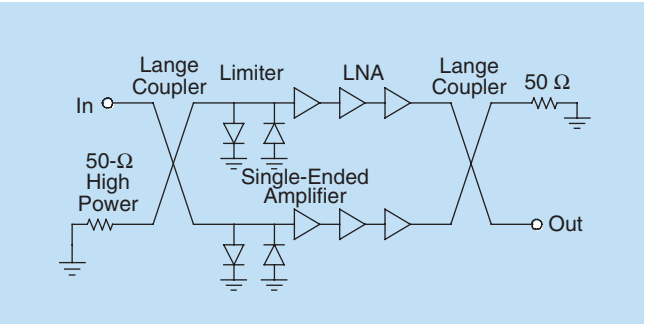

Figure 1. *A balanced three-stage LNA with limiter.*

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(limiter active), then using a detector to measure the response time as the RF level drops back to normal operating levels. Due to equipment limitations, a method to pulse the RF from a small but detectable signal level to a large-signal level was not readily available.

Consequently, a system to measure recovery time using two RF tones was developed. By injecting a CW small signal level at the low end of the device under test's (DUT's) band of operation (F1) and a pulsed high power signal at the upper end (F2), it was possible to measure the small signal recovery time by separating the two signals at the output of the device using typical components found in most test labs. The frequencies of the two signals were chosen to allow the use of existing low pass filters to remove the F2 signal so only the response of the F1 signal would be measured. For this test, a dual directional coupler was used to combine the signals. The F1 signal was injected through the reflected power port of the coupler and the pulsed F2 signal at the thru path. This uses the reverse isolation of the coupler to separate the small signal F1 tone from the pulsed high power F2 tone. For this device, F1 was a 7-GHz, –10-dBm CW signal and F2 was 12-GHz, 40-dBm pulsed at 10-μS pulsewidth at a 5% duty cycle, and they were separated using 8-GHz

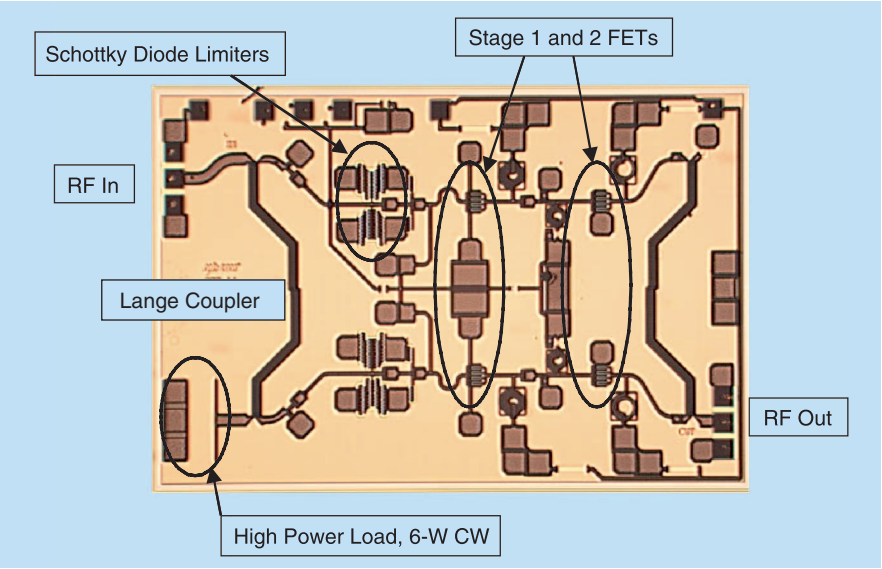

Figure 2. *MA01502D, a commercially available C/X-band integrated LNA/Limiter. MMIC size: 4.6 ×3.1 mm.*

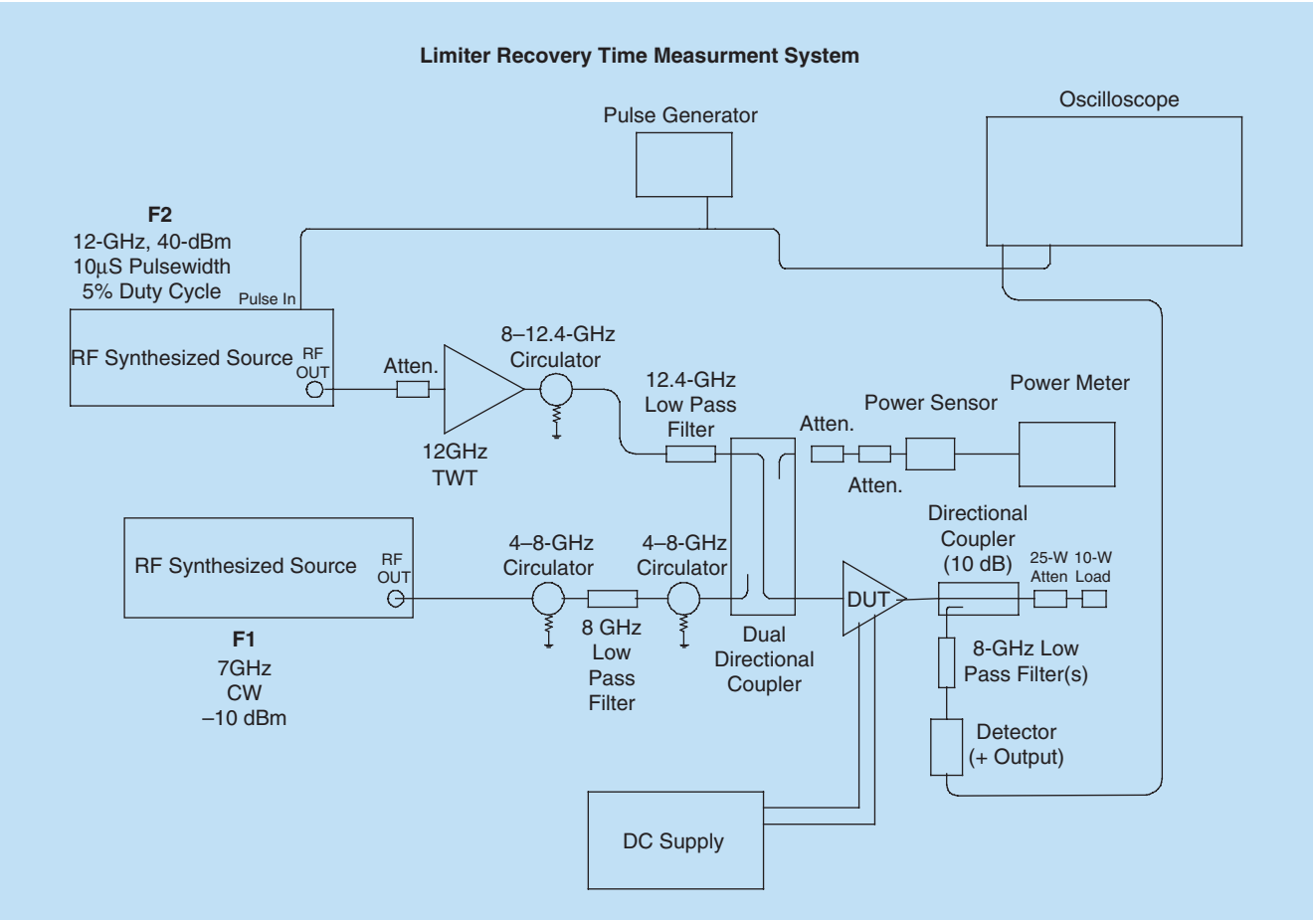

Figure 3. *A LNA/limiter recovery time test set-up.*

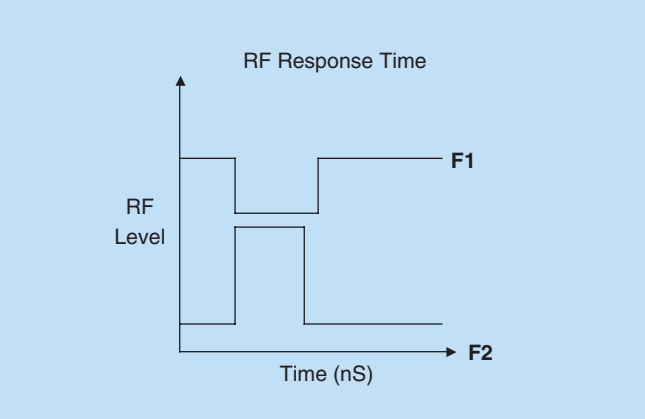

Figure 4. *A representational plot of relationship between F1 (CW, small-signal) and F2 (pulsed, large-signal) tones.*

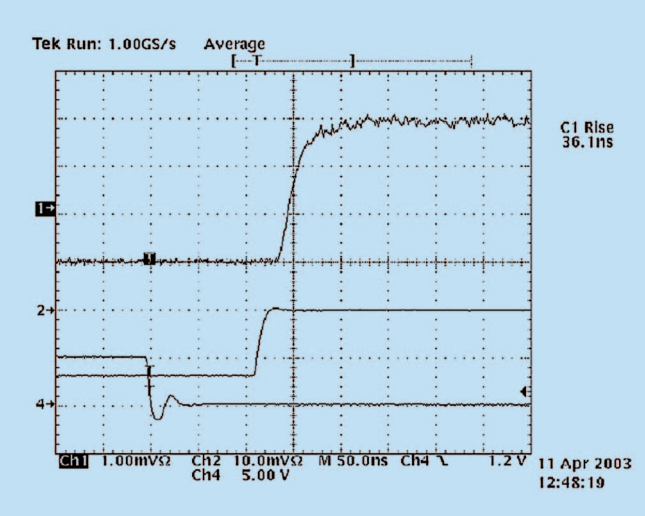

Figure 5. *A LNA small-signal recovery time plot of F1 tone (Channel 1) under high-power pulsed stimulus (F2 tone, P_{out} ~10 W, Chan. 2, negative detector). Channel 4 is pulse generator signal used to trigger F2 source and oscilloscope.*

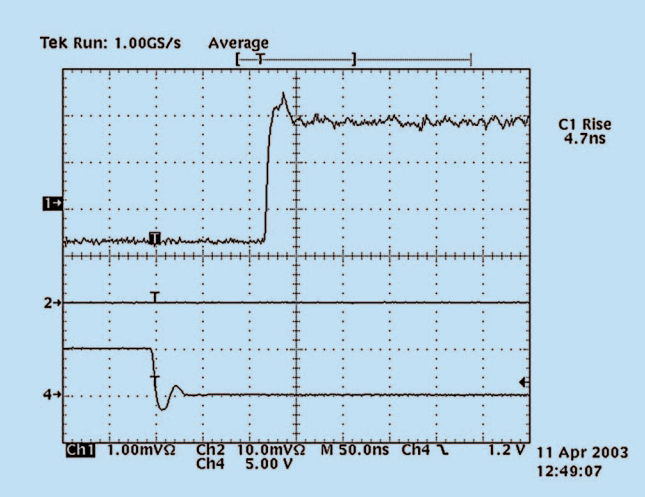

Figure 6. *An LNA small-signal recovery time plot of F1 tone (Channel 1) under moderate power pulsed stimulus (F2 tone, Channel 2, negative detector). F2 tone no longer detectable. F1 tone weakly attenuated.*

low pass filters. At the output of the device, a directional coupler was used to sample the combined signals and low pass filters were used to filter out the pulsed F2 tone. The recovery time measurement was then made using a positive output voltage detector connected to a high frequency oscilloscope. Refer to Figure 3 for the test set-up block diagram.

Test Results

Figure 4 represents the RF levels of the two frequency tones versus time. When the high power F2 signal is on ("high"), the Schottky diodes of the limiter are effectively short circuited to ground. The CW F1 signal is subsequently attenuated and goes low, as shown in Figure 4.

Figure 5 shows a typical RF recovery time plot from the oscilloscope using the internal "rise time" measurement capability to determine the 10–90% rise time (in this example 36.6 ns). By using a negative detector to look at the F2 pulse (at incident port of dual directional coupler), one could also measure the delay between the two signals. This plot was taken at the full rated power of the limiter, 10 W, CW. A limiter recovery time acceptance limit of < 100 ns could easily be achieved based on this data.

Figure 6 indicates how the limiter recovery time improves with a lower incident power level. In this plot, the power tone F2 is no longer detectable. The small-signal tone F1 is still clipping, but not as much as in Figure 4. Under these conditions, the 10–90% rise time is <5 ns.

When this testing was conducted several test "issues" were noted and are listed below:

1) To avoid damaging test components and equipment, be absolutely sure that the low power signal path is sufficiently isolated from the high power signal and that all other components are able to withstand the high power levels.
2) Be sure to use an oscilloscope with sufficient bandwidth to measure the response times. By going from a 150-MHz scope to a 500-MHz scope, the measured recovery time decreased by approximately 50%.
3) Use the "cleanest" pulse generator possible to pulse the RF source. Typically the falling edge of a pulse is noisier than the rising edge, this leads to "noise" on the falling edge of the pulsed high power signal, which leads to "noise" in the recovery time measurement.
4) Experiment with different types of pulse generators (even different units of the same type) to get the best signal.
5) Watch for thermal problems. Even though our DUT was attached to a heatsink, the RF signal level dropped as the RF level of the pulsed signal was increased (originally 100-μS wide). By decreasing the pulsewidth, it was possible to maintain the normal small signal gain levels of the DUT.

References

[1] Microwave MMIC Products, M/A-COM, Roanoke, VA.

[2] I.J. Bahl, "10W CW broadband balanced limiter/LNA fabricated using MSAG MESFET process," *Int. J. RF and Microw. Computer-Aided Eng.*, vol. 13, pp. 118–127, Mar. 2003.