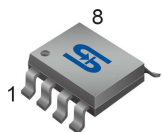



**SOP-8EP**

**Pin Definition:**

1. GND	8. EN
2. FB	7. POK
3. VOUT	6. VCNTL
4. VOUT	5. VIN

### General Description

The TS9230 is a 3A ultra low dropout voltage regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The TS9230 integrates multi-functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The TS9230 can be enabled by other power system. Pulling and holding the EN pin below 0.4V shuts off the output.

### Features

- Ultra Low Dropout 200mV(typ) @  $I_{OUT}=3A$
- Suit for Low ESR Output Capacitor (MLCC)
- 0.5V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset for VCNTL and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit Protection
- Thermal Shutdown Protection
- Power-OK Output with a Delay Time

### Ordering Information

Part No.	Package	Packing
TS9230CS RLG	SOP-8EP	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

### Application

- Telecommunication
- Notebook
- Mother Board

### Absolute Maximum Rating

Parameter	Symbol	Limit	Unit
$V_{CNTL}$ Supply Voltage	$V_{CNTL}$	-0.3 to 7	V
$V_{IN}$ Supply Voltage	$V_{IN}$	-0.3 to 6	V
EN and FB Pin Voltage	$V_{I/O}$	-0.3 to $V_{CNTL}+0.3$	V
Power good Voltage	$V_{POK}$	-0.3 to 7	V
Power Dissipation	SOP-8EP PD	2.5	W
Storage Temperature Range	$T_{ST}$	-65 to +150	°C
Junction Temperature Range	$T_J$	-40 to 125	°C
Operating Temperature Range	$T_{OP}$	-40 to +85	°C
Thermal Resistance from Junction to case	SOP-8EP $\theta_{JC}$	15	°C/W
Thermal Resistance from Junction to ambient	SOP-8EP $\theta_{JA}$	40	°C/W

**Recommended Operating Condition**

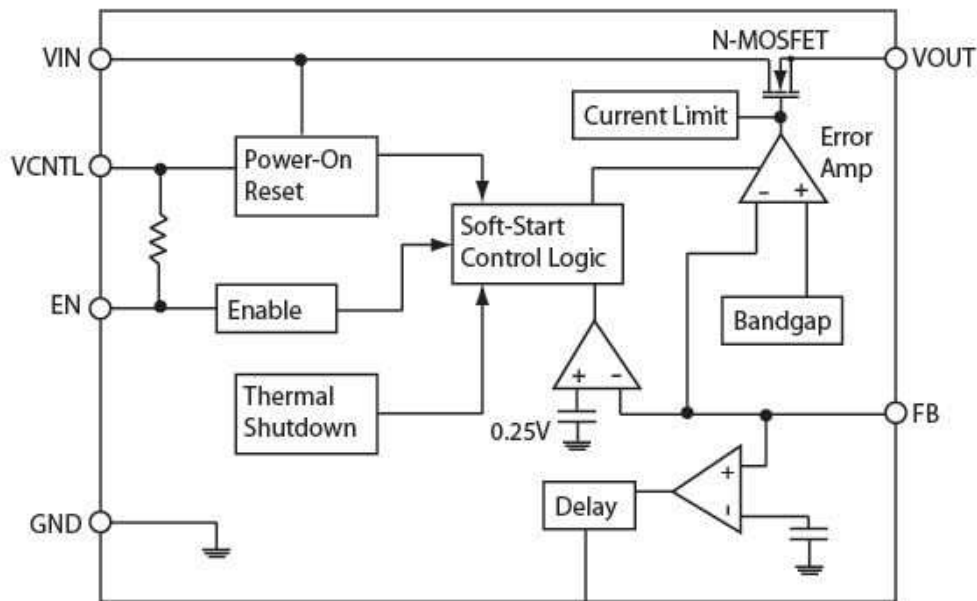
Parameter	Symbol	Conditions	Limit	Unit
$V_{\text{CNTL}}$ Supply Voltage	$V_{\text{CNTL}}$		3 to 5.5	V
$V_{\text{IN}}$ Supply Voltage	$V_{\text{IN}}$		0.9 to 3.65	V
Output Voltage	$V_{\text{OUT}}$	$V_{\text{CNTL}} - V_{\text{OUT}} > 1.9\text{V}$	0.6 to $V_{\text{IN}} - V_{\text{DROP}}$	V
Output Current	$I_{\text{OUT}}$		0 to 3	A

**Electrical Specifications**

( $V_{\text{CNTL}}=5\text{V}$ ,  $V_{\text{IN}}=1.5\text{V}$ ,  $V_{\text{OUT}}=1.2\text{V}$ ,  $T_{\text{A}}=25^{\circ}\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$V_{\text{CNTL}}$ POR Threshold	$V_{\text{CNTL}}$		2.5	2.7	2.9	V
$V_{\text{CNTL}}$ POR Hysteresis	$V_{\text{CNTL(hys)}}$		--	0.5	--	V
$V_{\text{IN}}$ POR Threshold	$V_{\text{IN}}$		0.6	0.7	0.8	V
$V_{\text{IN}}$ POR Hysteresis	$V_{\text{IN(hys)}}$		--	0.4	--	V
$V_{\text{CNTL}}$ Nominal Supply Current	$I_{\text{CNTL}}$	$\text{EN} = V_{\text{CNTL}}$	--	1	1.8	mA
$V_{\text{CNTL}}$ Shutdown Current	$I_{\text{SD}}$	$\text{EN} = 0\text{V}$	--	15	30	uA
Feedback Voltage	$V_{\text{FB}}$	$V_{\text{CNTL}}=5\text{V}$ , $I_{\text{OUT}}=10\text{mA}$	0.49	0.5	0.51	V
Load Regulation		$I_{\text{OUT}}=0\text{A} \sim 3\text{A}$	--	0.2	0.6	%
Line Regulation		$V_{\text{CNTL}} = V_{\text{EN}} = 5\text{V}$ $V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{V} \sim 5\text{V}$ $I_{\text{OUT}} = 10\text{mA}$	--	0.01	0.1	%/V
Dropout Voltage	$V_{\text{DROP}}$	$I_{\text{OUT}} = 3\text{A}$ , $V_{\text{CNTL}} = 5\text{V}$   $V_{\text{OUT}} = 0.9\text{V}$	--	0.20	0.28	V
$V_{\text{OUT}}$ Pull Low Resistance		$\text{EN} = 0\text{V}$	--	85	--	$\Omega$
Soft Start Time	$T_{\text{SS}}$		--	2	4	mS
EN Pin Logic High threshold voltage	$V_{\text{ENH}}$	Enable	1.2	--	--	V
	$V_{\text{ENL}}$	Disable	--	--	0.4	
EN Hysteresis			--	50	--	mV
EN Pin Pull-Up Current	$I_{\text{EN}}$	$\text{EN} = \text{GND}$	--	10	--	uA
Current Limit	$I_{\text{LIM}}$	$V_{\text{CNTL}} = 3 \sim 5.5\text{V}$ $T_{\text{J}} = -40 \sim 125^{\circ}\text{C}$	4.2	--	--	A
Ripple Rejection	$V_{\text{IN}}$	PSRR $F = 120\text{Hz}$ , $I_{\text{OUT}} = 100\text{mA}$	--	65	--	dB
	$V_{\text{CNTL}}$		--	65	--	
Under-Voltage Threshold		VFB Falling	--	0.25	--	V
POK Threshold Voltage for Power OK	$V_{\text{POK}}$	VFB Rising	90%	93%	96%	VFB
POK Threshold Voltage for Power Not OK	$V_{\text{PNOK}}$	VFB Falling	82%	85%	88%	VFB
POK Low Voltage		POK sinks 5mA	--	0.25	0.4	V
POK Delay Time	$T_{\text{DELAY}}$		0.8	2	4	mS
Thermal shutdown Temp	$T_{\text{SD}}$		--	160	--	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	$T_{\text{SH}}$		--	50	--	$^{\circ}\text{C}$

### Block Diagram

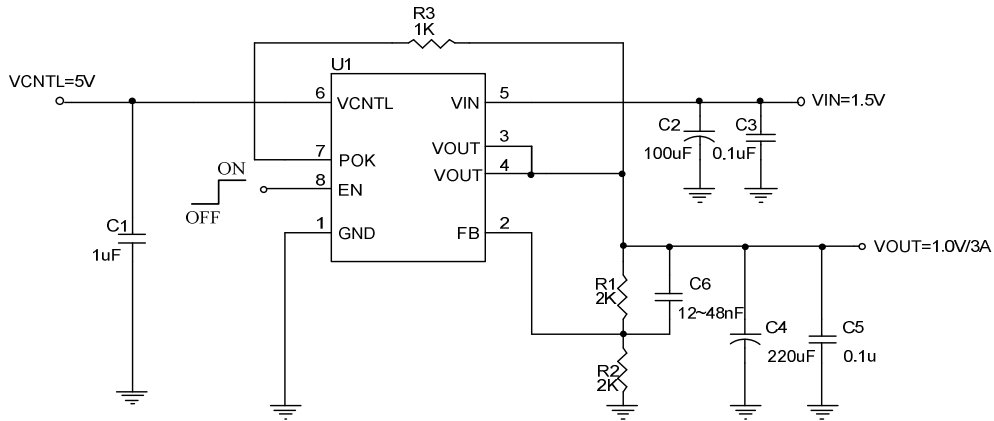


### Pin Function Description

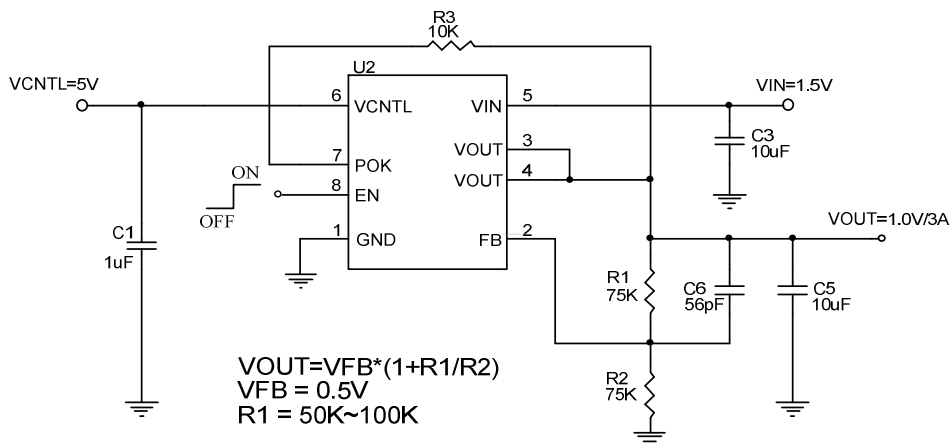
Pin Name	Pin Description
VIN	Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose
VCNTL	Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.
GND	Ground Pin.
POK	Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the $V_{POK}$ threshold or the falling FB voltage is below the $V_{POK}$ threshold, indicating the output is not OK
EN	Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, this pin is internal pulled up to $V_{CNTL}$ voltage, enabling the regulator.
FB	Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by: $V_{OUT} = 0.5 \times \left(1 + \frac{R1}{R2}\right) (V)$ Where R1 is connected from $V_{OUT}$ to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100K $\Omega$ .

**Typical Application Circuit**

**Using an Output Capacitor with  $ESR \geq 20m\Omega$**



**Using an MLCC as the Output Capacitor (SOP-8EP)**



## **Function Description**

### **Power-On-Reset**

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

### **Internal Soft-Start**

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2mS.

### **Output Voltage Regulation**

An error amplifier working with a temperature compensated 0.5V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

### **Current Limit**

The TS9230 monitors the current via the output NMOS and limits the maximum current to prevent load and TS9230 from damages during overload or short circuit conditions.

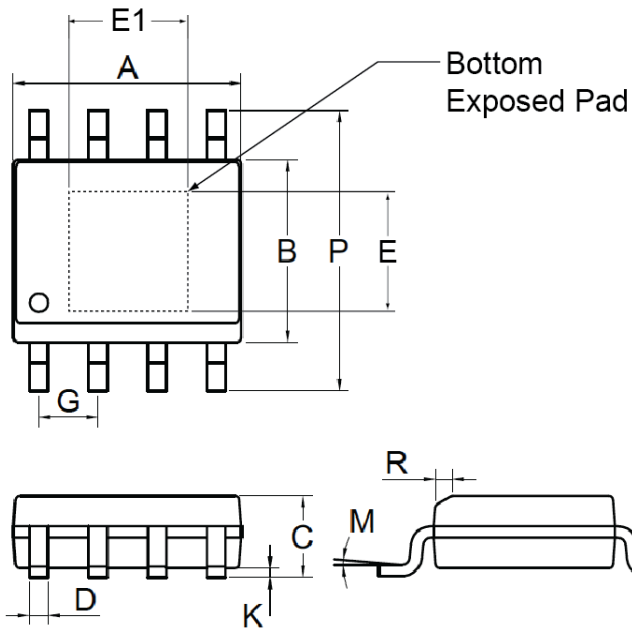
### **Under Voltage Protection**

The TS9230 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the TS9230 starts a new soft-start to regulate output.

### **Thermal Shutdown**

A thermal shutdown circuit limits the junction temperature of TS9230. When the junction temperature exceeds +160°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed.

**SOP-8EP Mechanical Drawing**



DIM	SOP-8EP DIMENSION			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	2.05	2.41	0.081	0.095
E1	2.82	3.30	0.111	0.130
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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