REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
J	Add device types 05, 06, 07, 08, and 09. Delete two vendors, CAGE 01295 and 27014. Add margin test. Change to military format. Make parameter changes through drawing.	13 July 1987	
K	Delete one vendor from device 01, CAGE 34335. Add a footnote to table I. Make editorial changes throughout.	1988 MAY 24	

CURRENT CAGE CODE 67268

REV																										
PAGE																										
REV STATUS OF PAGES	REV	K	K	K	K	K	K	J	J	J	K	K	J	J	J	J	J	K								
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17								

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
02 February 1979

AMSC N/A

PREPARED BY
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APPROVED BY

SIZE A | CODE IDENT. NO. 14933

REV K

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, NMOS, 2KX8 UV ERASEABLE PROM, MONOLITHIC SILICON

DWG NO. 78022

PAGE 1 OF 17

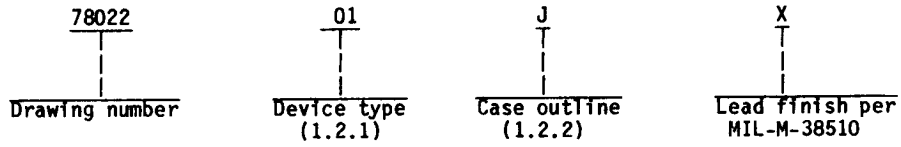
5962-E793

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.4)	2Kx8-Bit UV EPROM	450 ns
02	(see 6.4)	2Kx8-Bit UV EPROM	450 ns
03	(see 6.4)	2Kx8-Bit UV EPROM	350 ns
04	(see 6.4)	2Kx8-Bit UV EPROM	350 ns
05	(see 6.4)	2Kx8-Bit UV EPROM	150 ns
06	(see 6.4)	2Kx8-Bit UV EPROM	200 ns
07	(see 6.4)	2Kx8-Bit UV EPROM	250 ns
08	(see 6.4)	2Kx8-Bit UV EPROM	300 ns
09	(see 6.4)	2Kx8-Bit UV EPROM	450 ns

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-pin, 1.290" x .610" x .225"), dual-in-line package 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC}	-0.3 V dc to +6 V dc 2/
Temperature under bias	-65°C to +135°C
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	635 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	(See MIL-M-38510, appendix C)
Junction temperature (T_J)	+160°C
All input or output voltages with respect to ground	-0.3 V dc to +6 V dc
V_{PP} supply voltage with respect to ground during program (device types 01, 02, 03, 04)	-0.3 V dc to +26.5 V dc
V_{PP} supply voltage with respect to ground during program (device types 05, 06, 07, 08, and 09)	-0.3 V dc to +13.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Input low voltage, V_{IL}	-0.1 V dc to +0.8 V dc
Input high voltage, V_{IH}	2.0 V dc to 6.5 V dc
High level program input voltage, $V_{IH(PR)}$, (device types 01, 02, 03, and 04)	24 V dc to 26 V dc (program method A)
High level program input voltage, $V_{IH(PR)}$, (device types 05, 06, 07, 08, and 09)	12.0 V dc to 13.3 V dc (program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5, 4.6, tables IIIA and IIIB.

3.5.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions Unless otherwise specified, T_C = -55°C to +125°C, GND = 0 V, V_{CC} = 5 V, V_{PP} = V_{CC}	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -400 µA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1, 2, 3		0.45	V
Output leakage current	I_{LO}	V_{OUT} = 5.5 V	All	1, 2, 3		10	µA
V_{PP} read current 1/ 2/	I_{PP1}	V_{PP} = 5.5 V T_C = +25°C, +125°C	01,03	1, 2		5	mA
		V_{PP} = 5.5 V T_C = -55°C		3		10	
	I_{PP2}	V_{PP} = 5.5 V	05,06, 07,08, 09	1, 2, 3		5	
V_{CC} current (standby) 2/	I_{CC1}	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL}	01,03	1, 2, 3		30	mA
			05,06, 07,08, 09			40	
V_{CC} current (active) 2/	I_{CC2}	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	01,03	1, 2, 3		115	mA
			05,06, 07,08, 09			100	
V_{PP} read, V_{CC} current combined	I_{PP1}+ I_{CC}	V_{PP} = 5.5 V;	02,04	1, 2, 3		125	mA
	I_{PP2}+ I_{CC}		05,06, 07,08, 09			105	
Input capacitance 3/	C_{IN}	V_{IN} = 0 V T_C = +25°C f = 1 MHz	All	4		7	pF
Address to output delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 4/ See figure 4	01,02,09	9, 10, 11		450	ns
			03,04			350	
			05			150	
			06			200	
			07			250	
			08			300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions Unless otherwise specified, T_C = -55°C to +125°C, GND = 0 V, V_{CC} = 5 V, V_{PP} = V_{CC}	Device type	Group A subgroups	Limits Min	Limits Max	Unit
$\overline{CE}$ to output delay	t_{CE}	$\overline{OE}$ = V_{IL} 4/ See figure 4	01,02,09	9, 10, 11		450	ns
			03,04			350	
			05			150	
			06			200	
			07			250	
			08			300	
Output enable to output delay	t_{OE}	$\overline{CE}$ = V_{IL} 4/ See figure 4	01,02,09	9, 10, 11		150	ns
			03,04			120	
			05,06			75	
			07			100	
			08			110	
Output enable high to output float	t_{DF}	$\overline{CE}$ = V_{IL} 4/ 5/ See figure 4	01,02, 03,04	9, 10, 11	0	130	ns
			05, 06, 07,08		0	60	
			09		0	80	
Address to output hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 4/ See figure 4	All	9, 10, 11	0		ns

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2/ V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

3/ See 4.3.1c.

4/ Output load: 1 TTL gate and C_L = 100 pF; t_r and t_f ≤20 ns; input pulse levels: 0.45 V to 2.4 V; input timing reference level: 1.0 V and 2.0 V; output timing reference level: 0.8 V and 2.0 V.

5/ If not tested, shall be guaranteed to the limits specified in table I.

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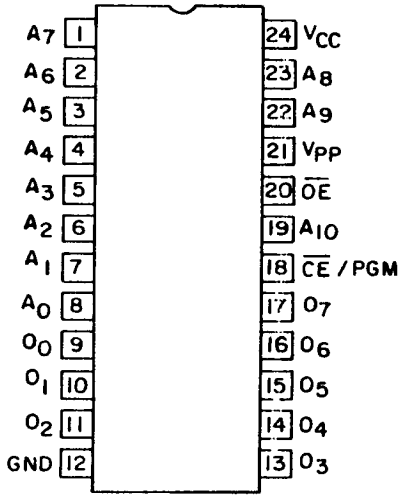
Device types 01 through 09

Case J



PIN NAMES

A_0-A_{10}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_0-O_7	Outputs

FIGURE 1. Terminal connections (top view).

TRUTH TABLE (UNPROGRAMMED) 1/

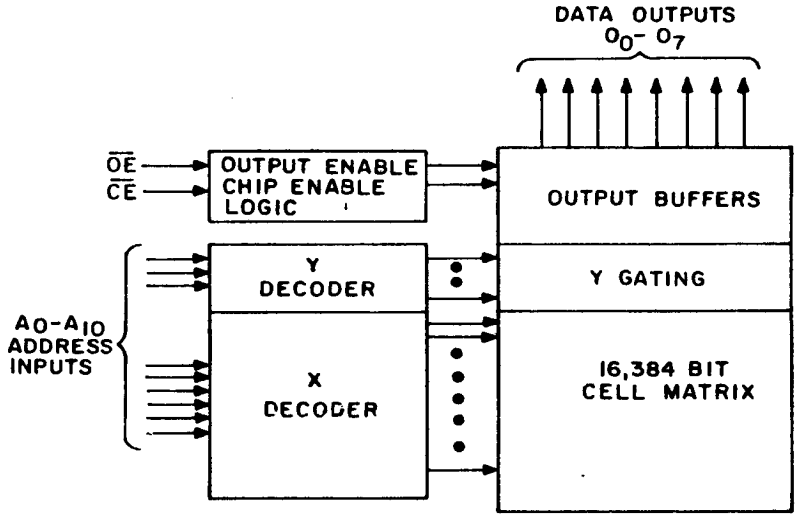
Mode	Input				Outputs 2/
	$\overline{CE}$	$\overline{OE}$	+Vpp	+V_{CC}	
Read	L	L	5	5	Data Out
Standby	H	X	5	5	High Z
Program	Pulsed L to H	H	25	5	Data In
Program Verify	L	L	25	5	Data Out
Program Inhibit	L	H	25	5	High Z

1/ Positive logic

H = High logic level
L = Low logic level
X = Irrelevant
High Z = High-impedance state

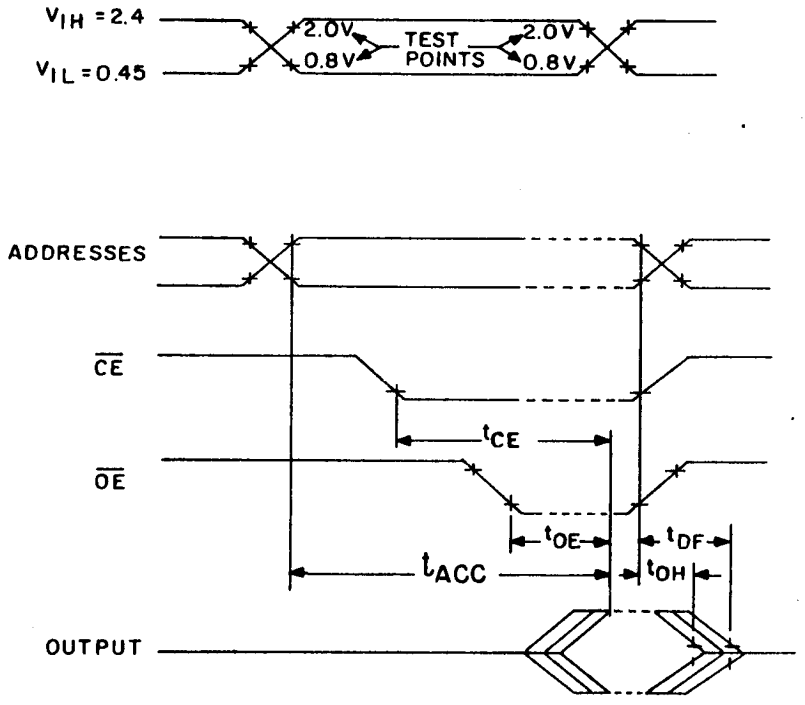
2/ Outputs have internal active pullups.

FIGURE 2. Truth table.



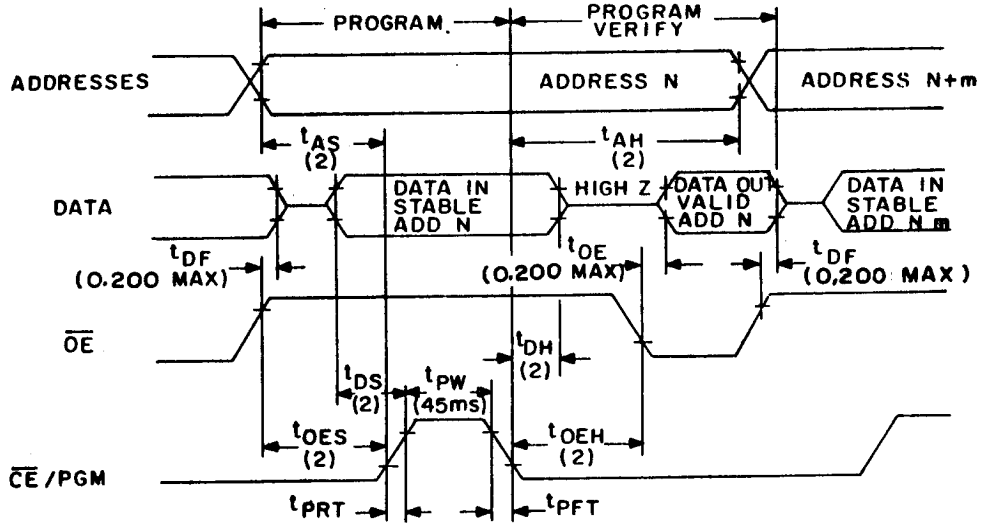
NOTES:
1. A_0 = least significant address bit; A_{10} = most significant address bit.
2. O_0 = least significant data output bit; O_7 = most significant data output bit.

FIGURE 3. Block diagram.



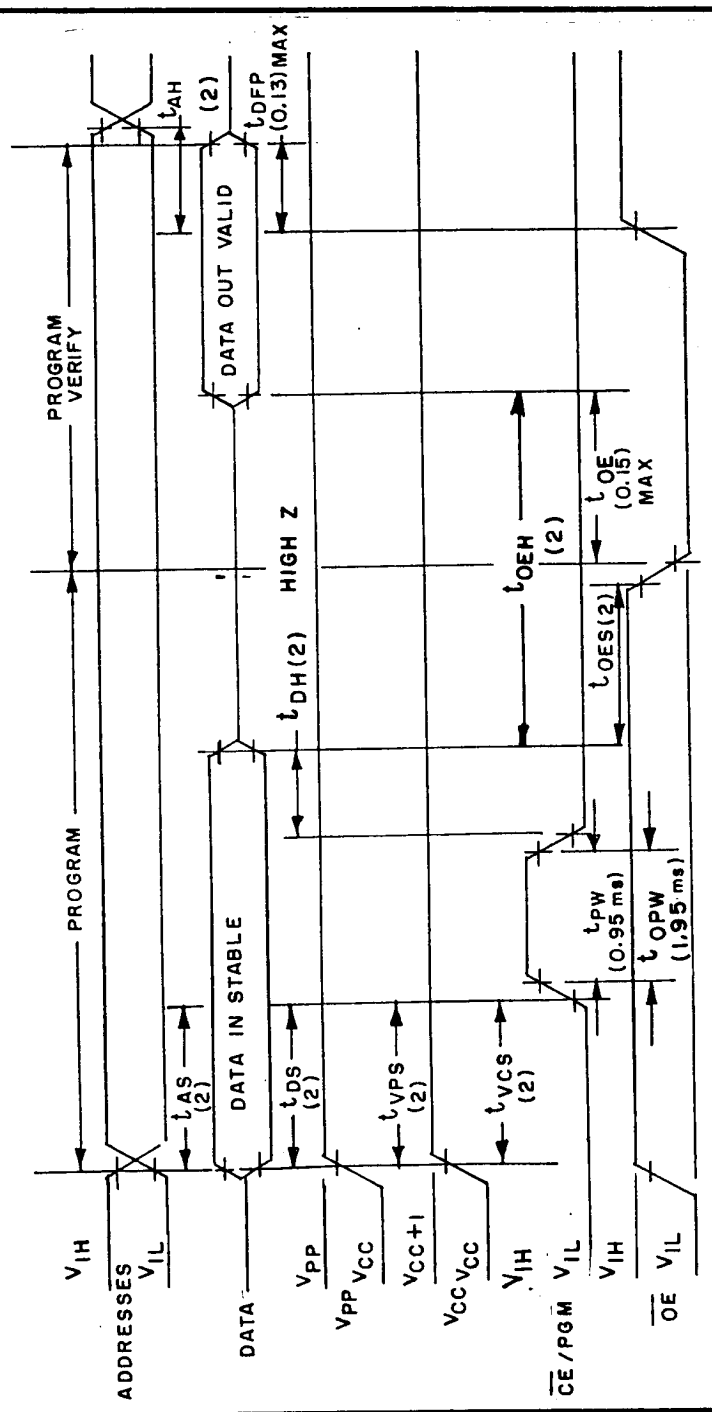
NOTE:
1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 4. Timing diagram.



NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% to 90%) are 20 ns.
4. Input pulse levels are 0.8 V to 2.2 V.
5. All times shown in parentheses are minimum times in µs unless otherwise specified.

FIGURE 5. Programming waveforms for method A.



NOTES:
1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}
2. The t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

FIGURE 6. Programming waveforms for method B.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2 or 2, 8(+125°C),10

1/ * PDA applies to subgroup 1.
2/ Any or all subgroup may be combined when using a high speed tester.
3/ Subgroup 7 shall consist of verifying the pattern specified.
4/ For all electrical tests, the device shall be programmed to the pattern specified.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

Margin test method A

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).
2. Bake, unbiased, for 12 hours at +200°C.
3. Perform a margin test using Vm = V_{CC} = 6.0 V at +25°C using loose timing.
4. Erase device, then program 45 to 50 percent of the bits to a worst case speed pattern.
5. Perform dynamic burn-in (see 4.2a).
6. Perform a margin test using Vm = V_{CC} = 6.0 V at +25°C.
7. Perform 100 percent electrical testing at +125°C and -55°C. Perform 100 percent ac and dc electricals at +25°C.
8. Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D.
9. Verify erasure (see 3.5.3).

Margin test method B

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

2. Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

3. Perform a margin test using Vm = +6.0 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

4. Perform dynamic burn-in (see 4.2a).

5. Margin at Vm = 6.0 V.

6. Perform electrical tests (see 4.2).

7. Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

8. Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The device is erased by exposure to high intensity shortwave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 shortwave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about one inch from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures for method A. The programming characteristics in table IIIA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms of figure 5 and programming characteristics of table IIIA shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{pp} is 25.0 ±1.0 V and $\overline{CE}$/PGM is brought to V_{IH}, also $\overline{OE}$ is at V_{IH}.

4.6 Programming procedures for method B. The programming characteristics in table IIIB and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and programming characteristics of table IIIB shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{pp} is 12.0 to 13.3 V and $\overline{CE}$/PGM is brought to V_{IH}.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/2210XBXX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

TABLE IIIA. Programming characteristics for method A.

Parameters	Symbol	Test conditions	Limits Min	Limits Max	Unit
V_{CC} supply current	I_{CC}	T_C = +25°C, V_{CC} = 5.0 V, V_{IH} = 2.0 V minimum, V_{IL} = 0.80 maximum, V_{IH} = $\overline{OE}$ = 5.0 V ±10%		100	mA
V_{PP} read current	I_{PP1}	V_{PP} = 5.5 V, $\overline{CE}$/PGM = V_{IL}		5	mA
V_{PP} program current	I_{PP2}	$\overline{CE}$/PGM = V_{IH}, V_{PP} = 25 V ±1.0 V		30	mA
Address setup time	t_{AS}	See figure 5	2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		2		µs
$\overline{OE}$ hold time	t_{OEH}		2		µs
Data hold time	t_{DH}		2		µs
Chip deselect to output float delay	t_{DF}		0	200	ns
Output enable to output delay	t_{OE}			200	ns
Program pulse width	t_{PW}		45	55	ms
Program pulse rise time	t_{PRT}		5	100	ns
Program pulse fall time	t_{PFT}		5	100	ns

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TABLE IIIB. Programming characteristics for method B.

Parameters	Symbol	Test conditions	Limits Min	Limits Max	Unit
V_{CC} supply current	I_{CC}	T_C = +25°C, V_{CC} = 5.0 V, V_{IH} = 2.0 V minimum, V_{IL} = 0.80 maximum, V_{IH} = $\overline{OE}$ = 5.0 V ±10%		100	mA
V_{PP} read current	I_{PP1}	V_{PP} = 5.5 V, $\overline{CE}$/PGM = V_{IL}		5	mA
V_{PP} program current	I_{PP2}	$\overline{CE}$/PGM = V_{IH}, V_{PP} = 25 V ±1.0 V		30	mA
Address setup time	t_{AS}	See figure 6	2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		2		µs
$\overline{OE}$ hold time	t_{OEH}		2		µs
Data hold time	t_{DH}		2		µs
Chip deselect to output float delay	t_{DFP}		0	130	ns
Output enable to output delay	t_{OE}			150	ns
Program pulse width	t_{PW}		.95	1.05	ms
Over program pulse width	t_{OPW}		1.95	55	ms
V_{CC} setup time	t_{VCS}		2		µs
V_{PP} setup time	t_{VPS}		2		µs

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6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part 1/ number	Replacement military specification part number	Programming method
7802201JX	2/ 34649	AM2716/BJA MD2716M/B	M38510/22101BJX M38510/22101BJX	A
7802202JX	2/	MM2716QM/883B		A
7802203JX	2/ 2/ 2/	AM2716-1DLB SMJ2516-35JM PMJ2516-35JM		A
7802204JX	2/	MM2716-1QM/883B		---
7802205JX	34335	AM2716B-150/BJA		B
7802206JX	34335	AM2716B-200/BJA		B
7802207JX	34335	AM2716B-250/BJA		B
7802208JX	34335	AM2716B-300/BJA		B
7802209JX	34335	AM2716B-450/BJA		B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address	Margin test method
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086	A
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051	B