Data Sheet **December 2001**

Radiation Hardened, SEGR Resistant N-Channel Power MOSFETs

The Discrete Products Operation of Fairchild has developed a series of Radiation Hardened MOSFETs specifically designed for commercial and military space applications. Enhanced Power MOSFET immunity to Single Event Effects (SEE), Single Event Gate Rupture (SEGR) in particular, is combined with 100 krads of total dose hardness to provide devices which are ideally suited to harsh space environments. The dose rate and neutron tolerance necessary for military applications have not been sacrificed.

The Fairchild portfolio of SEGR resistant radiation hardened MOSFETs includes N-Channel and P-Channel devices in a variety of voltage, current and on-resistance ratings. Numerous packaging options are also available.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Reliability screening is available as either commercial, TXV equivalent of MIL-PRF-19500, or Space equivalent of MIL-PRF-19500. Contact Fairchild for any desired deviations from the data sheet.

Formerly available as type TA17699W.

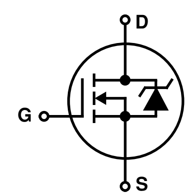
Ordering Information

RAD LEVEL	SCREENING LEVEL	PART NUMBER/BRAND
10K	Commercial	FSYE33A0D1
100K	TXV	FSYE33A0R3
100K	Space	FSYE33A0R4

Features

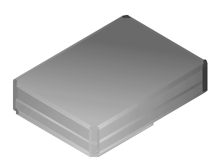
- 5A, 400V, $r_{DS(ON)} = 1.2\Omega$
- Total Dose
  - Meets Pre-RAD Specifications to 100 krad(Si)
- Single Event
  - Safe Operating Area Curve for Single Event Effects
  - SEE Immunity for LET of 36MeV/mg/cm^2 with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 10V Off-Bias
- Dose Rate
  - Typically Survives 3E9 rad (Si)/s at 80% BV_{DSS}
  - Typically Survives 2E12 if Current Limited to I_{DM}
- Photo Current
  - 6nA Per-rad(Si)/s Typically
- Neutron
  - Maintain Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2

Symbol



Packaging

SMD.5



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		FSYE33A0D, FSYE33A0R	UNITS
Drain to Source Voltage	V_{DS}	400	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	400	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	5	A
$T_C = 100^oC$	I_D	3	A
Pulsed Drain Current	I_{DM}	15	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = 25^oC$	P_T	75	W
$T_C = 100^oC$	P_T	30	W
Linear Derating Factor		0.60	$W/^oC$
Single Pulsed Avalanche Current, L = 100μH (See Test Figure)	I_{AS}	15	A
Continuous Source Current (Body Diode)	I_S	5	A
Pulsed Source Current (Body Diode)	I_{SM}	15	A
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Lead Temperature (During Soldering) (Distance >0.063in (1.6mm) from Case, 10s Max)	T_L	300	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1mA$, $V_{GS} = 0V$		400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1mA$	$T_C = -55^oC$	-	-	5.0	V
			$T_C = 25^oC$	1.5	-	4.0	V
			$T_C = 125^oC$	0.5	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 320V$, $V_{GS} = 0V$	$T_C = 25^oC$	-	-	25	μA
			$T_C = 125^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm20V$	$T_C = 25^oC$	-	-	100	nA
			$T_C = 125^oC$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12V$, $I_D = 5A$		-	-	6.6	V
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 3A$, $V_{GS} = 12V$	$T_C = 25^oC$	-	1.0	1.2	Ω
			$T_C = 125^oC$	-	-	2.4	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 200V$, $I_D = 5A$, $R_L = 40\Omega$, $V_{GS} = 12V$, $R_{GS} = 7.5\Omega$		-	-	20	ns
Rise Time	t_r			-	-	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	55	ns
Fall Time	t_f			-	-	25	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 200V$, $I_D = 5A$	-	55	-	nC
Gate Charge at 12V	$Q_{g(12)}$	$V_{GS} = 0V$ to $12V$		-	33	36	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $2V$		-	2	-	nC
Gate Charge Source	Q_{gs}			-	5	7	nC
Gate Charge Drain	Q_{gd}			-	15	18	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 5A$, $V_{DS} = 15V$		-	6	-	V
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	750	-	pF
Output Capacitance	C_{OSS}			-	105	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	26	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.67	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 5A	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 5A, dI_{SD}/dt = 100A/µs	-	-	520	ns

Electrical Specifications up to 100 krad $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts	(Note 3)	BV_{DSS}	V_{GS} = 0, I_D = 1mA	400	-	V
Gate to Source Threshold Volts	(Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA	1.5	4.0	V
Gate to Body Leakage	(Notes 2, 3)	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	100	nA
Zero Gate Leakage	(Note 3)	I_{DSS}	V_{GS} = 0, V_{DS} = 320V	-	25	µA
Drain to Source On-State Volts	(Notes 1, 3)	$V_{DS(ON)}$	V_{GS} = 12V, I_D = 5A	-	6.6	V
Drain to Source On Resistance	(Notes 1, 3)	$r_{DS(ON)12}$	V_{GS} = 12V, I_D = 3A	-	1.2	Ω

NOTES:

1. Pulse test, 300µs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both V_{GS} = 12V, V_{DS} = 0V and V_{GS} = 0V, V_{DS} = 80% BV_{DSS}.

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)			APPLIED V_{GS} BIAS (V)	(NOTE 6) MAXIMUM V_{DS} BIAS (V)
		ION SPECIES	TYPICAL LET (MeV/mg/cm)	TYPICAL RANGE (µ)		
Single Event Effects Safe Operating Area	SEESOA	Ni	26	43	-15	400
		Ni	26	43	-20	360
		Br	37	36	-5	400
		Br	37	36	-10	320
		Br	37	36	-15	200
		Br	37	36	-20	80

NOTES:

4. Testing conducted at Brookhaven National Labs; sponsored by Naval Surface Warfare Center (NSWC), Crane, IN.
5. Fluence = 1E5 ions/cm^2 (typical), T = 25^oC.
6. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

Performance Curves Unless Otherwise Specified

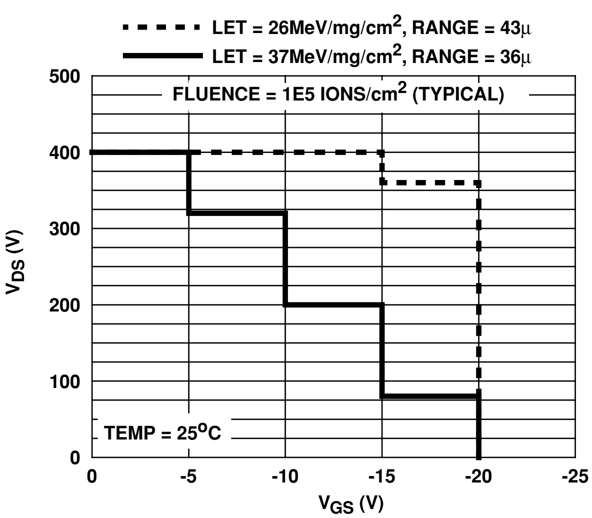


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

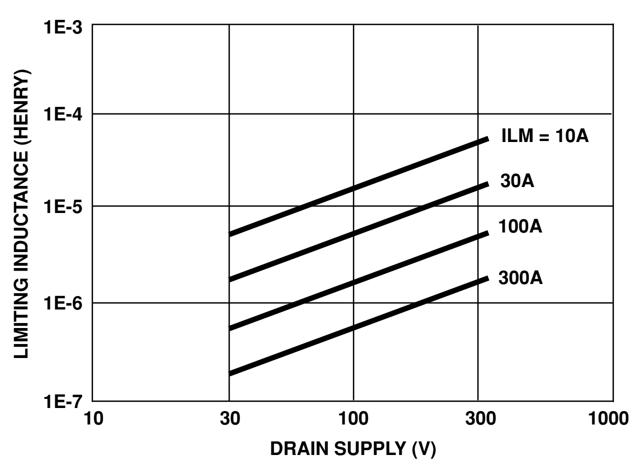


FIGURE 2. TYPICAL DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{AS}

Performance Curves Unless Otherwise Specified **(Continued)**

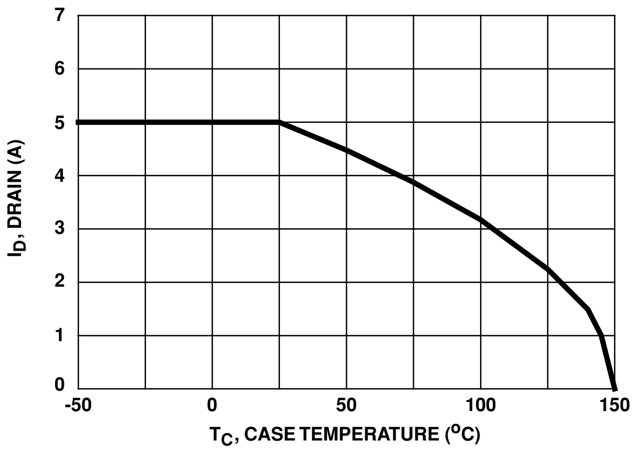


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

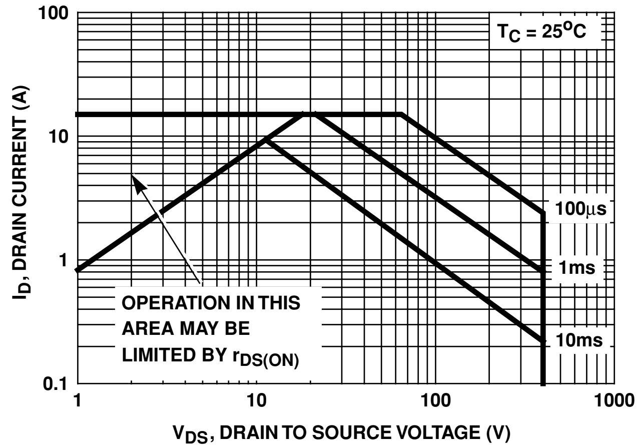


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

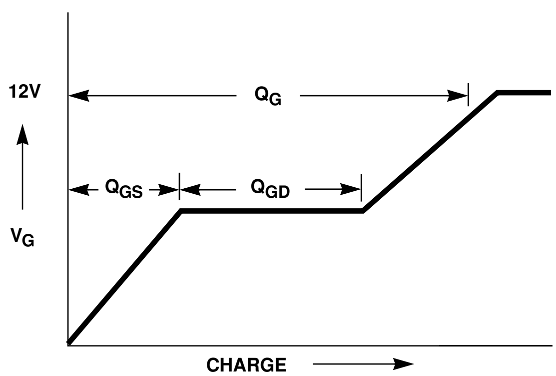


FIGURE 5. BASIC GATE CHARGE WAVEFORM

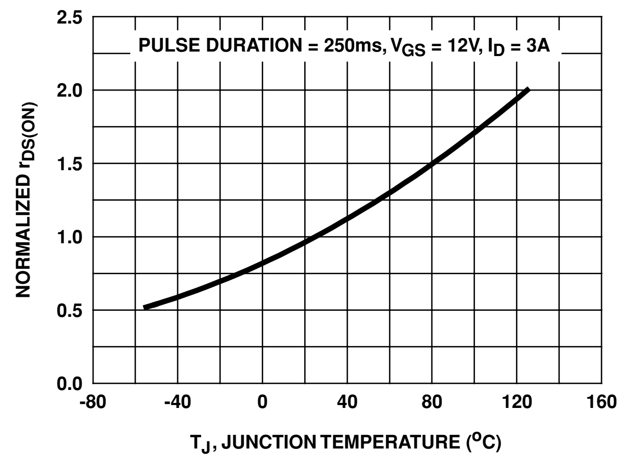


FIGURE 6. TYPICAL NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

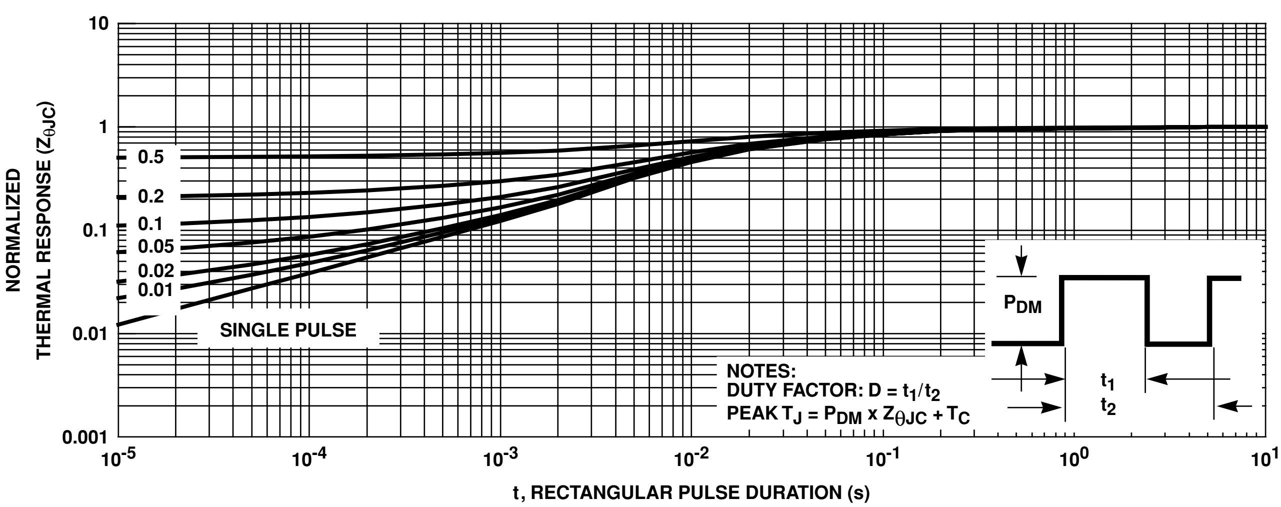


FIGURE 7. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

Performance Curves Unless Otherwise Specified (Continued)

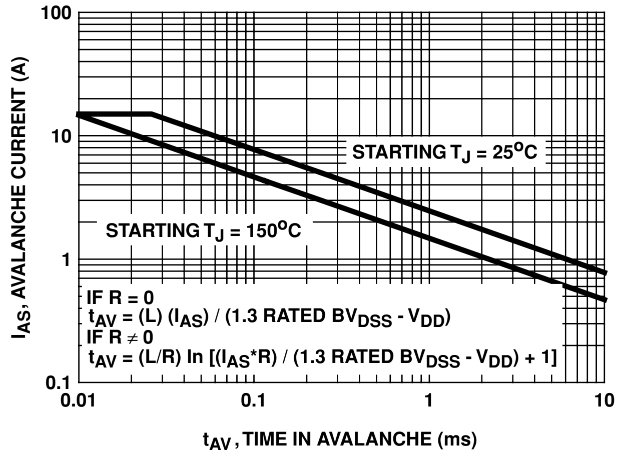


FIGURE 8. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

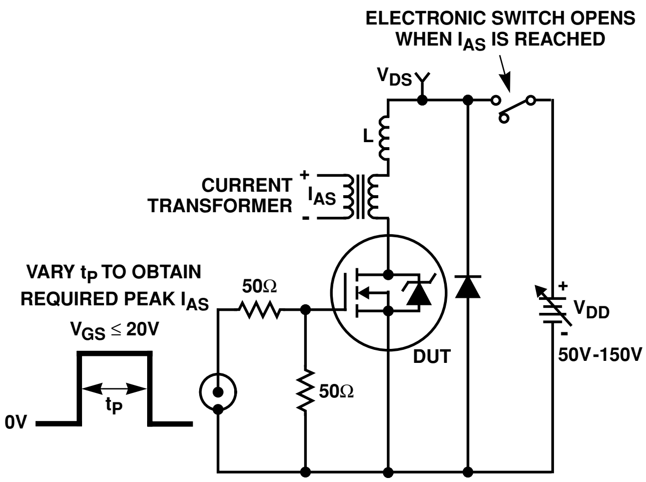


FIGURE 9. UNCLAMPED ENERGY TEST CIRCUIT

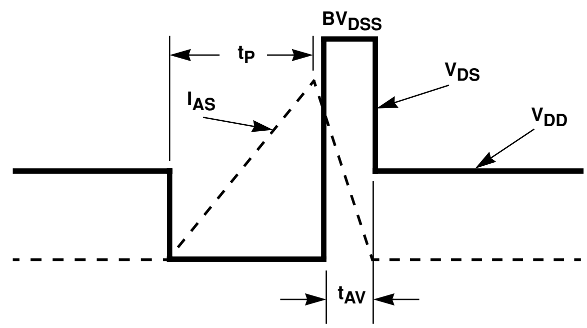


FIGURE 10. UNCLAMPED ENERGY WAVEFORMS

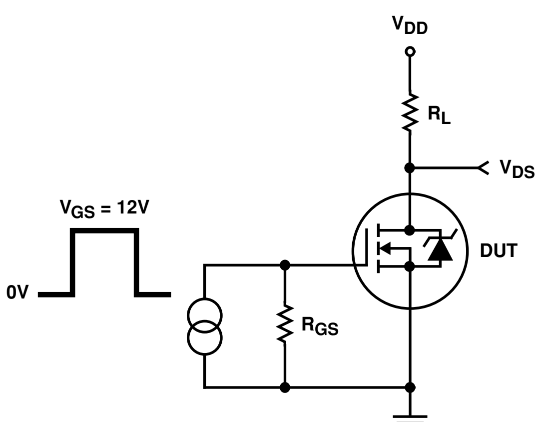


FIGURE 11. RESISTIVE SWITCHING TEST CIRCUIT

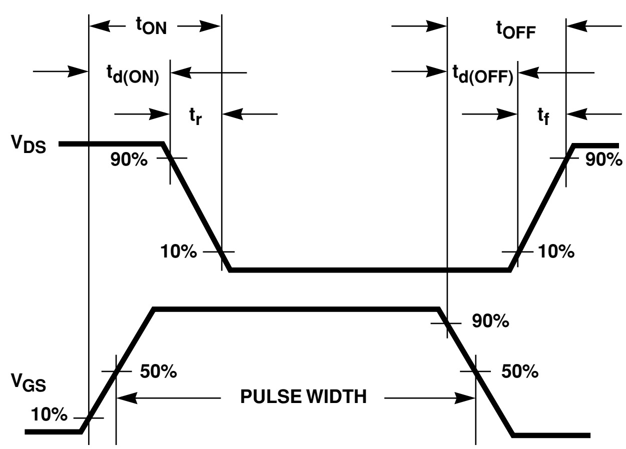


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-PRF-19500, (Screening Information Table).

Delta Tests and Limits (JANTXV Equivalent, JANS Equivalent) $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	±20 (Note 7)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value	±25 (Note 7)	µA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^oC$ at Rated I_D	±20% (Note 8)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0mA$	±20% (Note 8)	V

NOTES:

7. Or 100% of Initial Reading (whichever is greater).
8. Of Initial Reading.

Screening Information

TEST	JANTXV EQUIVALENT	JANS EQUIVALENT
Unclamped Inductive Switching	$V_{GS(PEAK)} = 15V$, L = 0.1mH; Limit = 15A	$V_{GS(PEAK)} = 15V$, L = 0.1mH; Limit = 15A
Thermal Response	$t_H = 10ms$; $V_H = 25V$; $I_H = 1A$; LIMIT = 74mV	$t_H = 10ms$; $V_H = 25V$; $I_H = 1A$; LIMIT = 74mV
Gate Stress	$V_{GS} = 30V$, t = 250µs	$V_{GS} = 30V$, t = 250µs
Pind	Optional	Required
Pre Burn-In Tests (Note 9)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at 25°C)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-PRF-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, $T_A = 150^oC$, Time = 48 hours	MIL-PRF-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, $T_A = 150^oC$, Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-PRF-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, $T_A = 150^oC$, Time = 160 hours	MIL-PRF-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, $T_A = 150^oC$, Time = 240 hours
PDA	10%	5%
Final Electrical Tests (Note 9)	MIL-PRF-19500, Group A, Subgroup 2	MIL-PRF-19500, Group A, Subgroups 2 and 3

NOTE:

9. Test limits are identical pre and post burn-in.

Additional Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 200V$, t = 10ms	0.43	A
Thermal Impedance	ΔV_{SD}	$t_H = 100ms$; $V_H = 25V$; $I_H = 1A$	165	mV

Rad Hard Data Packages - Fairchild Power Transistors

TXV Equivalent

1. RAD HARD TXV EQUIVALENT - STANDARD DATA PACKAGE

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning - Attributes Data Sheet

D. Group A - Attributes Data Sheet

E. Group B - Attributes Data Sheet

F. Group C - Attributes Data Sheet

G. Group D - Attributes Data Sheet

2. RAD HARD TXV EQUIVALENT - OPTIONAL DATA PACKAGE

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning
- Attributes Data Sheet
- Pre and Post Burn-In Read and Record Data

D. Group A - Attributes Data Sheet

E. Group B
- Attributes Data Sheet
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
- Bond Strength Data (Subgroup B3)
- Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)

F. Group C
- Attributes Data Sheet
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
- Bond Strength Data (Subgroup C6)

G. Group D
- Attributes Data Sheet
- Pre and Post RAD Read and Record Data

Class S - Equivalents

1. RAD HARD “S” EQUIVALENT - STANDARD DATA PACKAGE

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

F. Group A - Attributes Data Sheet

G. Group B - Attributes Data Sheet

H. Group C - Attributes Data Sheet

I. Group D - Attributes Data Sheet

2. RAD HARD MAX. “S” EQUIVALENT - OPTIONAL DATA PACKAGE

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- X-Ray and X-Ray Report

F. Group A
- Attributes Data Sheet
- Subgroups A2, A3, A4, A5 and A7 Data

G. Group B
- Attributes Data Sheet
- Subgroups B1, B3, B4, B5 and B6 Data

H. Group C
- Attributes Data Sheet
- Subgroups C1, C2, C3 and C6 Data

I. Group D
- Attributes Data Sheet
- Pre and Post Radiation Data

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DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
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Definition of Terms

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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4