AsahiKASEI
ASAHI KASEI EMD

AKD4691-A
Evaluation board Rev.0 for AK4691

GENERAL DESCRIPTION

The AKD4691 is an evaluation board for the AK4691, 16bit 4ch ADC + 2ch DAC with built-in MIC/Headphone/Speaker Amplifier. The AKD4691 can evaluate A/D converter and D/A converter separately in addition to loop-back mode (A/D → D/A). The AKD4691 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ **Ordering guide**

AKD4691-A --- Evaluation board for AK4691
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **10pin Header for Digital Audio I/F**
- **RCA connector for an external clock input**
- **10pin Header for Serial Control I/F**

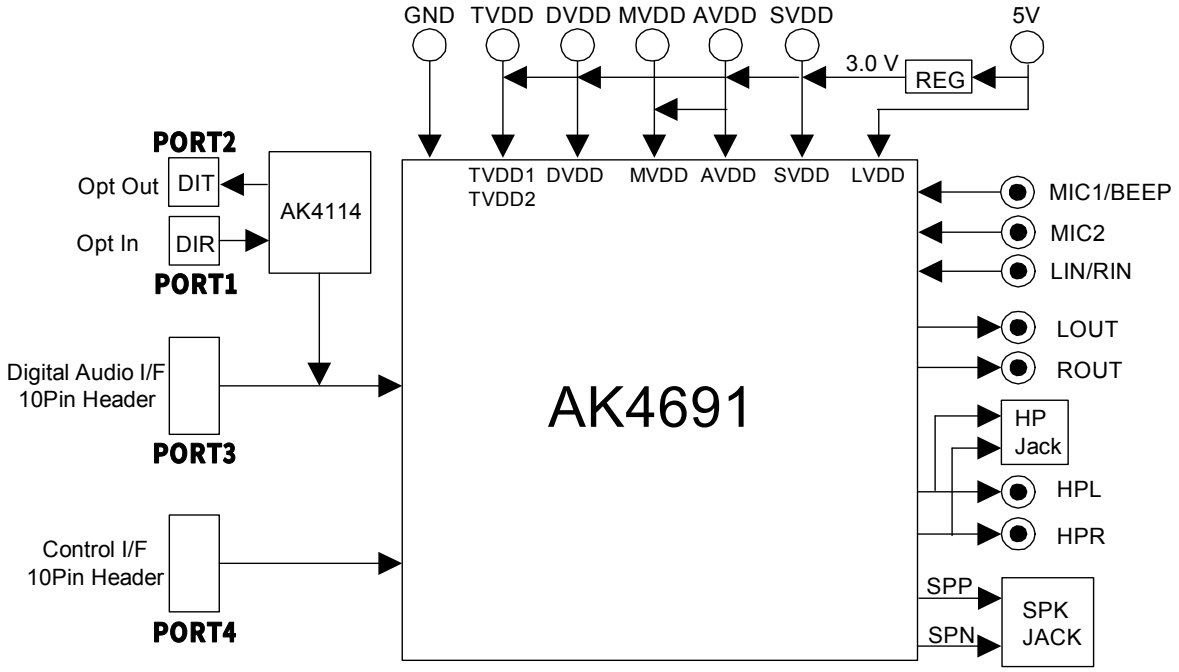


Figure 1. AKD4691 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

(1) Set up the power supply lines.

(1-1) In case of using the regulator.

Set up the jumper pins.

JP	JP2	JP3	JP4	JP5	JP6	JP7	JP8
	REG	SVDD-SEL	AVDD-SEL	DVDD-SEL	TVDD-SEL	VCC-SEL	MVDD-SEL
State	Short	Short	Short	Short	Short	Short	Short

Set up the power supply lines.

[5V] (red)	= 5.0V	: for LVDD of AK4691 (typ. 5.0V) for regulator (3.0V output : SVDD, MVDD, AVDD, DVDD, TVDD1 and TVDD2 of AK4691 and logic)
[D3V] (orange)	= 2.7 ~ 3.6V	: for AK4114 and logic (typ. 3.3V)
[AGND] (black)	= 0V	: for analog ground
[DGND] (black)	= 0V	: for logic ground

(1-2) In case of using the power supply connectors.

Set up the jumper pins.

JP	JP2	JP3	JP4	JP5	JP6	JP7	JP8
	REG	SVDD-SEL	AVDD-SEL	DVDD-SEL	TVDD-SEL	VCC-SEL	MVDD-SEL
State	Open	Open	Open	Open	Open	Open	Open

Set up the power supply lines.

[5V] (red)	= 2.6 ~ 5.5V	: for LVDD of AK4691 (typ. 3.0V)
[SVDD] (orange)	= 2.6 ~ 3.6V	: for SVDD of AK4691 (typ. 3.0V)
[MVDD] (orange)	= 2.6 ~ 5.5V	: for MVDD of AK4691 (typ. 3.0V)
[AVDD] (orange)	= 2.6 ~ 3.6V	: for AVDD of AK4691 (typ. 3.0V)
[DVDD] (orange)	= 2.6 ~ 3.6V	: for DVDD of AK4691 (typ. 3.0V)
[TVDD] (orange)	= 1.6 ~ 3.6V	: for TVDD1, TVDD2 of AK4691 (typ. 3.0V)
[VCC] (orange)	= 1.6 ~ 3.6V	: for logic (typ. 3.0V: This voltage must be same as TVDD.)
[D3V] (orange)	= 2.7 ~ 3.6V	: for AK4114 and logic (typ. 3.3V)
[AGND] (black)	= 0V	: for analog ground
[DGND] (black)	= 0V	: for logic ground

* Each supply line should be distributed from the power supply unit.

(2) Set up the evaluation mode, jumper pins and DIP switch. (See the followings.)

(3) Power on.

The AK4691 and AK4114 should be resets once bringing SW1 (PDN) and SW2 (DIR) “L” upon power-up.

■ Evaluation mode

In case of the AK4691 evaluation using the AK4114, it is necessary to correspond to audio interface format for the AK4691 and AK4114. About the AK4691's audio interface format, refer to datasheet of the AK4691. About the AK4114's audio interface format, refer to Table 2.
The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, please use other mode.
In addition, MCLK of AK4114 supports 256fs and 512fs. When evaluate it in a condition except this, please use other mode.
About the setup of the AK4691's register, refer to datasheet of the AK4691.

Applicable Evaluation Mode

(1) Evaluation of A/D using DIT of AK4114.
  (1-1) Setting with External Slave Mode

(2) Evaluation of D/A using DIR of AK4114.
  (2-1) Setting with External Slave Mode

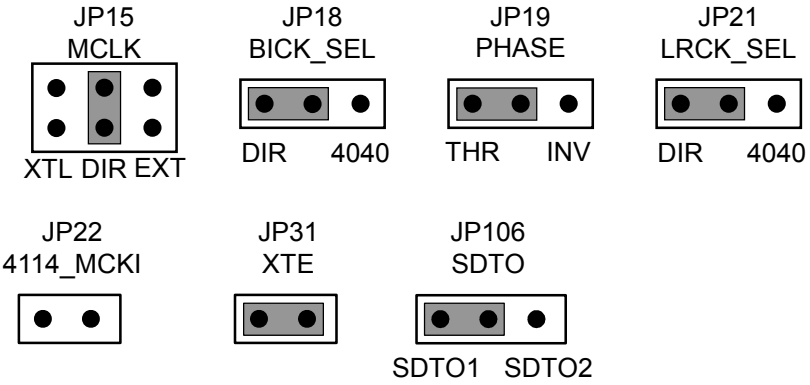
(3) Evaluation of A/D, D/A using PORT3 (DSP).
  (3-1) Setting with PLL Master Mode
  (3-2) Setting with PLL Slave Mode
  (3-3) Setting with External Slave Mode

(4) Evaluation of Loop-back.
  (4-1) Setting with PLL Master Mode
  (4-2) Setting with PLL Slave Mode
  (4-3) Setting with External Slave Mode <Default>

(1) Evaluation of A/D using DIT of AK4114.
(1-1) Setting with External Slave Mode

X1 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, the register of AK4691 should be set to "EXT Slave Mode". MCKI, BICK and LRCK are supplied from AK4114, and SDTO1 or SDTO2 of the AK4691 is output to the AK4114.

The jumper pins should be set as the following.

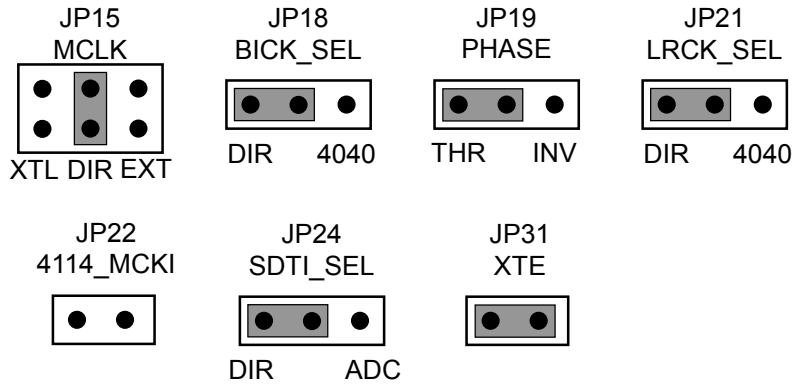


* When SDTO2 data is output to PORT2 (DIT), JP106 should be set to "SDTO2". TDM Mode is not supported in this mode.

(2) Evaluation of D/A using DIR of AK4114.
(2-1) Setting with External Slave Mode

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, the register of AK4691 should be set to "EXT Slave Mode".

The jumper pins should be set as the following.



(3) Evaluation of A/D, D/A using PORT3 (DSP).

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).

(3-1) Setting with PLL Master Mode

The master clock is input from MCKI of PORT3 (DSP). An internal PLL circuit generates MCKO, BICK, and LRCK.

JP23 (M/S) should be set to "Master". In addition, the register of AK4691 should be set to "PLL Master Mode".

SDTI, SDTO, LRCK and BICK of PORT3 are respectively connected with SDTO, SDTI, LRCK and BICK of DSP. When MCKO is supplied to DSP, test pin (MCKO) should be directly connected to DSP.

Loop-filter of PLL should be properly selected. Because resistor and capacitor values are 10kΩ and 4.7uF respectively on this board.

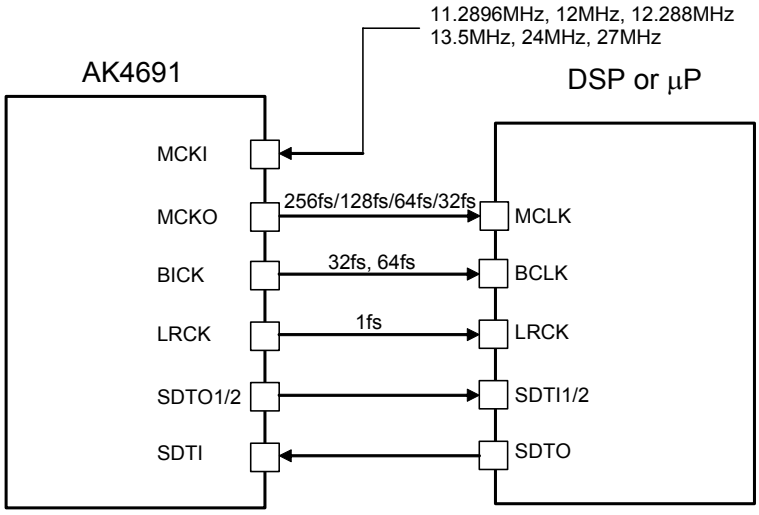
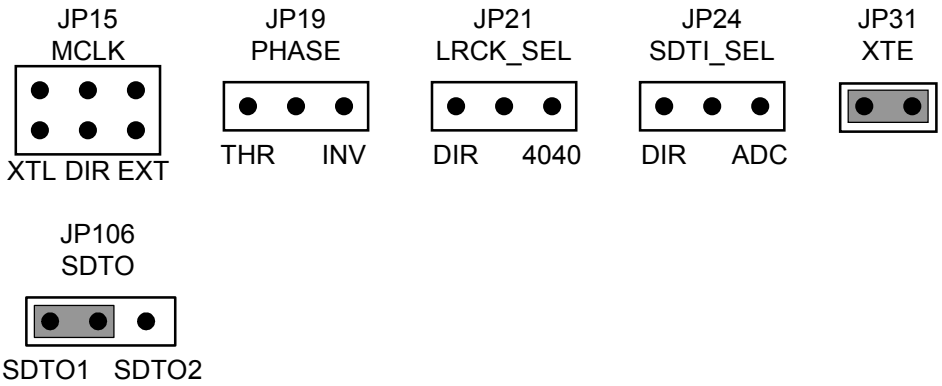


Figure 2. PLL Master Mode

The jumper pins should be set as the following.



* When SDTO2 data is output to PORT3 (DSP), JP106 should be set to "SDTO2".

(3-2) Setting with PLL Slave Mode

A reference clock of PLL is selected among the input clocks supplied from PORT3 (DSP) to MCKI, BICK or LRCK pin. The required clock to the AK4691 is generated by an internal PLL circuit.
JP23 (M/S) should be set to "Slave".

(3-2-1) PLL Reference Clock: MCKI pin

The register of AK4691 should be set to "PLL Slave Mode" (Reference Clock: MCKI).
BICK and LRCK inputs should be synchronized with MCKO output. But the phase between MCKO and LRCK dose not matter.

Loop-filter of PLL should be properly selected. Because resistor and capacitor values are 10kΩ and 4.7uF respectively on this board.

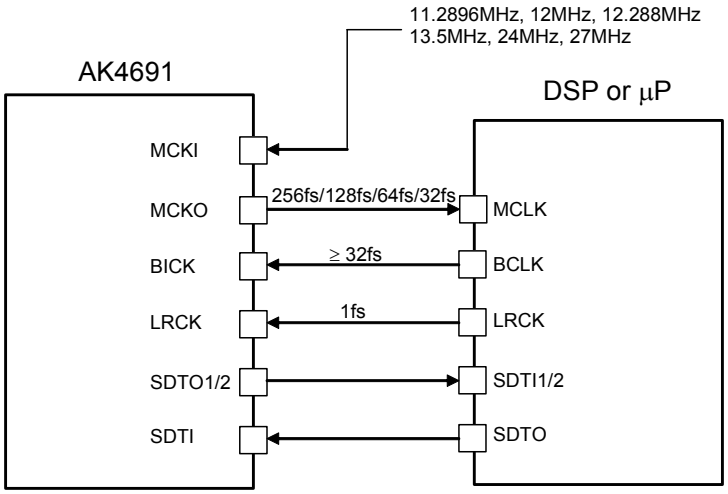


Figure 3. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

The jumper pins should be set as the following.

* When SDTO2 data is output to PORT3 (DSP), JP106 should be set to "SDTO2".

(3-2-2) PLL Reference Clock: BICK or LRCK pin

The register of AK4691 should be set to "PLL Slave Mode" (Reference Clock = BICK or LRCK).

Loop-filter of PLL should be properly selected. Because resistor and capacitor values are 10kΩ and 4.7uF respectively on this board.

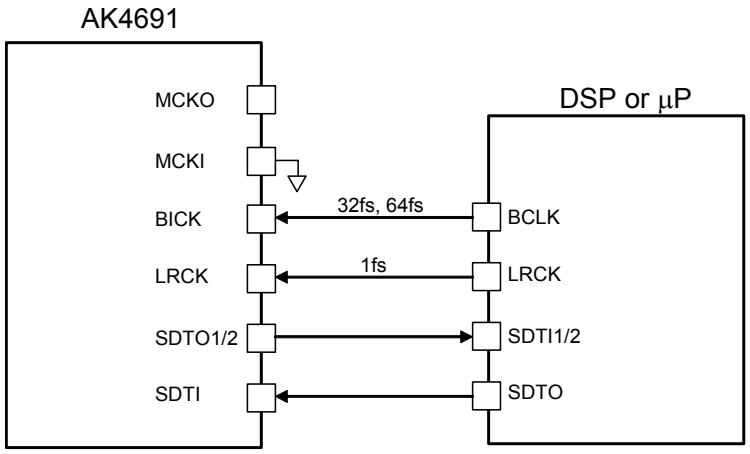
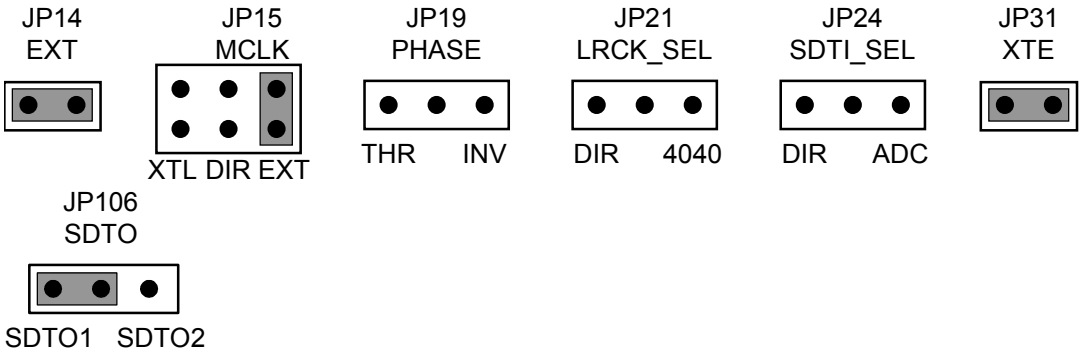


Figure 4. PLL Slave Mode 2(PLL Reference Clock: BICK or LRCK pin)

The jumper pins should be set as the following.



* When SDTO2 data is output to PORT3 (DSP), JP106 should be set to "SDTO2".

(3-3) Setting with External Slave Mode

MCLK, BICK, LRCK, and SDTI are input from PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, the register of AK4691 should be set to "EXT Slave Mode".

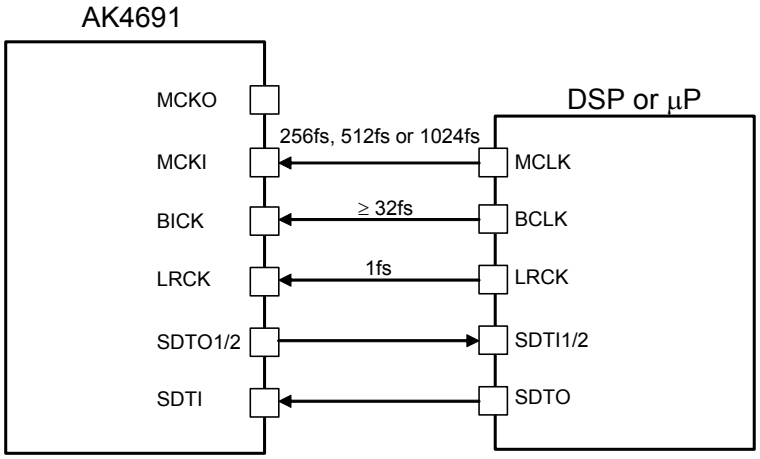
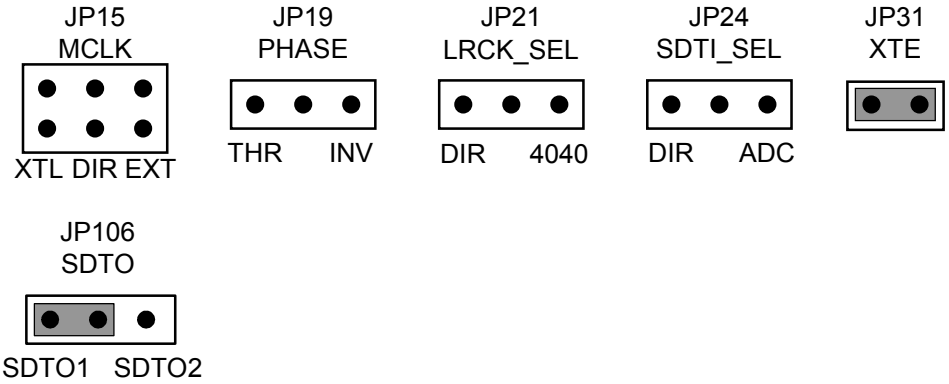


Figure 5. EXT Slave Mode

The jumper pins should be set as the following.



* When SDTO2 data is output to PORT3 (DSP), JP106 should be set to "SDTO2".

(4) Evaluation of Loop-back.

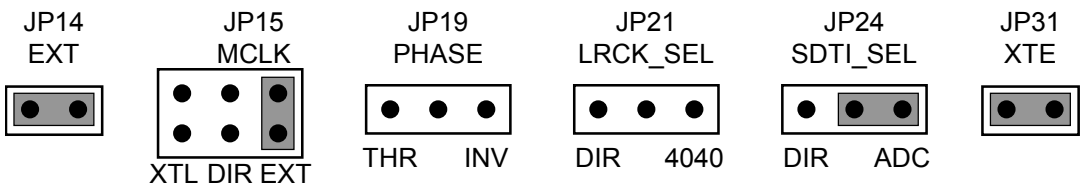
(4-1) Setting with PLL Master Mode

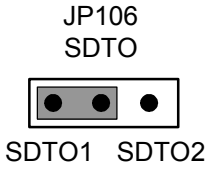
Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
JP23 (M/S) should be set to "Master". In addition, the register of AK4691 should be set to "PLL Master Mode".

(4-1-1) In case of supplying MCLK from J11 (EXT)

Loop-filter of PLL should be properly selected. Because resistor and capacitor values are 10kΩ and 4.7uF respectively on this board.

The jumper pins should be set as the following.

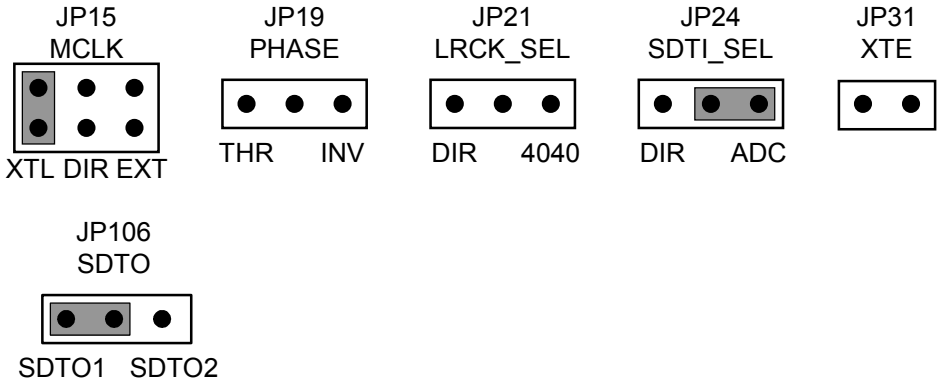




* When a termination (51Ω) is not used, JP14 (EXT) should be open.
When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

(4-1-2) In case of supplying MCKI from X2 (11.2896MHz)

The jumper pins should be set as the following.



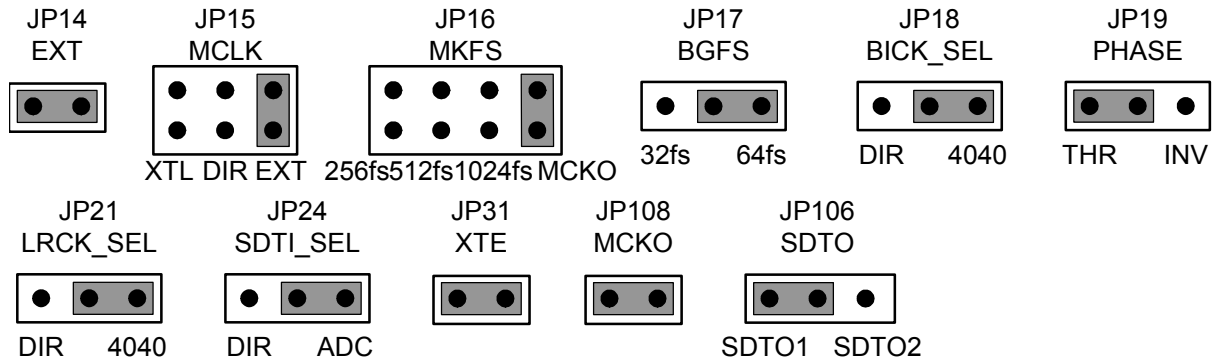
* When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

(4-2) Setting with PLL Slave Mode

BICK and LRCK are generated from MCKO of AK4691 on board divider. The generated BICK and LRCK is input to the AK4691.
JP23 (M/S) should be set to "Slave". In addition, the register of AK4691 should be set to "PLL Master Mode" (Reference Clock: MCKI).
Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).

(4-2-1) In case of supplying MCLK from J11 (EXT)

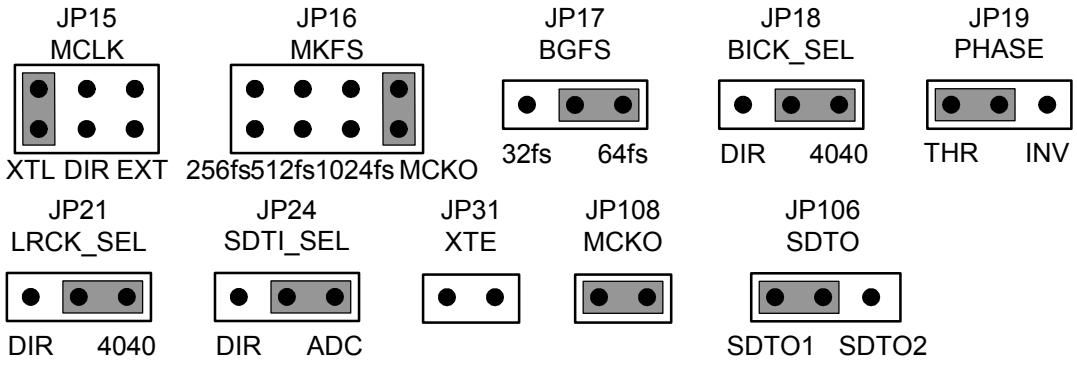
The jumper pins should be set as the following.



*When a termination (51Ω) is not used, JP14 (EXT) should be open.
When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

(4-2-2) In case of supplying MCKI from X2 (11.2896MHz)

The jumper pins should be set as the following.



* When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

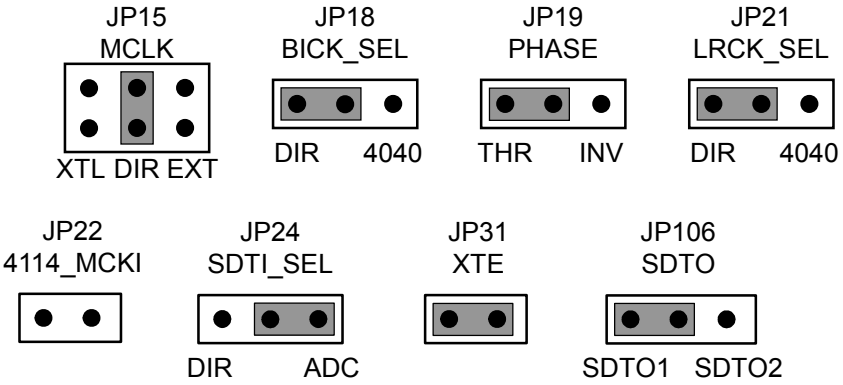
(4-3) Setting with External Slave Mode

JP23 (M/S) should be set to "Slave". In addition, the register of AK4691 should be set to "EXT Slave Mode". Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).

(4-3-1) In case of using clocks from AK4114

X1 (12.288MHz) is used.

The jumper pins should be set as the following.

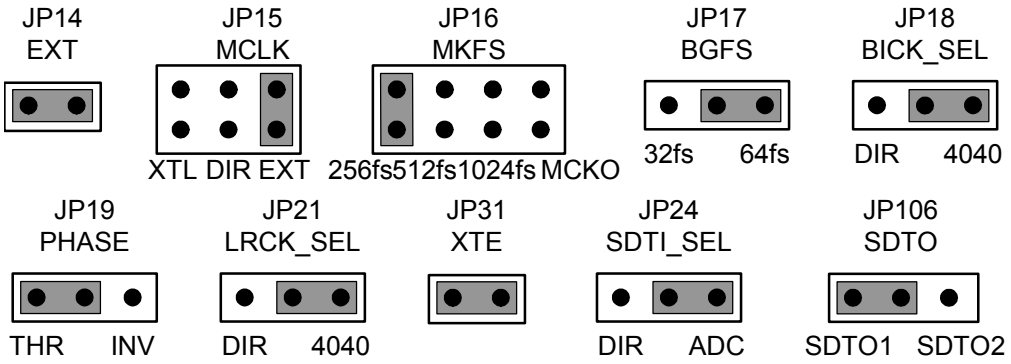


* When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

(4-3-2) In case of using the clock divider on the board

① In case of supplying MCLK from J11 (EXT)
(e.g. MCLK=256fs, BICK=64fs)

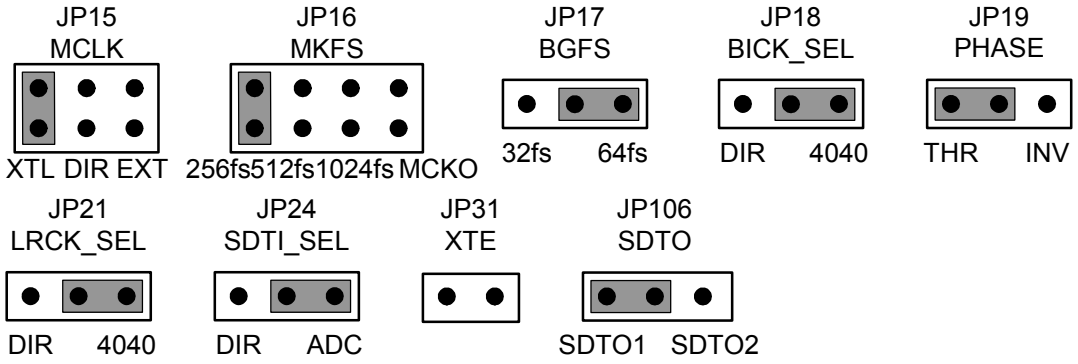
The jumper pins should be set as the following.



* When a termination (51Ω) is not used, JP14 (EXT) should be open.
When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

② In case of supplying MCKI from X2 (11.2896MHz)

The jumper pins should be set as the following.



* When SDTO2 data is looped back to SDTI, JP106 should be set to "SDTO2".

■ DIP Switch set up

[S1] (SW DIP-6): Mode setting for AK4691 and AK4114.

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Audio Format Setting See Table 2		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	AK4114 Master Clock Setting : See Table 3		OFF
5	CAD0	AK4691Control Mode Setting : See Table 4		OFF
6	MUTE	MUTE	Normal Operation	OFF

Table 1. Mode Setting for AK4691 and AK4114

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64 -128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64 -128fs	I	

Table 2. Setting for AK4114 Audio Interface Format

OCKS1	MCKO1	X'tal	
0	256fs	256fs	Default
1	512fs	512fs	

Table 3. Setting for AK4114 Master Clock

■ Jumper pins set up

Main Board

[JP1] (GND): Analog ground and Digital ground
OPEN: Separated.
SHORT: Common. (The connector "DGND" can be open.) <Default>

[JP2] (REG): Selection of REG
OPEN: REG is not used.
SHORT: REG is used. <Default>

[JP3] (SVDD-SEL): SVDD of the AK4691
OPEN: SVDD is supplied from "SVDD" jack.
SHORT: SVDD is supplied from the regulator ("SVDD" jack should be open). <Default>

[JP4] (AVDD-SEL): AVDD of the AK4691
OPEN: AVDD is supplied from "AVDD" jack.
SHORT: AVDD is supplied from the regulator ("AVDD" jack should be open). <Default>

[JP5] (DVDD-SEL): DVDD of the AK4691
OPEN: DVDD is supplied from "DVDD" jack.
SHORT: DVDD is supplied from "AVDD" ("DVDD" jack should be open). <Default>

[JP6] (TVDD-SEL): TVDD of the AK4691
OPEN: TVDD is supplied from "TVDD" jack.
SHORT: TVDD is supplied from "DVDD" ("TVDD" jack should be open). <Default>

[JP7] (VCC-SEL): VCC of the AK4691
OPEN: VCC is supplied from "VCC" jack.
SHORT: VCC is supplied from "TVDD" ("VCC" jack should be open). <Default>

[JP8] (MVDD-SEL): MVDD of the AK4691
OPEN: MVDD is supplied from "MVDD" jack.
SHORT: MVDD is supplied from "AVDD" ("MVDD" jack should be open). <Default>

[JP16] (MKFS): MCLK Frequency
256fs: 256fs. <Default>
512fs: 512fs.
1024fs: 1024fs.
MCKO: MCKO is used.

[JP17] (BCFS): BICK Frequency
32fs: 32fs.
64fs: 64fs. <Default>

[JP22] (4114-MCKI): AK4114 Clock Source
OPEN: X'tal of AK4114 is used. <Default>
SHORT: MCKO of the AK4691 is supplied to the AK4114.

Sub Board

[JP106] (SDTO-SEL): Selection of SDTO output
SDTO1: SDTO1 is output. <Default>
SDTO2: SDTO2 is output.

[JP107] (TVDD2): TVDD2 of the AK4691
SHORT: TVDD2 is supplied from TVDD. <Default>

[JP108] (MCKO): Selection of MCKO output
OPEN: MCKO is not used. <Default>
SHORT: MCKO is used.

■ The function of the toggle SW

*Upper-side is “H” and lower-side is “L”.

[SW1] (PDN): Power down of AK4691. Keep “H” during normal operation.

[SW2] (DIR): Power down of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AKD4691 can be connected via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4691. Table 4 shows switch and jumper settings for serial control. 3-WIRE Mode should be selected in Table4.

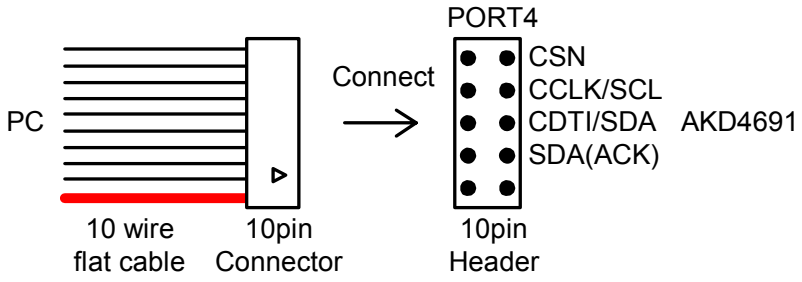


Figure 6. Connect of 10 wire flat cable

Mode		S1	JP25	JP109	
		CAD0	CTRL-SEL	I2C	
3-WIRE		OFF	3-WIRE	Open	Default
I2C	CAD=0	OFF	I2C	Short	
	CAD=1	ON			

Table 4. Control Mode Setting

■ Analog Input/Output Circuits

(1) Input Circuits

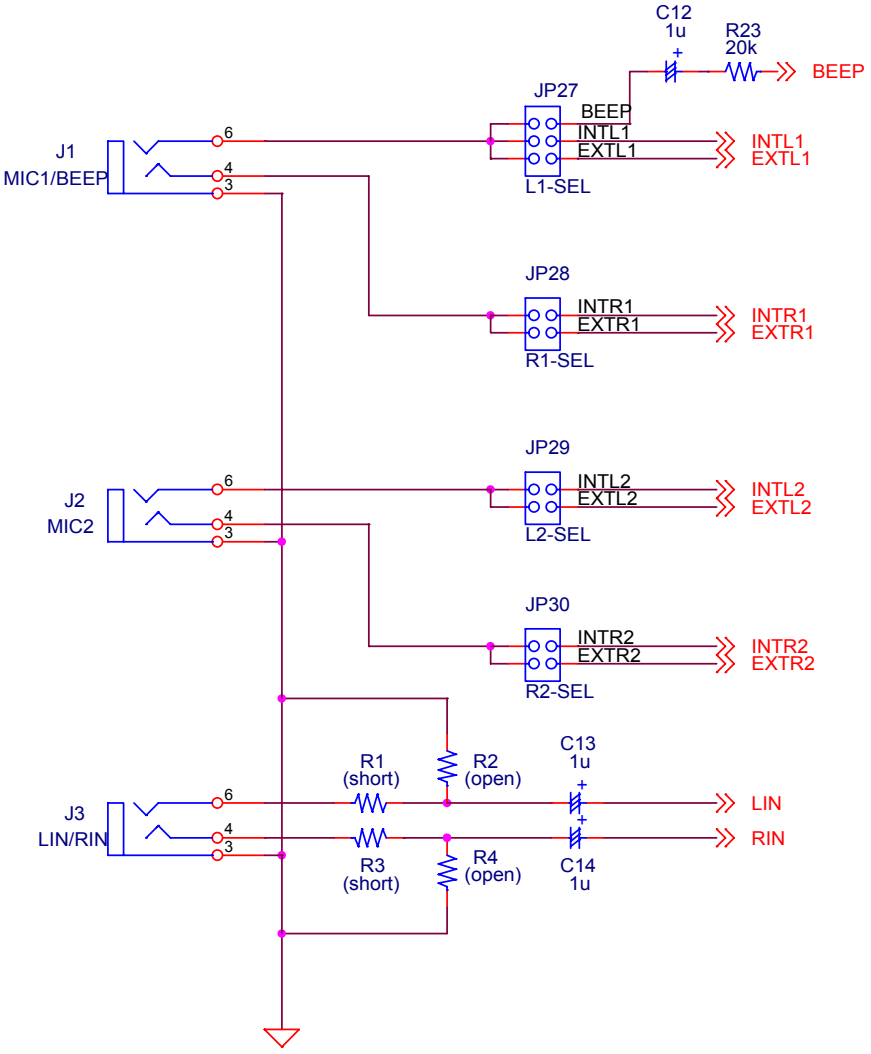
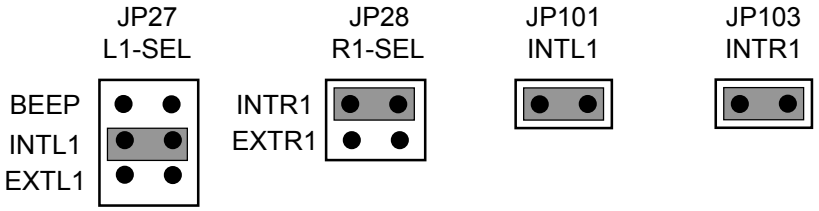


Figure 7. INTL1/INTR1, INTL2/INTR2, EXTL1/EXTR1, EXTL2/EXTR2, BEEP, LIN/RIN Input Circuits

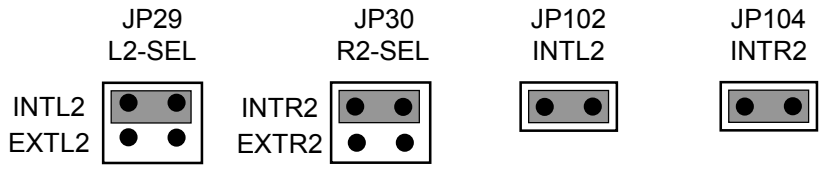
(1-1) INTL1/INTR1 Input Circuit

INTL1/INTR1 is input from J1. JP27 and JP28 should be set as the following.
When the Mic Power is not used, JP101 and JP103 should be set to open.



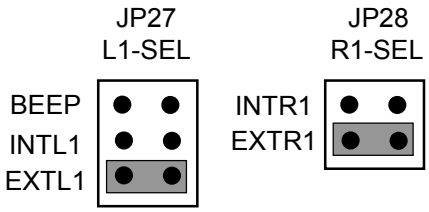
(1-2) INTL2/INTR2 Input Circuit

INTL2/INTR2 is input from J2. JP29 and JP30 should be set as the following.
When the Mic Power is not used, JP102 and JP104 should be set to open.



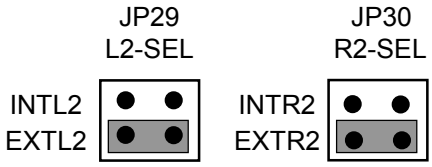
(1-3) EXTL1/EXTR1 Input Circuit

EXTL1/EXTR1 is input from J1. JP27 and JP28 should be set as the following.



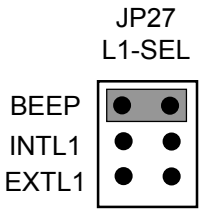
(1-4) EXTL2/EXTR2 Input Circuit

EXTL2/EXTR2 is input from J2. JP29 and JP30 should be set as the following.



(1-5) BEEP Input Circuit

BEEP is input from J1. JP27 should be set as the following.



(1-6) LIN/RIN Input Circuit

LIN/RIN is input from J3.

(2) Output Circuits

(2-1) LOUT/ROUT Output Circuit

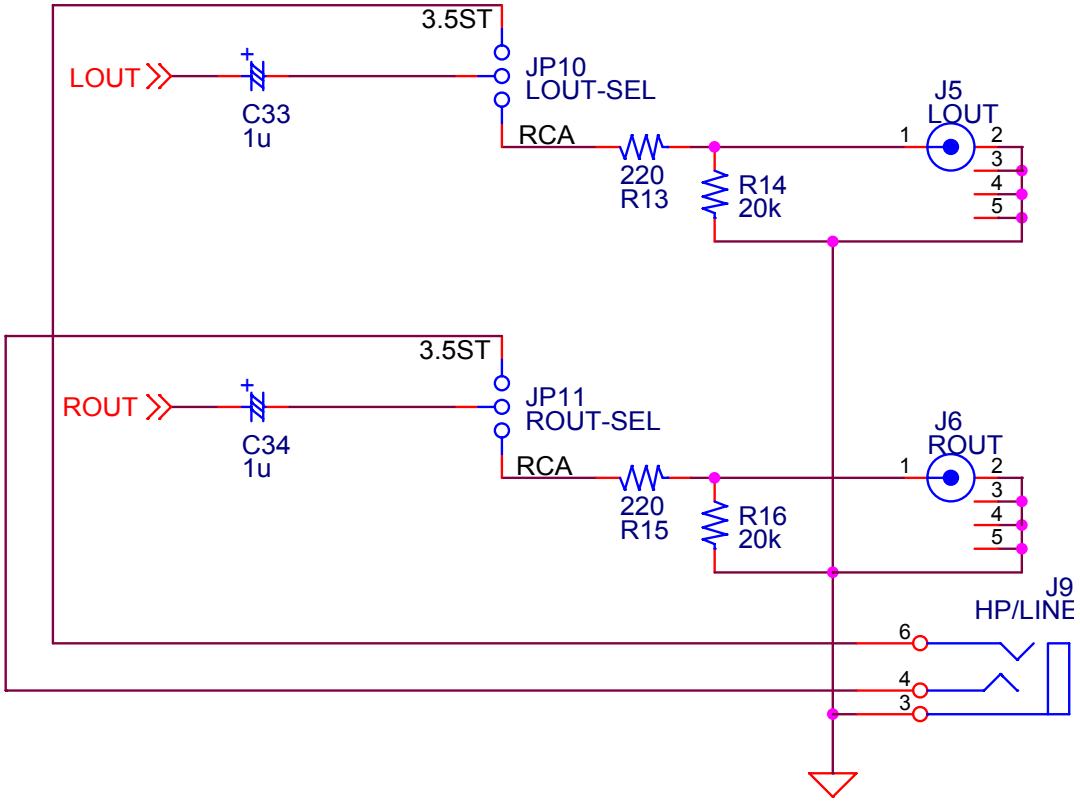
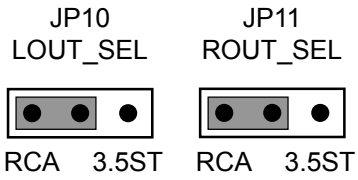
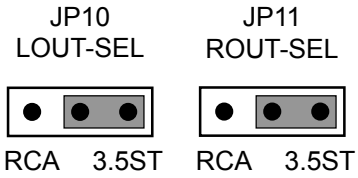


Figure 8. LOUT/ROUT Output Circuit

(2-1-1) In case that LOUT/ROUT is output from J5 and J6.



(2-1-2) In case that LOUT/ROUT is output from J9.



* J9 is shared with HPL/HPR.
When LOUT/ROUT is output from J9, JP12 and JP13 should be set to “RCA”.

(2-2) HPL/HPR Output Circuit

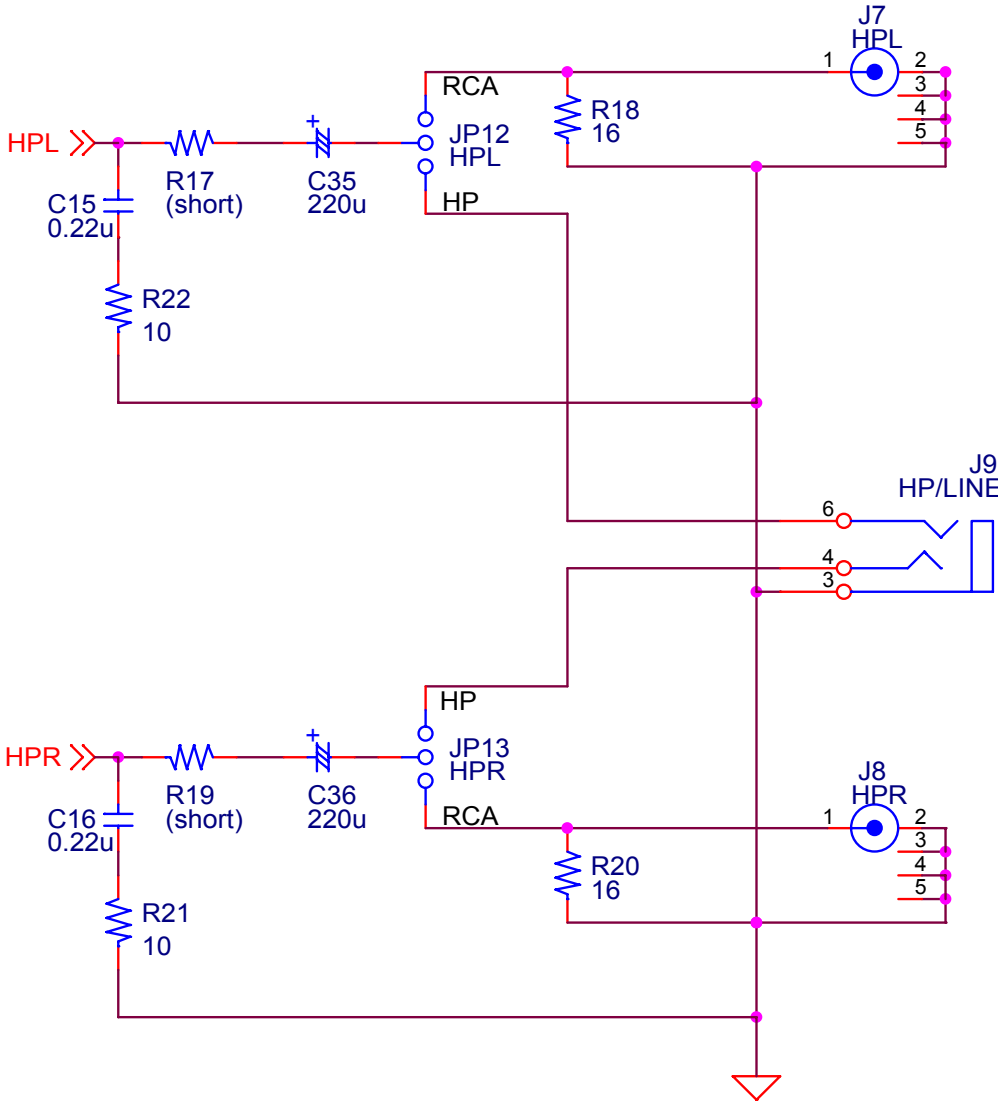
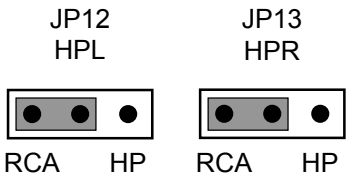
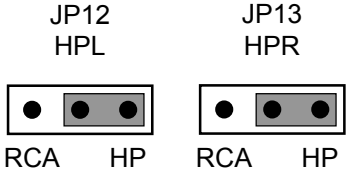


Figure 9. HPL/HPR Output Circuit

(2-2-1) In case that HPL/HPR is output from J7 and J8.



(2-2-2) In case that HPL/HPR is output from J9.

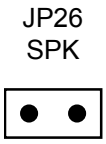


* J9 is shared with LOUT/ROUT.
When HPL/HPR is output from J9, JP10 and JP11 should be set to “RCA”.

(2-3) SPP/SPN Output Circuit

Figure 10. SPP/SPN Output Circuit

SPP/SPN is output from J10. JP26 should be set as the following.



* AKEMD assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4691 according to previous term.

2. Connect IBM-AT compatible PC with AKD4691 by 10-line type flat cable (packed with AKD4691). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4691 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4691.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default] : Initialize the register of AK4691.
3. [All Write] : Write all registers that is currently displayed.
4. [All Read] : Read all registers that is currently displayed.
5. [Function1] : Dialog to write data by keyboard operation.
6. [Function2] : Dialog to write data by keyboard operation.
7. [Function3] : The sequence of register setting can be set and executed.
8. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
9. [Function5] : The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
10. [SAVE] : Save the current register setting.
11. [OPEN] : Write the saved values to all register.
12. [Write] : Dialog to write data by mouse operation.
13. [Read] : Dialog to read data by mouse operation.
14. [Filter] : Set Programmable Filter (FIL1, FIL3, EQ) of AK4691 easily.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4691, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4691, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate Volume

There are dialogs corresponding to register of 0Ah, 0Bh, 0Ch and 0Dh.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4691 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4691, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4691. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

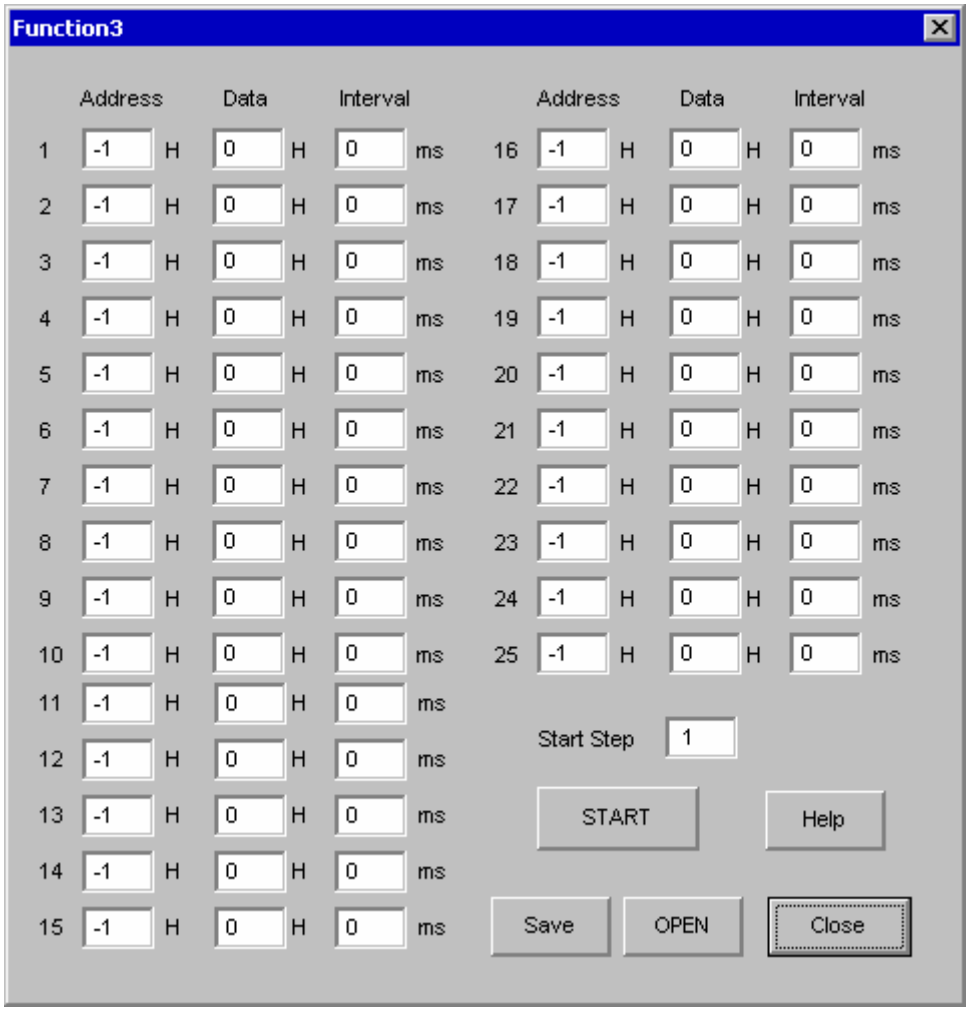


Figure 11. [F3] Window

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 12 opens.

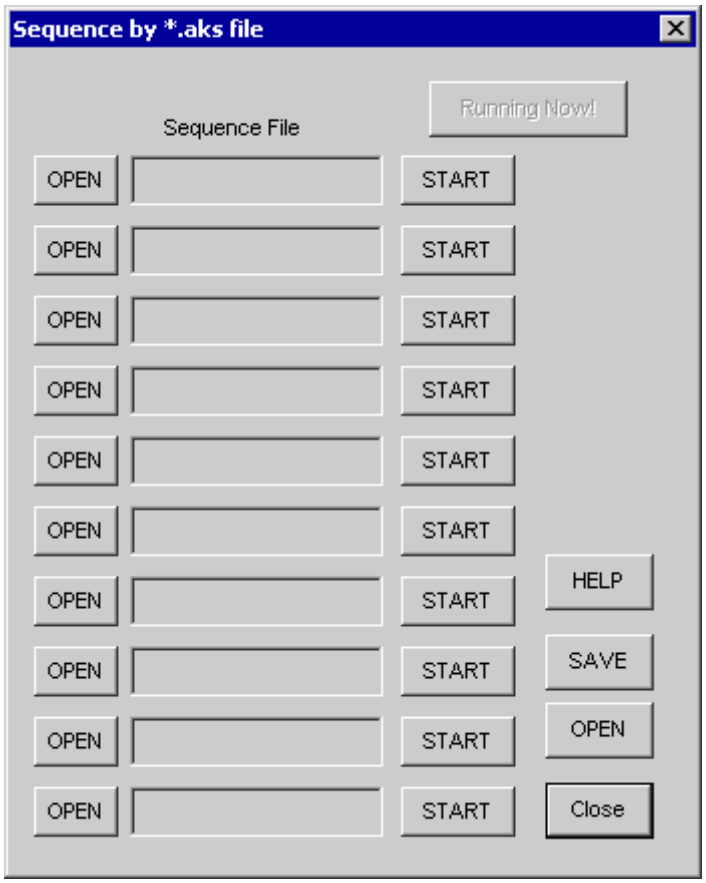


Figure 12. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 13. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

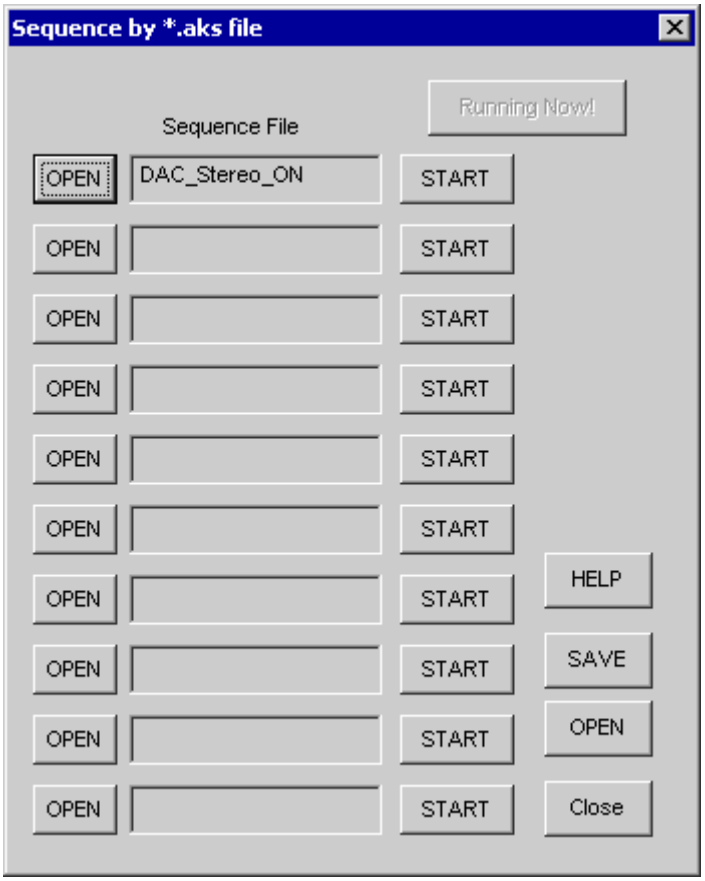


Figure 13. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 14 opens.

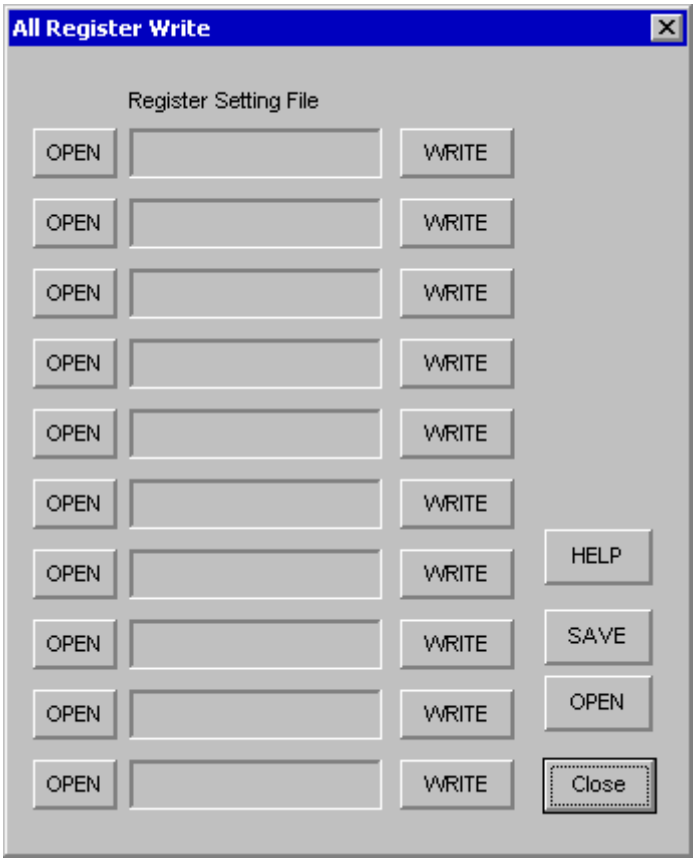


Figure 14. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 15. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

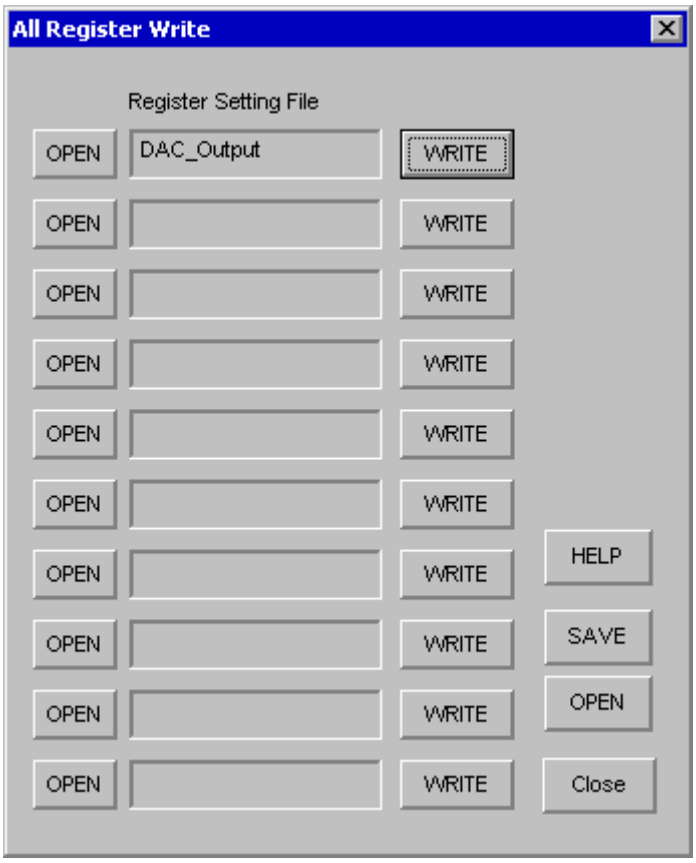


Figure 15. [F5] window (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

8. [Filter Dialog]

This dialog can calculate of a coefficient of Digital Programmable Filter (FIL1, FIL3 and EQ), write to a register and check frequency response.
Window as shown in Figure 16 opens when push a [Filter] button.

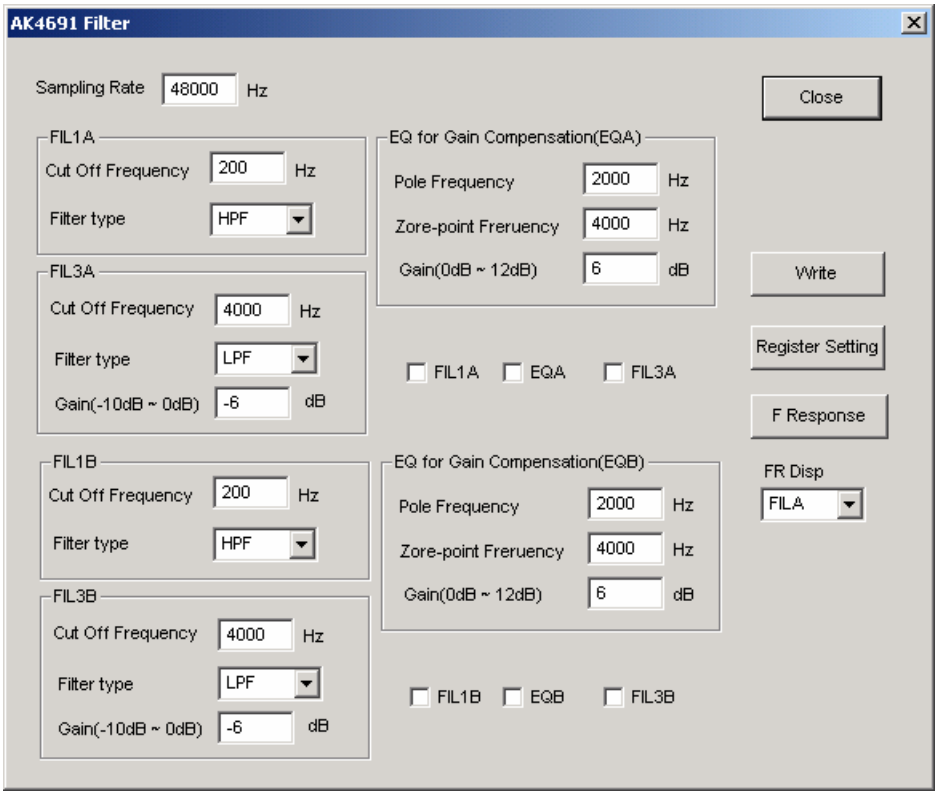


Figure 16. [Filter] window

8-1. Setting of a parameter

(1) Please set a parameter of each Filter.

[Sampling Rate] → Input value of sampling frequency [unit: Hz] <Default: 48000>
[FIL1A Cut Off Frequency] → Input value of cut off frequency of FIL1A [unit: Hz] <Default: 200>
[FIL3A Cut Off Frequency] → Input value of cut off frequency of FIL3A [unit: Hz] <Default: 4000>
[FIL3A GAIN] → Input value of gain of FIL3A (0~-10dB) [unit: dB] <Default: -6>
[EQA Pole Frequency] → Input value of pole frequency of EQA [unit: Hz] <Default: 2000>
[EQA Zero-point Frequency] → Input value of zero frequency of EQA [unit: Hz] <Default: 4000>
[EQA GAIN] → Input value of gain of EQA (+12~0dB) [unit: dB] <Default: 6>
[FIL1B Cut Off Frequency] → Input value of cut off frequency of FIL1B [unit: Hz] <Default: 200>
[FIL3B Cut Off Frequency] → Input value of cut off frequency of FIL3B [unit: Hz] <Default: 4000>
[FIL3B GAIN] → Input value of gain of FIL3B (0~-10dB) [unit: dB] <Default: -6>
[EQB Pole Frequency] → Input value of pole frequency of EQB [unit: Hz] <Default: 2000>
[EQB Zero-point Frequency] → Input value of zero frequency of EQB [unit: Hz] <Default: 4000>
[EQB GAIN] → Input value of gain of EQB (+12~0dB) [unit: dB] <Default: 6>

(2) Please set a filter type of FIL1 and FIL3.
Select “LPF” or “HPF” from [Filter type] of FIL1A, FIL3A, FIL1B and FIL3B.

(3) Please set ON/OFF of “FIL1A”, “FIL3A”, “EQA”, “FIL1B”, “FIL3B”, “EQB” with a check button. When checked it, the filter becomes ON.

8-2. A calculation of a register

A register value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and, a calculation of register setting is not carried out.

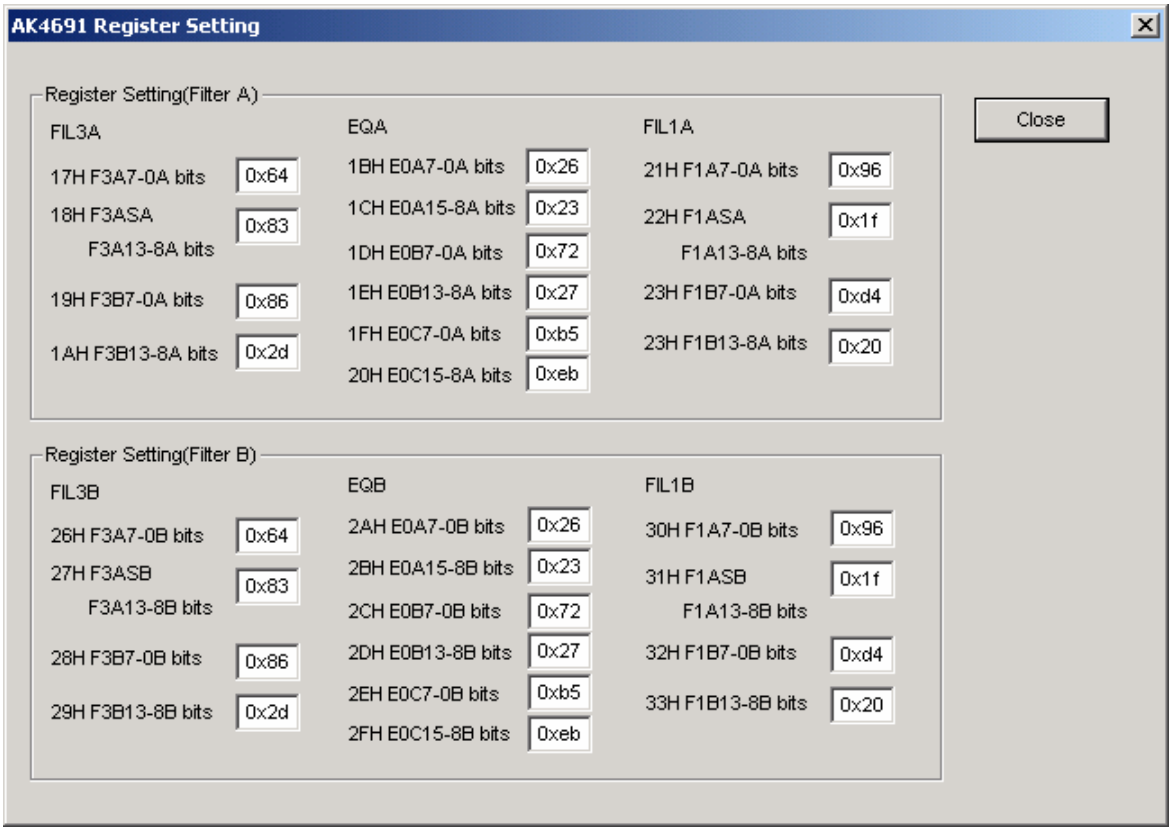


Figure 17. A register setting calculation result

When it is as follows that a register value is updated.
(1) When [Register Setting] button was pushed.
(2) When [F Response] button was pushed.
(3) When [UpDate] button on a frequency characteristic indication window was pushed.

8-3.Indication of a frequency characteristic

A frequency characteristic is displayed after a [Frequency Response] button is pushed. A register value is also updated.
After "Frequency Range" is changed and a [UpDate] button is pushed, indication of a frequency characteristic is updated.

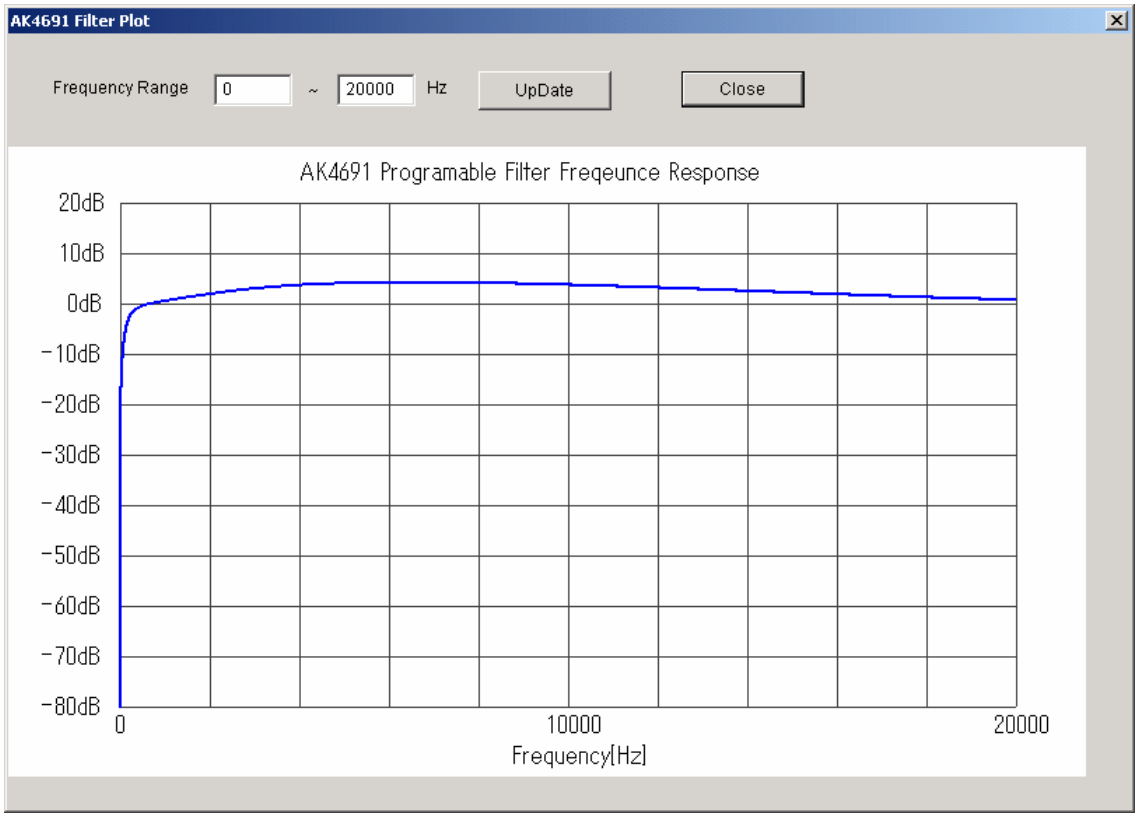


Figure 18. A frequency characteristic indication result

When it is as follows that a register value is updated.
(1) When [Register Setting] button was pushed.
(2) When [F Response] button was pushed.
(3) When [UpDate] button on a frequency characteristic indication window was pushed.

Measurement Result

[Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCKI : 256fs (12.288MHz)
- BICK : 64fs
- fs : 48kHz
- Bit : 16bit
- Measurement Mode : EXT Slave Mode
- Power Supply : AVDD=DVDD=MVDD=LVDD=SVDD=TVDD1=TVDD2=3.0V
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz
- Temperature : Room

[Measurement Results]

1. ADC1

	Result		Unit
	Lch	Rch	
ADC: LIN/RIN → ADC1, IVOL=0dB			
S/(N+D) (-1dBFS)	89.8	90.2	dB
DR (-60dBFS, A-Weighted)	94.5	94.5	dB
S/N (A-weighted)	94.6	94.6	dB

2. ADC2

	Result		Unit
	Lch	Rch	
INTL2/INTR2 → ADC2, Pre-Amp Gain=+24dB, IVOL=+29.625dB			
S/(N+D) (-1dBFS)	87.5	86.5	dB
DR IVOL=0dB, (-60dBFS, A-Weighted)	62.1	62.2	dB
S/N (A-weighted)	62.1	62.2	dB

3. DAC

	Result		Unit
	Lch	Rch	
DAC: DAC → LOUT/ROUT, IVOL=DVOL=LVOL=0dB, RL=10kΩ			
S/(N+D) (0dBFS)	86.2	86.1	dB
DR (-60dBFS, A-Weighted)	89.5	89.6	dB
S/N (A-weighted)	90.2	90.2	dB
Headphone-Amp: DAC → HPL/HPR, IVOL=DVOL=0dB, RL=22.8Ω, HPG bit = "0"			
S/(N+D) (-3dBFS)	72.5	72.2	dB
DR (-60dBFS, A-Weighted)	89.5	89.4	dB
S/N (A-weighted)	90.3	90.3	dB
Speaker-Amp: DAC → SPP/SPN, IVOL=DVOL=0dB, RL=8Ω			
S/(N+D) SPKG=+10.65dB, (-3dBFS)	61.3		dB
S/N (A-Weighted)	89.7		dB

[Plot Data]

1. ADC (LIN/RIN → ADC, IVOL=0dB)

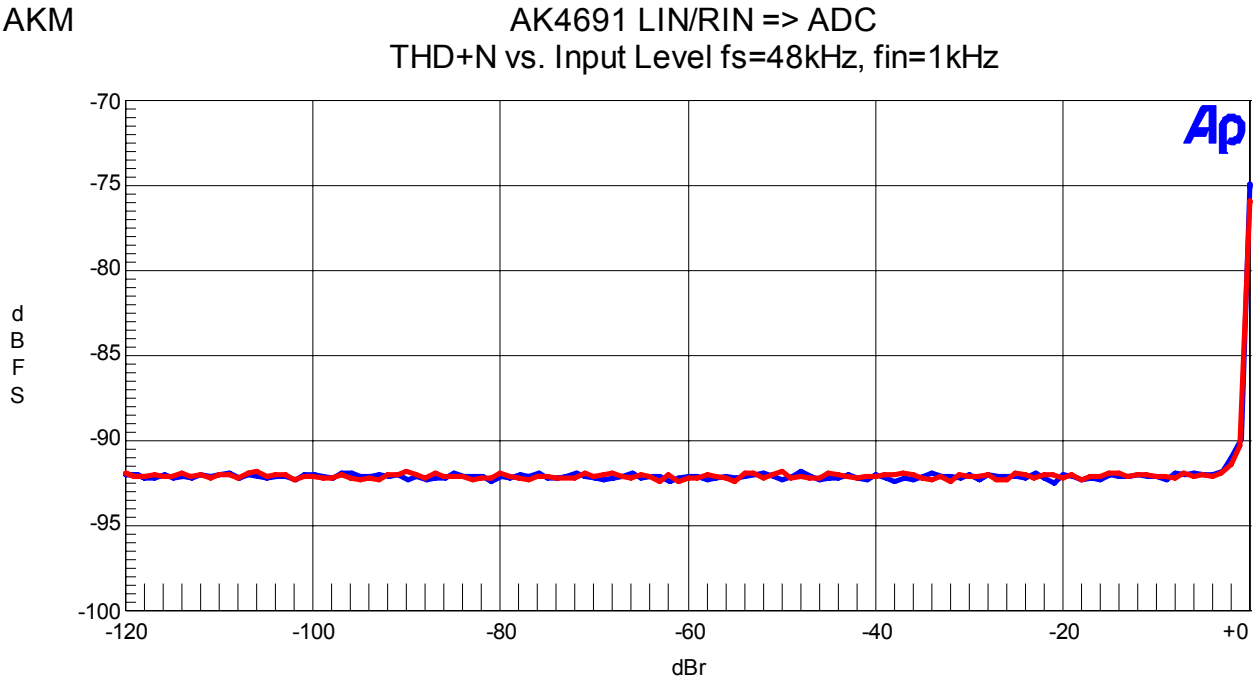


Figure 19. THD+N vs. Input Level

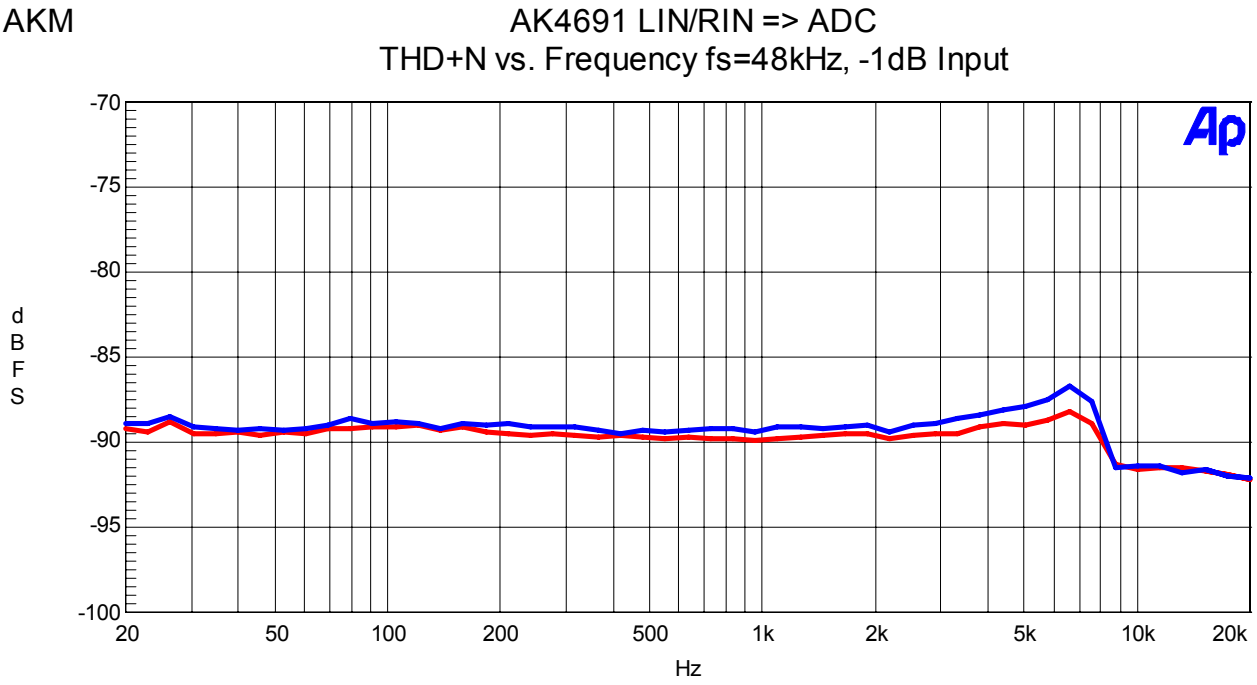


Figure 20. THD+N vs. Input Frequency

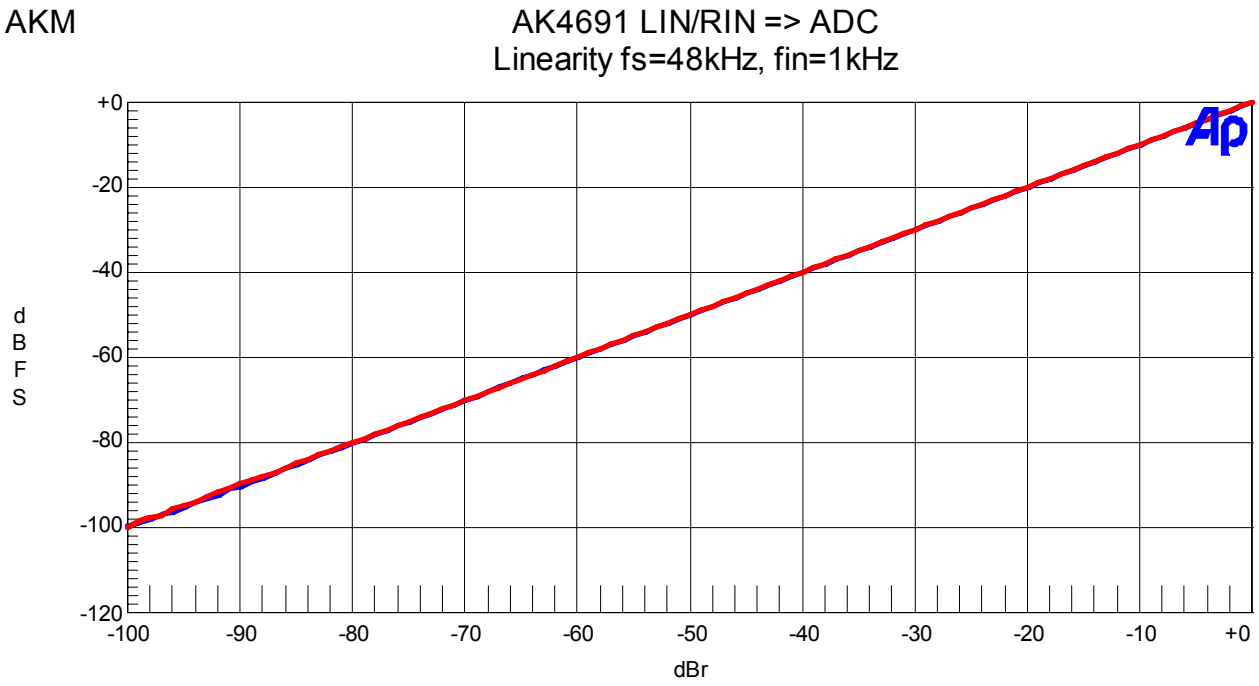


Figure 21. Linearity

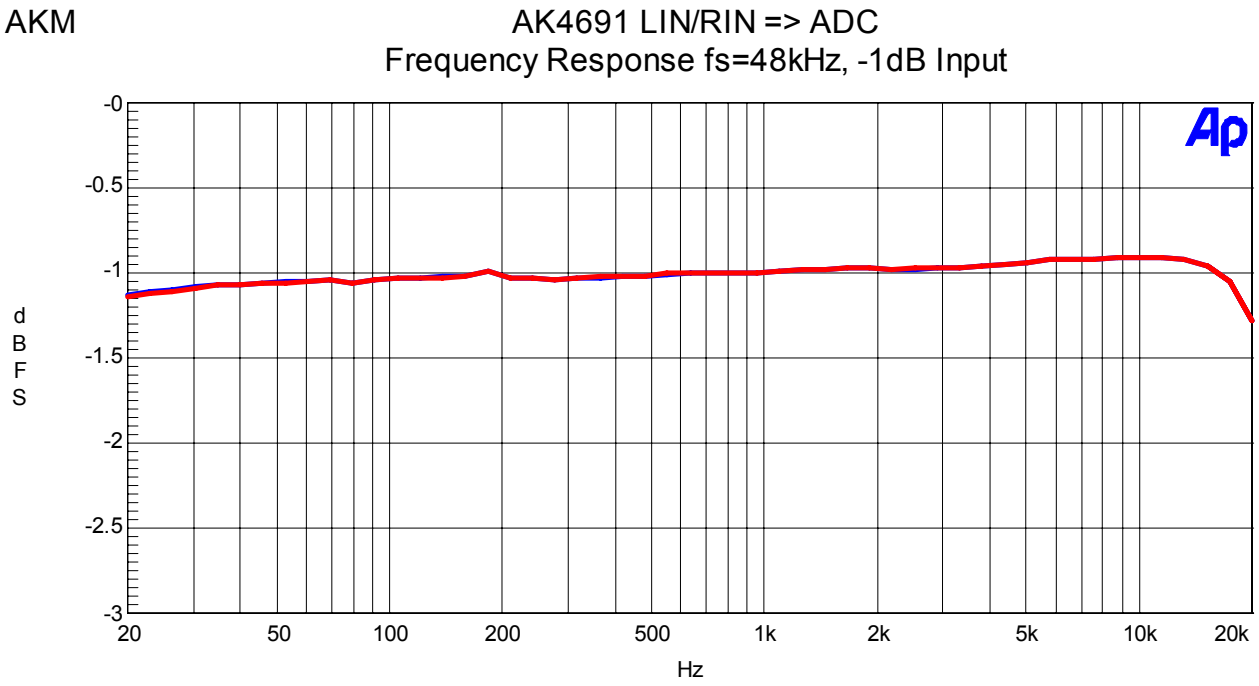


Figure 22. Frequency Response

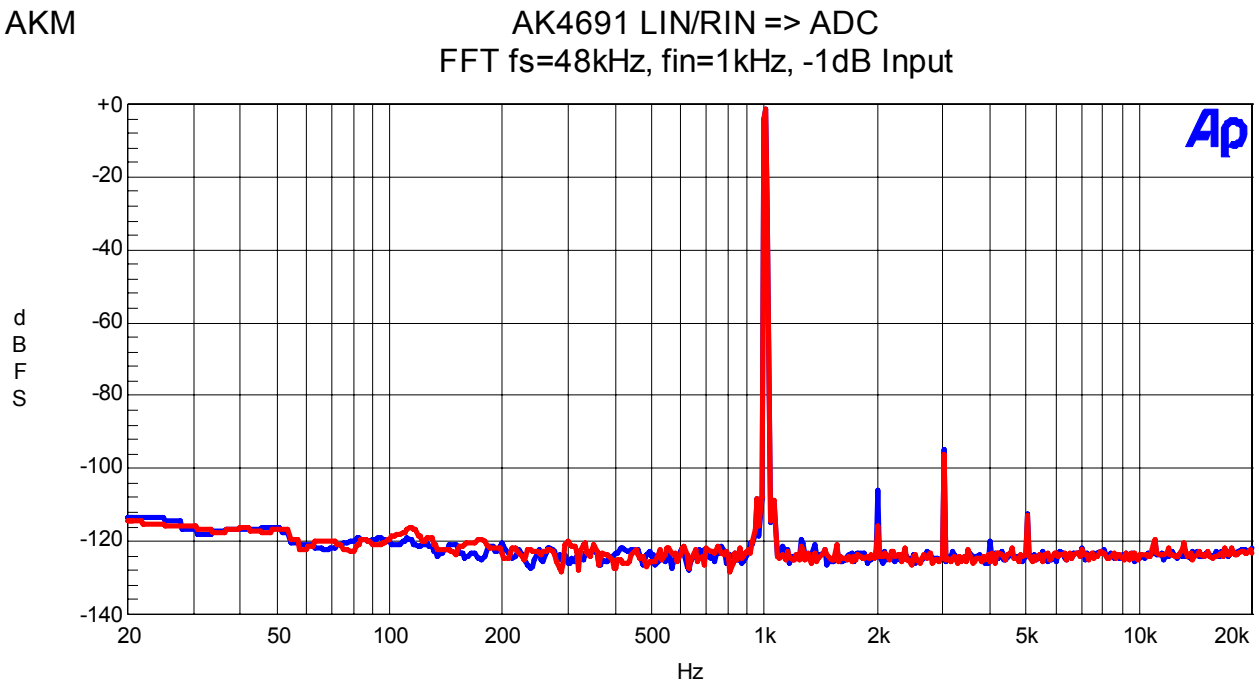


Figure 23. FFT (1kHz, -1dBFS)

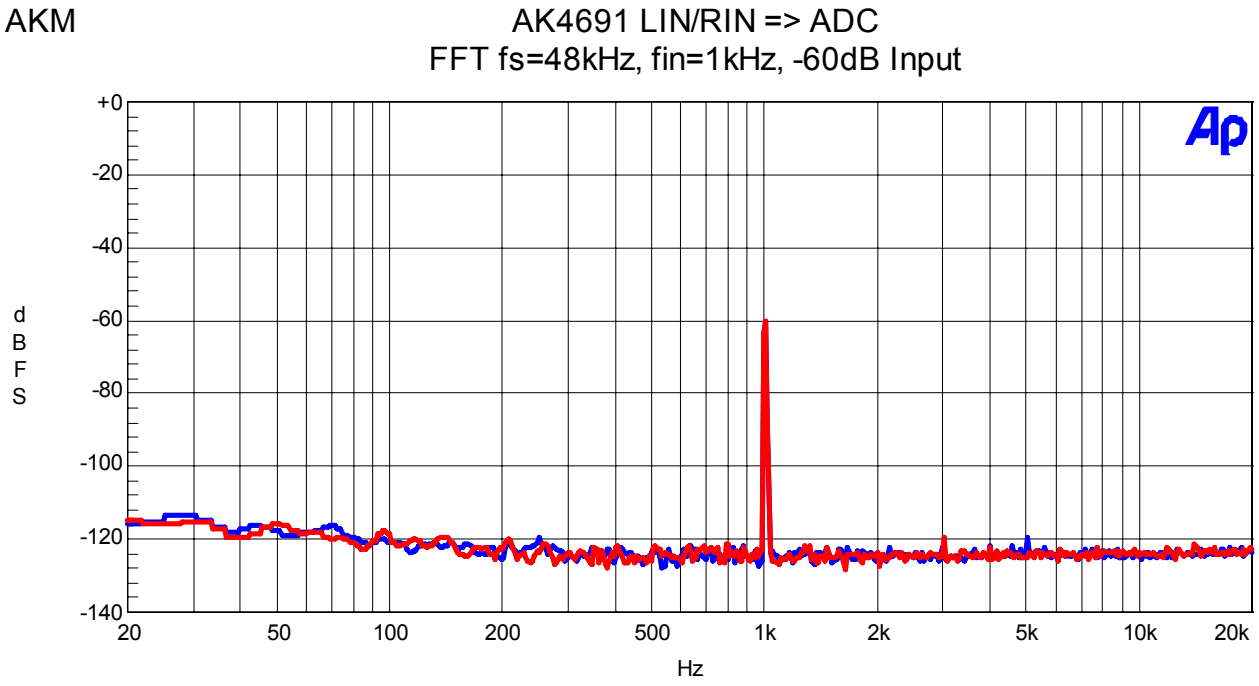


Figure 24. FFT (1kHz, -60dBFS)

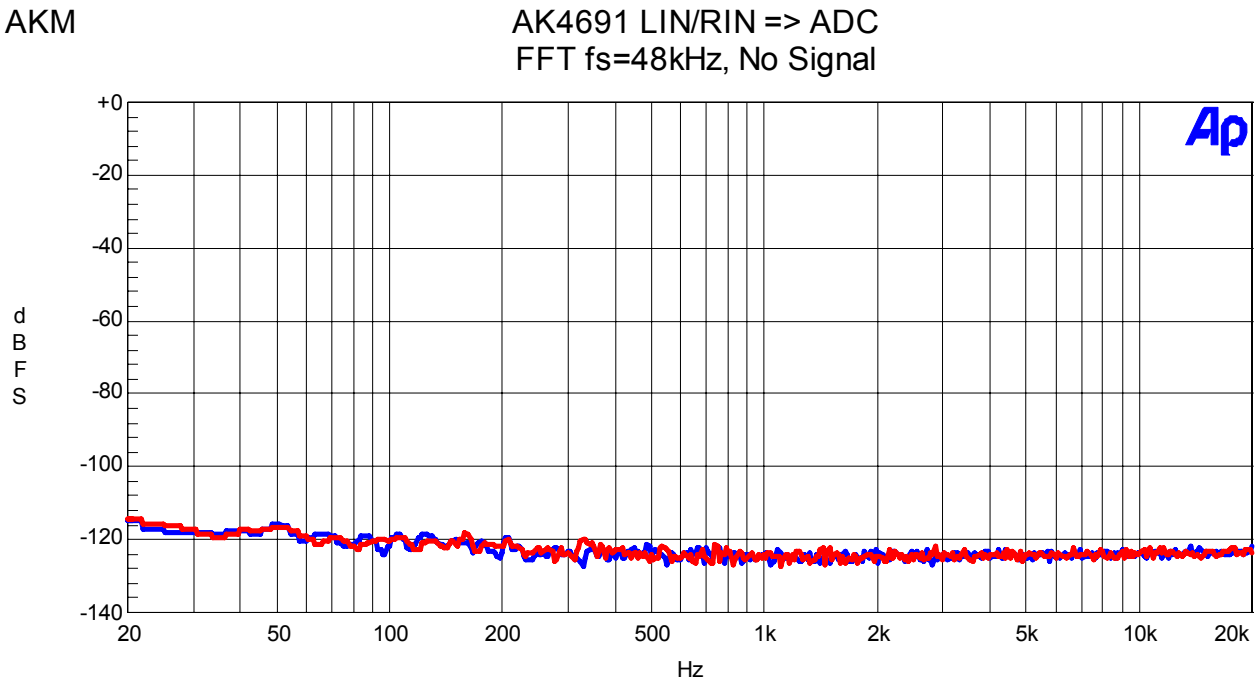


Figure 25. FFT (Noise Floor)

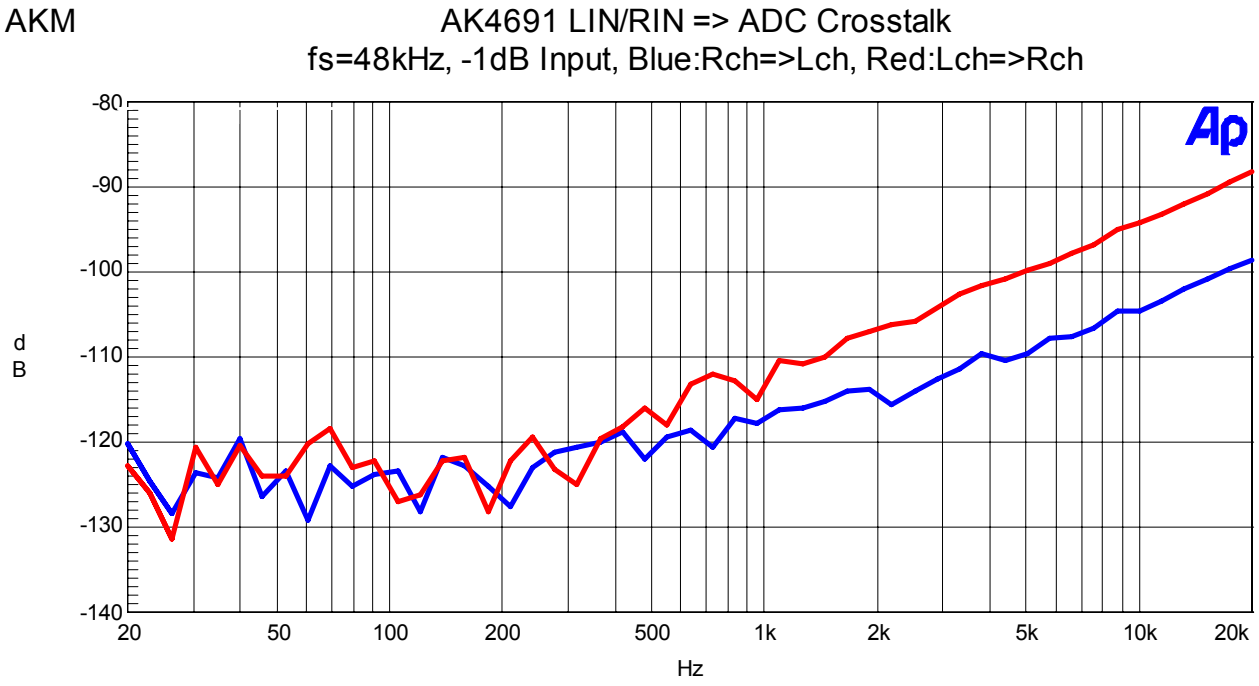


Figure 26. Crosstalk

2. ADC (INTL1/INTR1 → ADC, INTL2/INTR2 → ADC, Pre-Amp Gain=+24dB, IVOL=0dB)

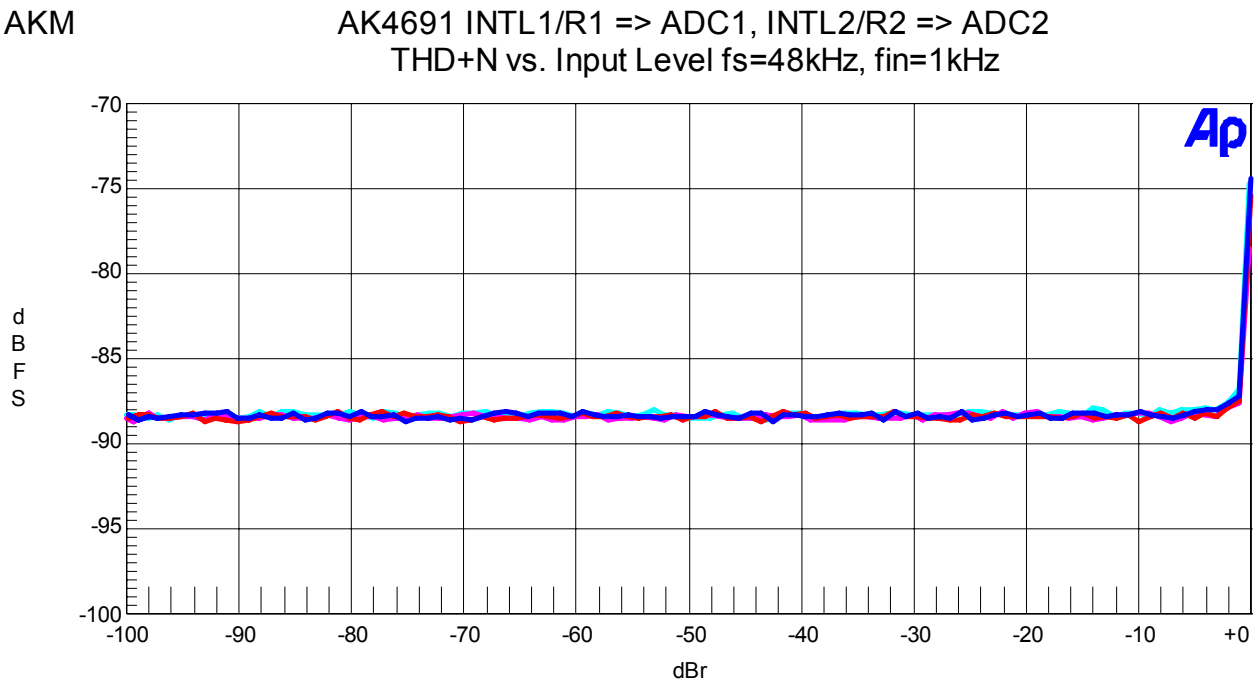


Figure 27. THD+N vs. Input Level

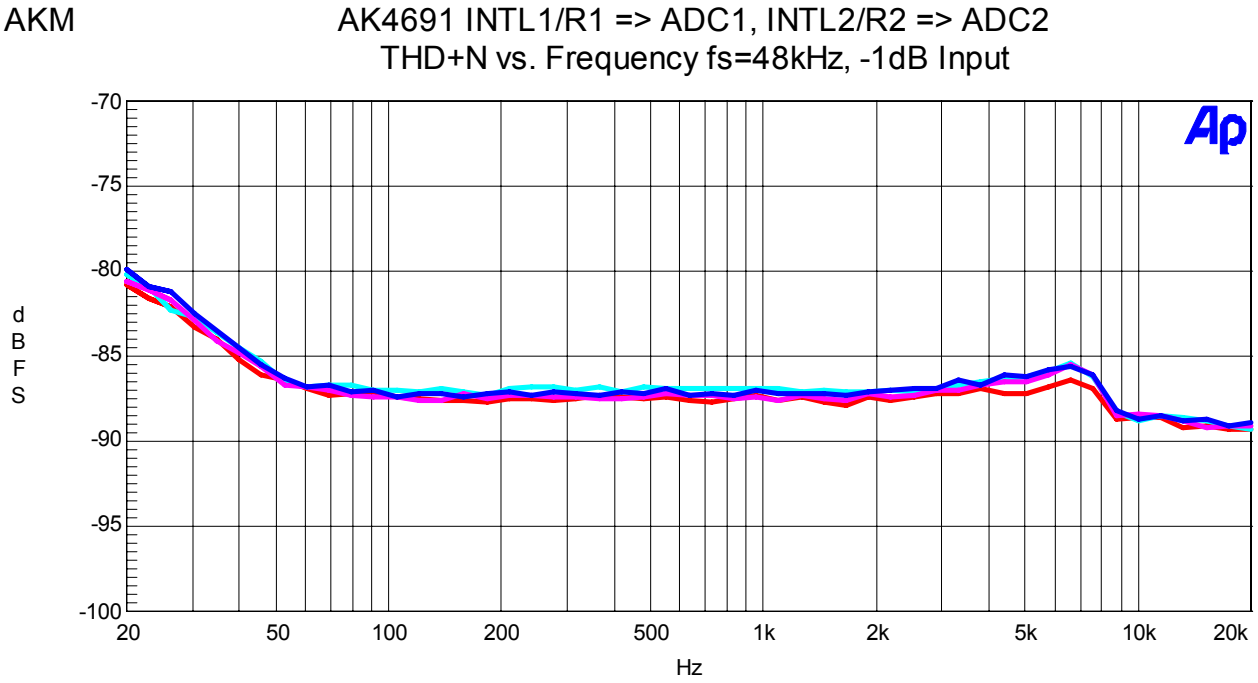


Figure 28. THD+N vs. Input Frequency

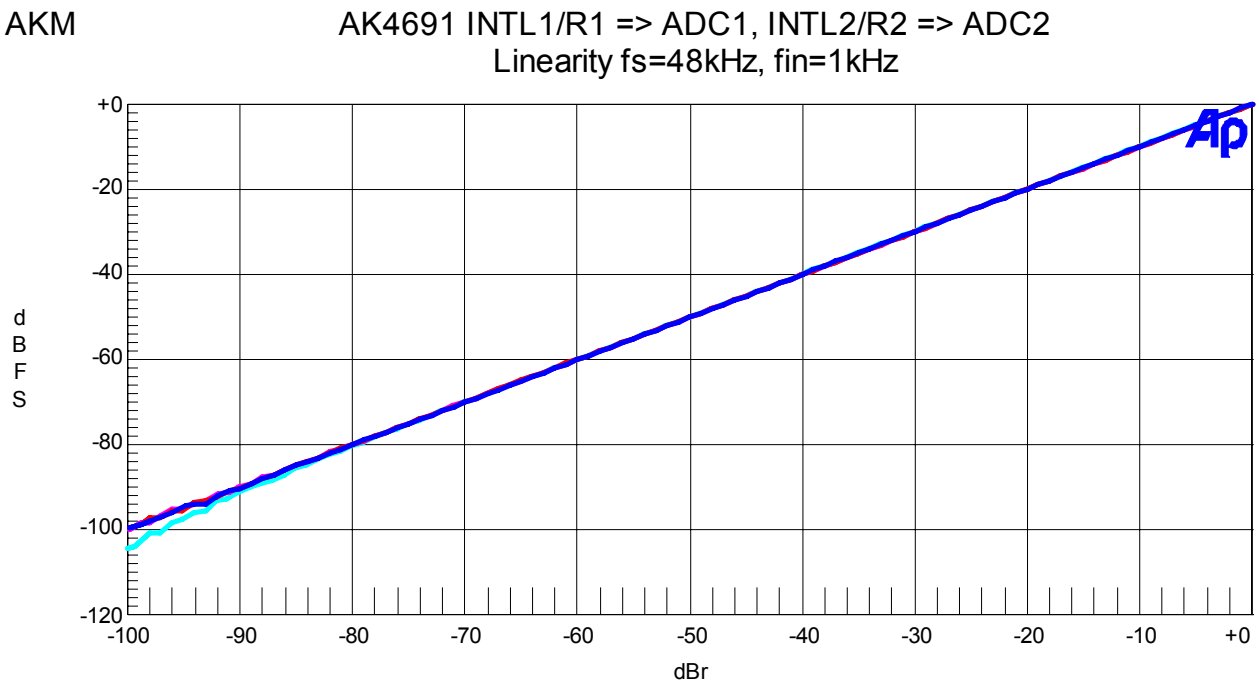
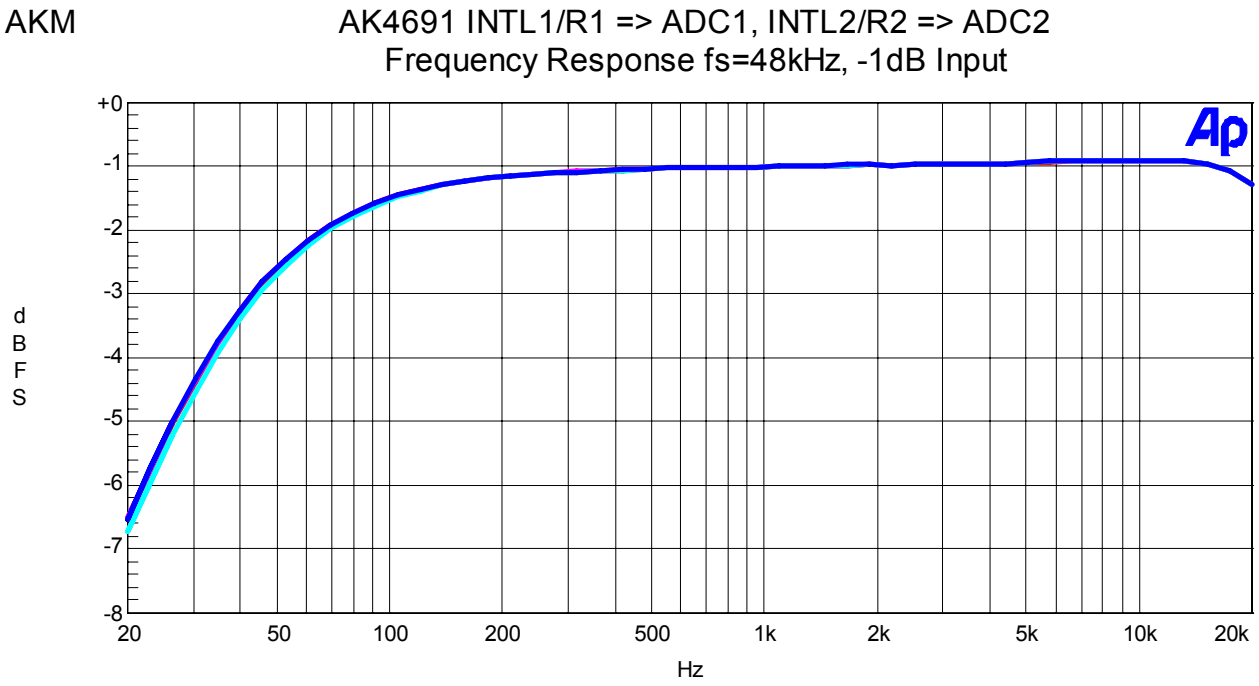


Figure 29. Linearity



*Positive Input: C=1µF, Ri=100kΩ(Ext HPF: fc=1.6Hz); Negative Input: C=2.2µF, Rn=2.2kΩ(Ext HPF: fc=33Hz)
Figure 30. Frequency Response

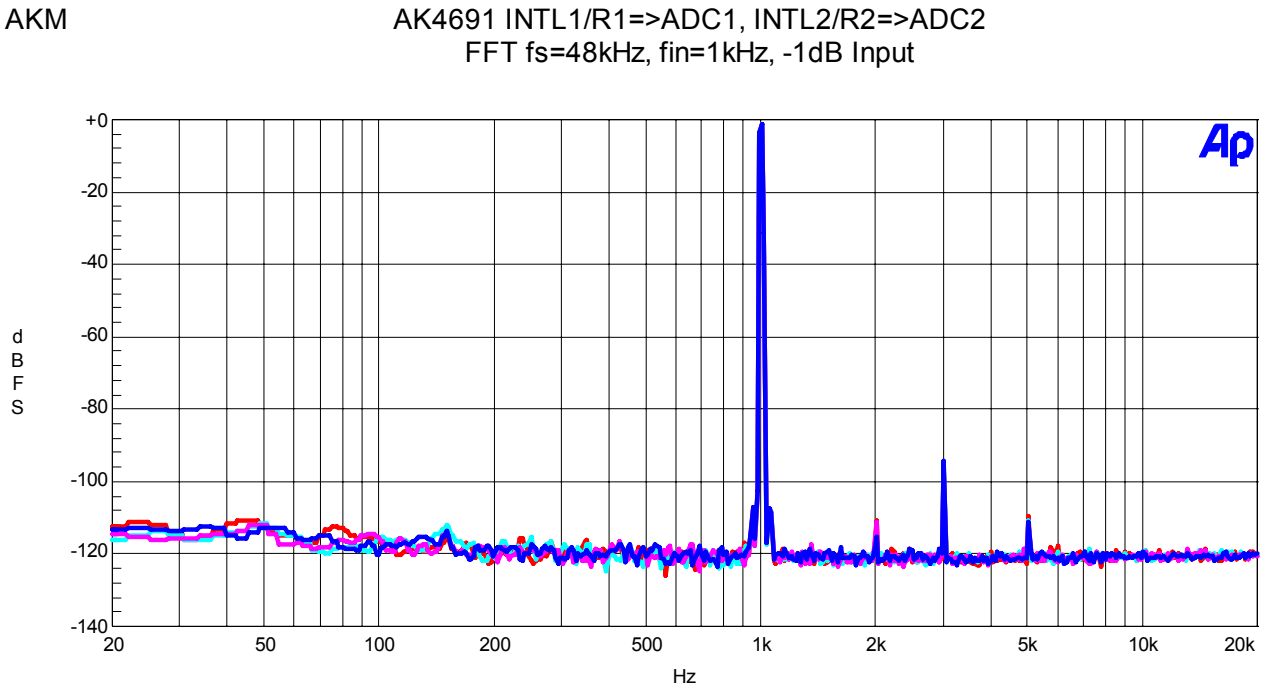


Figure 31. FFT (1kHz, -1dBFS)

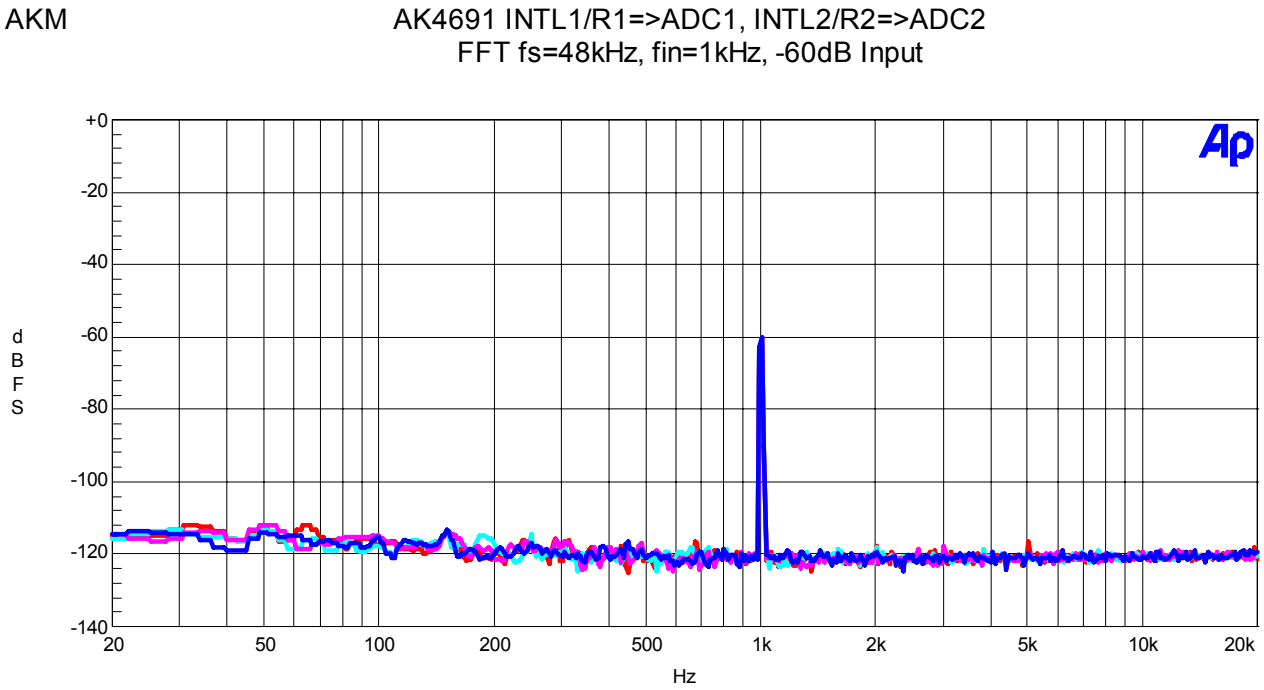


Figure 32. FFT (1kHz, -60dBFS)

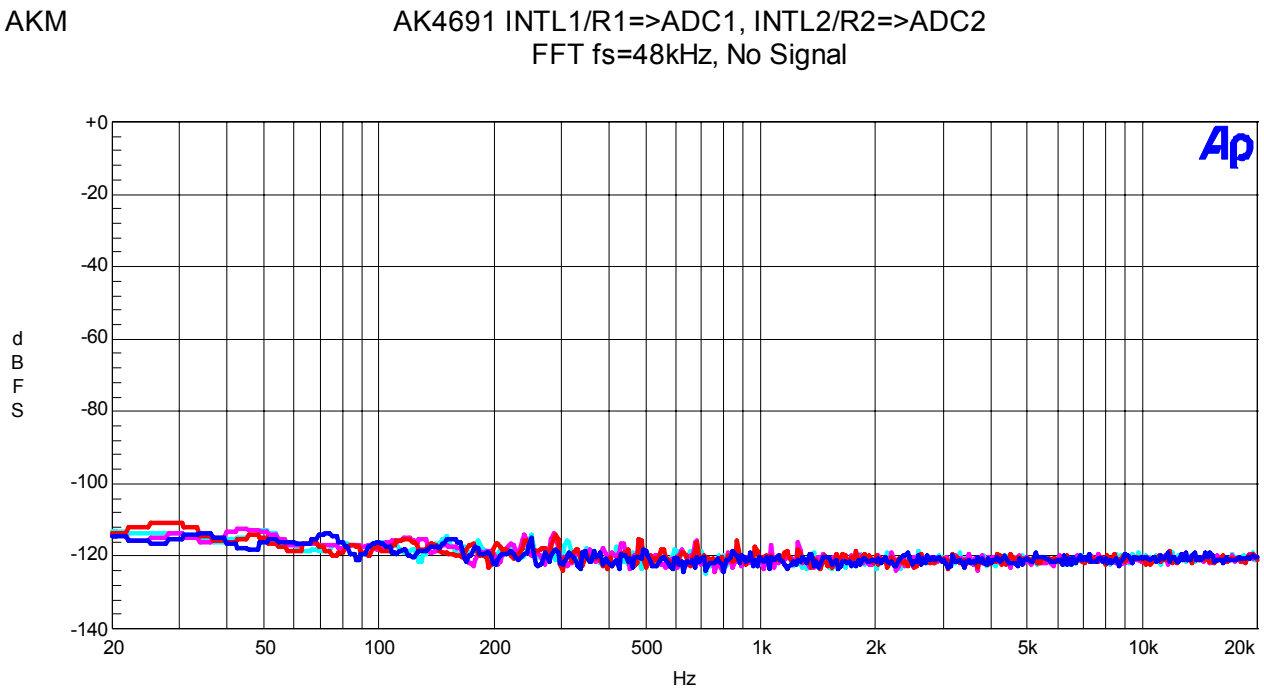


Figure 33. FFT (Noise Floor)

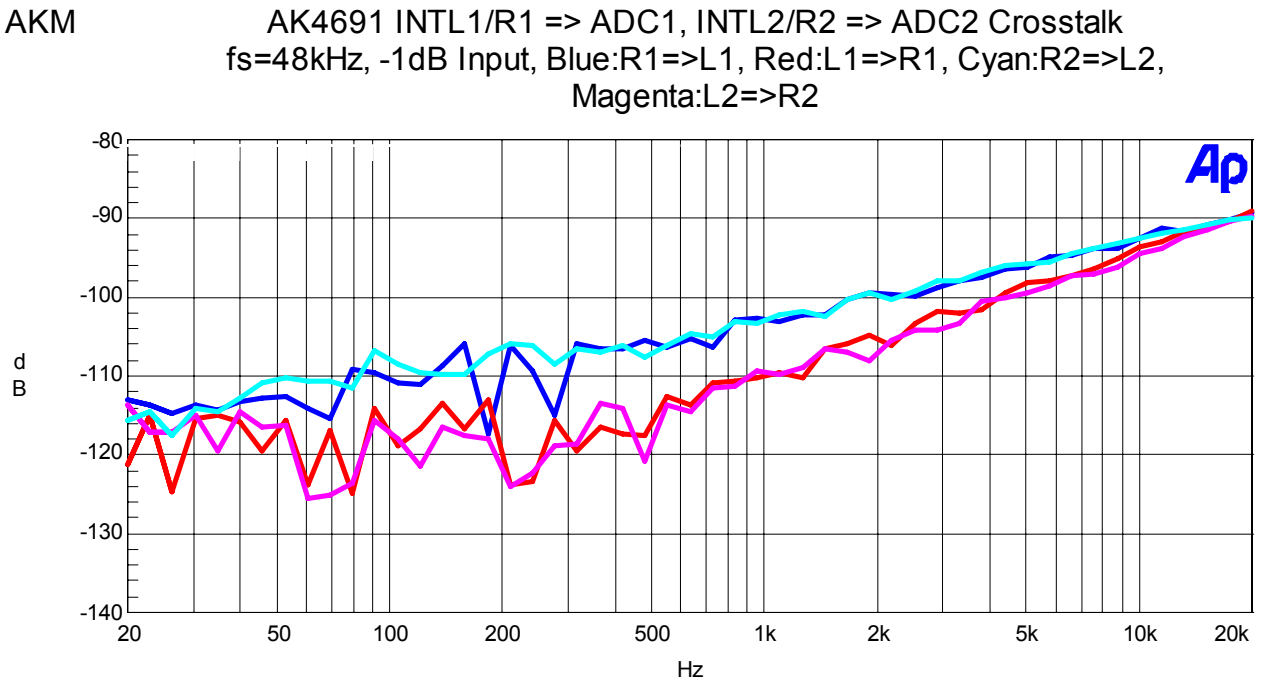


Figure 34. Crosstalk

3. DAC (DAC → LOUT/ROUT)

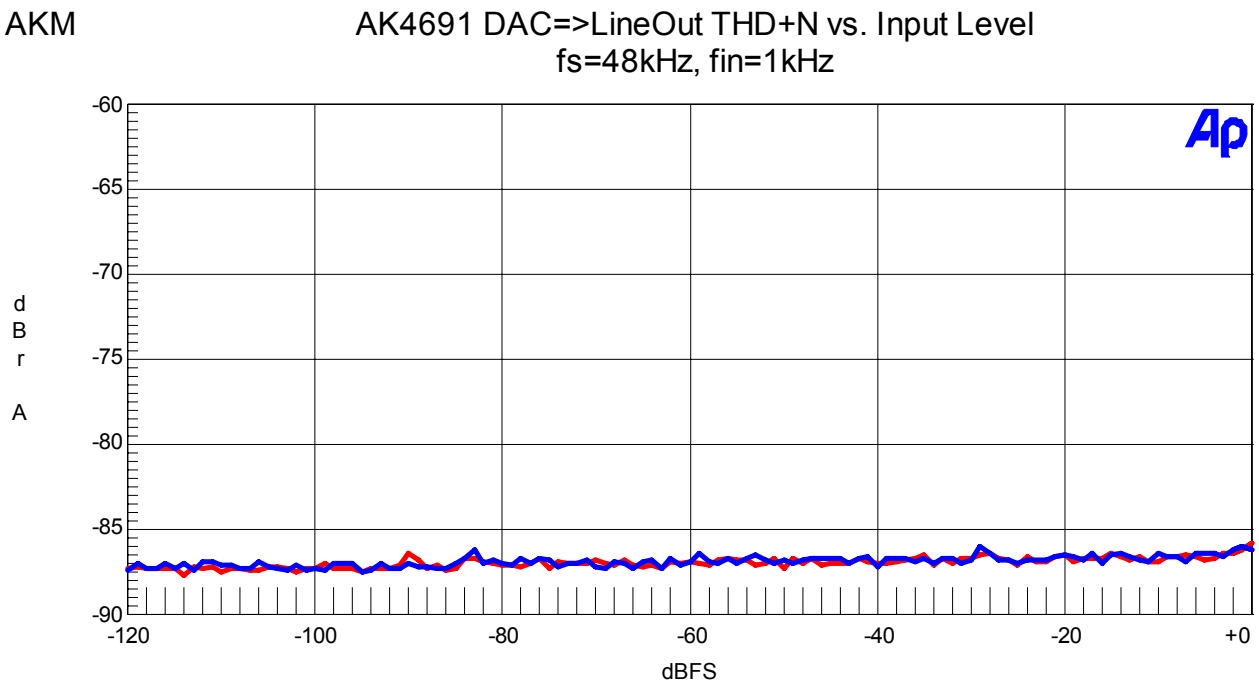


Figure 35. THD+N vs. Input Level

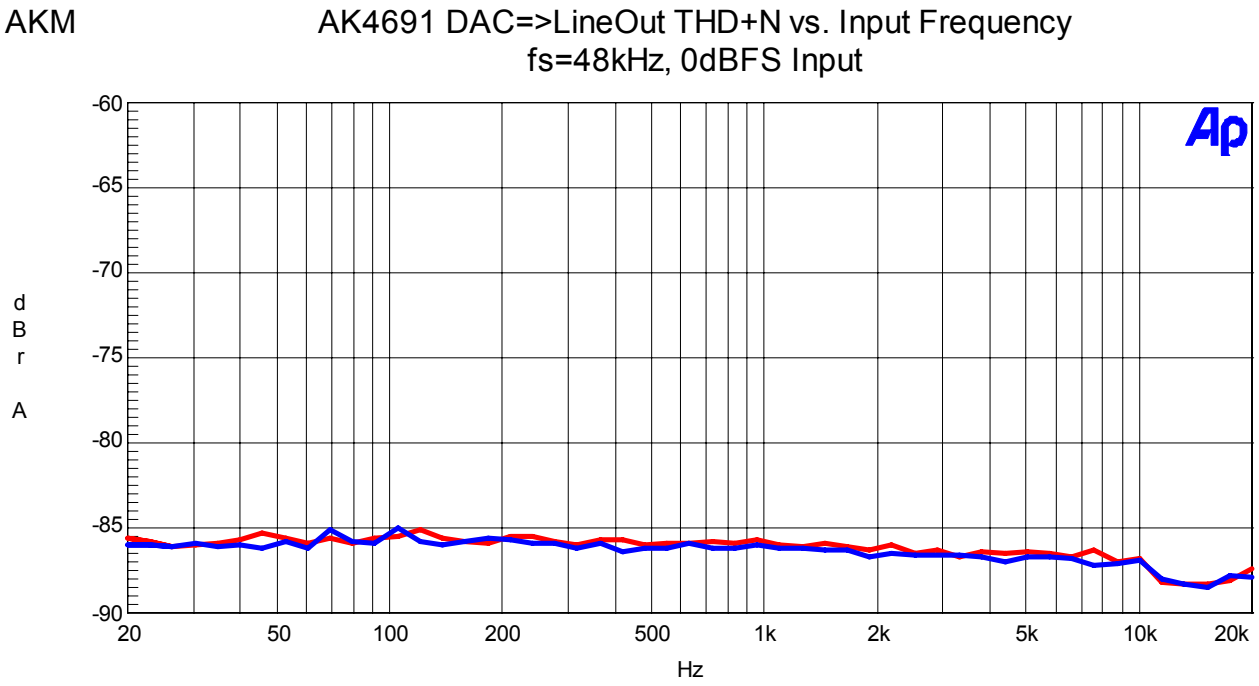


Figure 36. THD+N vs. Input Frequency

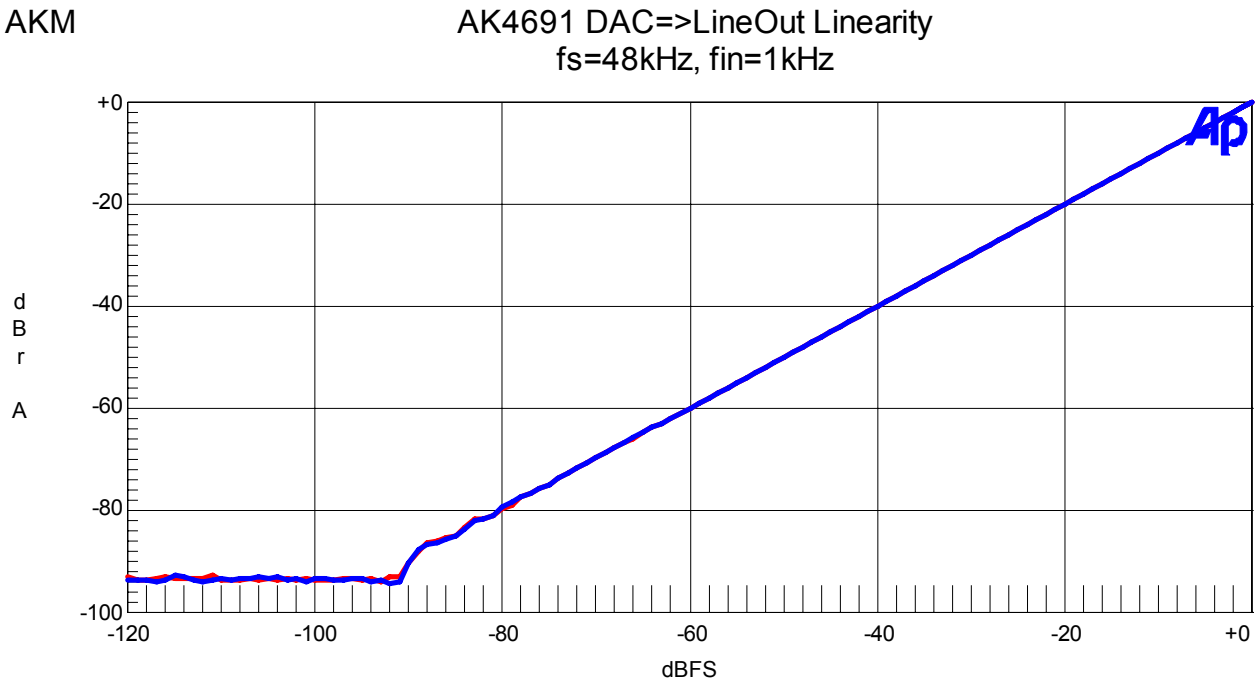
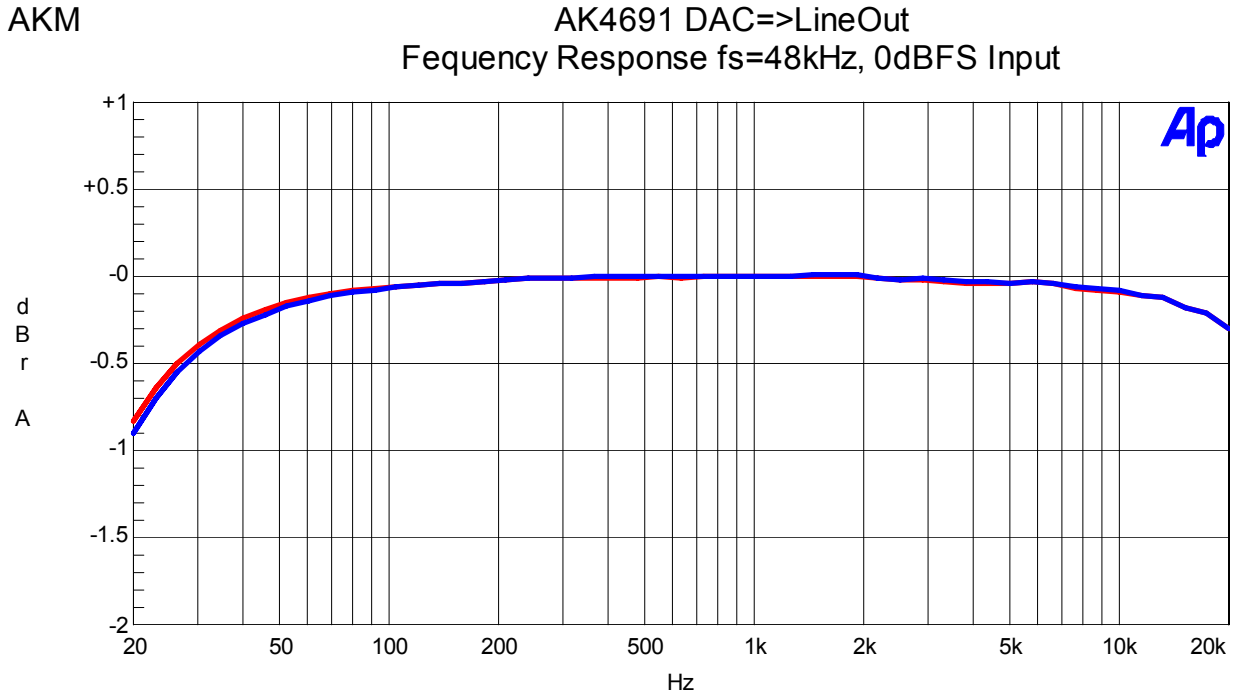


Figure 37. Linearity



*Line Out: C=1μF, Rseries=220Ω, RL=20kΩ(Ext HPF: fc=7.9Hz)
Figure 38. Frequency Response

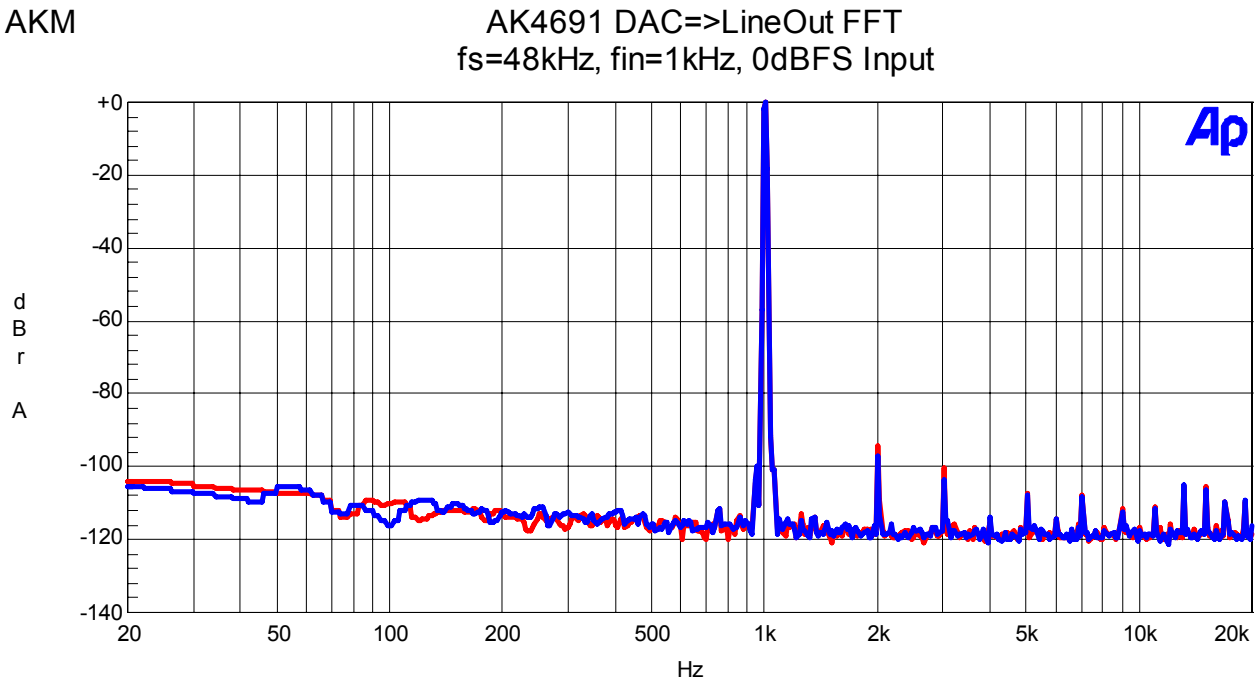


Figure 39. FFT (1kHz, 0dBFS)

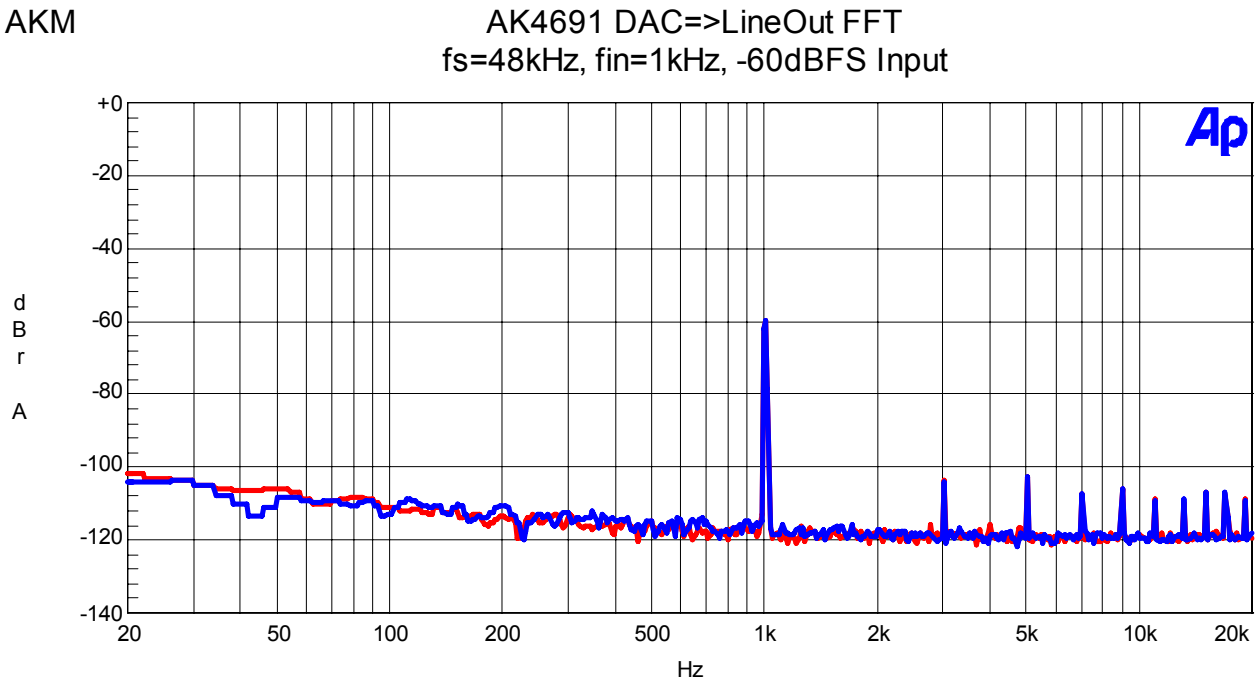


Figure 40. FFT (1kHz, -60dBFS)

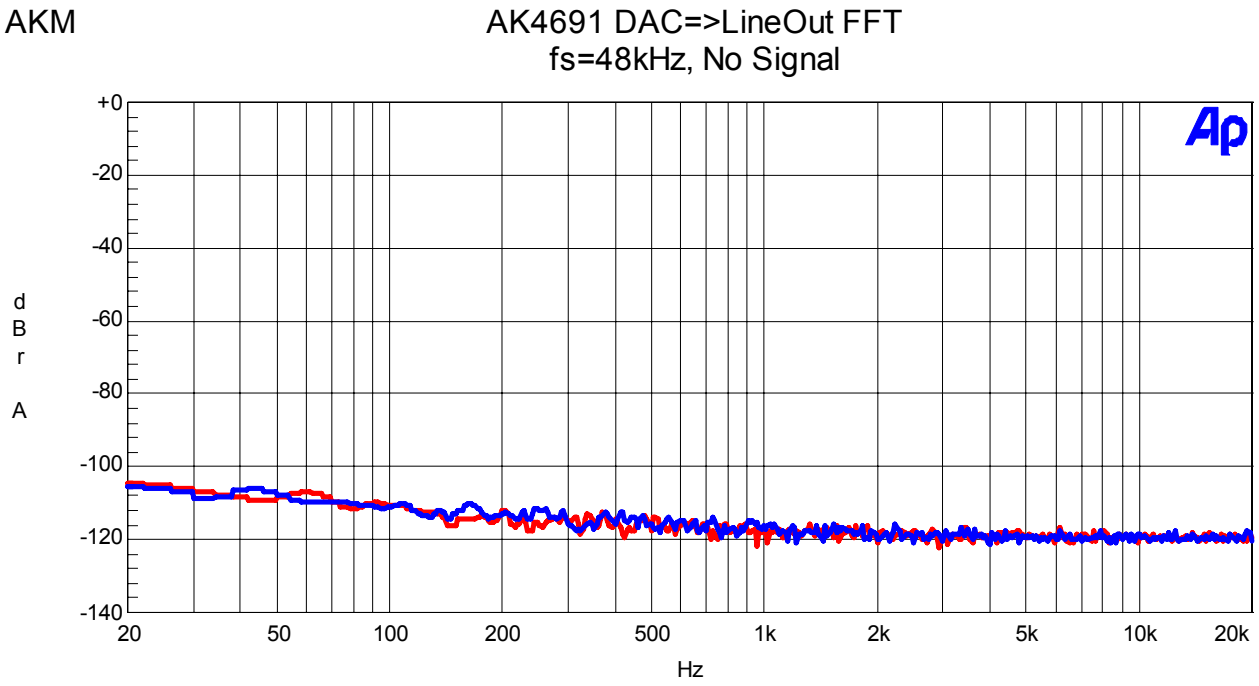


Figure 41. FFT (Noise Floor)

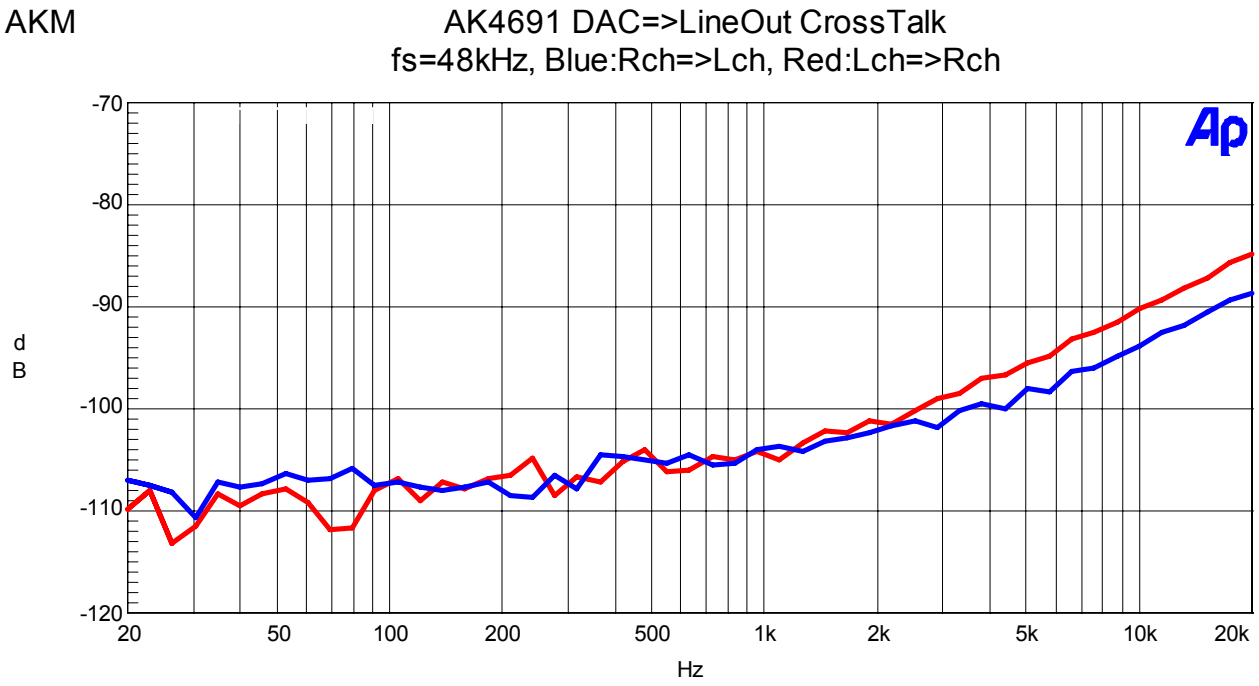


Figure 42. Crosstalk

4. Headphone (DAC → HPL/HPR)

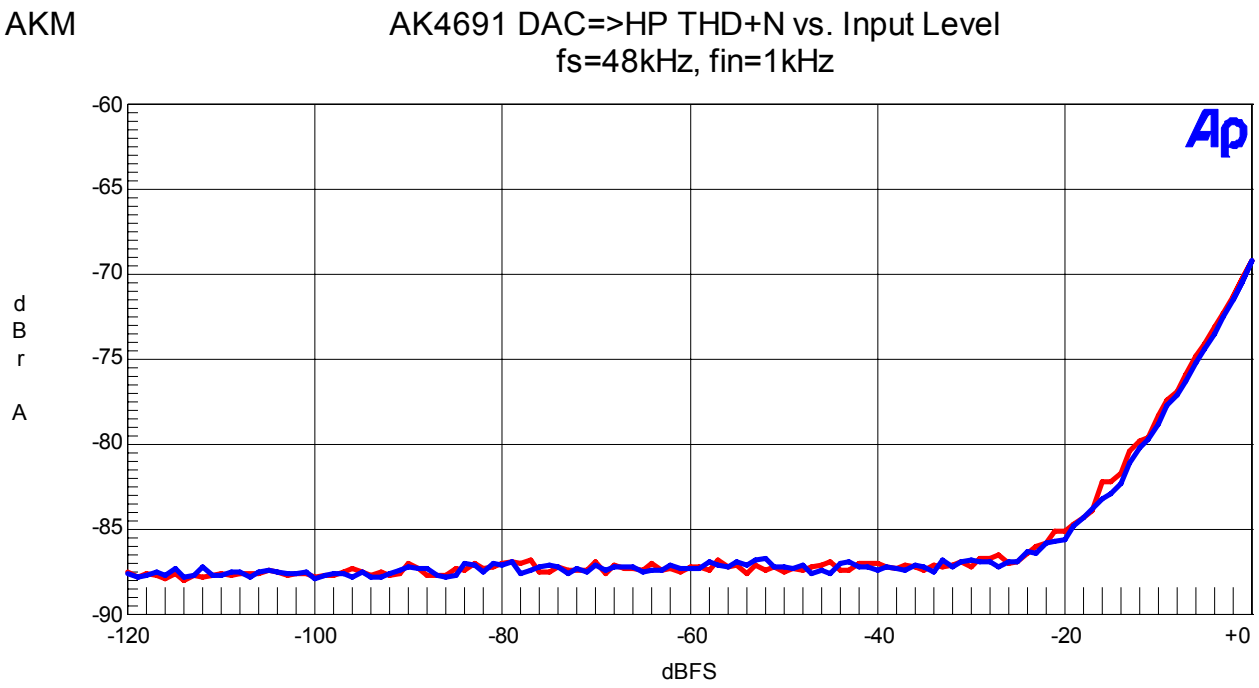


Figure 43. THD+N vs. Input Level

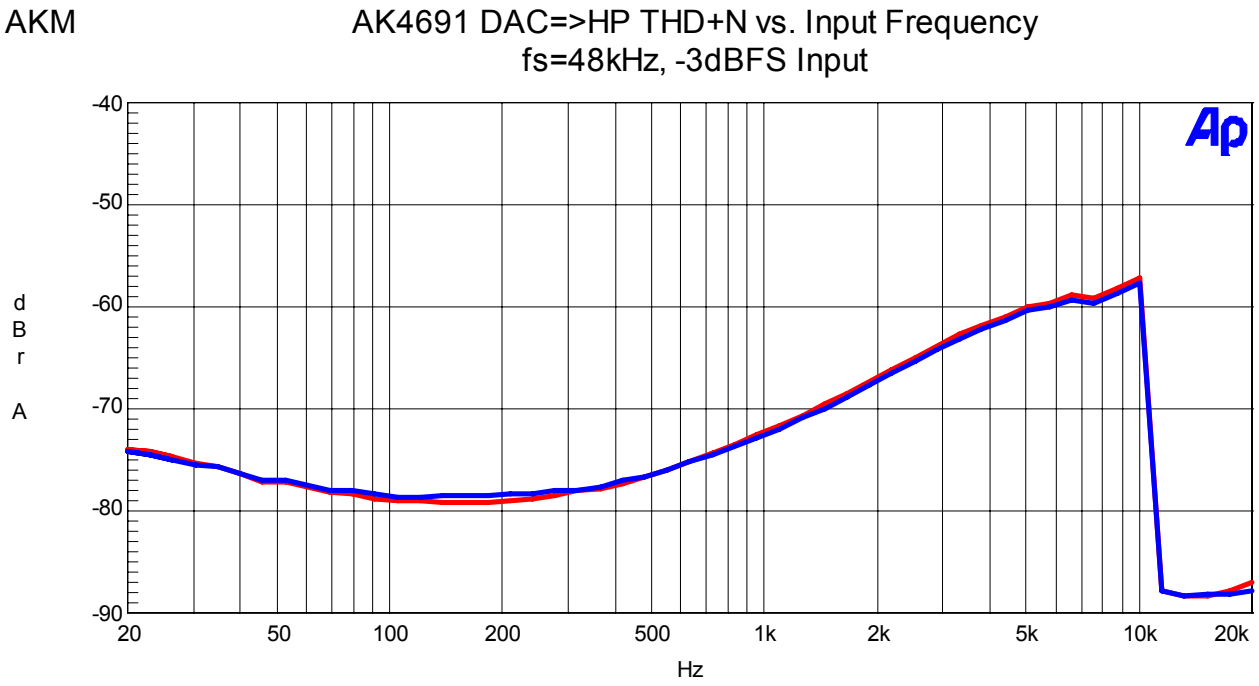


Figure 44. THD+N vs. Input Frequency (Filter: 20kHz AES17)

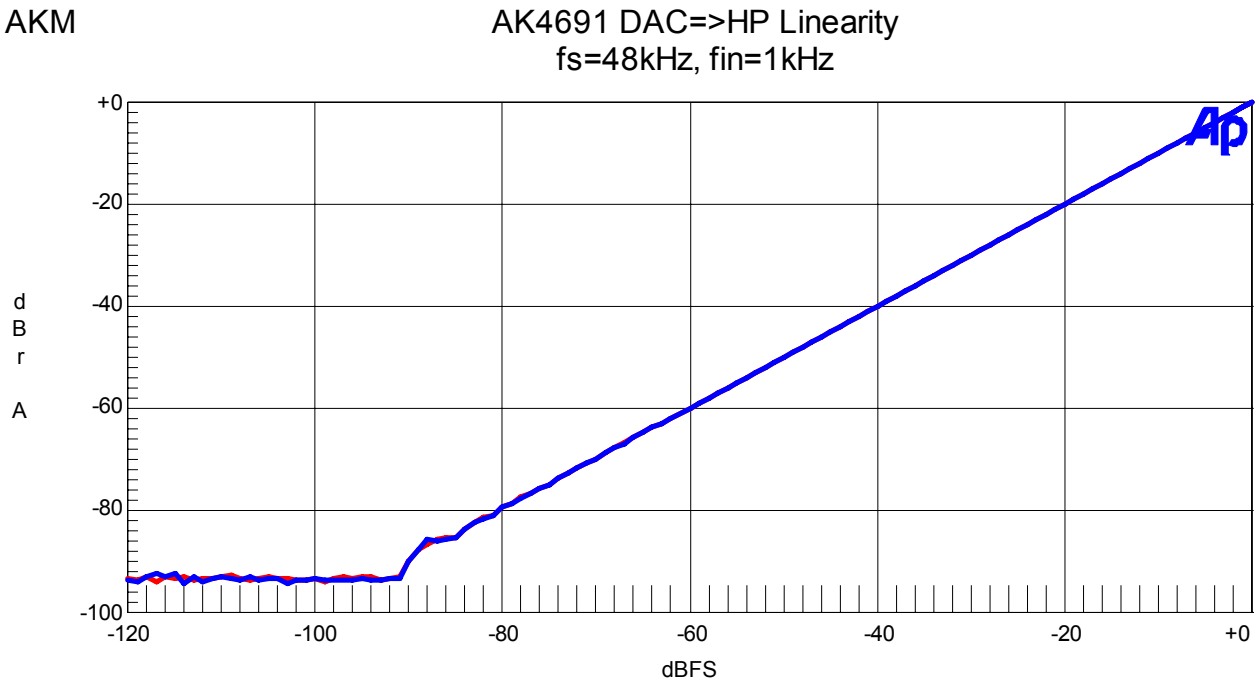
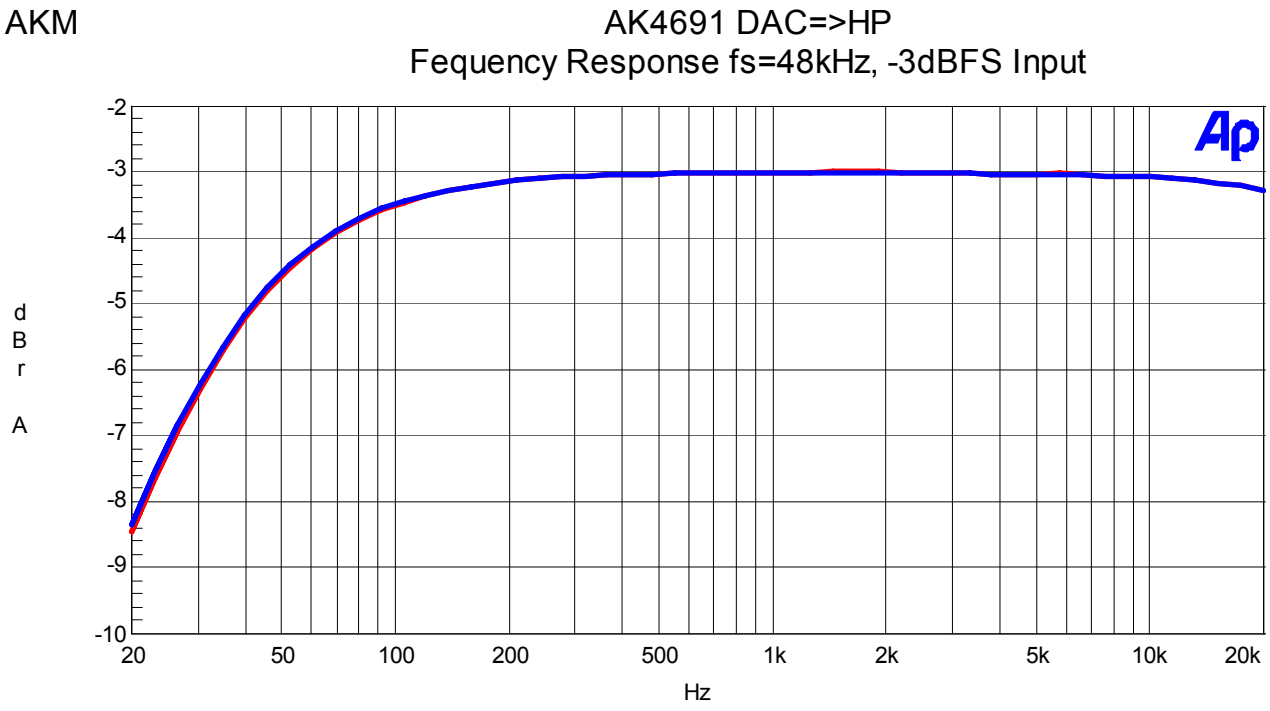


Figure 45. Linearity



*Headphone Out: C=220µF, Rseries=6.8Ω, RL=16Ω(Ext HPF: fc=31.7Hz)
Figure 46. Frequency Response

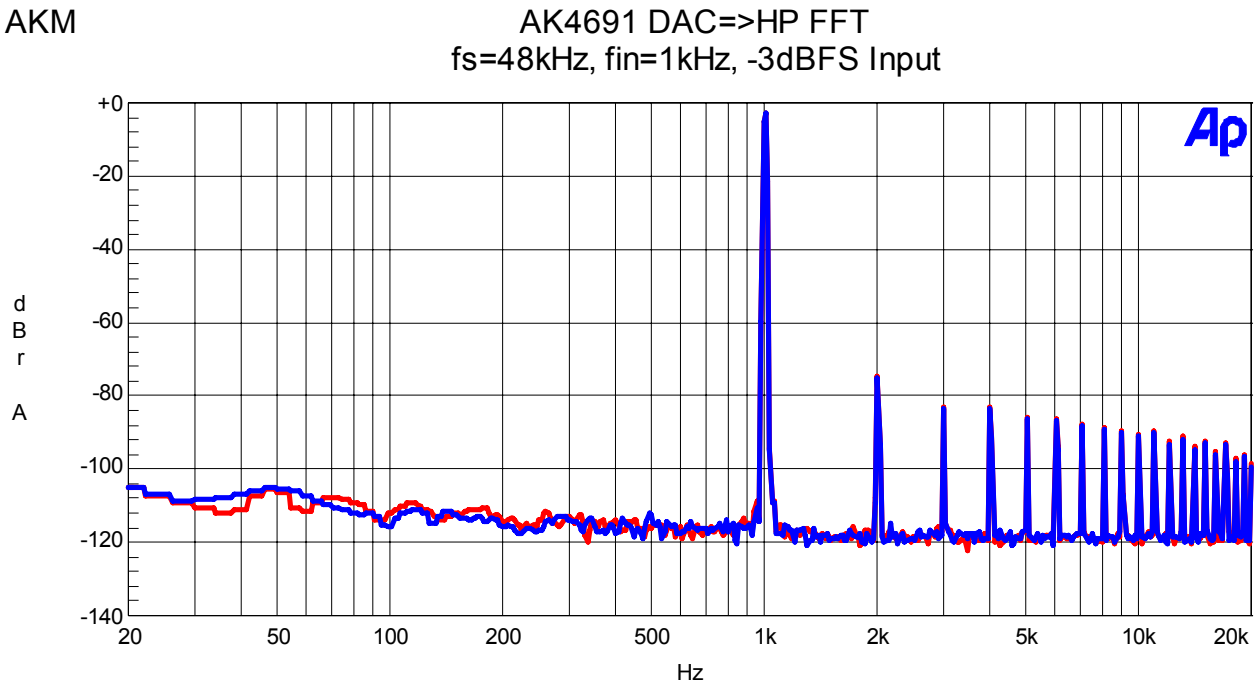


Figure 47. FFT (1kHz, -3dBFS)

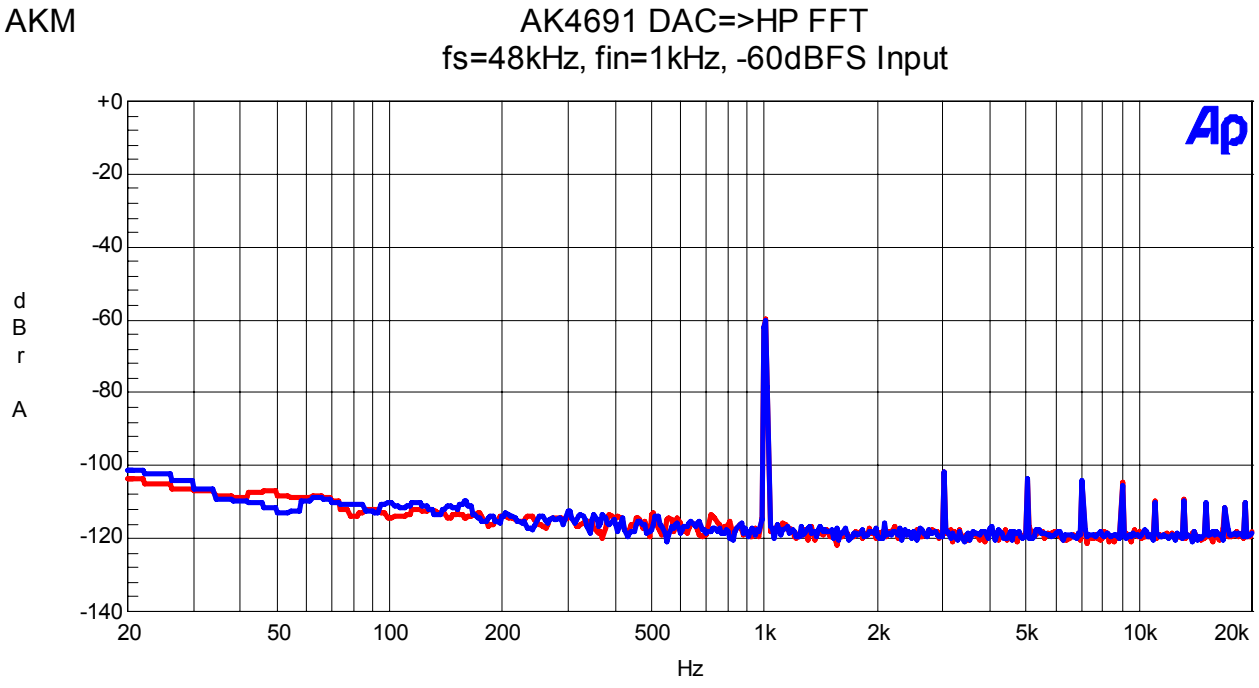


Figure 48. FFT (1kHz, -60dBFS)

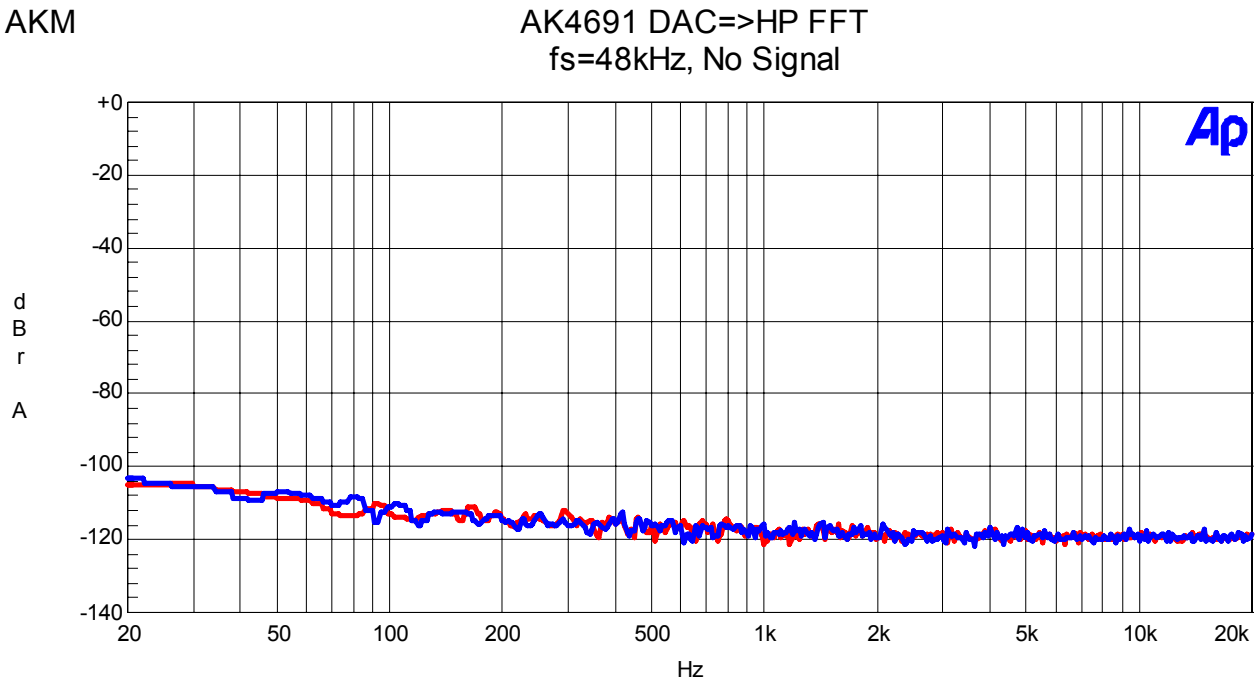


Figure 49. FFT (Noise Floor)

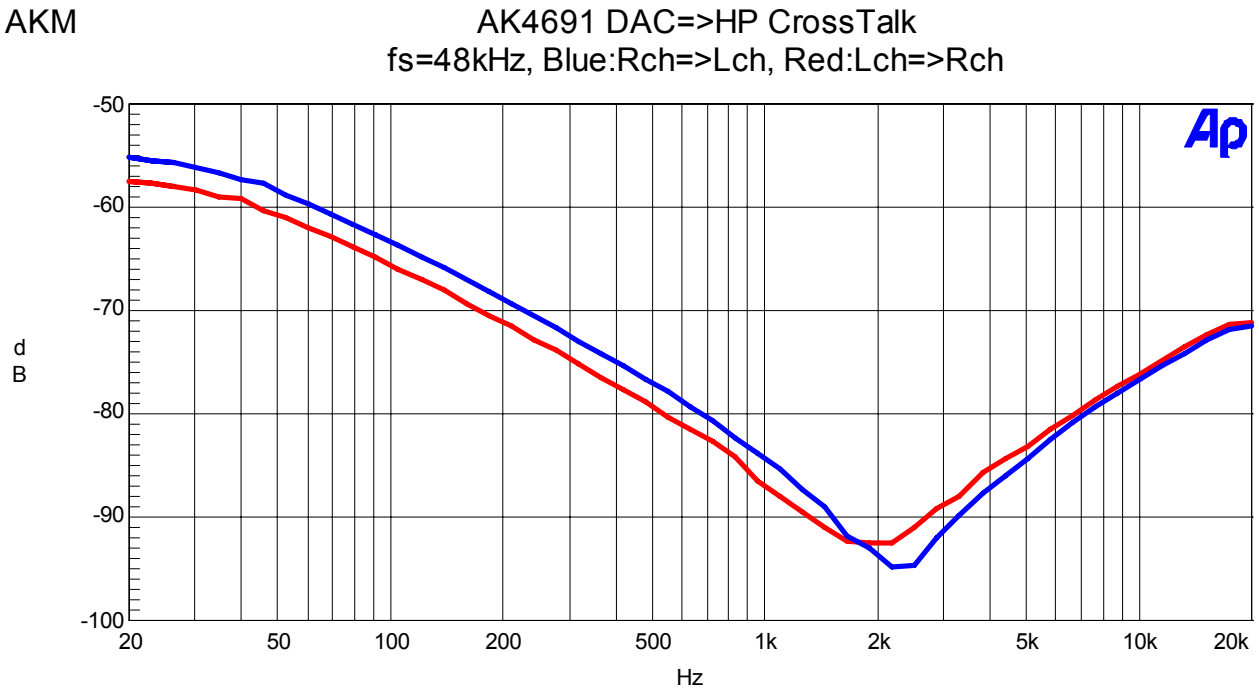


Figure 50. Crosstalk

4. Speaker (DAC → SPP/SPN, SPKG=+10.65dB)

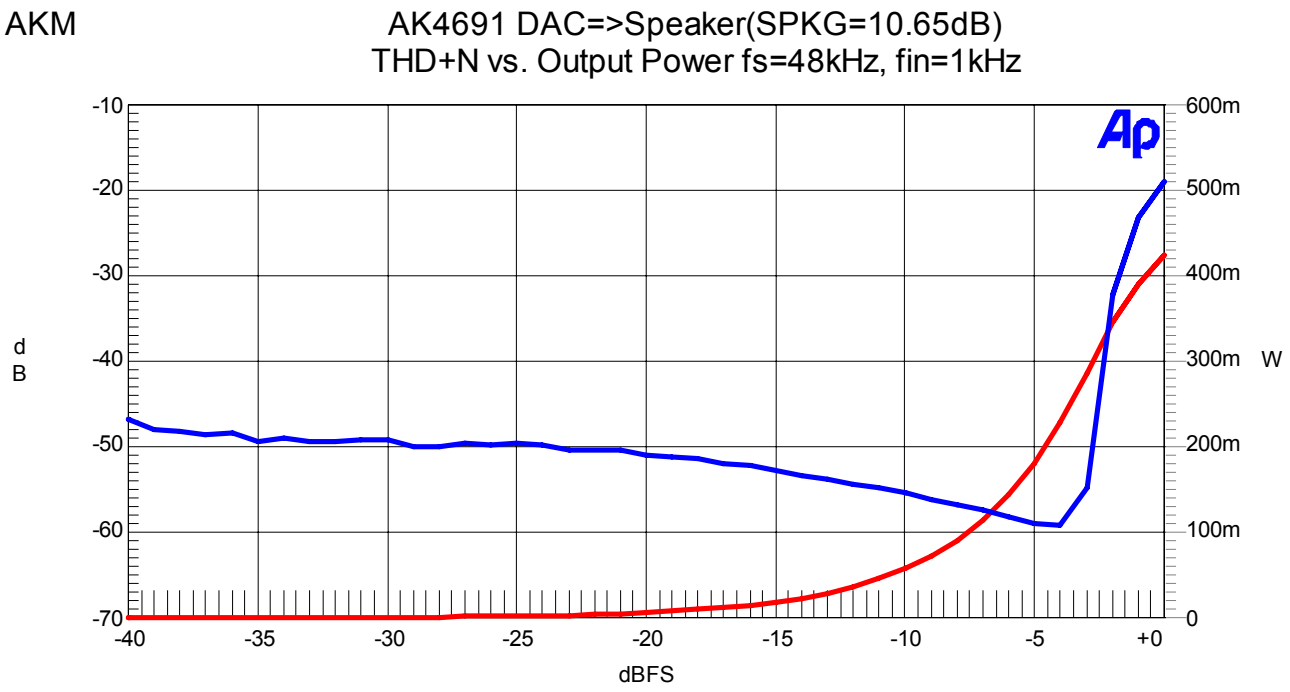


Figure 51. THD+N vs. Output Power

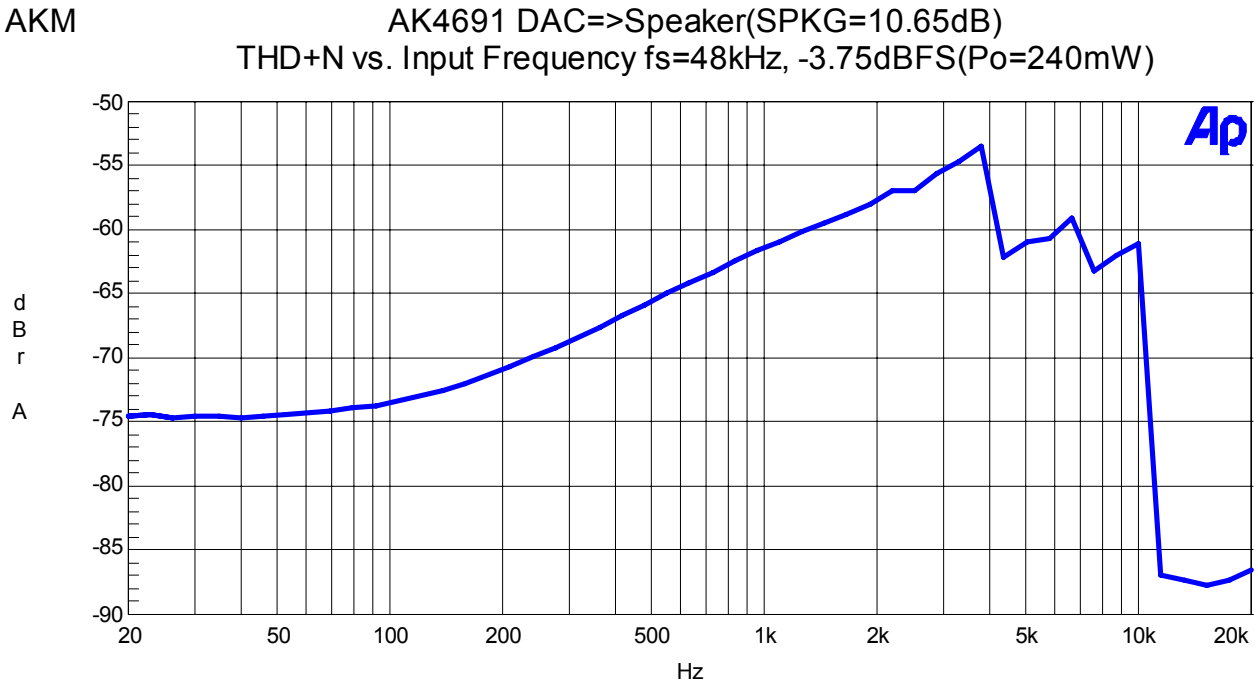


Figure 52. THD+N vs. Input Frequency

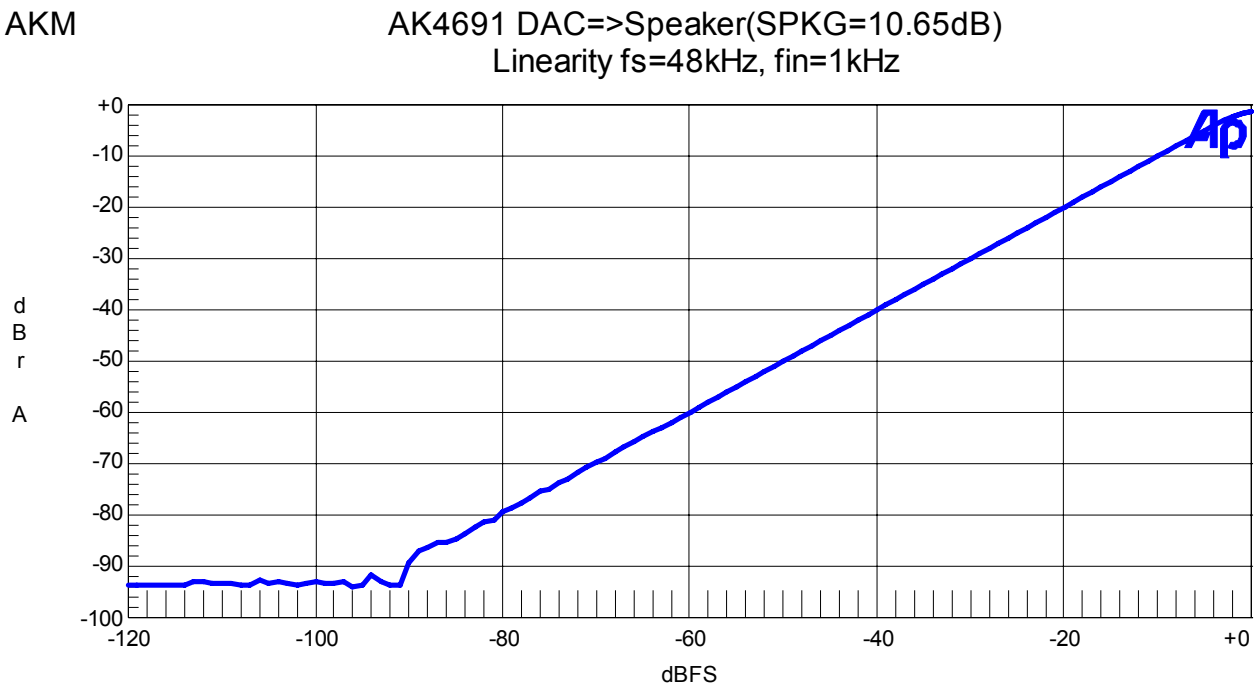


Figure 53. Linearity

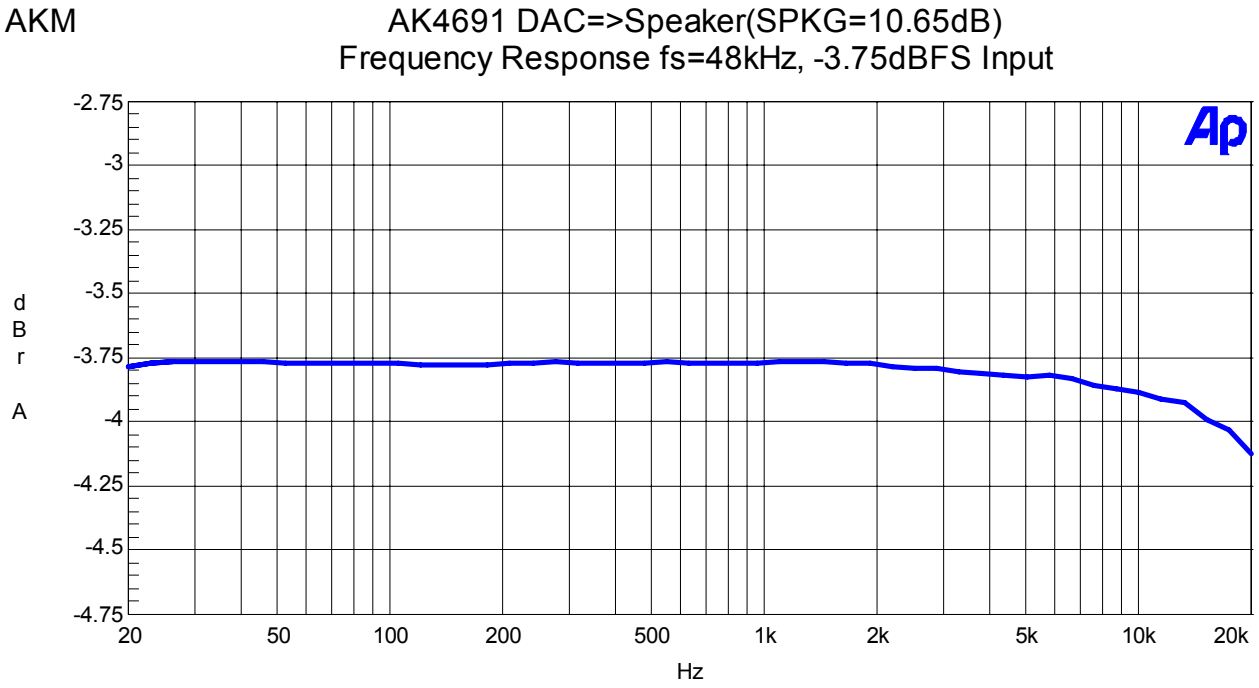


Figure 54. Frequency Response

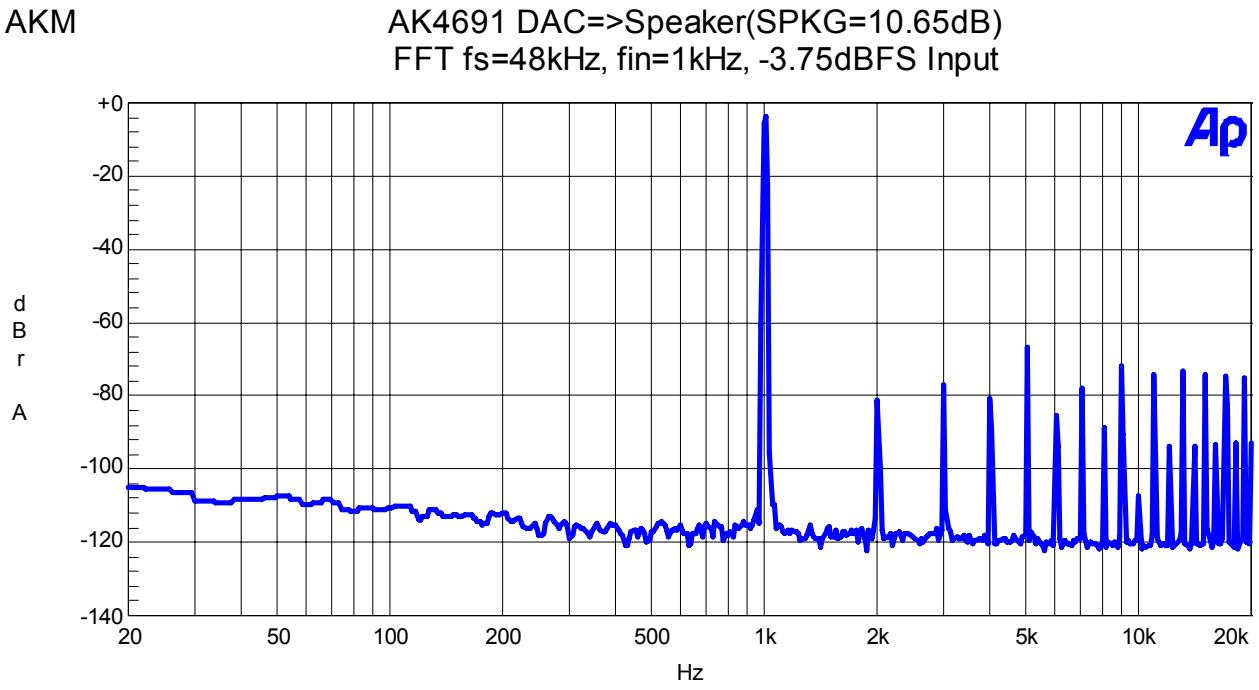


Figure 55. FFT (1kHz, -3.75dBFS)

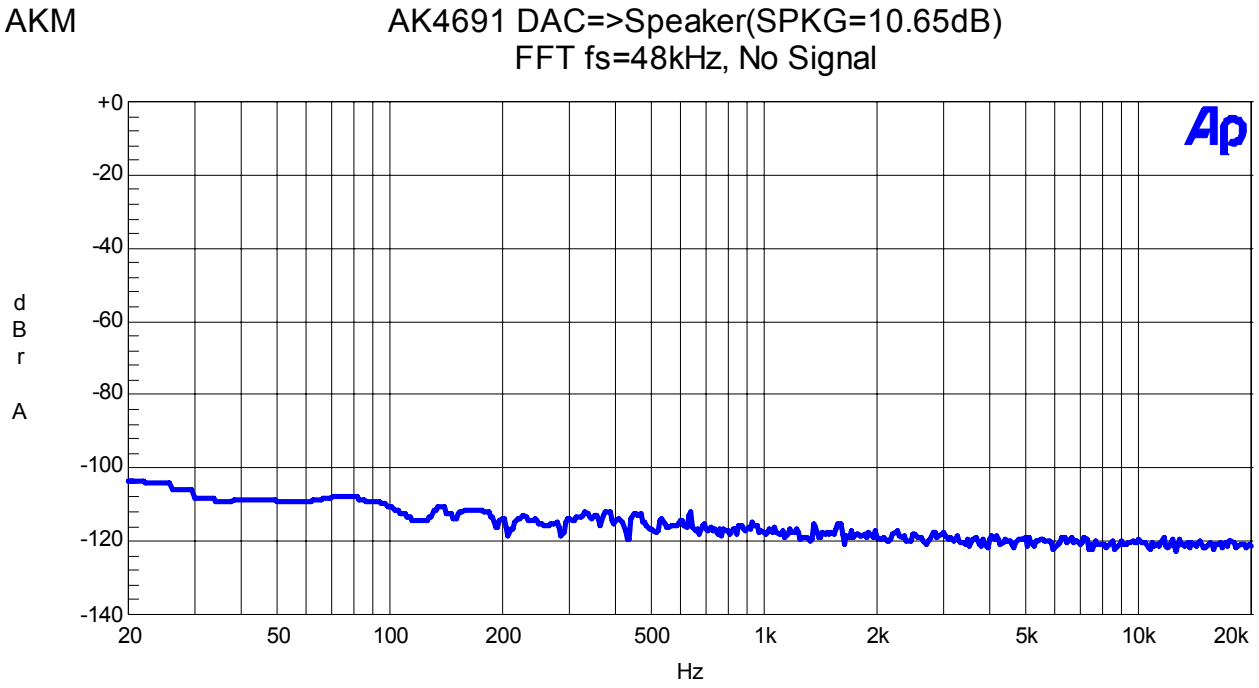
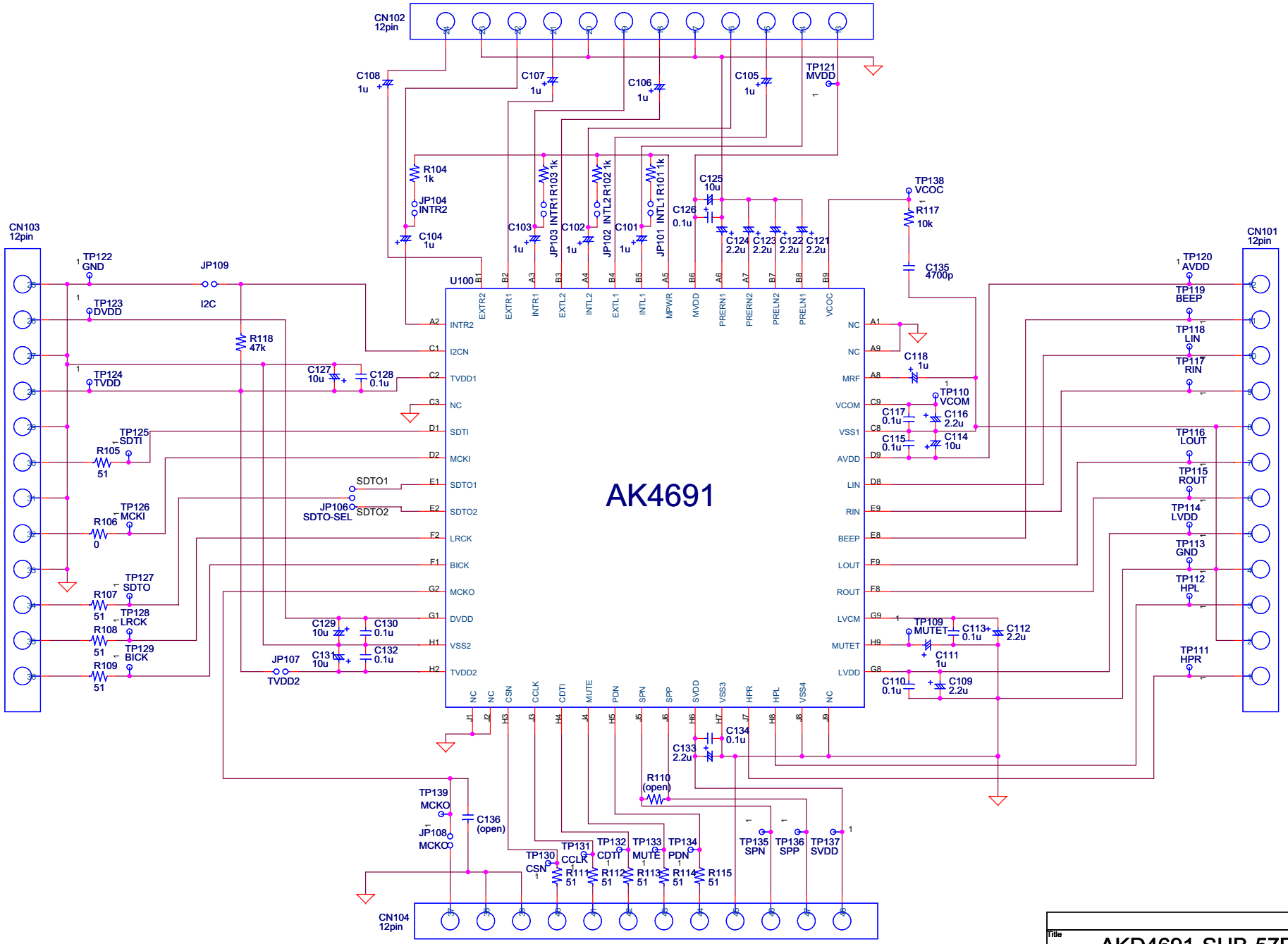


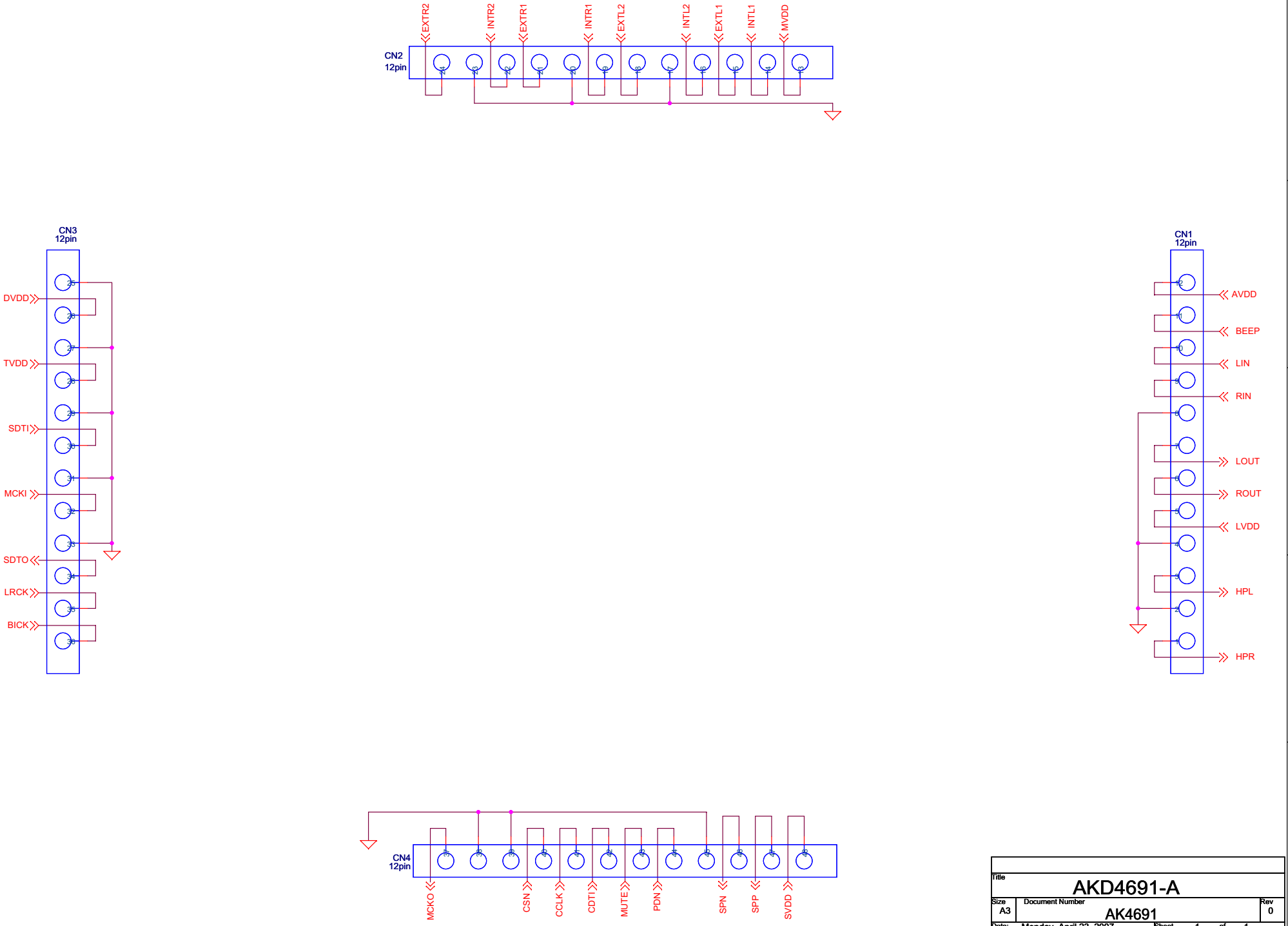
Figure 56. FFT (Noise Floor)

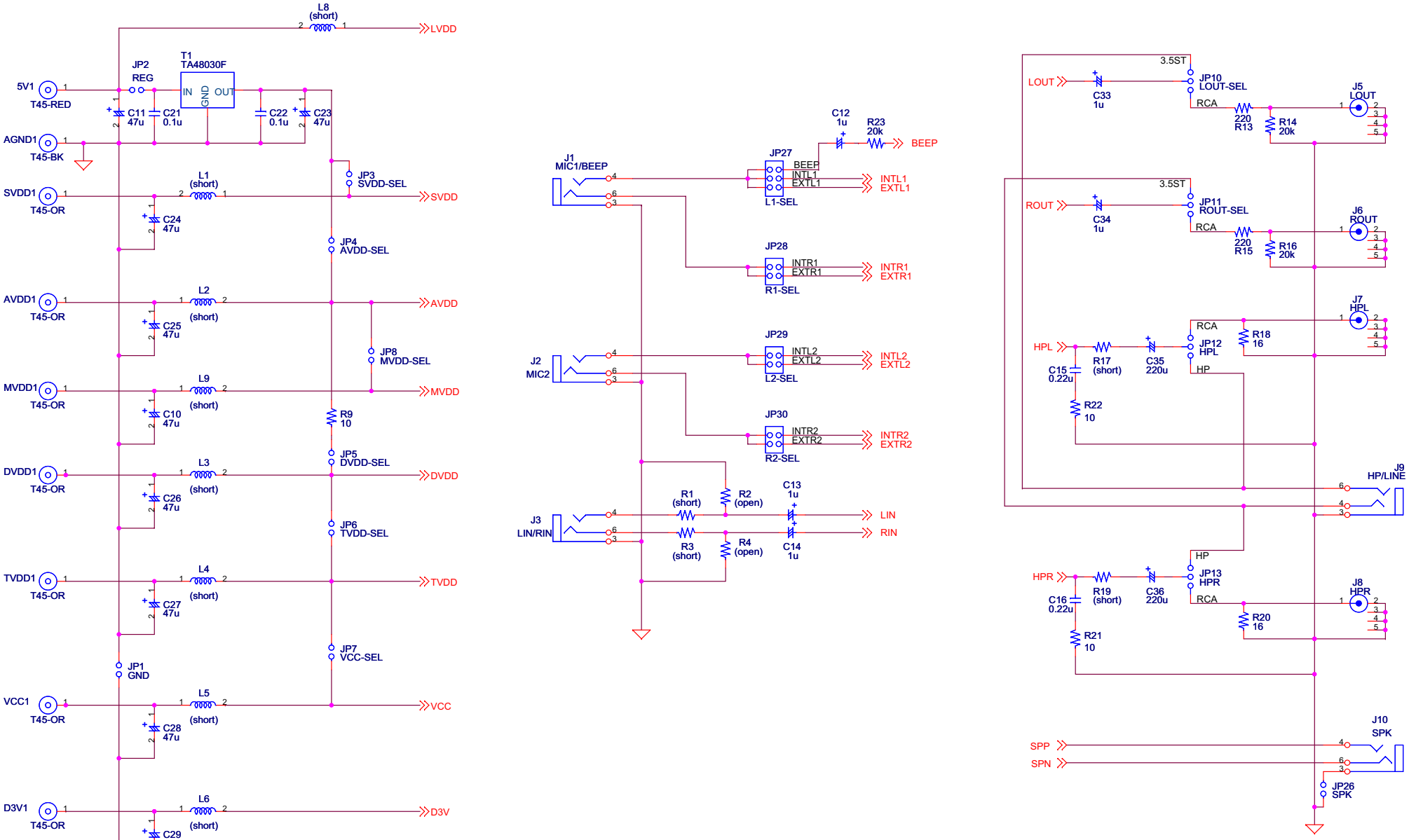
Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/06/14	KM089100	0	First edition	

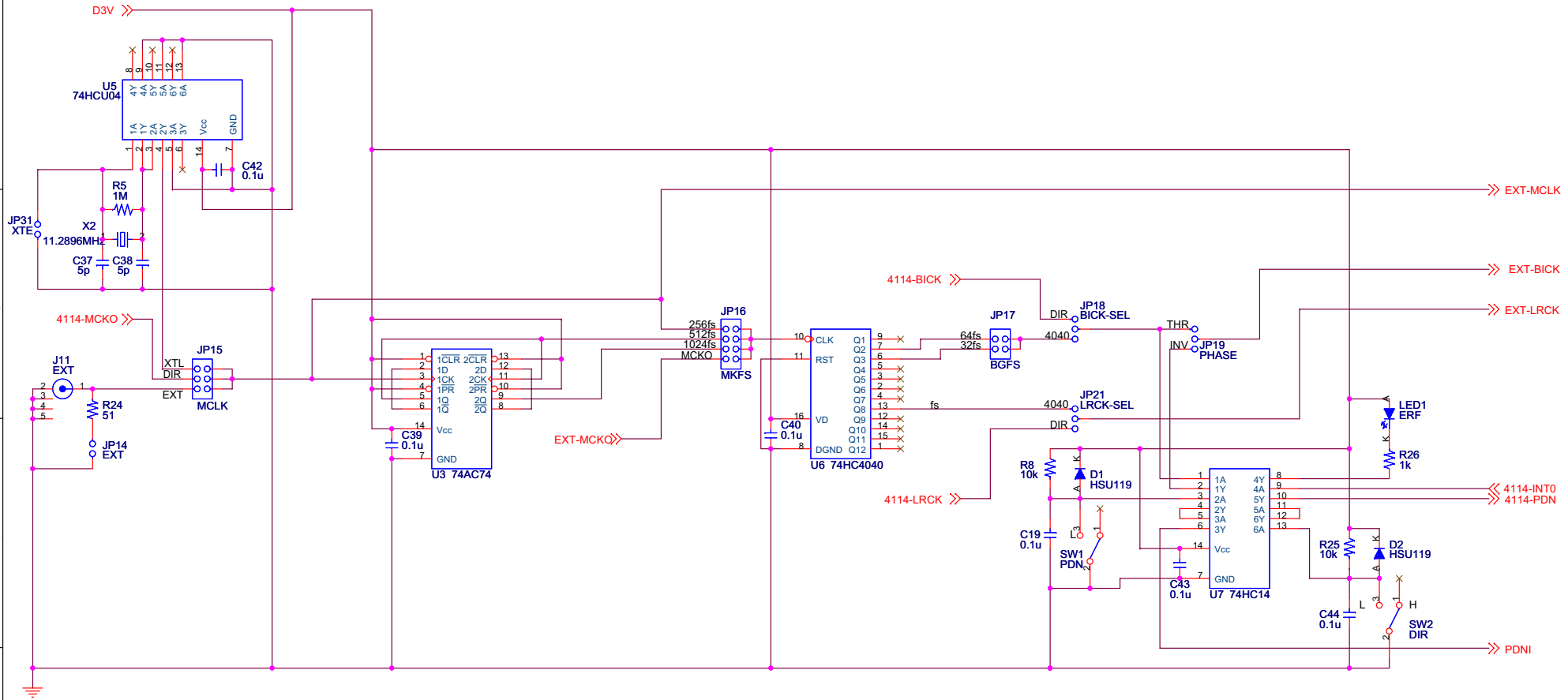


Title	AKD4691-SUB-57BGA		
Size A3	Document Number AK4691		Rev 0
Date: Friday, April 13, 2007		Sheet 1 of 1	

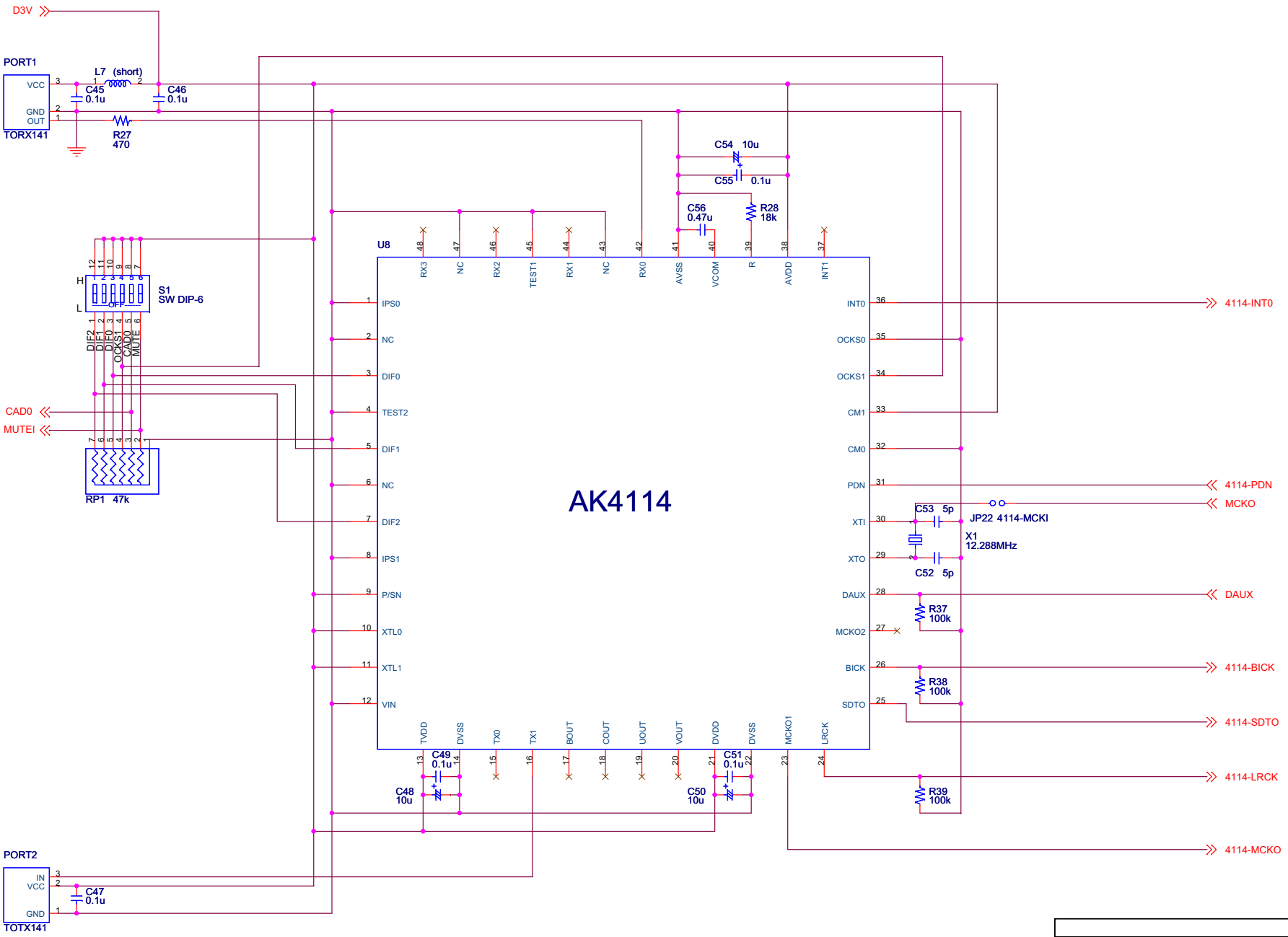

CN2
12pin
EXTR2
INTR2
EXTR1
INTR1
EXTL2
INTL2
EXTL1
INTL1
MVDD
CN3
12pin
DVDD
TVDD
SDTI
MCKI
SDTO
LRCK
BICK
CN1
12pin
AVDD
BEEP
LIN
RIN
LOUT
ROUT
LVDD
HPL
HPR
CN4
12pin
MCKO
CSN
CCLK
CDTI
MUTE
PDN
SPN
SPP
SVDD
Title
AKD4691-A
Size
A3
Document Number
AK4691
Rev
0
Date:
Monday, April 23, 2007
Sheet
1
of
1



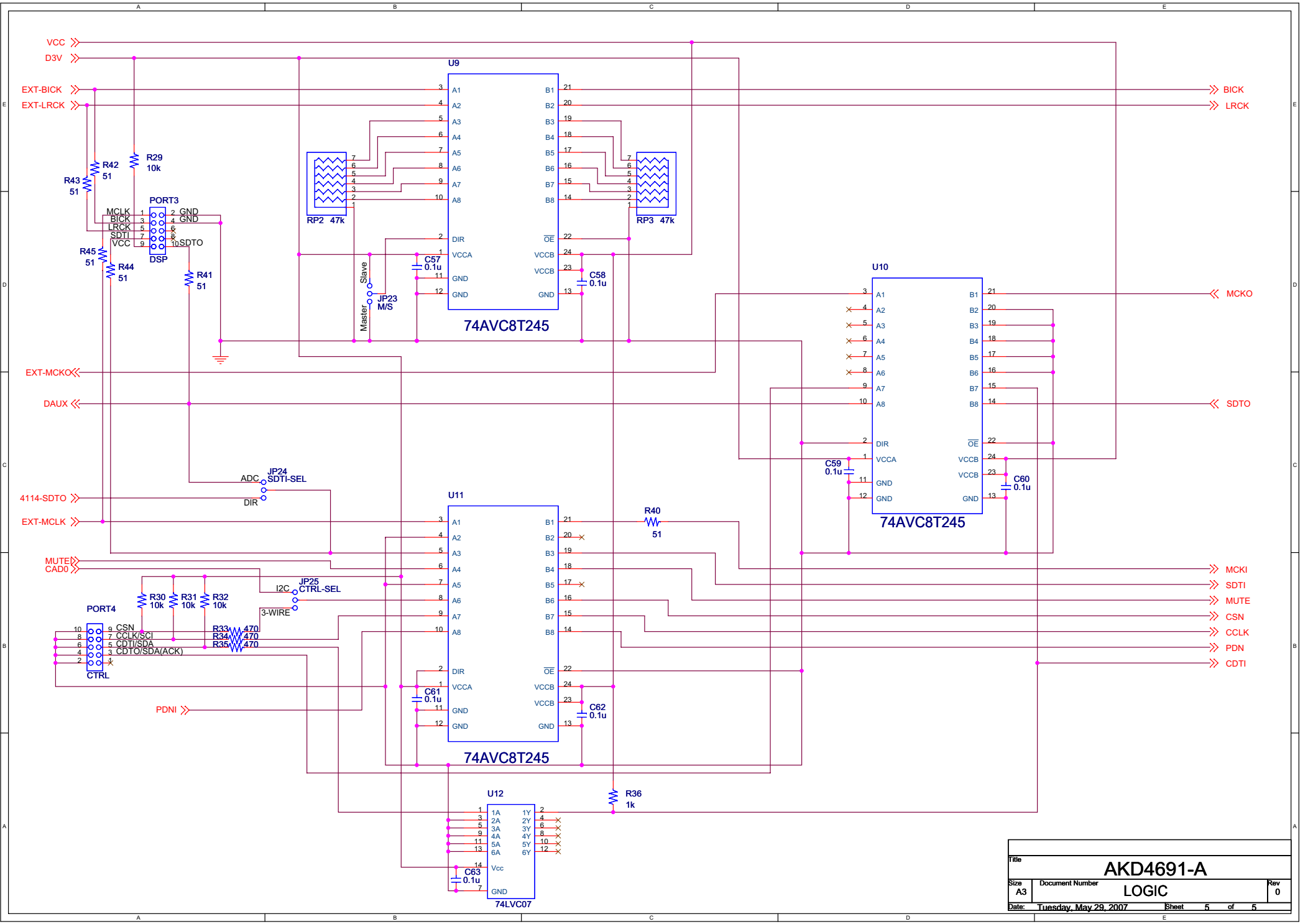
Title	AKD4691-A	
Size A3	Document Number Power Supply, I/O	Rev 0
Date: Monday, May 21, 2007	Sheet 2 of 5	

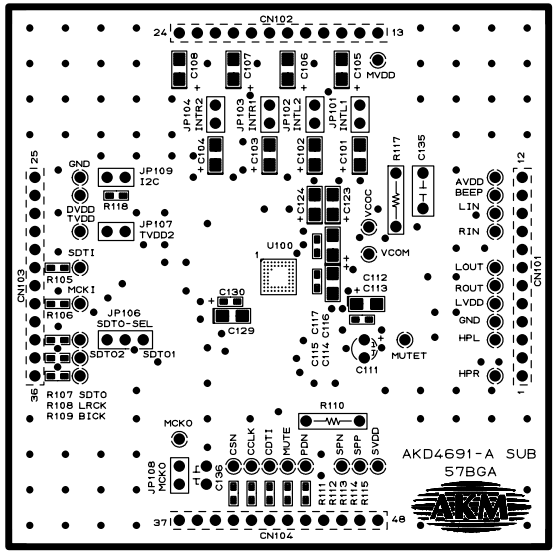


Title	AKD4691-A	
Size: A3	Document Number: CLOCK	Rev: 0
Date: Monday, May 21, 2007	Sheet 3 of 5	



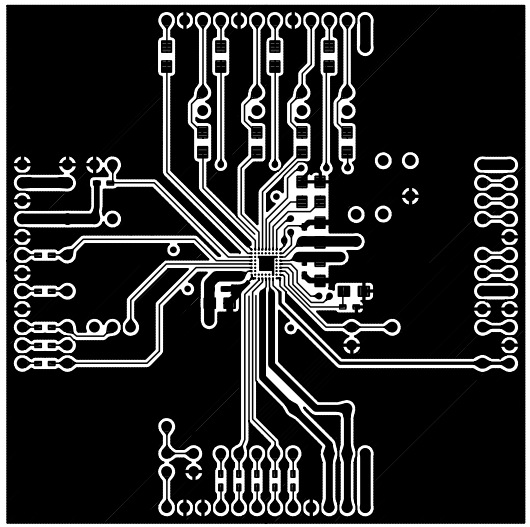
Title	AKD4691-A	
Size A3	Document Number DIR/DIT	Rev 0
Date: Monday, May 21, 2007	Sheet 4 of 5	


VCC
D3V
EXT-BICK
EXT-LRCK
R42 51
R43 51
R29 10k
PORT3
MCLK
BICK
LRCK
SDTI
VCC
GND
GND
SDTO
DSP
R45 51
R44 51
R41 51
U9
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
DIR
OE
VCCA
VCCB
VCCB
GND
GND
74AVC8T245
RP2 47k
RP3 47k
C57 0.1u
C58 0.1u
Slave
Master
JP23 M/S
BICK
LRCK
U10
MCKO
SDTO
C59 0.1u
C60 0.1u
74AVC8T245
EXT-MCKO
DAUX
4114-SDTO
EXT-MCLK
ADC
DIR
JP24 SDTI-SEL
U11
R40 51
MUTE
CAD0
I2C
3-WIRE
JP25 CTRL-SEL
R30 10k
R31 10k
R32 10k
PORT4
CSN
CCLK/SCI
CDTI/SDA
CDTO/SDA(ACK)
CTRL
R33 470
R34 470
R35 470
MCKI
SDTI
MUTE
CSN
CCLK
PDN
CDTI
C61 0.1u
C62 0.1u
74AVC8T245
PDNI
U12
1A
2A
3A
4A
5A
6A
1Y
2Y
3Y
4Y
5Y
6Y
Vcc
GND
74LVC07
C63 0.1u
R36 1k
Title
AKD4691-A
Size
A3
Document Number
LOGIC
Rev
0
Date:
Tuesday, May 29, 2007
Sheet
5
of
5

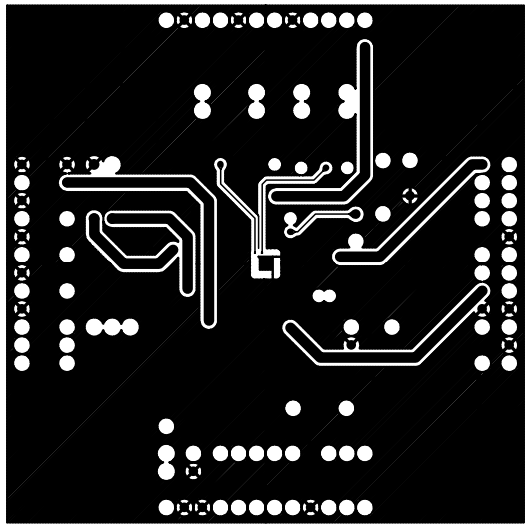


AKD4691-A SUB 57BGA L1 SILK

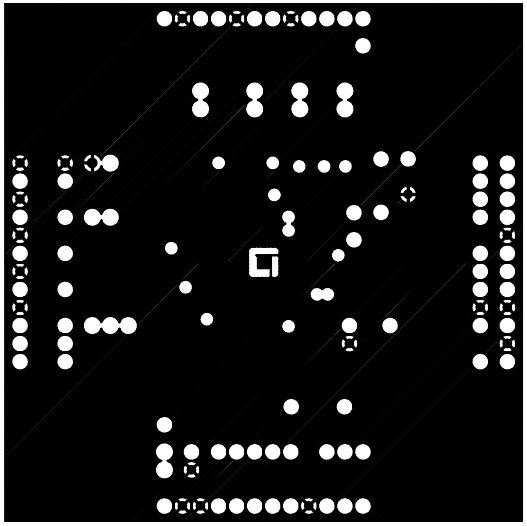
AKD4691-A SUB 2TBGA LY SILK



AKD4691-A SUB 57BGA L1

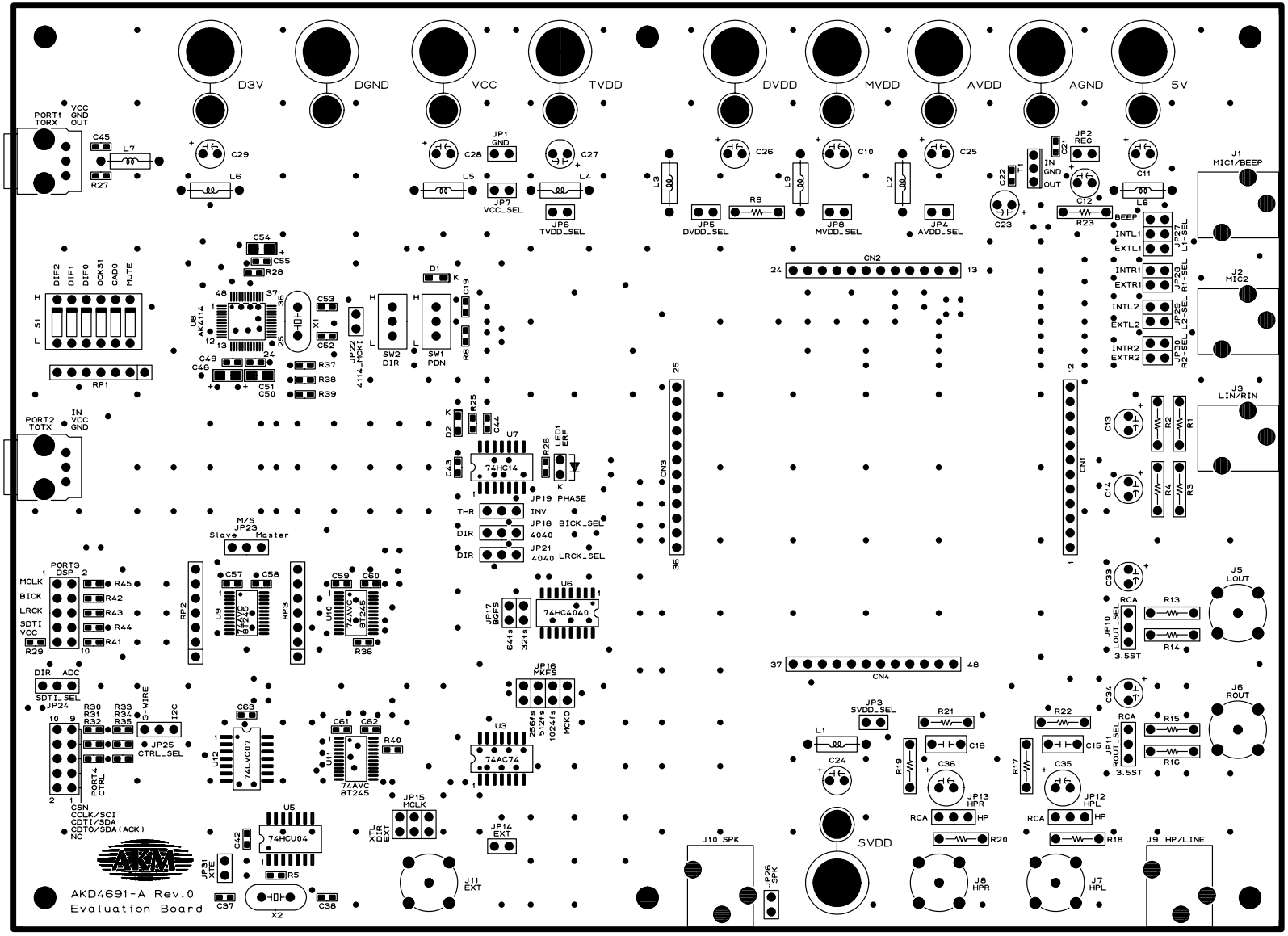


AKD4691-A SUB 57BGA L2



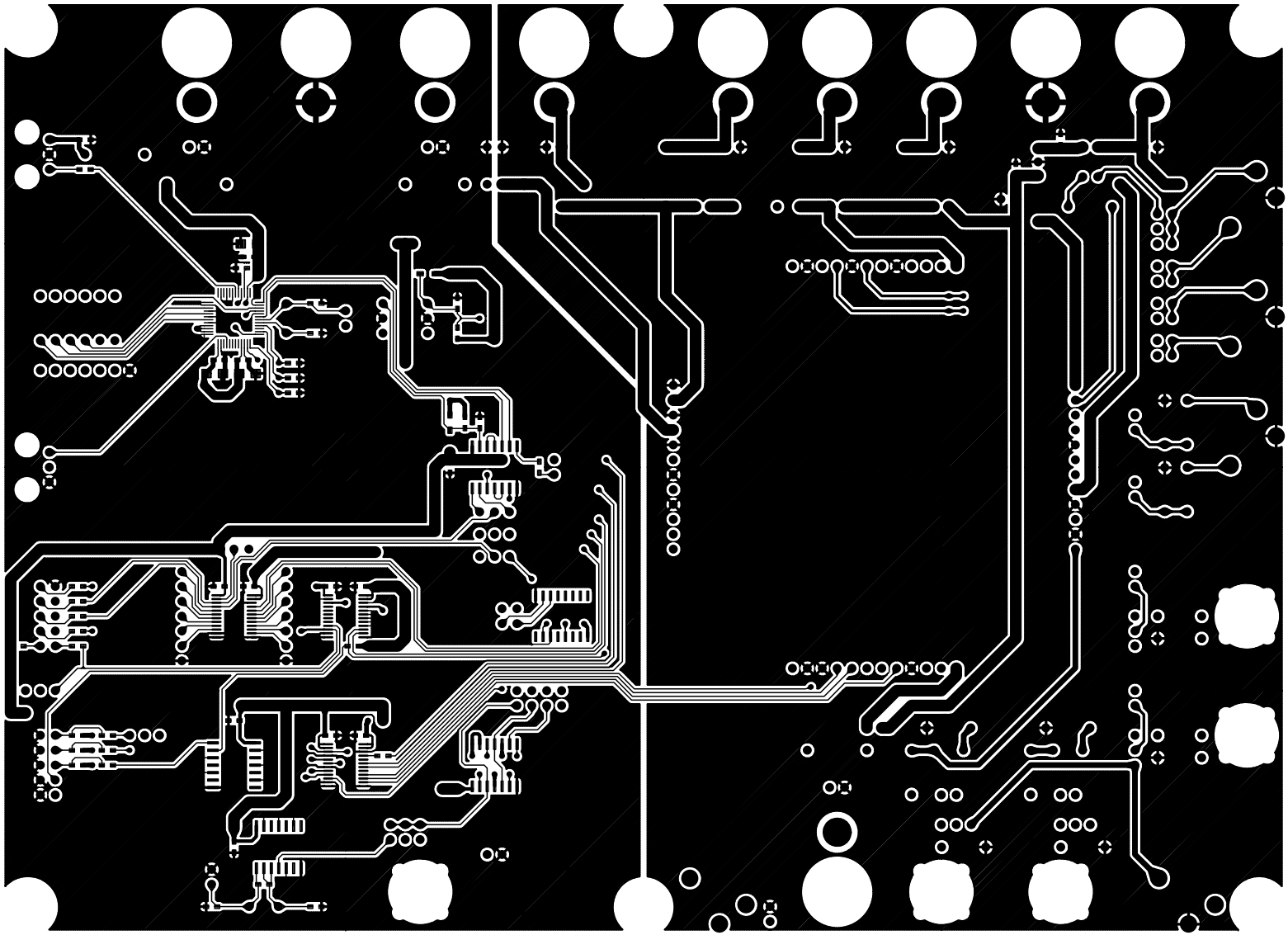
AKD4691-A SUB 57BGA L3

AKD6691-A SUB STBGA L4



AKD4691-A L1 SILK

AKD4691-A L2 SILK



AKD4691-A L1

AKD4691-A L2