

## V853™

## 32-BIT SINGLE-CHIP MICROCONTROLLERS

## DESCRIPTION

The  $\mu$ PD703003A, 703004A, 703025A, 703003A(A), and 703025A(A) are members of the V850 Series™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features including a 32-bit CPU core, ROM, RAM, an interrupt controller, a real-time pulse unit, a serial interface, an A/D converter, a D/A converter, and PWM.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V853 Hardware User's Manual: U10913E  
V850 Series Architecture User's Manual: U10243E

## FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 30 ns (@ 33 MHz operation)
- General-purpose registers: 32 bits  $\times$  32 registers
- Instruction set optimized for control applications
- Internal memory
  - ROM: 256 KB ( $\mu$ PD703025A, 703025A(A))
  - 128 KB ( $\mu$ PD703003A, 703003A(A))
  - 96 KB ( $\mu$ PD703004A)
  - RAM: 8 KB ( $\mu$ PD703025A, 703025A(A))
  - 4 KB ( $\mu$ PD703003A, 703004A, 703003A(A))
- Advanced internal interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (With on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- 8-/9-/10-/12-bit resolution PWM: 2 channels
- Power saving functions

## ★ ORDERING INFORMATION

Part Number	Package	Quality Grade
$\mu$ PD703003AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 $\times$ 14)	Standard
$\mu$ PD703004AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 $\times$ 14)	Standard
$\mu$ PD703025AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 $\times$ 14)	Standard
$\mu$ PD703003AGC(A)-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 $\times$ 14)	Special
$\mu$ PD703025AGC(A)-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 $\times$ 14)	Special

**Remark** xxx indicates ROM code suffix.

The  $\mu$ PD703003A, 703025A and  $\mu$ PD703003A(A), 703025A(A) differ in the quality grade only.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**APPLICATIONS**

μPD703003A, 703004A, 703025A: Camcorders, VCRs, PPCs, LBPs, printers, motor controllers, NC machine tools, mobile telephones, etc.

μPD703003A(A), 703025A(A): Medical equipment, automotive appliances, etc.

**★ PIN CONFIGURATION**

- 100-pin plastic LQFP (fine pitch) (14 × 14)

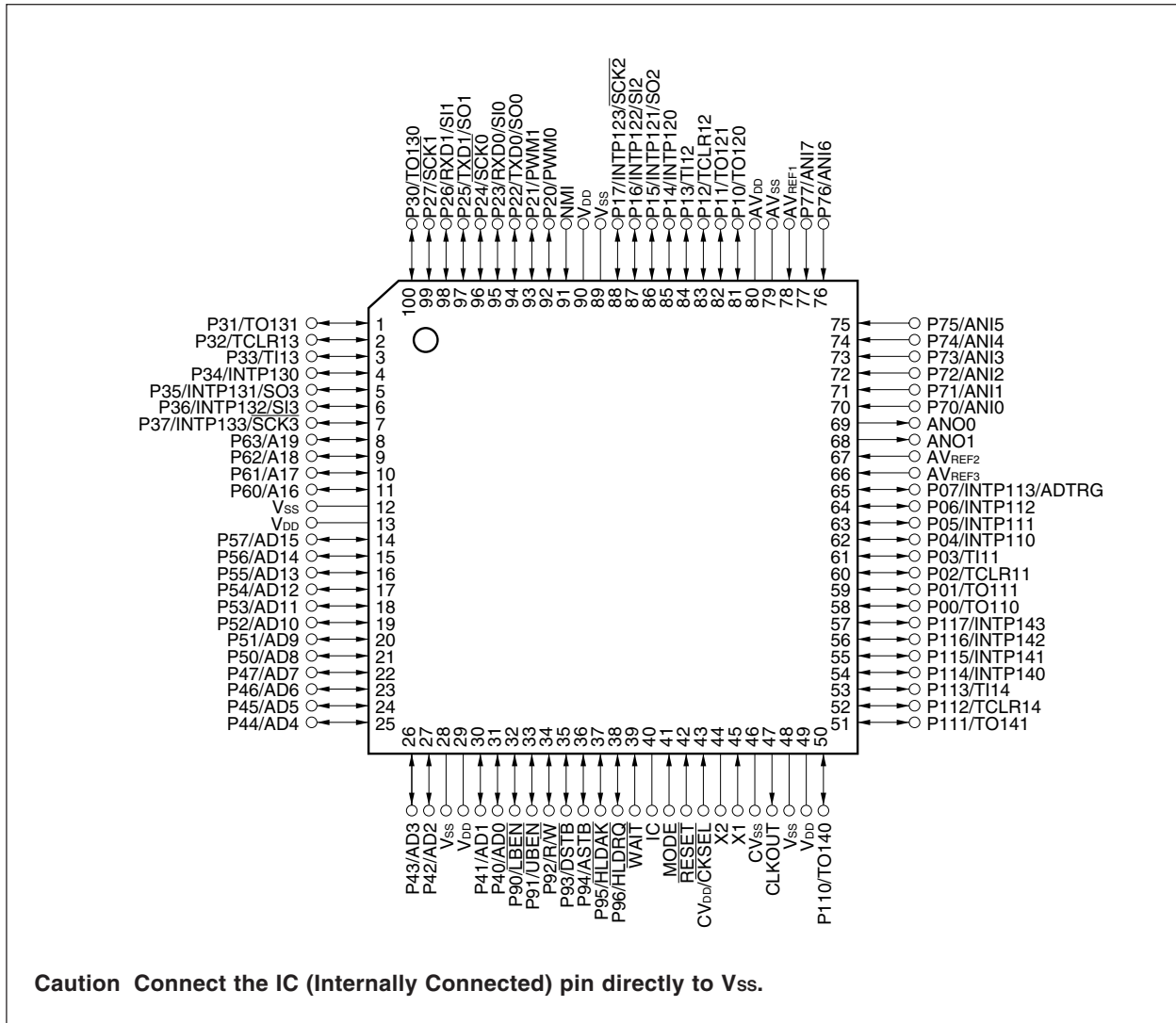
μPD703003AGC-33-xxx-8EU

μPD703003AGC(A)-33-xxx-8EU

μPD703004AGC-33-xxx-8EU

μPD703025AGC(A)-33-xxx-8EU

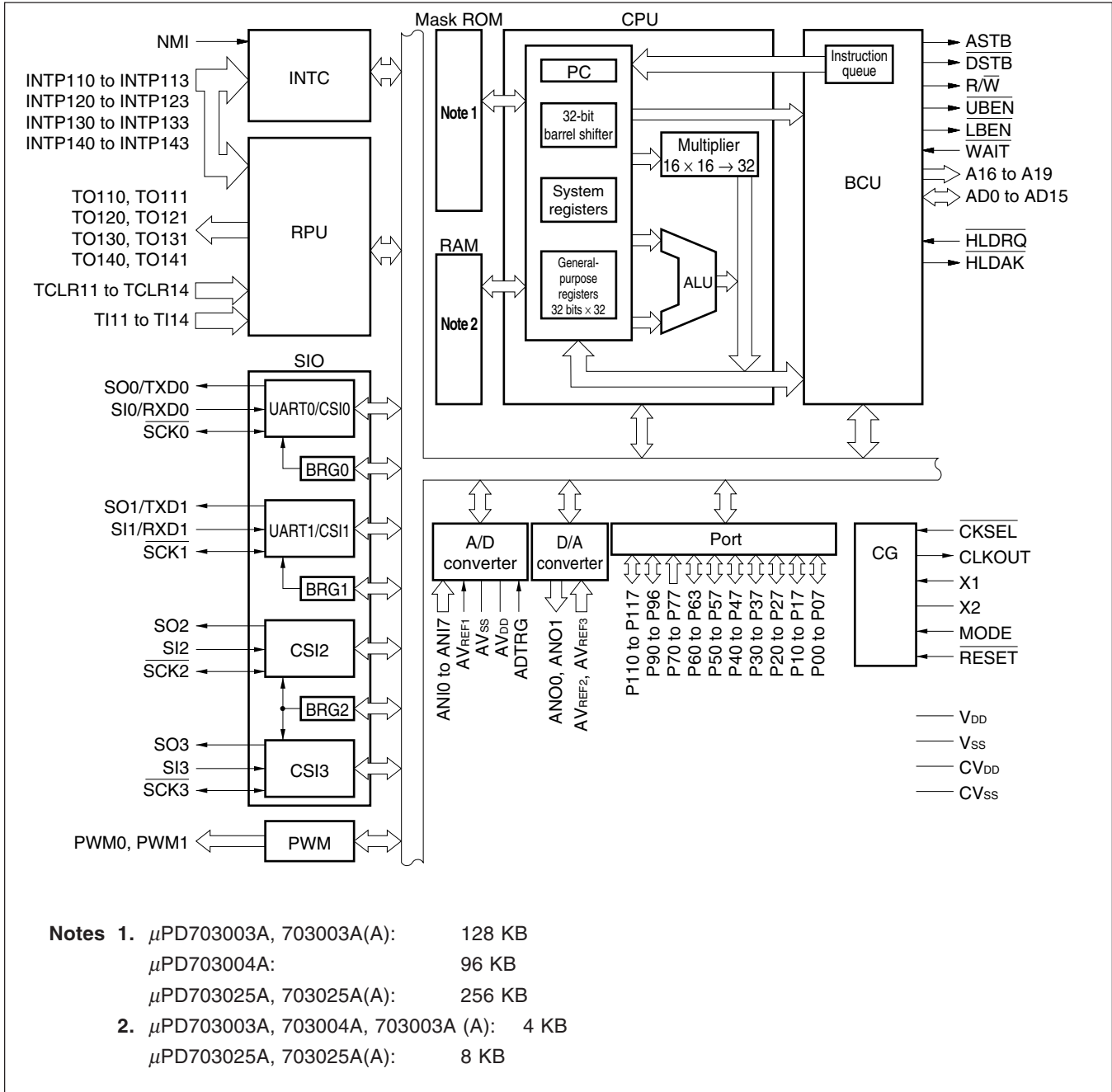
μPD703025AGC-33-xxx-8EU



**PIN NAMES**

A16 to A19:	Address bus	P30 to P37:	Port 3
AD0 to AD15:	Address/data bus	P40 to P47:	Port 4
ADTRG:	A/D trigger input	P50 to P57:	Port 5
ANI0 to ANI7:	Analog input	P60 to P63:	Port 6
ANO0, ANO1:	Analog output	P70 to P77:	Port 7
ASTB:	Address strobe	P90 to P96:	Port 9
AV <sub>DD</sub> :	Analog power supply	P110 to P117:	Port 11
AV <sub>REF1</sub> to AV <sub>REF3</sub> :	Analog reference voltage	PWM0, PWM1:	Pulse width modulation
AV <sub>SS</sub> :	Analog ground	RESET:	Reset
CV <sub>DD</sub> :	Power supply for clock generator	R/W:	Read/write status
CV <sub>SS</sub> :	Ground for clock generator	RXD0, RXD1:	Receive data
CKSEL:	Clock select	SCK0 to SCK3:	Serial clock
CLKOUT:	Clock output	SI0 to SI3:	Serial input
DSTB:	Data strobe	SO0 to SO3:	Serial output
HLD <sub>AK</sub> :	Hold acknowledge	TO110, TO111,	
HLD <sub>RQ</sub> :	Hold request	TO120, TO121,	
IC:	Internally connected	TO130, TO131,	
INTP110 to INTP113,		TO140, TO141:	Timer output
INTP120 to INTP123,		TCLR11 to TCLR14:	Timer clear
INTP130 to INTP133,		TI11 to TI14:	Timer input
INTP140 to INTP143:	Interrupt request from peripherals	TXD0, TXD1:	Transmit data
LBEN:	Lower byte enable	UBEN:	Upper byte enable
MODE:	Mode	WAIT:	Wait
NMI:	Non-maskable interrupt request	X1, X2:	Crystal
P00 to P07:	Port 0	V <sub>DD</sub> :	Power supply
P10 to P17:	Port 1	V <sub>SS</sub> :	Ground
P20 to P27:	Port 2		

INTERNAL BLOCK DIAGRAM



**CONTENTS**

<b>1. DIFFERENCES BETWEEN PRODUCTS .....</b>	<b>6</b>
<b>2. PIN FUNCTIONS .....</b>	<b>7</b>
<b>2.1 Port Pins .....</b>	<b>7</b>
<b>2.2 Non-Port Pins .....</b>	<b>9</b>
<b>2.3 Pin I/O Circuits and Recommended Connection of Unused Pins .....</b>	<b>11</b>
<b>3. ELECTRICAL SPECIFICATIONS .....</b>	<b>14</b>
<b>4. PACKAGE DRAWING .....</b>	<b>35</b>
<b>5. RECOMMENDED SOLDERING CONDITIONS .....</b>	<b>36</b>
<b>★ APPENDIX NOTES ON TARGET SYSTEM DESIGN .....</b>	<b>37</b>

1. DIFFERENCES BETWEEN PRODUCTS

Item	μPD703003A	μPD703004A	μPD703025A	μPD703003A(A)	μPD703025A(A)	μPD70F3003A	μPD70F3025A	μPD70F3003A(A)
Internal ROM	Mask ROM					Flash memory		
	128 KB	96 KB	256 KB	128 KB	256 KB	128 KB	256 KB	128 KB
Internal RAM	4 KB		8 KB	4 KB	8 KB	4 KB	8 KB	4 KB
Flash memory programming mode	None					Provided		
V <sub>PP</sub> pin	None					Provided		
Quality grade	Standard			Special		Standard		Special
Electrical specifications	Current consumption, etc. differs. (Refer to each product data sheets.)							
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.							

**Caution** There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units.	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/SCK2
P20	I/O	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/SCK3
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8 to AD15

(2/2)

Pin Name	I/O	Function	Alternate Function
P60 to P63	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units.	A16 to A19
P70 to P77	Input	Port 7 8-bit input port	ANI0 to ANI7
P90	I/O	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/W
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			$\overline{\text{HLDK}}$
P96			$\overline{\text{HLDRQ}}$
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units.	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143



2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO110	Output	Pulse signal output from timers 11 to 14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal input for timers 11 to 14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock input for timers 11 to 14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt request input, also used as external capture trigger input for timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt request input, also used as external capture trigger input for timer 12	P14
INTP121			P15/SO2
INTP122			P16/SI2
INTP123			P17/SCK2
INTP130	Input	External maskable interrupt request input, also used as external capture trigger input for timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/SCK3
INTP140	Input	External maskable interrupt request input, also used as external capture trigger input for timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output for CSI0 to CSI3 (3-wire)	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data input for CSI0 to CSI3 (3-wire)	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{SCK0}}$	I/O	Serial clock I/O for CSI0 to CSI3 (3-wire)	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P17/INTP123
$\overline{\text{SCK3}}$			P37/INTP133
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	PWM pulse signal output	P20
PWM1			P21
AD0 to AD7	I/O	16-bit multiplexed address/data bus for external memory expansion	P40 to P47
AD8 to AD15			P50 to P57
A16 to A19	Output	Higher address bus used for external memory expansion	P60 to P63
$\overline{\text{LBEN}}$	Output	External data bus's lower byte enable signal output	P90
$\overline{\text{UBEN}}$		External data bus's higher byte enable signal output	P91
$\overline{\text{R/W}}$	Output	External read/write status output	P92
$\overline{\text{DSTB}}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P96
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
ANO0, ANO1	Output	Analog output from D/A converter	—
NMI	Input	Non-maskable interrupt request input	—
CLKOUT	Output	System clock output	—
$\overline{\text{CKSEL}}$	Input	Input for specifying clock generator's operation mode	CV <sub>DD</sub>
$\overline{\text{WAIT}}$	Input	Control signal input for inserting wait in bus cycle	—
MODE	Input	Operation mode specification	—
$\overline{\text{RESET}}$	Input	System reset input	—
X1	Input	Resonator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV <sub>REF1</sub>	Input	Reference voltage input for A/D converter	—
AV <sub>REF2</sub>	Input	Reference voltage input for D/A converter	—
AV <sub>REF3</sub>			—
AV <sub>DD</sub>	—	Positive power supply for A/D converter	—
AV <sub>SS</sub>	—	Ground potential for A/D converter	—
CV <sub>DD</sub>	—	Positive power supply for on-chip clock generator	$\overline{\text{CKSEL}}$
CV <sub>SS</sub>	—	Ground potential for on-chip clock generator	—
V <sub>DD</sub>	—	Positive power supply	—
V <sub>SS</sub>	—	Ground potential	—
IC	—	Internally connected pin (Connect directly to V <sub>SS</sub> )	—

**2.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. Figure 2-1 illustrates the various circuit types using partially abridged diagrams.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V<sub>DD</sub> or V<sub>SS</sub> via a resistor.

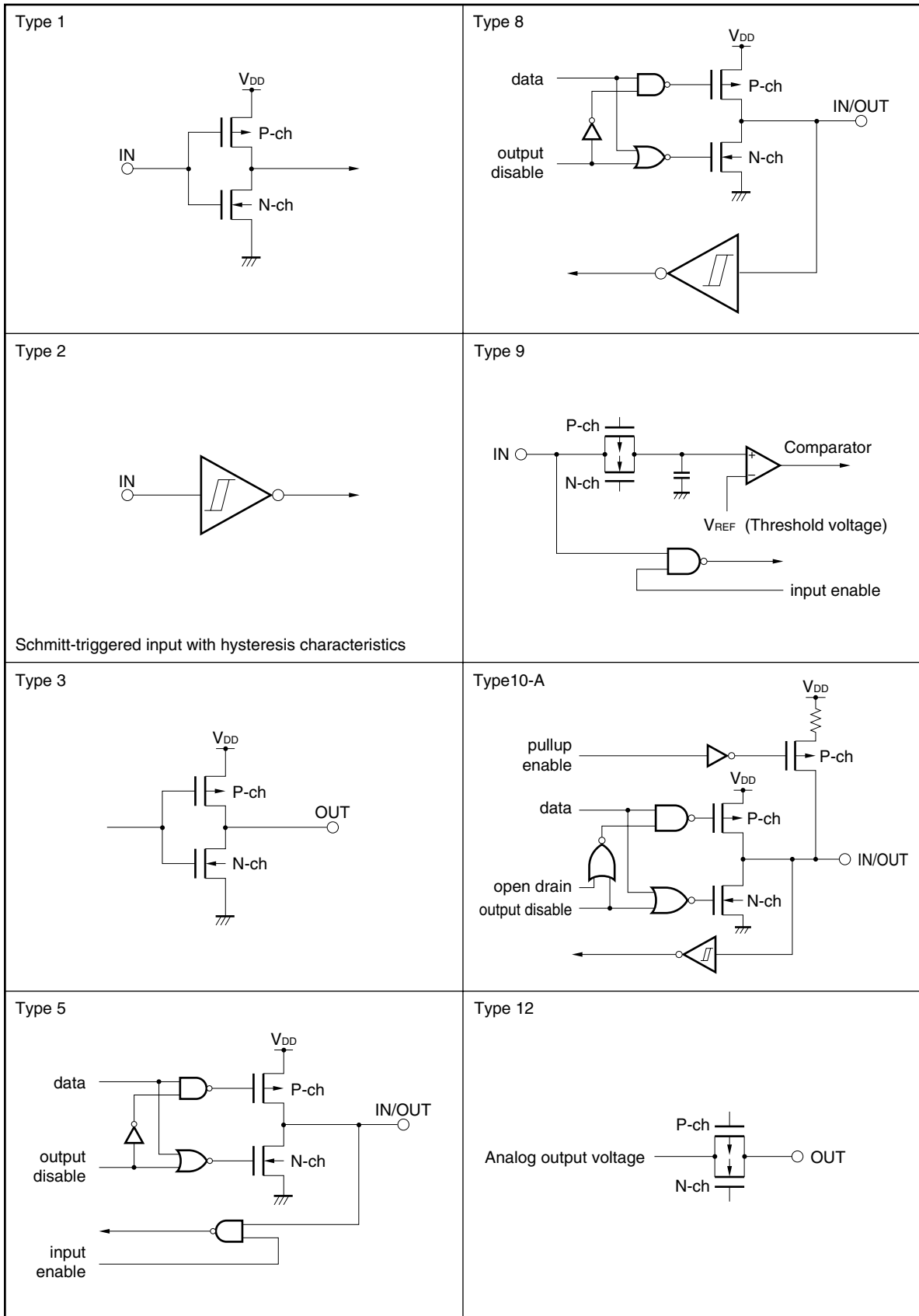
**Table 2-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)**

Pin Name	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO110, P01/TO111	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113/ADTRG	8	
P10/TO120, P11/TO121	5	
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/SCK2	8	
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5	
P23/RXD0/SI0, P24/SCK0	8	
P25/TXD1/SO1	5	
P26/RXD1/SI1, P27/SCK1	8	
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13 P34/INTP130	8	
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/SCK3	10-A	
P40/AD0 to P47/AD7	5	
P50/AD8 to P57/AD15		
P60/A16 to P63/A19		
P70/ANI0 to P77/ANI7	9	Connect directly to V <sub>SS</sub> .
P90/LBEN	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P91/UBEN		
P92/R/W		
P93/DSTB		
P94/ASTB		
P95/HLDAK		
P96/HLDRQ		
P110/TO140, P111/TO141		
P112/TCLR14, P113/TI14 P114/INTP140 to P117/INTP143	8	
ANO0, ANO1	12	Leave open.
NMI	2	Connect directly to V <sub>SS</sub> .

Table 2-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

Pin Name	I/O Circuit Type	Recommended Connection of Unused Pins
CLKOUT	3	Leave open.
WAIT	1	Connect directly to V <sub>DD</sub> .
MODE	2	—
RESET		
CV <sub>DD</sub> /CKSEL		
AV <sub>REF1</sub> to AV <sub>REF3</sub> , AV <sub>SS</sub>	—	Connect directly to V <sub>SS</sub> .
AV <sub>DD</sub>	—	Connect directly to V <sub>DD</sub> .
IC	—	Connect directly to V <sub>SS</sub> .

Figure 2-1. Pin I/O Circuits



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub> pin	-0.5 to +7.0	V	
	CV <sub>DD</sub>	CV <sub>DD</sub> pin	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V	
	CV <sub>SS</sub>	CV <sub>SS</sub> pin	-0.5 to +0.5	V	
	AV <sub>DD</sub>	AV <sub>DD</sub> pin	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V	
	AV <sub>SS</sub>	AV <sub>SS</sub> pin	-0.5 to +0.5	V	
Input voltage	V <sub>I1</sub>	<b>Note 2</b> , V <sub>DD</sub> = 5.0 V ±10%	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V	
Clock input voltage	V <sub>K</sub>	X1 pin, V <sub>DD</sub> = 5.0 V ±10%	-0.5 to V <sub>DD</sub> + 1.0 <sup>Note 1</sup>	V	
Output current, low	I <sub>OL</sub>	Per pin	4.0	mA	
		Total for all pins	100	mA	
Output current, high	I <sub>OH</sub>	Per pin	-4.0	mA	
		Total for all pins	-100	mA	
Output voltage	V <sub>O</sub>	V <sub>DD</sub> = 5.0 V ±10%	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V	
Analog input voltage	V <sub>IAN</sub>	P70/ANI0 to P77/ANI7	AV <sub>DD</sub> > V <sub>DD</sub>	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
			V <sub>DD</sub> ≥ AV <sub>DD</sub>	-0.5 to AV <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Analog reference input voltage	AV <sub>REF</sub>	AV <sub>REF1</sub> to AV <sub>REF3</sub>	AV <sub>DD</sub> > V <sub>DD</sub>	-0.5 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
			V <sub>DD</sub> ≥ AV <sub>DD</sub>	-0.5 to AV <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C	
Storage temperature	T <sub>stg</sub>		-65 to +150	°C	

- Notes**
1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.
  2. X1, P70 to P77, AV<sub>REF1</sub> to AV<sub>REF3</sub>, and their alternate-function pins are excluded.

- Cautions**
1. **Avoid direct connections among the IC device output (or I/O) pins and between V<sub>DD</sub> or V<sub>CC</sub> and GND. However, direct connections among open-drain and open-collector pins are possible, as are direct connections to external circuits that have timing designed to prevent output conflict with pins that become high-impedance.**
  2. **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**  
The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f <sub>C</sub> = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C <sub>IO</sub>				15	pF
Output capacitance	C <sub>O</sub>				15	pF

**Operating Conditions**

Operation Mode	Internal System Clock Frequency ( $\phi$ )	Operating Ambient Temperature ( $T_A$ )	Power Supply Voltage ( $V_{DD}$ )
Direct mode, PLL mode	2 to 33 MHz <sup>Note 1</sup>	-40 to +85°C	5.0 V ±10%
	5 to 33 MHz <sup>Note 2</sup>	-40 to +85°C	5.0 V ±10%

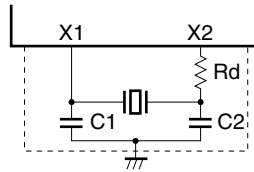
- Notes**
1. When not using A/D converter
  2. When using A/D converter

**Recommended Oscillator**

**Caution** For the resonator selection and oscillator constant of the μPD703003A(A) and 703025A(A), customers are requested to apply to the resonator manufacturer for evaluation.

(1) Ceramic resonator connection ( $T_A = -40$  to  $+85^\circ\text{C}$ )

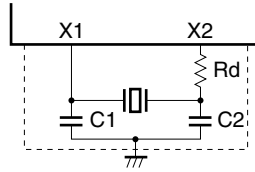
(a) μPD703003A, 703004A



Manufacturer	Part Number	Oscillation Frequency $f_{xx}$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms)
			C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC5.00B	5.0	On-chip	On-chip	680	4.5	5.5	0.14
	PBRC6.60B	6.6	On-chip	On-chip	—	4.5	5.5	0.08
TDK	CCR5.0MC3	5.0	On-chip	On-chip	—	4.5	5.5	0.19
	FCR5.0MC5	5.0	On-chip	On-chip	—	4.5	5.5	0.16
	CCR6.6MC3	6.6	On-chip	On-chip	—	4.5	5.5	0.17
Murata Mfg. Co., Ltd	CSA5.00MG040	5.0	100	100	—	4.5	5.5	0.32
	CST5.00MGW040	5.0	On-chip	On-chip	—	4.5	5.5	0.32
	CSA6.60MTZ040	6.6	100	100	—	4.5	5.5	0.72
	CST6.60MTW040	6.6	On-chip	On-chip	—	4.5	5.5	0.72

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the μPD703003A or 703004A and the resonator.

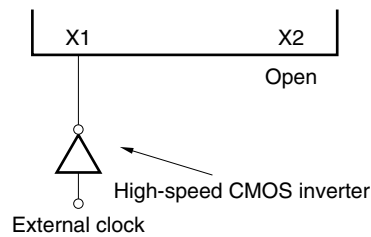
(b)  $\mu$ PD703025A



Manufacturer	Part Number	Oscillation Frequency $f_{xx}$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms)
			C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC4.00HR	4.0	On-chip	On-chip	—	4.5	5.5	0.08
	PBRC5.00HR	5.0	On-chip	On-chip	—	4.5	5.5	0.06
	PBRC6.00HR	6.0	On-chip	On-chip	—	4.5	5.5	0.08
	PBRC6.60HR	6.6	On-chip	On-chip	—	4.5	5.5	0.08
TDK	CCR4.0MC3	4.0	On-chip	On-chip	—	4.5	5.5	0.22
	CCR5.0MC3	5.0	On-chip	On-chip	—	4.5	5.5	0.28
Murata Mfg. Co., Ltd	CSA4.00MG040	4.0	100	100	—	4.5	5.5	0.40
	CST4.00MGW040	4.0	On-chip	On-chip	—	4.5	5.5	0.40
	CSTS0400MG06	4.0	On-chip	On-chip	—	4.5	5.5	0.16
	CSA6.60MTZ040	6.6	100	100	—	4.5	5.5	0.50
	CST6.60MTW040	6.6	On-chip	On-chip	—	4.5	5.5	0.50
	CSTS0660MG06	6.6	On-chip	On-chip	—	4.5	5.5	0.20

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the  $\mu$ PD703025A and the resonator.

(2) External clock input



- Cautions**
1. Put the high-speed CMOS inverter as close to the X1 pins as possible.
  2. Sufficiently evaluate the matching between the  $\mu$ PD703003A, 703004A, 703025A, 703003A(A), or 703025A(A) and the high-speed CMOS inverter.



DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 5.0 V ±10%, V<sub>SS</sub> = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH</sub>	Except for X1 and pins listed in <b>Note 1</b>		2.2		V <sub>DD</sub> + 0.3	V	
			<b>Note 1</b>	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	
Input voltage, low	V <sub>IL</sub>	Except for X1 and pins listed in <b>Note 1</b>		-0.5		+0.8	V	
			<b>Note 1</b>	-0.5		0.2V <sub>DD</sub>	V	
Clock input voltage, high	V <sub>XH</sub>	X1		0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.5	V	
Clock input voltage, low	V <sub>XL</sub>	X1		-0.5		+0.6	V	
Schmitt-triggered input Threshold voltage	V <sub>T+</sub> V <sub>T-</sub>	<b>Note 1</b> , rising edge			3.0		V	
		<b>Note 1</b> , falling edge			2.0		V	
Schmitt-triggered input hysteresis width	V <sub>T+</sub> - V <sub>T-</sub>	<b>Note 1</b>		0.5			V	
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA		0.7V <sub>DD</sub>			V	
		I <sub>OH</sub> = -100 μA		V <sub>DD</sub> - 0.4			V	
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 2.5 mA				0.45	V	
Input leakage current, high	I <sub>LIH</sub>	V <sub>I</sub> = V <sub>DD</sub>				10	μA	
Input leakage current, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V				-10	μA	
Output leakage current, high	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub>				10	μA	
Output leakage current, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V				-10	μA	
Software pull-up resistor	R	P35 to P37 and their alternate-function pins		15	40	90	kΩ	
Power supply current	μPD703003A, 703004A, 703003A(A)	When operating	I <sub>DD1</sub>	Direct mode		1.9 × φ + 5	2.1 × φ + 17	mA
				PLL mode		2.0 × φ + 7	2.2 × φ + 20	mA
		In HALT mode	I <sub>DD2</sub>	Direct mode		1.2 × φ + 5	1.3 × φ + 13	mA
				PLL mode		1.3 × φ + 7	1.4 × φ + 15	mA
		In IDLE mode	I <sub>DD3</sub>	Direct mode		8 × φ + 300	10 × φ + 500	μA
				PLL mode		0.1 × φ + 2	0.2 × φ + 3	mA
	In STOP mode	I <sub>DD4</sub>	<b>Note 2</b>		2	50	μA	
			<b>Note 3</b>		2	200	μA	
	μPD703025A, 703025A(A)	When operating	I <sub>DD1</sub>	Direct mode		2.5 × φ + 2	2.8 × φ + 16.5	mA
				PLL mode		2.6 × φ + 4	2.9 × φ + 19.5	mA
		In HALT mode	I <sub>DD2</sub>	Direct mode		1.3 × φ + 5	1.4 × φ + 13	mA
				PLL mode		1.3 × φ + 10	1.4 × φ + 18	mA
		In IDLE mode	I <sub>DD3</sub>	Direct mode		8 × φ + 300	10 × φ + 500	μA
				PLL mode		0.1 × φ + 2	0.2 × φ + 3	mA
In STOP mode		I <sub>DD4</sub>	<b>Note 2</b>		2	50	μA	
			<b>Note 3</b>		2	200	μA	

- Notes**
1. P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, RESET, NMI, MODE, and their alternate-function pins.
  2. -40°C ≤ T<sub>A</sub> ≤ +50°C
  3. 50°C < T<sub>A</sub> ≤ 85°C

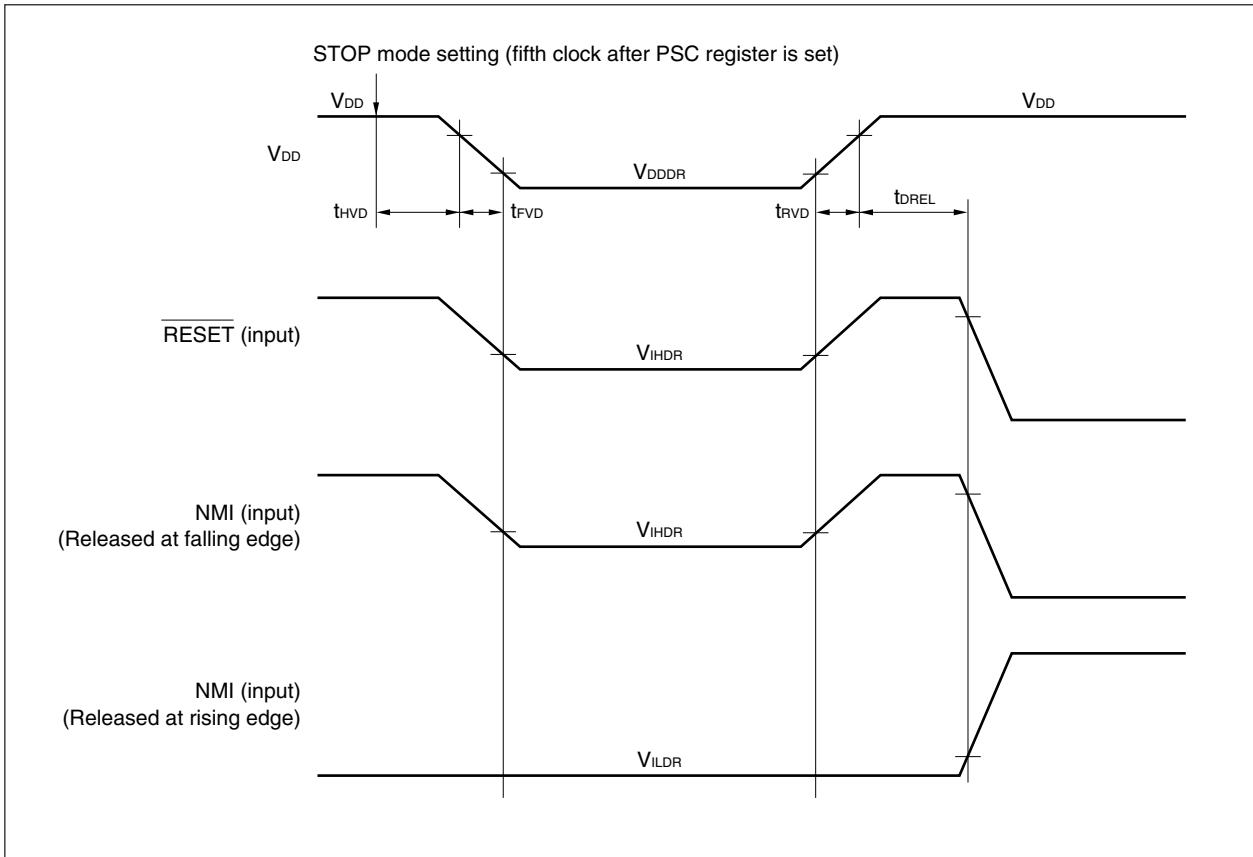
- Remarks**
1. TYP. values are reference values for when T<sub>A</sub> = 25°C (except for the conditions in **Note 3**) and V<sub>DD</sub> = 5.0 V. The power supply current does not include AV<sub>REF1</sub> to AV<sub>REF3</sub> or the current that flows through software pull-up resistors.
  2. φ = Internal system clock frequency

**Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = V<sub>DDDR</sub>)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V <sub>DDDR</sub>	STOP mode	1.5		5.5	V
Data retention current	I <sub>DDDR</sub>	<b>Note 1</b>		0.4V <sub>DDDR</sub>	50	μA
		<b>Note 2</b>		0.4V <sub>DDDR</sub>	200	μA
Power supply voltage rise time	t <sub>rvd</sub>		200			μs
Power supply voltage fall time	t <sub>fvd</sub>		200			μs
Power supply voltage hold time (vs. STOP mode setting)	t <sub>hvd</sub>		0			ms
STOP mode release signal input time	t <sub>drel</sub>	<b>Note 3</b>	0			ns
Data retention high-level input voltage	V <sub>IHDR</sub>	<b>Note 3</b>	0.9V <sub>DDDR</sub>		V <sub>DDDR</sub>	V
Data retention low-level input voltage	V <sub>ILDR</sub>		0		0.1V <sub>DDDR</sub>	V

- Notes**
1. -40°C ≤ T<sub>A</sub> ≤ +50°C
  2. 50°C < T<sub>A</sub> ≤ 85°C
  3. P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117,  $\overline{\text{RESET}}$ , NMI, MODE, X1, and their alternate-function pins.

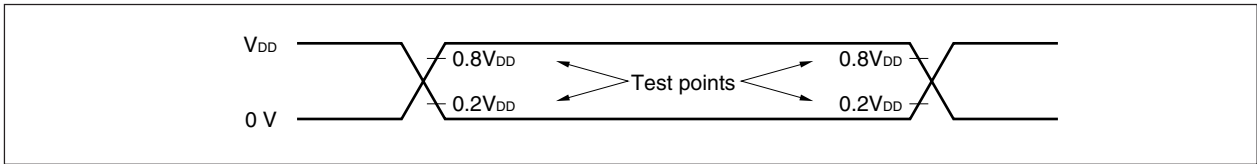
**Remark** TYP. values are reference values for when T<sub>A</sub> = 25°C (except for the conditions in **Note 2**) and V<sub>DD</sub> = 5.0 V.



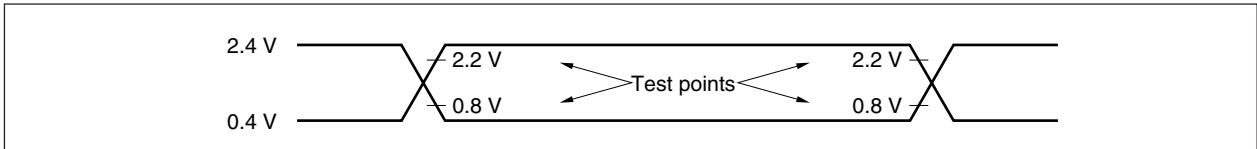
AC Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

AC test input test points

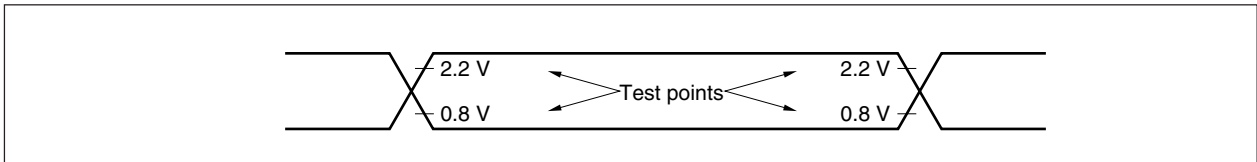
- (a) P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117,  $\overline{\text{RESET}}$ , NMI, MODE, X1, and their alternate-function pins



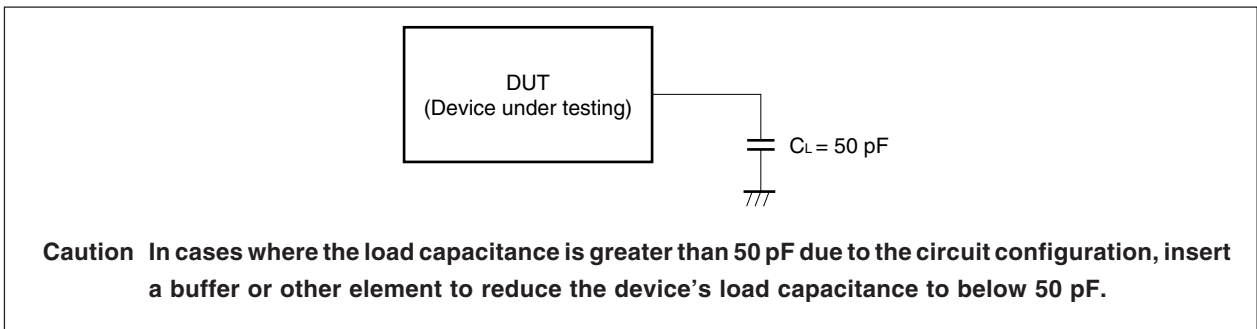
- (b) Pins other than those listed in (a) above



AC test output test points



Load condition

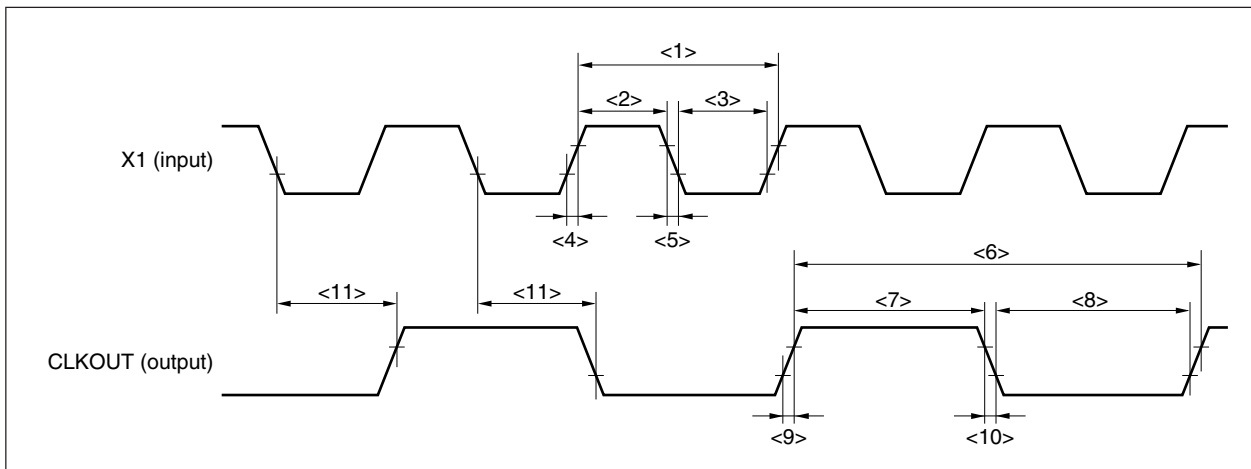


(1) Clock timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 input cycle	<1> t <sub>CYX</sub>	Direct mode	15	<b>Note 1</b>	ns
		PLL mode (PLL locked)	151 <sup>Note 2</sup>	<b>Note 3</b>	ns
X1 input high-level width	<2> t <sub>WXH</sub>	Direct mode	6		ns
		PLL mode	60		ns
X1 input low-level width	<3> t <sub>WXL</sub>	Direct mode	6		ns
		PLL mode	60		ns
X1 input rise time	<4> t <sub>XR</sub>	Direct mode		7	ns
		PLL mode		10	ns
X1 input fall time	<5> t <sub>XF</sub>	Direct mode		7	ns
		PLL mode		10	ns
CPU operating frequency	— φ		<b>Note 4</b>	33	MHz
CLKOUT output cycle	<6> t <sub>CYK</sub>		30	<b>Note 5</b>	ns
CLKOUT input high-level width	<7> t <sub>WKH</sub>		0.5T – 5		ns
CLKOUT input low-level width	<8> t <sub>WKL</sub>		0.5T – 5		ns
CLKOUT input rise time	<9> t <sub>KR</sub>			5	ns
CLKOUT input fall time	<10> t <sub>KF</sub>			5	ns
Delay time from X1↓ to CLKOUT	<11> t <sub>DXK</sub>	Direct mode	3	17	ns

- Notes**
1. When using A/D converter: 100 ns  
When not using A/D converter: 250 ns
  2. When using A/D converter: The value when φ = 5 × f<sub>XX</sub> and φ = f<sub>XX</sub> are set. Setting φ = 1/2 × f<sub>XX</sub> is prohibited.  
When not using A/D converter: The value when φ = 5 × f<sub>XX</sub>, φ = f<sub>XX</sub>, and φ = 1/2 × f<sub>XX</sub> are set.
  3. When using A/D converter: 250 ns (when φ = 5 × f<sub>XX</sub> is set) and 200 ns (when φ = f<sub>XX</sub> is set). Setting φ = 1/2 × f<sub>XX</sub> is prohibited.  
When not using A/D converter: 250 ns (when φ = 5 × f<sub>XX</sub>, φ = f<sub>XX</sub>, and φ = 1/2 × f<sub>XX</sub> are set).
  4. When using A/D converter: 5 MHz  
When not using A/D converter: 2 MHz
  5. When using A/D converter: 200 ns  
When not using A/D converter: 500 ns

**Remark** T = t<sub>CYK</sub>



(2) Input waveform

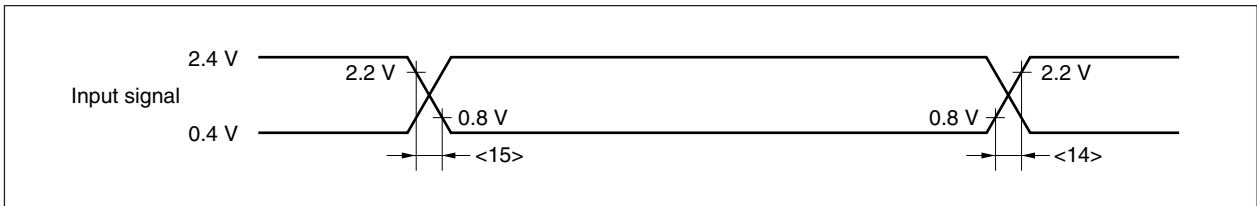
(a) P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, RESET, NMI, MODE, and their alternate-function pins

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input rise time	<12> $t_{IR2}$			20	ns
Input fall time	<13> $t_{IF2}$			20	ns



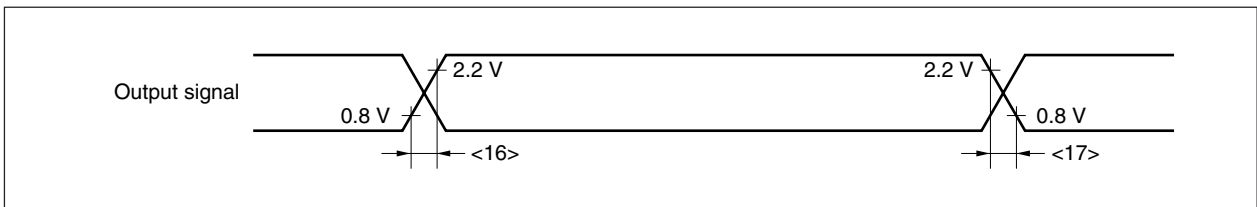
(b) Pins other than those listed in (a) above

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input rise time	<14> $t_{IR1}$			10	ns
Input fall time	<15> $t_{IF1}$			10	ns



(3) Output waveform (other than CLKOUT)

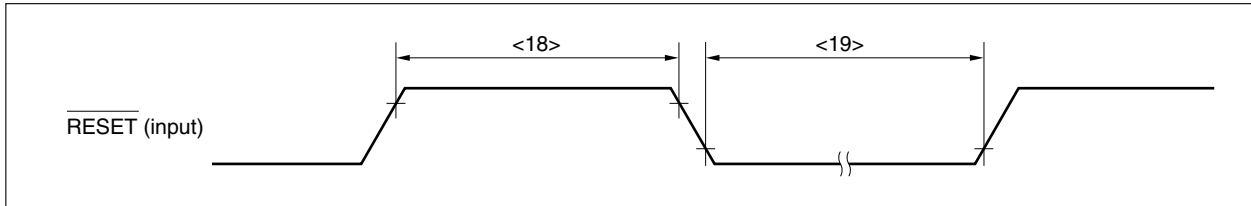
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	<16> $t_{OR}$			10	ns
Output fall time	<17> $t_{OF}$			10	ns



(4) Reset timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESET high-level width	<18> $t_{WRSH}$		500		ns
RESET low-level width	<19> $t_{WRSL}$	When power supply is ON and STOP mode has been released	$500 + T_{OST}$		ns
		Other than when power supply is ON and STOP mode has been released	500		ns

**Remark**  $T_{OST}$ : Oscillation stabilization time



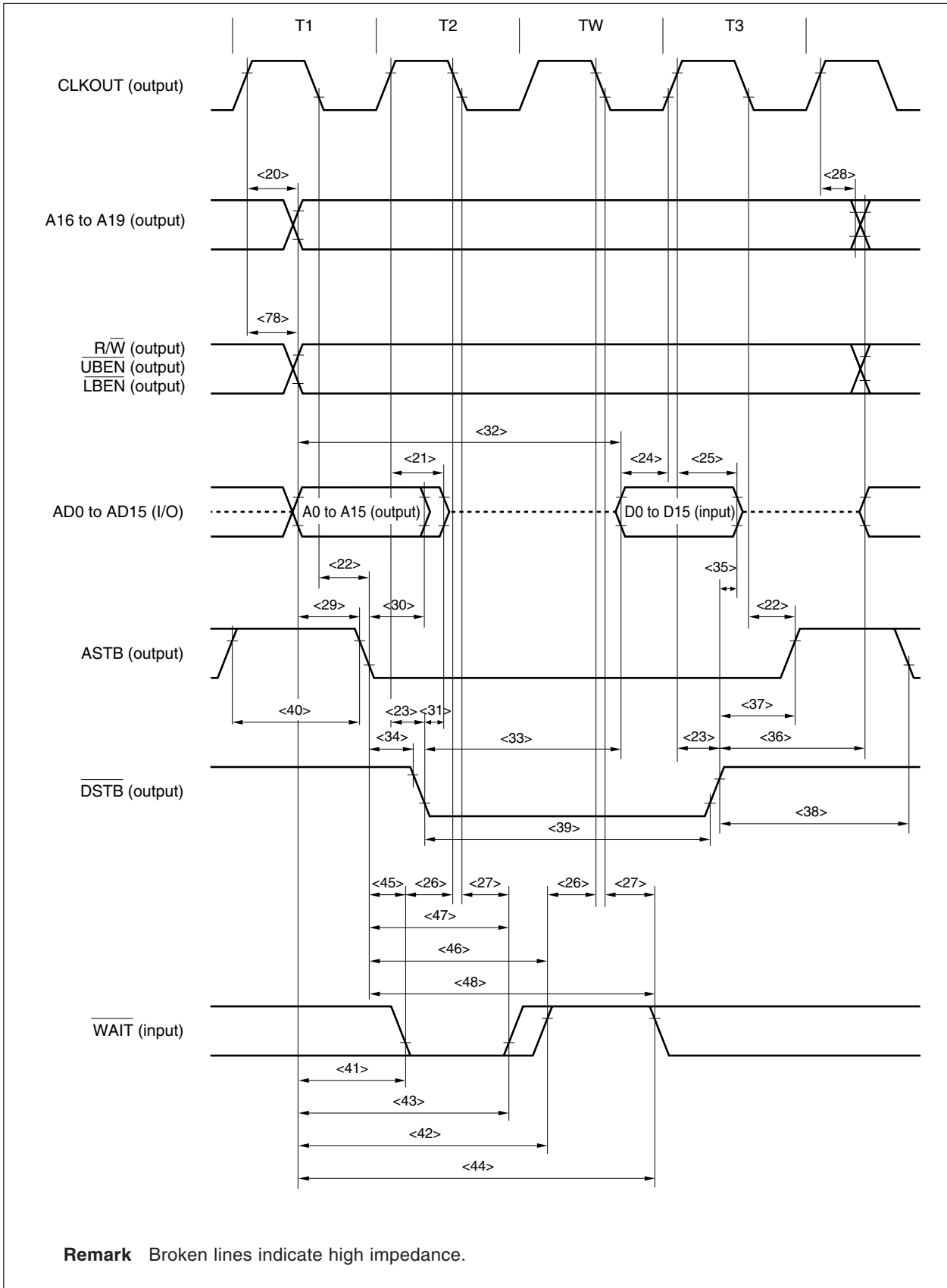
(5) Read timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<20> t <sub>DKA</sub>		3	20	ns
Delay time from CLKOUT↑ to R/W, $\overline{UBEN}$ , $\overline{LBEN}$	<78> t <sub>DKA2</sub>		-2	+13	ns
Delay time from CLKOUT↑ to address float	<21> t <sub>FKA</sub>		3	15	ns
Delay time from CLKOUT↓ to ASTB	<22> t <sub>DKST</sub>		3	15	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<23> t <sub>DKD</sub>		3	15	ns
Data input setup time (to CLKOUT↑)	<24> t <sub>SIDK</sub>		5		ns
Data input hold time (from CLKOUT↑)	<25> t <sub>HKID</sub>		5		ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<26> t <sub>SWTK</sub>		5		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<27> t <sub>HKWT</sub>		5		ns
Address hold time (from CLKOUT↑)	<28> t <sub>HKA</sub>		0		ns
Address setup time (to ASTB↓)	<29> t <sub>SAST</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C	0.5T - 10		ns
		70°C < T <sub>A</sub> ≤ 85°C	0.5T - 12		ns
Address hold time (from ASTB↓)	<30> t <sub>HSTA</sub>		0.5T - 10		ns
Delay time from $\overline{DSTB}$ ↓ to address float	<31> t <sub>FDA</sub>			0	ns
Data input setup time (to address)	<32> t <sub>SAID</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C		(2 + n)T - 22	ns
		70°C < T <sub>A</sub> ≤ 85°C		(2 + n)T - 25	ns
Data input setup time (to $\overline{DSTB}$ ↓)	<33> t <sub>SDID</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C		(1 + n)T - 20	ns
		70°C < T <sub>A</sub> ≤ 85°C		(1 + n)T - 24	ns
Delay time from ASTB↓ to $\overline{DSTB}$ ↓	<34> t <sub>DSTD</sub>		0.5T - 10		ns
Data input hold time (from $\overline{DSTB}$ ↑)	<35> t <sub>HDID</sub>		0		ns
Delay time from $\overline{DSTB}$ ↑ to address output	<36> t <sub>DDA</sub>		(1 + i)T		ns
Delay time from $\overline{DSTB}$ ↑ to ASTB↑	<37> t <sub>DDSTH</sub>		0.5T - 10		ns
Delay time from $\overline{DSTB}$ ↑ to ASTB↓	<38> t <sub>DDSTL</sub>		(1.5 + i)T - 10		ns
$\overline{DSTB}$ low-level width	<39> t <sub>WDL</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C	(1 + n)T - 10		ns
		70°C < T <sub>A</sub> ≤ 85°C	(1 + n)T - 13		ns
ASTB high-level width	<40> t <sub>WSTH</sub>		T - 10		ns
$\overline{WAIT}$ setup time (to address)	<41> t <sub>SAWT1</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		1.5T - 20	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		1.5T - 24	ns
	<42> t <sub>SAWT2</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		(1.5 + n)T - 20	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		(1.5 + n)T - 24	ns
$\overline{WAIT}$ hold time (from address)	<43> t <sub>HAWT1</sub>	n ≥ 1	(0.5 + n)T		ns
	<44> t <sub>HAWT2</sub>	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<45> t <sub>SSWT1</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		T - 18	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		T - 20	ns
	<46> t <sub>SSWT2</sub>	n ≥ 1		(1 + n)T - 15	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<47> t <sub>HSTWT1</sub>	n ≥ 1	nT		ns
	<48> t <sub>HSTWT2</sub>	n ≥ 1	(1 + n)T		ns

Remarks 1. T = t<sub>CYK</sub>

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.
3. i indicates the number of idle states (0 or 1) that are inserted after a read cycle.
4. Maintain at least one of the two data input hold times, either t<sub>HKID</sub> (<25>) or t<sub>HDID</sub> (<35>).

(5) Read timing (2/2): 1 wait





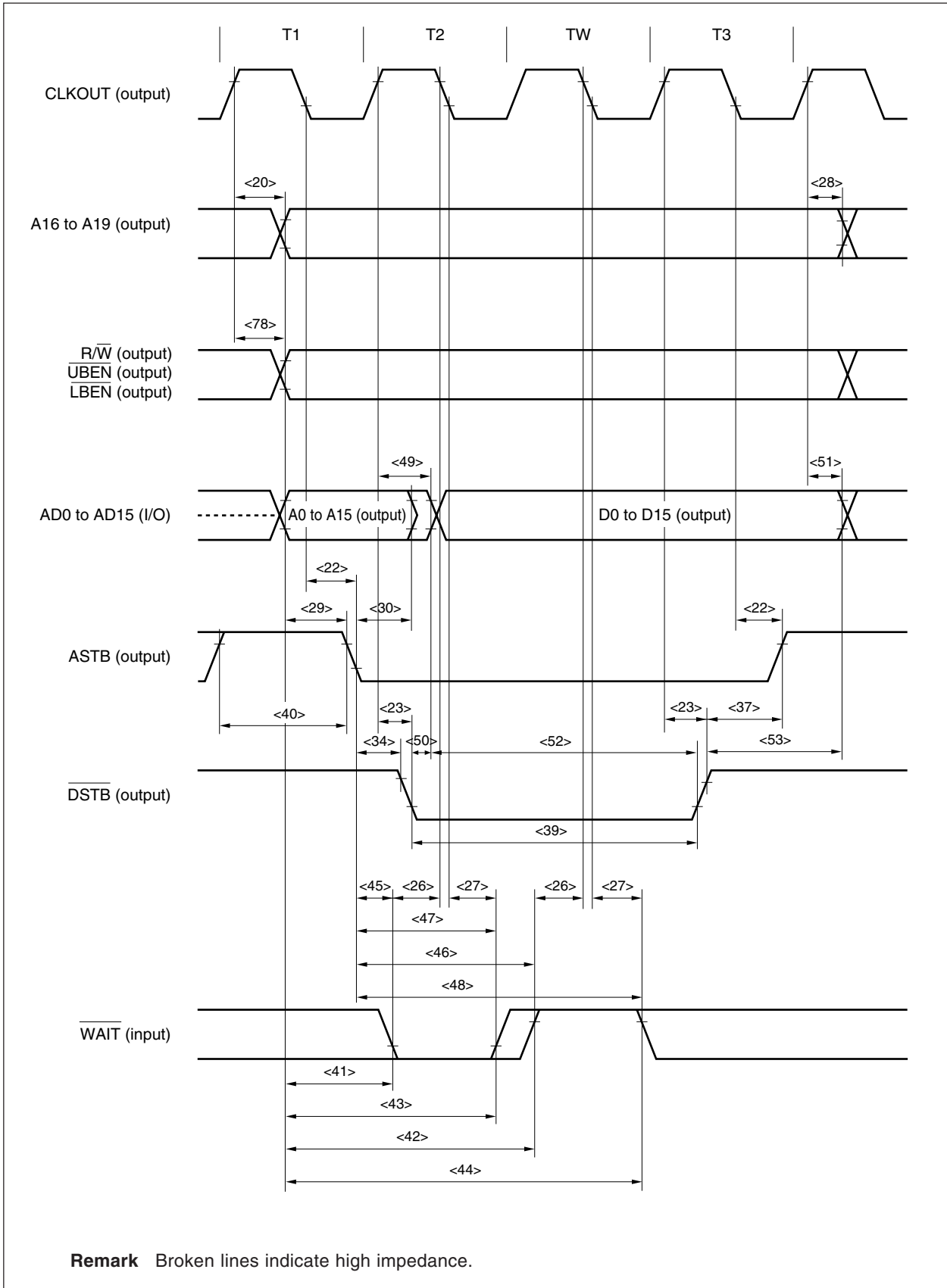
(6) Write timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<20> t <sub>DKA</sub>		3	20	ns
Delay time from CLKOUT↑ to R/W, UBEN, LBEN	<78> t <sub>DKA2</sub>		-2	+13	ns
Delay time from CLKOUT↓ to ASTB	<22> t <sub>DKST</sub>		3	15	ns
Delay time from CLKOUT↑ to DSTB	<23> t <sub>DKD</sub>		3	15	ns
WAIT setup time (to CLKOUT↓)	<26> t <sub>SWTK</sub>		5		ns
WAIT hold time (from CLKOUT↓)	<27> t <sub>HKWT</sub>		5		ns
Address hold time (from CLKOUT↑)	<28> t <sub>HKA</sub>		0		ns
Address setup time (to ASTB↓)	<29> t <sub>SAST</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C	0.5T - 10		ns
		70°C < T <sub>A</sub> ≤ 85°C	0.5T - 12		ns
Address hold time (from ASTB↓)	<30> t <sub>HSTA</sub>		0.5T - 10		ns
Delay time from ASTB↓ to DSTB↓	<34> t <sub>DSTD</sub>		0.5T - 10		ns
Delay time from DSTB↓ to ASTB↓	<37> t <sub>DDSTH</sub>		0.5T - 10		ns
DSTB low-level width	<39> t <sub>WDL</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C	(1 + n)T - 10		ns
		70°C < T <sub>A</sub> ≤ 85°C	(1 + n)T - 13		ns
ASTB high-level width	<40> t <sub>WSTH</sub>		T - 10		ns
WAIT setup time (to address)	<41> t <sub>SAWT1</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		1.5T - 20	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		1.5T - 24	ns
	<42> t <sub>SAWT2</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		(1.5 + n)T - 20	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		(1.5 + n)T - 24	ns
WAIT hold time (from address)	<43> t <sub>HAWT1</sub>	n ≥ 1	(0.5 + n)T		ns
	<44> t <sub>HAWT2</sub>	n ≥ 1	(1.5 + n)T		ns
WAIT setup time (to ASTB↓)	<45> t <sub>SSWT1</sub>	n ≥ 1, -40°C ≤ T <sub>A</sub> ≤ +70°C		T - 18	ns
		n ≥ 1, 70°C < T <sub>A</sub> ≤ 85°C		T - 20	ns
	<46> t <sub>SSWT2</sub>	n ≥ 1		(1 + n)T - 15	ns
WAIT hold time (from ASTB↓)	<47> t <sub>HSTWT1</sub>	n ≥ 1	nT		ns
	<48> t <sub>HSTWT2</sub>	n ≥ 1	(1 + n)T		ns
Address hold time (from CLKOUT↑)	<49> t <sub>DKOD</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C		20	ns
		70°C < T <sub>A</sub> ≤ 85°C		23	ns
Delay time from DSTB↓ to data output	<50> t <sub>DDOD</sub>			10	ns
Data output hold time (from CLKOUT↑)	<51> t <sub>HKOD</sub>		0		ns
Data output setup time (to DSTB↑)	<52> t <sub>SODD</sub>		(1 + n)T - 15		ns
Data output hold time (from DSTB↑)	<53> t <sub>HDOD</sub>		T - 10		ns

Remarks 1. T = t<sub>cyk</sub>

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

(6) Write timing (2/2): 1 wait



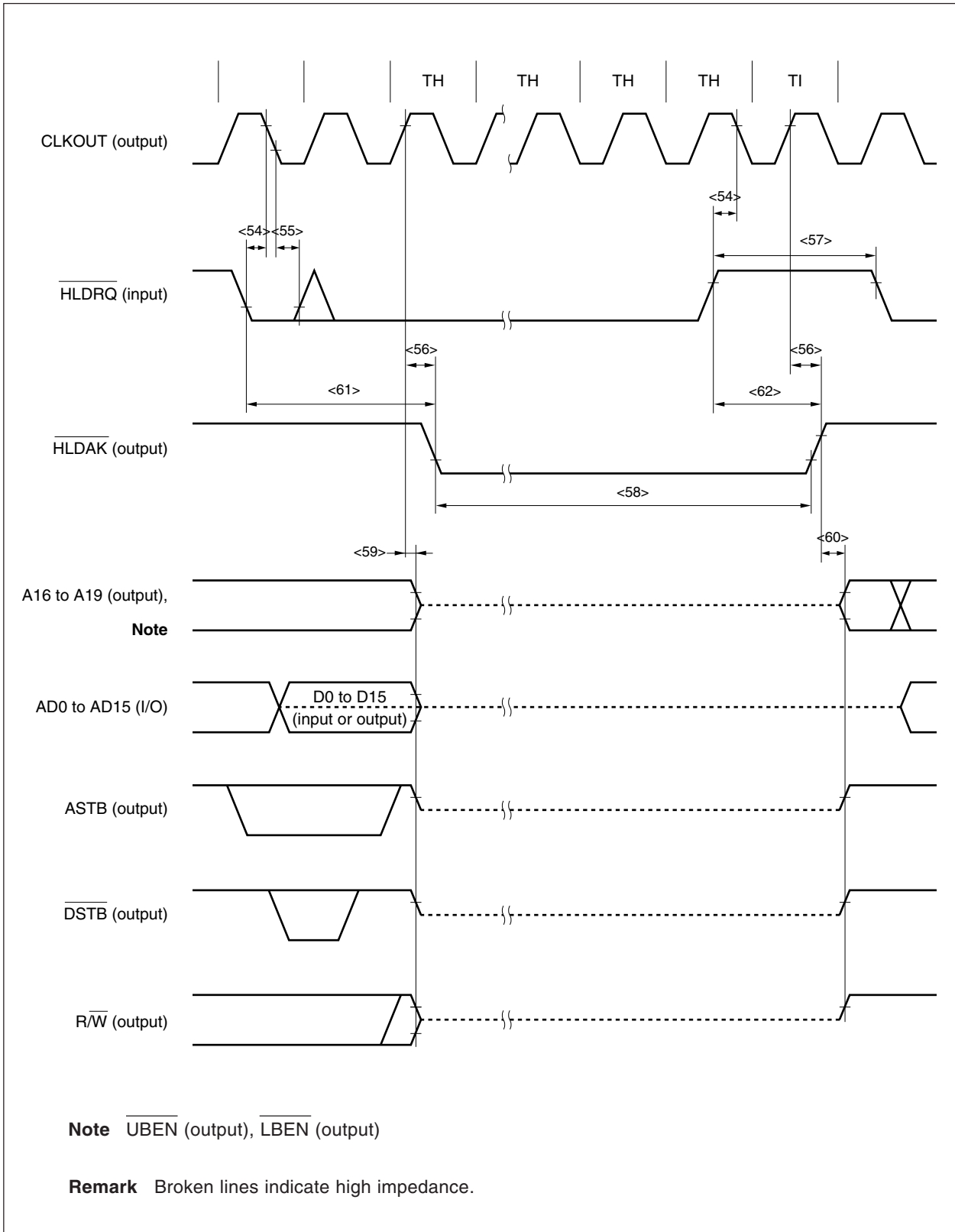
(7) Bus hold timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Units
HLD $\overline{RQ}$ setup time (to CLKOUT $\downarrow$ )	<54> t <sub>SHQK</sub>		5		ns
HLD $\overline{RQ}$ hold time (from CLKOUT $\downarrow$ )	<55> t <sub>HKHQ</sub>		5		ns
HLD $\overline{AK}$ delay time from CLKOUT $\uparrow$	<56> t <sub>DKHA</sub>			20	ns
HLD $\overline{RQ}$ high-level width	<57> t <sub>WHQH</sub>		T + 10		ns
HLD $\overline{AK}$ low-level width	<58> t <sub>WHAL</sub>	-40°C ≤ T <sub>A</sub> ≤ +70°C	T - 10		ns
		70°C < T <sub>A</sub> ≤ 85°C	T - 12		ns
Delay time from CLKOUT $\uparrow$ to bus float	<59> t <sub>DKF</sub>			20	ns
Delay time from HLD $\overline{AK}$ $\uparrow$ to bus output	<60> t <sub>DHAC</sub>		-3		ns
Delay time from HLD $\overline{RQ}$ $\downarrow$ to HLD $\overline{AK}$ $\downarrow$	<61> t <sub>DHQHA1</sub>			(2n + 7.5)T + 20	ns
Delay time from HLD $\overline{RQ}$ $\uparrow$ to HLD $\overline{AK}$ $\uparrow$	<62> t <sub>DHQHA2</sub>		0.5T	1.5T + 20	ns

**Remarks** 1. T = t<sub>CYK</sub>

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

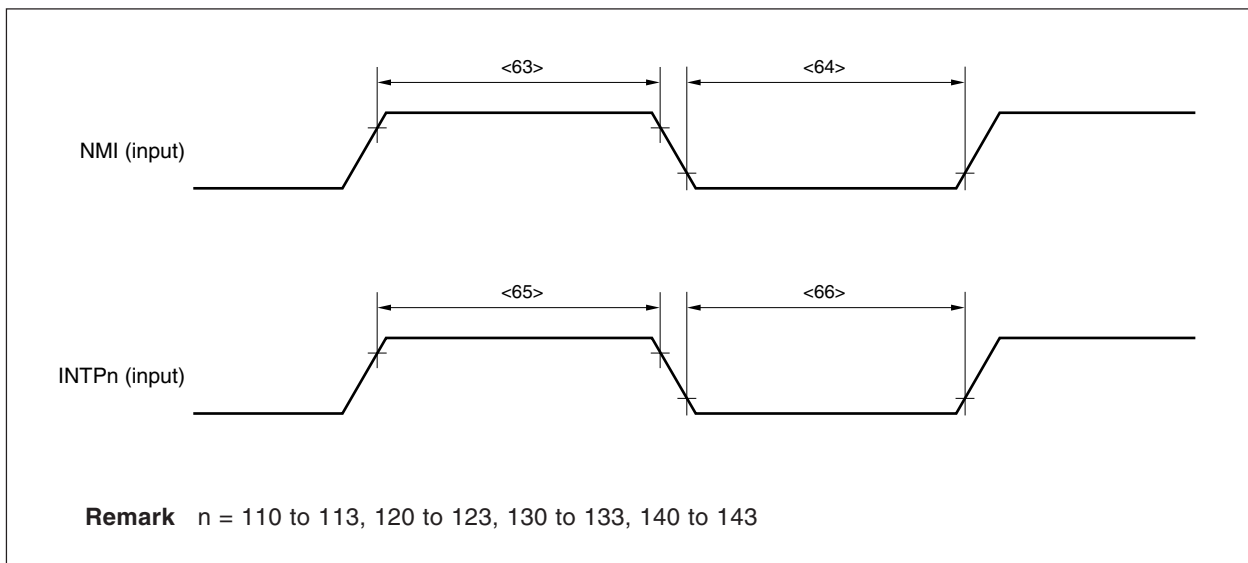
(7) Bus hold timing (2/2)



(8) Interrupt timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high-level width	<63> $t_{WNIH}$		500		ns
NMI low-level width	<64> $t_{WNIL}$		500		ns
INTPn high-level width	<65> $t_{WITH}$	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		ns
INTPn low-level width	<66> $t_{WITL}$	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		ns

**Remark** T =  $t_{CYK}$



(9) CSI timing (1/2)

(a) Master mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<67> $t_{CYSK1}$	Output	120		ns
$\overline{SCKn}$ high-level width	<68> $t_{WSKH1}$	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<69> $t_{WSKL1}$	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<70> $t_{SSISK1}$		30		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<71> $t_{HSKS11}$		0		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<72> $t_{DSKSO1}$			18	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<73> $t_{HSKSO1}$		$0.5t_{CYSK1} - 5$		ns

**Remark** n = 0 to 2

(ii) Timing of CSI3

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK3}$ cycle	<67> $t_{CYSK3}$	Output	500		ns
$\overline{SCK3}$ high-level width	<68> $t_{WSKH3}$	Output			
$\overline{SCK3}$ low-level width	<69> $t_{WSKL3}$	Output			
SI3 setup time (to $\overline{SCK3}\uparrow$ )	<70> $t_{SSISK3}$		100		ns
SI3 hold time (from $\overline{SCK3}\uparrow$ )	<71> $t_{HSKS13}$		50		ns
SO3 output delay time (from $\overline{SCK3}\downarrow$ )	<72> $t_{DSKSO3}$	$R_L = 1.5\text{ k}\Omega$		150	ns
SO3 output hold time (from $\overline{SCK3}\uparrow$ )	<73> $t_{HSKSO3}$	$C_L = 50\text{ pF}$	$0.5t_{CYSK3} - 5$		ns

**Remark**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the  $\overline{SCK3}$  and SO3 output lines.

(b) Slave mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<67> $t_{CYSK2}$	Input	120		ns
$\overline{SCKn}$ high-level width	<68> $t_{WSKH2}$	Input	30		ns
$\overline{SCKn}$ low-level width	<69> $t_{WSKL2}$	Input	30		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<70> $t_{SSISK2}$		10		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<71> $t_{HSKS12}$		10		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<72> $t_{DSKSO2}$			30	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<73> $t_{HSKSO2}$		$t_{WSKH2}$		ns

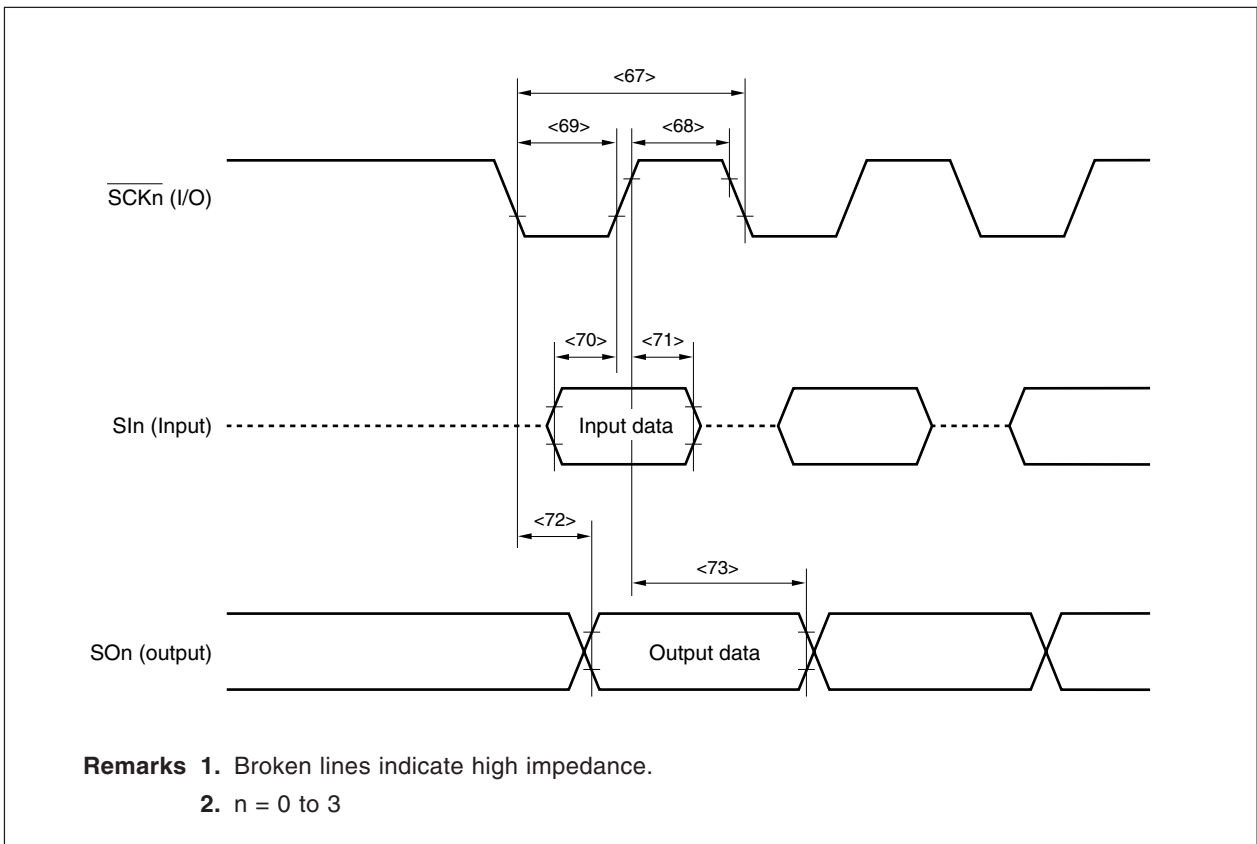
**Remark** n = 0 to 2

(9) CSI timing (2/2)

(ii) Timing of CSI3

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle	<67> $t_{\text{CYSK4}}$	Input	500		ns
$\overline{\text{SCK3}}$ high-level width	<68> $t_{\text{WSKH4}}$	Input	180		ns
$\overline{\text{SCK3}}$ low-level width	<69> $t_{\text{WSKL4}}$	Input	180		ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$ )	<70> $t_{\text{SSISK4}}$		100		ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$ )	<71> $t_{\text{HSKSI4}}$		50		ns
SO3 output delay time (from $\overline{\text{SCK3}}\downarrow$ )	<72> $t_{\text{DSKSO4}}$	$R_L = 1.5 \text{ k}\Omega$ $C_L = 50 \text{ pF}$		150	ns
SO3 output hold time (from $\overline{\text{SCK3}}\uparrow$ )	<73> $t_{\text{HSKSO4}}$		$t_{\text{WSKH4}}$		ns

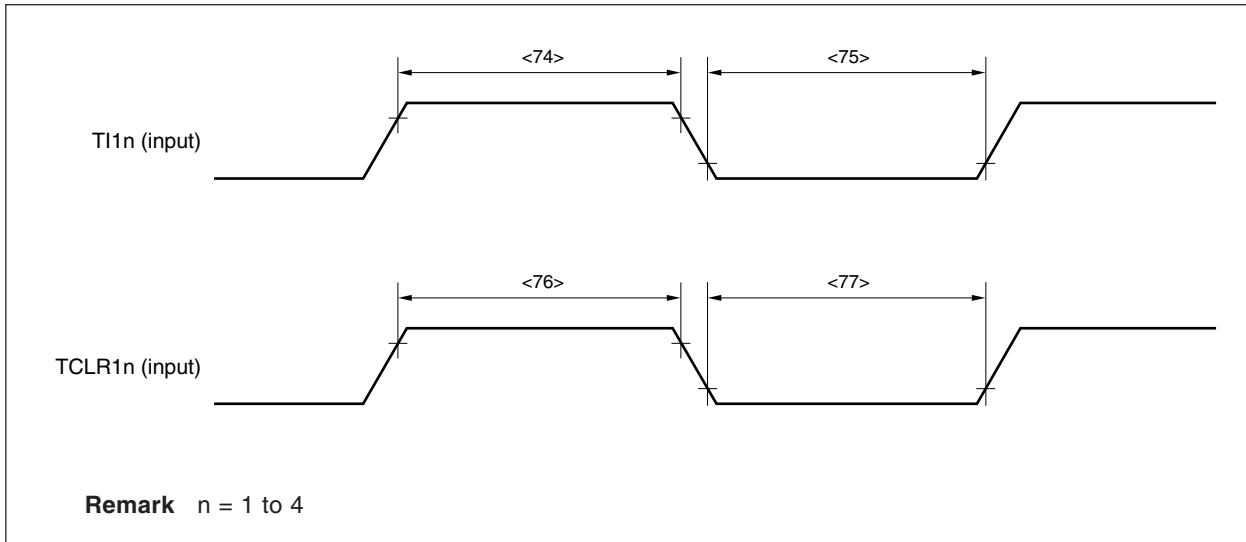
**Remark**  $R_L$  and  $C_L$  are the load resistance and load capacitance of the  $\overline{\text{SCK3}}$  and SO3 output lines.



(10) RPU timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
T11n high-level width	<74> $t_{WTH}$		$3T + 10$		ns
T11n low-level width	<75> $t_{WTL}$		$3T + 10$		ns
TCLR1n high-level width	<76> $t_{WCH}$		$3T + 10$		ns
TCLR1n low-level width	<77> $t_{WCL}$		$3T + 10$		ns

**Remark** T =  $t_{CYK}$





**A/D Converter Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = AV<sub>DD</sub> = 5 V ±10%, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—		10	10	10	bit
Overall error <sup>Note 1</sup>	—	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>			±0.4	%FSR
	—	3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>			±0.7	%FSR
Quantization error	—				±1/2	LSB
Conversion time	t <sub>CONV</sub>	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>	60			t <sub>CYK</sub>
		3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>	60			t <sub>CYK</sub>
Sampling time	t <sub>SAMP</sub>	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>	10			t <sub>CYK</sub>
		3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>	10			t <sub>CYK</sub>
Zero-scale error <sup>Note 1</sup>	—	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±3.5	LSB
	—	3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±4.5	LSB
Full-scale error <sup>Note 1</sup>	—	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±2.5	LSB
	—	3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±4.5	LSB
Non-linearity error <sup>Note 1</sup>	—	4.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±2.5	LSB
	—	3.5 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>		±1.5	±4.5	LSB
Analog input voltage <sup>Note 2</sup>	V <sub>IAN</sub>		-0.3		AV <sub>DD</sub> + 0.3	V
Reference voltage	AV <sub>REF1</sub>		3.5		AV <sub>DD</sub>	V
AV <sub>REF1</sub> current	AI <sub>REF1</sub>			1.2	3.0	mA
AV <sub>DD</sub> supply current	AI <sub>DD</sub>			2.3	6.0	mA

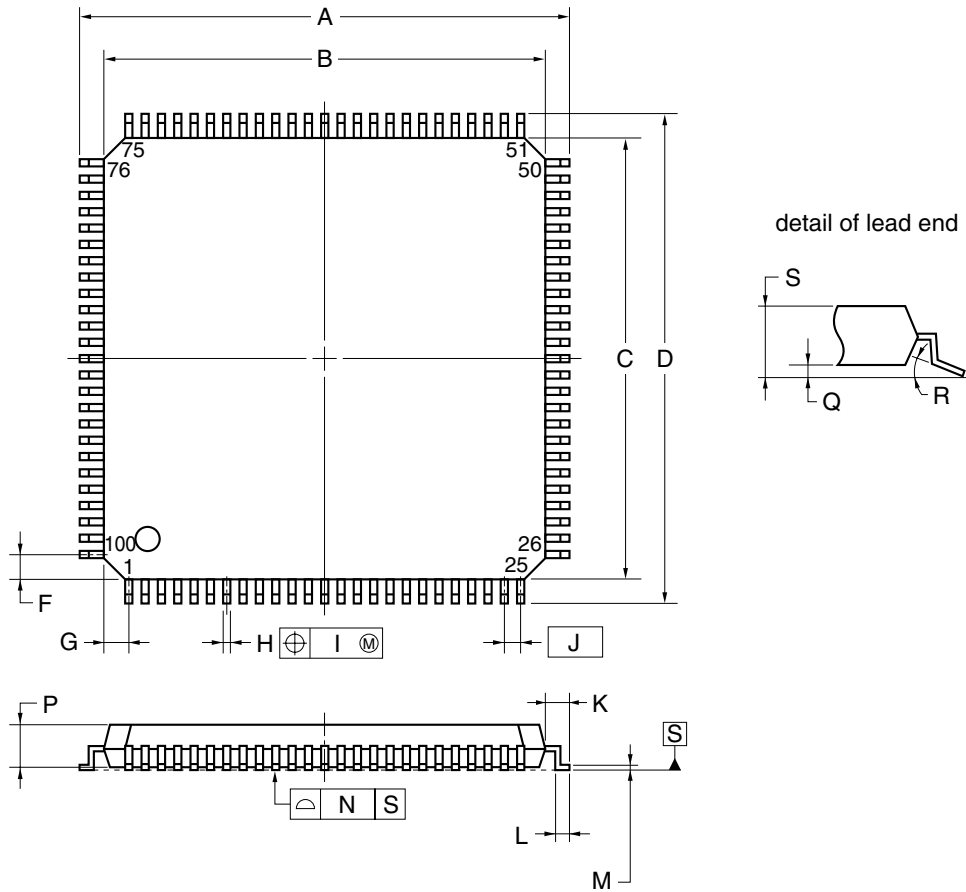
- Notes**
1. Excludes quantization error.
  2. When V<sub>IAN</sub> = 0, the conversion result becomes 000H.  
 When 0 < V<sub>IAN</sub> < AV<sub>REF1</sub>, conversion has 10-bit resolution.  
 When AV<sub>REF1</sub> ≤ V<sub>IAN</sub> ≤ AV<sub>DD</sub>, the conversion result becomes 3FFH.

D/A Converter Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—		8	8	8	bit
Overall error	—	Load condition: 2 M $\Omega$ , 30 pF $AV_{REF2} = V_{DD}$ $AV_{REF3} = 0$			0.8	%
	—	Load condition: 2 M $\Omega$ , 30 pF $AV_{REF2} = 0.75V_{DD}$ $AV_{REF3} = 0.25V_{DD}$			1.0	%
	—	Load condition: 4 M $\Omega$ , 30 pF $AV_{REF2} = V_{DD}$ $AV_{REF3} = 0$			0.6	%
	—	Load condition: 4 M $\Omega$ , 30 pF $AV_{REF2} = 0.75V_{DD}$ $AV_{REF3} = 0.25V_{DD}$			0.8	%
Settling time	—	Load condition: 2 M $\Omega$ , 30 pF			10	$\mu\text{s}$
Output resistance	RO			8		k $\Omega$
$AV_{REF2}$ input voltage	$AV_{REF2}$		$0.75V_{DD}$		$V_{DD}$	V
$AV_{REF3}$ input voltage	$AV_{REF3}$		0		$0.25V_{DD}$	V
Resistance between $AV_{REF2}$ and $AV_{REF3}$	$R_{AIREF}$	DACS0, DACS1 = 55H	2	4		k $\Omega$

★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 <sup>+0.05</sup> <sub>-0.04</sub>
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° <sup>+7°</sup> <sub>-3°</sub>
S	1.60 MAX.

**S100GC-50-8EU, 8EA-2**

5. RECOMMENDED SOLDERING CONDITIONS

The μPD703003A, 703004A, 703025A, 703003A(A), and 703025A(A) should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representatives.

★ **Table 5-1. Soldering Conditions**

- μPD703003AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD703004AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD703025AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD703003AGC(A)-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD703025AGC(A)-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

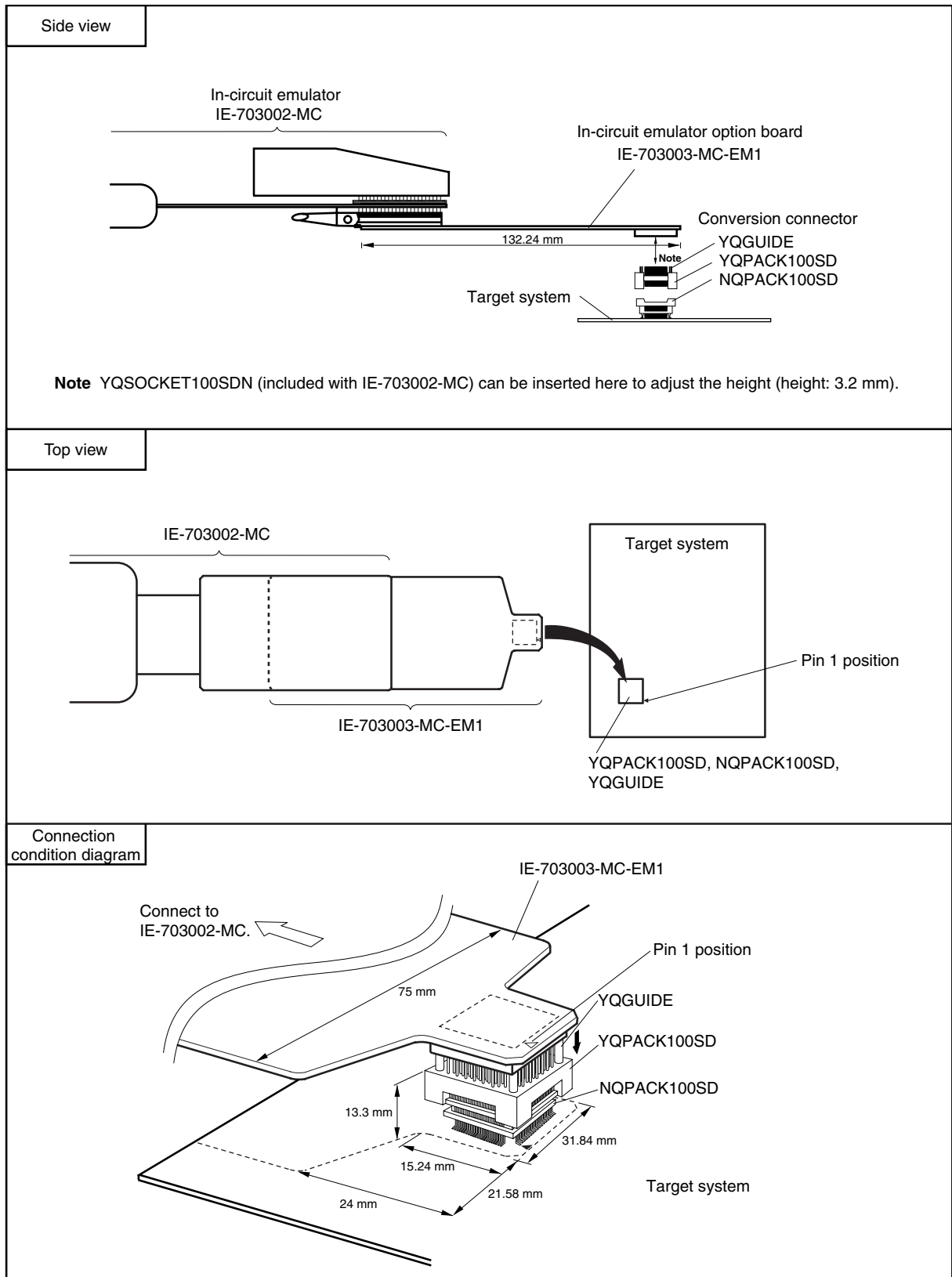
Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time 3 seconds max. (per pin row)	—

**Note** After opening a dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

★ APPENDIX NOTES ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.



## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**RELATED DOCUMENTS**  $\mu$ PD70F3003A, 70F3025A, 70F3003A(A) Data Sheet (U13189E)

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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