ELPIDA

DATA SHEET

2G bits GDDR5 SGRAM

EDW2032BBBG (64M words x 32 bits)

Specifications

- Density: 2G bits
- Organization
— 4Mbit x 32 I/O x 16 banks
— 8Mbit x 16 I/O x 16 banks
- Package
— 170-ball FBGA
— Lead-free (RoHS compliant) and Halogen-free
- Power supply:
— VDD: 1.6V/1.5V ± 3% and 1.35V ± 3%
— VDDQ: 1.6V/1.5V ± 3% and 1.35V ± 3%
- Data rate: 7.0Gbps/6.0Gbps/5.0Gbps (max.)
- 16 internal banks
- Four bank groups for tCCDL = 3tCK
- 8n prefetch architecture: 256 bit per array Read or Write access for x32; 128 bit for x16
- Burst length (BL): 8 only
- Programmable CAS latency: 6 to 20
- Programmable Write latency: 3 to 7
- Programmable CRC READ latency: 1 to 3
- Programmable CRC WRITE latency: 8 to 14
- Programmable EDC hold pattern for CDR
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 16384 cycles/32ms
- Interface: Pseudo open drain (POD-15)
- On-die termination (ODT): nom. values of 60Ω or 120Ω
- Pseudo open drain (POD-15) compatible outputs
— 40Ω pulldown
— 60Ω pullup
- ODT and output driver strength auto-calibration with external resistor ZQ pin (120Ω)
- Programmable termination and driver strength offsets
- Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
- Separate external VREF for address / command inputs
- Operating case temperature range
— TC = 0°C to +95°C

Features

- x32/x16 mode configuration set at power-up with EDC pin
- Single ended interface for data, address and command
- Quarter data-rate differential clock inputs CK, /CK for address and commands
- Two half data-rate differential clock inputs WCK, /WCK, each associated with two data bytes (DQ, /DBI, EDC)
- Double Data Rate (DDR) data (WCK)
- Single Data Rate (SDR) command (CK)
- Double Data Rate (DDR) addressing (CK)
- Write data mask function via address bus (single/double byte mask)
- Data Bus Inversion (DBI) and Address Bus Inversion (ABI)
- Input/output PLL on/off mode
- Duty cycle corrector (DCC) for data clock (WCK)
- Address training: address input monitoring via DQ pins
- WCK2CK clock training: phase information via EDC pins
- Data read and write training via Read FIFO (FIFO depth = 6)
- Read FIFO pattern preload by LDFF command
- Direct write data load to Read FIFO by WRTR command
- Consecutive read of Read FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic redundancy check (CRC–8)
- Read/Write EDC on/off mode
- DQ Preamble for Read on/off mode
- Low Power modes
- RDQS mode on EDC pin
- On-chip temperature sensor with read-out
- Automatic temperature sensor controlled self-refresh rate
- Digital tRAS lockout
- Vendor ID, FIFO depth and Density info fields for identification
- Mirror function with MF pin
- Boundary Scan function with SEN pin

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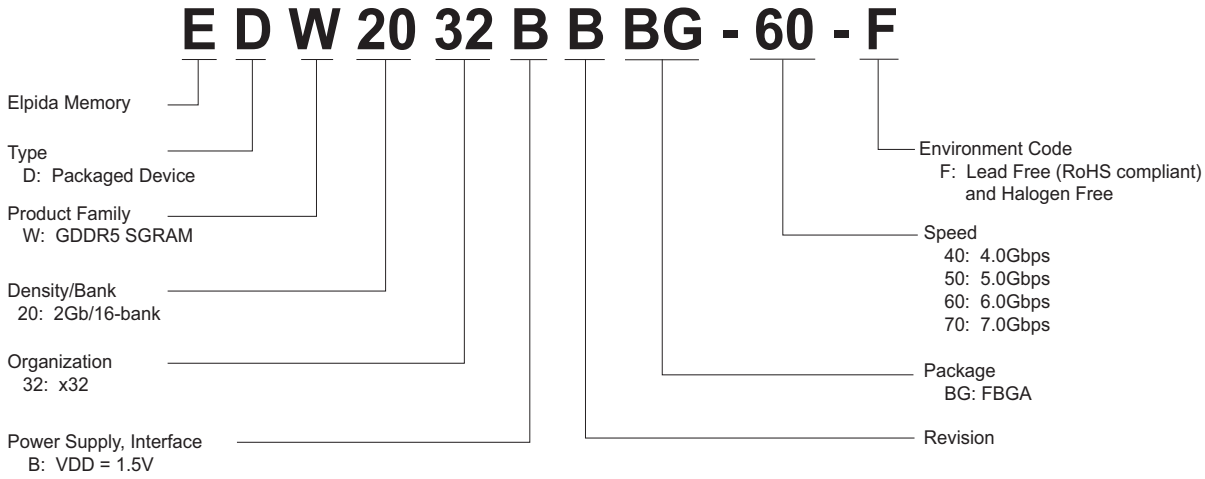
Ordering Information

Part number	Organization (words x bits)	VDD, VDDQ	Max. Data Rate	Package
EDW2032BBBG-40-F	64M x 32	1.5V / 1.35V	4.0Gbps / 3.2Gbps	170-ball FBGA
EDW2032BBBG-50-F		1.5V / 1.35V	5.0Gbps / 4.0Gbps	
EDW2032BBBG-60-F		1.6V / 1.35V	6.0Gbps / 4.0Gbps	
EDW2032BBBG-70-F		1.6V / 1.35V	7.0Gbps / 4.0Gbps	

Part Number



Pin Configuration

170-ball FBGA (MF=0 Configuration)

1	2	3	4	5	6	7	8	9	10	11	12	13	14
VSSQ	DQ1	VSSQ	DQ0	NC		A			VREFD	DQ8	VSSQ	DQ9	VSSQ
VDDQ	DQ3	VDDQ	DQ2	VSS		B			VSS	DQ10	VDDQ	DQ11	VDDQ
VSSQ	EDC0	VSSQ	VSSQ	VDD		C			VDD	VSSQ	VSSQ	EDC1	VSSQ
VDDQ	/DBI0	VDDQ	WCK01	/WCK01		D			VSS	VDD	VDDQ	/DBI1	VDDQ
VSSQ	DQ5	VSSQ	DQ4	VDDQ		E			VDDQ	DQ12	VSSQ	DQ13	VSSQ
VDDQ	DQ7	VDDQ	DQ6	VSSQ		F			VSSQ	DQ14	VDDQ	DQ15	VDDQ
VDD	VDDQ	/RAS	VDD	VSS		G			VSS	VDD	/CS	VDDQ	VDD
VSS	VSSQ	VDDQ	A10 A0	A9 A1		H			BA3 A3	BA0 A2	VDDQ	VSSQ	VSS
MF	/RESET	/CKE	/ABI	A12 RFU		J			SEN	/CK	CK	ZQ	VREFC
VSS	VSSQ	VDDQ	A8 A7	A11 A6		K			BA1 A5	BA2 A4	VDDQ	VSSQ	VSS
VDD	VDDQ	/CAS	VDD	VSS		L			VSS	VDD	/WE	VDDQ	VDD
VDDQ	DQ31	VDDQ	DQ30	VSSQ		M			VSSQ	DQ22	VDDQ	DQ23	VDDQ
VSSQ	DQ29	VSSQ	DQ28	VDDQ		N			VDDQ	DQ20	VSSQ	DQ21	VSSQ
VDDQ	/DBI3	VDDQ	WCK23	/WCK23		P			VSS	VDD	VDDQ	/DBI2	VDDQ
VSSQ	EDC3	VSSQ	VSSQ	VDD		R			VDD	VSSQ	VSSQ	EDC2	VSSQ
VDDQ	DQ27	VDDQ	DQ26	VSS		T			VSS	DQ18	VDDQ	DQ19	VDDQ
VSSQ	DQ25	VSSQ	DQ24	NC		U			VREFD	DQ16	VSSQ	DQ17	VSSQ

□ = pin is OFF in x16 mode

(Top View)

170-ball FBGA (MF=1 Configuration)

1	2	3	4	5	6	7	8	9	10	11	12	13	14
VSSQ	DQ25	VSSQ	DQ24	NC		A			VREFD	DQ16	VSSQ	DQ17	VSSQ
VDDQ	DQ27	VDDQ	DQ26	VSS		B			VSS	DQ18	VDDQ	DQ19	VDDQ
VSSQ	EDC3	VSSQ	VSSQ	VDD		C			VDD	VSSQ	VSSQ	EDC2	VSSQ
VDDQ	/DBI3	VDDQ	WCK23	/WCK23		D			VSS	VDD	VDDQ	/DBI2	VDDQ
VSSQ	DQ29	VSSQ	DQ28	VDDQ		E			VDDQ	DQ20	VSSQ	DQ21	VSSQ
VDDQ	DQ31	VDDQ	DQ30	VSSQ		F			VSSQ	DQ22	VDDQ	DQ23	VDDQ
VDD	VDDQ	/CAS	VDD	VSS		G			VSS	VDD	/WE	VDDQ	VDD
VSS	VSSQ	VDDQ	A8 A7	A11 A6		H			BA1 A5	BA2 A4	VDDQ	VSSQ	VSS
MF	/RESET	/CKE	/ABI	A12 RFU		J			SEN	/CK	CK	ZQ	VREFC
VSS	VSSQ	VDDQ	A10 A0	A9 A1		K			BA3 A3	BA0 A2	VDDQ	VSSQ	VSS
VDD	VDDQ	/RAS	VDD	VSS		L			VSS	VDD	/CS	VDDQ	VDD
VDDQ	DQ7	VDDQ	DQ6	VSSQ		M			VSSQ	DQ14	VDDQ	DQ15	VDDQ
VSSQ	DQ5	VSSQ	DQ4	VDDQ		N			VDDQ	DQ12	VSSQ	DQ13	VSSQ
VDDQ	/DBI0	VDDQ	WCK01	/WCK01		P			VSS	VDD	VDDQ	/DBI1	VDDQ
VSSQ	EDC0	VSSQ	VSSQ	VDD		R			VDD	VSSQ	VSSQ	EDC1	VSSQ
VDDQ	DQ3	VDDQ	DQ2	VSS		T			VSS	DQ10	VDDQ	DQ11	VDDQ
VSSQ	DQ1	VSSQ	DQ0	NC		U			VREFD	DQ8	VSSQ	DQ9	VSSQ

□ = pin is OFF in x16 mode

(Top View)

Signal	Function	Signal	Function
CK, /CK	Clock	ZQ	Impedance Reference
WCK01, /WCK01, WCK23, /WCK23	Data Clocks	/RESET	Reset
/CKE	Clock Enable	MF	Mirror Function
/CS	Chip Select	SEN	Scan Enable
/RAS, /CAS, /WE	Command inputs	VREFC	Reference voltage for command and address
BA0 - BA3	Bank Address inputs	VREFD	Reference voltage for DQ and /DBI
A0 - A12	Address inputs	VDDQ	I/O power
DQ0 - DQ31	Data Input/Output	VSSQ	I/O ground
/DBI0 - /DBI3	Data bus inversion	VDD	Power supply
EDC0 - EDC3	Error Detection Code	VSS	Ground
/ABI	Address bus inversion	NC	Not connected

Note: 1. /xxx indicates active low signal.

1. Configuration

The Elpida GDDR5 SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It contains 2,147,483,648 bits and is internally configured as a 16-bank DRAM.

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.

The GDDR5 SGRAM operates from a differential clock CK and /CK. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of /CK.

GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK, /WCK) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the GDDR5 SGRAM are burst oriented; an access starts at a selected location and continues for a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising /CK edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising /CK edge are used to select the bank and the column location for the burst access.

1.1 Signal Description

Table 1: Signal Description

Signal	Type	Detailed Function
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. Command inputs are latched on the rising edge of CK. Address inputs are latched on the rising edge of CK and the rising edge of /CK. All latencies are referenced to CK. CK and /CK are externally terminated.
WCK01, /WCK01, WCK23, /WCK23	Input	Data Clocks: WCK and /WCK are differential clocks used for WRITE data capture and READ data output. WCK01, /WCK01 is associated with DQ0-DQ15, /DBI0, /DBI1, EDC0 and EDC1. WCK23, /WCK23 is associated with DQ16-DQ31, /DBI2, /DBI3, EDC2 and EDC3. WCK clocks operate at nominally twice the CK clock frequency.
/CKE	Input	Clock Enable: /CKE low activates and /CKE high deactivates internal clock, device input buffers and output drivers. Taking /CKE high provides Precharge Power-Down and Self-Refresh operations (all banks idle), or Active Power-Down (row active in any bank). /CKE is synchronous for Power-Down entry and exit and for Self-Refresh entry. /CKE must be maintained low throughout READ and WRITE accesses. Input buffers excluding CK, /CK, /CKE, WCK01, /WCK01, WCK23, /WCK23 are disabled during Power-Down. Input buffers excluding /CKE are disabled during Self-Refresh. The value of /CKE latched at power-up with /RESET going high determines the termination value of the address and command inputs.
/CS	Input	Chip Select: /CS low enables, and /CS high disables the command decoder. All commands are masked when /CS is registered high, but internal command execution continues. /CS provides for individual device selection on memory channels with multiple memory devices. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	Command inputs: /RAS, /CAS and /WE (along with /CS) define the command to be entered.
BA0 - BA3	Input	Bank Address inputs: BA0-BA3 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0-BA3 also determine which Mode Register is accessed with a MODE REGISTER SET command. BA0-BA3 are sampled with the rising edge of CK.
A0 - A12	Input	Address inputs: A0-A12 provide the row address for ACTIVE commands. A0-A5(A6) provide the column address and A8 defines the auto precharge function for READ and WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 low, bank selected by BA0-BA3) or all banks (A8 high). The address inputs also provide the op-code during an MODE REGISTER SET command, and the data bits during LDFF commands. A8-A12 are sampled with the rising edge of CK and A0-A7 are sampled with the rising edge of /CK.
DQ0 - DQ31	I/O	Data Input/Output: 32 bit data bus
/DBI0 - /DBI3	I/O	Data bus inversion: /DBI0 is associated with DQ0-DQ7, /DBI1 with DQ8-DQ15, /DBI2 with DQ16-DQ23, and /DBI3 with DQ24-DQ31.
EDC0 - EDC3	Output	Error Detection Code: The calculated CRC data is transmitted on these pins. In addition these pins drive a hold pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ0-DQ7, EDC1 with DQ8-DQ15, EDC2 with DQ16-DQ23, and EDC3 with DQ24-DQ31.
/ABI	Input	Address bus inversion
ZQ	-	Impedance Reference: external reference pin for auto-calibration
/RESET	Input	Reset: VDDQ CMOS input. A full chip reset may be performed at any time by pulling /RESET low. With /RESET low all ODTs are disabled.
MF	Input	Mirror Function: VDDQ CMOS input. Must be tied to Power or Ground.
SEN	Input	Scan Enable: VDDQ CMOS input. Must be tied to Ground when not in use.
VREFC	Supply	Reference voltage for command and address inputs.
VREFD	Supply	Reference voltage for DQ and /DBI inputs.
VDDQ	Supply	Isolated power for the input and output buffers.
VSSQ	Supply	Isolated ground for the input and output buffers.
VDD	Supply	Power supply
VSS	Supply	Ground
NC	-	Not connected

1.2 Mirror Function Mode

The GDDR5 SGRAM provides a mirror function (MF) pin to change the physical location of the command, address, data and WCK pins assisting in routing devices back to back. The MF ball should be tied directly to VSSQ or VDDQ depending on the control line orientation desired.

The pins affected by this Mirror Function mode are listed in Table 2.

Table 2: Ball Assignment with Mirror Function

	Signal			Signal			Signal			Signal	
Ball	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**	**Ball**	**MF=0**	**MF=1**
A2	DQ1	DQ25	A4	DQ0	DQ24	K5	A11 A6	A9 A1	G12	/CS	/WE
B2	DQ3	DQ27	B4	DQ2	DQ26	P5	/WCK23	/WCK01	L12	/WE	/CS
C2	EDC0	EDC3	D4	WCK01	WCK23	H10	BA3 A3	BA1 A5	A13	DQ9	DQ17
D2	/DBI0	/DBI3	E4	DQ4	DQ28	K10	BA1 A5	BA3 A3	B13	DQ11	DQ19
E2	DQ5	DQ29	F4	DQ6	DQ30	A11	DQ8	DQ16	C13	EDC1	EDC2
F2	DQ7	DQ31	H4	A10 A0	A8 A7	B11	DQ10	DQ18	D13	/DBI1	/DBI2
M2	DQ31	DQ7	K4	A8 A7	A10 A0	E11	DQ12	DQ20	E13	DQ13	DQ21
N2	DQ29	DQ5	M4	DQ30	DQ6	F11	DQ14	DQ22	F13	DQ15	DQ23
P2	/DBI3	/DBI0	N4	DQ28	DQ4	H11	BA0 A2	BA2 A4	M13	DQ23	DQ15
R2	EDC3	EDC0	P4	WCK23	WCK01	K11	BA2 A4	BA0 A2	N13	DQ21	DQ13
T2	DQ27	DQ3	T4	DQ26	DQ2	M11	DQ22	DQ14	P13	/DBI2	/DBI1
U2	DQ25	DQ1	U4	DQ24	DQ0	N11	DQ20	DQ12	R13	EDC2	EDC1
G3	/RAS	/CAS	D5	/WCK01	/WCK23	T11	DQ18	DQ10	T13	DQ19	DQ11
L3	/CAS	/RAS	H5	A9 A1	A11 A6	U11	DQ16	DQ8	U13	DQ17	DQ9

Functions within the GDDR5 SGRAM that refer to external signals are transparent with respect to Mirror Function mode, meaning that the signal names shown in the respective functional description apply both to mirrored (MF=1) and non-mirrored (MF=0) modes. The referenced package pin is determined by the Mirror Function mode the devices is configured to.

1.3 Clamshell Mode Detection

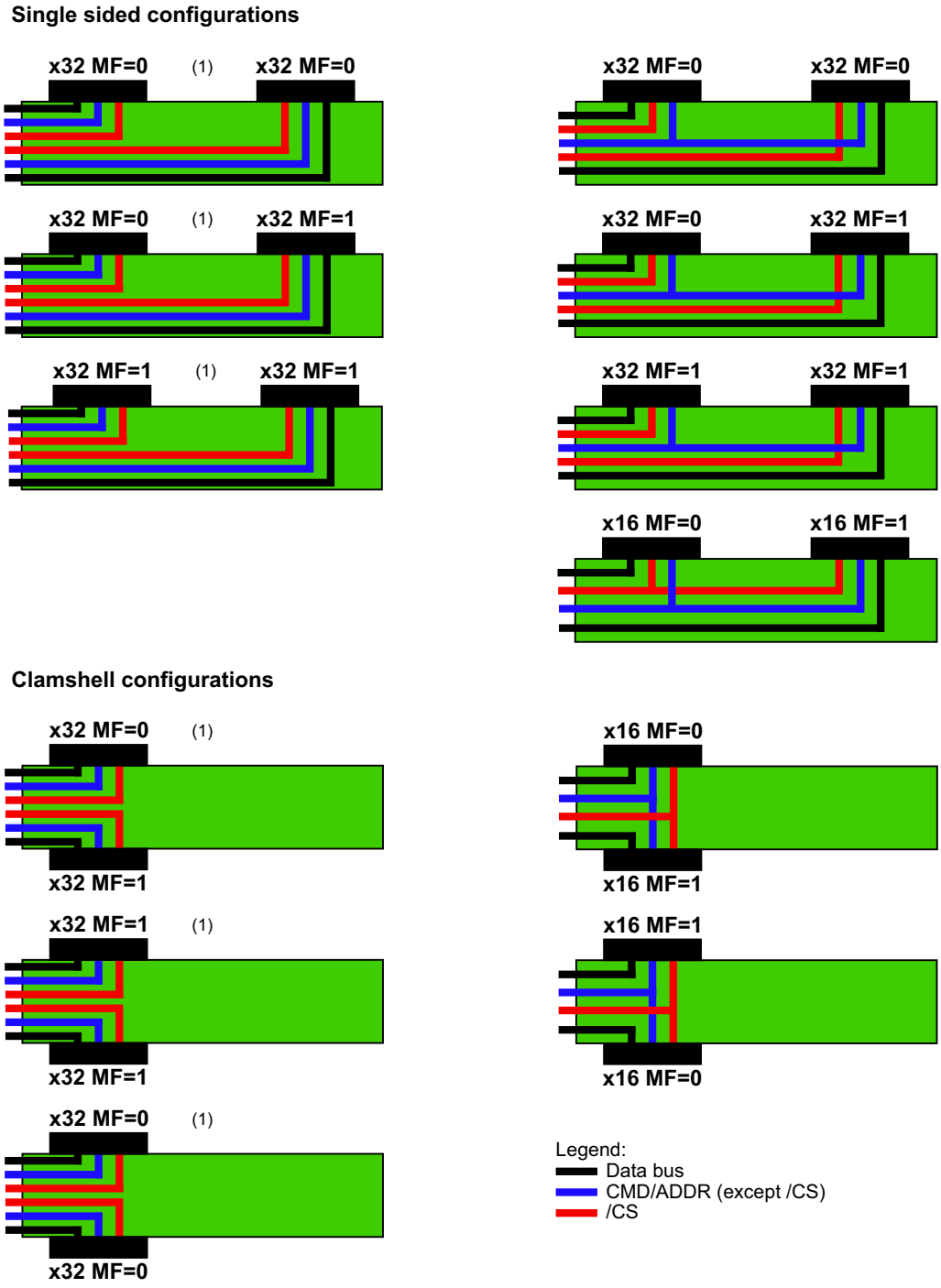
The GDDR5 SGRAM can operate in a x32 mode or a x16 mode to allow a clamshell configuration with a point to point connection on the high speed data signals. The disabled pins in x16 mode will be in Hi-Z state, non-terminating.

The x16 mode is detected at power-up on the pin at location C-13 which is EDC1 when configured to MF=0 and EDC2 when configured to MF=1. For x16 mode this pin is tied to VSSQ; the pin is part of the two bytes that are disabled in this mode and therefore not needed for EDC functionality. For x32 mode this pin is active and always terminated to VDDQ in the system or by the controller. The configuration is set with /RESET going high. Once the configuration has been set, it cannot be changed during normal operation. Usually the configuration is fixed in the system.

Table 3: Clamshell Mode and Mirror Function

Mode	MF	EDC1 (MF=0) or EDC2 (MF=1)
x16 non-mirrored	VSSQ	VSSQ
x32 non-mirrored	VSSQ	VDDQ (terminated by the system or controller)
x16 mirrored	VDDQ	VSSQ
x32 mirrored	VDDQ	VDDQ (terminated by the system or controller)

Figure 1 shows examples of the board channels and topologies that are supported in GDDR5 in order to illustrate the expected usage of x16 mode and the MF pin.



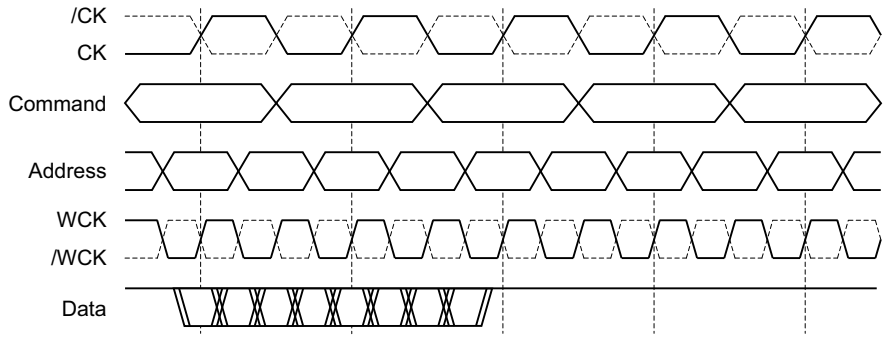
(1) : 32 bit channel is shown as an example; also applies with x16 on a 16 bit channel.

Figure 1: Example GDDR5 PCB Layout Topologies

1.4 Clocking

The GDDR5 SGRAM operates from a differential clock CK and /CK. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of /CK.

GDDR5 uses a double data rate data interface and an 8n-prefetch architecture. The data interface uses two differential forwarded clocks (WCK, /WCK). DDR means that the data is registered at every rising edge of WCK and rising edge of /WCK. WCK and /WCK are continuously running and operate at twice the frequency of the command/address clock (CK, /CK).



Note: the figure shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.

Figure 2: GDDR5 Clocking and Interface Relationship

1.5 Addressing

The GDDR5 SGRAM uses a double data rate address scheme to reduce pins required on the GDDR5 SGRAM as shown in Table 4. The addresses should be provided to the GDDR5 SGRAM in two parts; the first half is latched on the rising edge of CK along with the command pins such as /RAS, /CAS and /WE; the second half is latched on the rising edge of /CK.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 4: Address Pairs

Clock Edge	Address Inputs								
Rising CK	BA3	BA2	BA1	BA0	A12	A11	A10	A9	A8
Rising /CK	A3	A4	A5	A2	(RFU)	A6	A0	A1	A7

Addressing schemes for x32 mode and x16 mode differ only in the number of valid column addresses, as shown in Table 5.

Table 5: Addressing Scheme

	64M x 32	128M x 16
Row Address	A0-A12	A0-A12
Column address	A0-A5	A0-A6
Bank address	BA0-BA3	BA0-BA3
Autoprecharge	A8	A8
Page size	2 KB	2 KB
Refresh	16K/32ms	16K/32ms
Refresh period	1.9 µs	1.9 µs

1.6 Commands

Table 6: Command Truth Table

Operation	Code	/CKE n-1	/CKE n	/CS	/RAS	/CAS	/WE	BA3-BA0	A11	A10	A8	A6-A7, A9,A12	A0-A5 (A6)	Note
DESELECT	DESEL	L	X	H	X	X	X	X	X	X	X	X	X	2,8
NO OPERATION (NOP)	NOP	L	X	L	H	H	H	X	X	X	X	X	X	2,8
MODE REGISTER SET	MRS	L	L	L	L	L	L	MRA	OPCODE					2,3
ACTIVATE	ACT	L	L	L	L	H	H	BA	RA					2,4
READ	RD	L	L	L	H	L	H	BA	L	L	L	X	CA	2,5,9
READ with Autoprecharge	RDA	L	L	L	H	L	H	BA	L	L	H	X	CA	2,5
LOAD FIFO	LDFF	L	L	L	H	L	H	BST	H	L	L	DATA		2,7
READ TRAINING	RDTR	L	L	L	H	L	H	X	H	H	L	X	X	2
WRITE without Mask	WR	L	L	L	H	L	L	BA	L	L	L	X	CA	2,5
WRITE without Mask with Autoprecharge	WRA	L	L	L	H	L	L	BA	L	L	H	X	CA	2,5
WRITE with Single Byte Mask	WSM	L	L	L	H	L	L	BA	L	H	L	X	CA	2,5
WRITE with Autoprecharge, Single Byte Mask	WSMA	L	L	L	H	L	L	BA	L	H	H	X	CA	2,5
WRITE with Double Byte Mask	WDM	L	L	L	H	L	L	BA	H	L	L	X	CA	2,5
WRITE with Autoprecharge, Double Byte Mask	WDMA	L	L	L	H	L	L	BA	H	L	H	X	CA	2,5
WRITE TRAINING	WRTR	L	L	L	H	L	L	X	H	H	L	X	X	2
PRECHARGE	PRE	L	L	L	L	H	L	BA	X	X	L	X	X	2
PRECHARGE ALL	PREALL	L	L	L	L	H	L	X	X	X	H	X	X	2
REFRESH	REF	L	L	L	L	L	H	X	X	X	X	X	X	6
POWER-DOWN ENTRY	PDE	L	H	H	X	X	X	X	X	X	X	X	X	
				L	H	H	H							
POWER-DOWN EXIT	PDX	H	L	H	X	X	X	X	X	X	X	X	X	
				L	H	H	H							
SELF REFRESH ENTRY	SRE	L	H	L	L	L	H	X	X	X	X	X	X	6
SELF REFRESH EXIT	SRX	H	L	H	X	X	X	X	X	X	X	X	X	
				L	H	H	H							

Notes: 1. H = logic high level; L = logic low level; X = Don't Care. Signal may be H or L, but not floating.
2. Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and /ABI=L.
3. BA0-BA3 provide the Mode Register address (MRA), A0-A11 the opcode to be loaded.
4. BA0-BA3 provide the bank address (BA), A0-A12 provide the row address (RA).
5. BA0-BA3 provide the bank address, A0-A5 (A6) provide the column address (CA); no sub-word addressing within a burst of 8.
6. This command is REFRESH when /CKE(n) = L, and SELF-REFRESH ENTRY when /CKE(n) is H.
7. BA0-BA2 select burst location (BST) and A0-A9, BA3 provide the data.
8. DESELECT and NO OPERATION are functionally interchangeable.
9. In address training mode READ is decoded from the command pins only with /RAS = H, /CAS = L, /WE= H.

2. Electrical Characteristics

Table 7: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Voltage on VDD supply relative to VSS	VDD	-0.5	2.0	V
Voltage on VDDQ supply relative to VSSQ	VDDQ	-0.5	2.0	V
Voltage on VREF and inputs relative to VSS	VIN	-0.5	2.0	V
Voltage on I/O pins relative to VSS	VOUT	-0.5	2.0	V
Storage Temperature	TSTG	-55	+150	°C
Short Circuit output current	IOUT	—	50	mA

Caution: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of these specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8: Operating Temperature Range

Parameter	Symbol	Min	Max	Unit
Operating temperature	TC	0	+95	°C

Notes: 1. Operating temperature TC is the case surface temperature on the center / top side of the DRAM. It specifies the temperature where all DRAM specifications will be supported.

2. For measurement conditions, please refer to JEDEC document JESD51-2.

2.1 Operating Conditions

Table 9: DC Operating Conditions

		POD15			POD135				
Parameter	**Symbol**	**min.**	**typ.**	**max.**	**min.**	**typ.**	**max.**	**Unit**	**Note**
Device supply voltage (-60, -70)	VDD	1.552	1.6	1.648	1.3095	1.35	1.3905	V	2
Device supply voltage (-50, -40)	VDD	1.455	1.5	1.545	1.3095	1.35	1.3905	V	2
I/O Supply voltage (-60, -70)	VDDQ	1.552	1.6	1.648	1.3095	1.35	1.3905	V	2
I/O Supply voltage (-50, -40)	VDDQ	1.455	1.5	1.545	1.3095	1.35	1.3905	V	2
Reference voltage for DQ and /DBI pins	VREFD	0.69 * VDDQ	—	0.71 * VDDQ	0.69 * VDDQ	—	0.71 * VDDQ	V	3,4
Reference voltage for DQ and /DBI pins	VREFD2	0.49 * VDDQ	—	0.51 * VDDQ	0.49 * VDDQ	—	0.51 * VDDQ	V	3,4,5
External reference voltage for address and command	VREFC	0.69 * VDDQ	—	0.71 * VDDQ	0.69 * VDDQ	—	0.71 * VDDQ	V	6
DC input logic high voltage for address and command inputs	VIHA(DC)	VREFC + 0.15	—	—	VREFC + 0.135	—	—	V	
DC input logic low voltage for address and command inputs	VILA(DC)	—	—	VREFC - 0.15	—	—	VREFC - 0.135	V	
DC input logic high voltage for DQ, /DBI inputs with VREFD	VIHD(DC)	VREFD + 0.10	—	—	VREFD + 0.09	—	—	V	
DC input logic low voltage for DQ, /DBI inputs with VREFD	VILD(DC)	—	—	VREFD - 0.10	—	—	VREFD - 0.09	V	
DC input logic high voltage for DQ, /DBI inputs with VREFD2	VIHD2(DC)	VREFD2 + 0.30	—	—	VREFD2 + 0.27	—	—	V	
DC input logic low voltage for DQ, /DBI inputs with VREFD2	VILD2(DC)	—	—	VREFD2 - 0.30	—	—	VREFD2 - 0.27	V	
Input logic high voltage for /RESET, SEN, MF	VIHR	VDDQ - 0.5	—	—	VDDQ - 0.5	—	—	V	
Input logic low voltage for /RESET, SEN, MF	VILR	—	—	0.3	—	—	0.3	V	
Input logic high voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3	—	—	VDDQ - 0.3	—	—	V	9
Input logic low voltage for EDC1/2 (x16 mode detect)	VILX	—	—	0.3	—	—	0.3	V	9
Input leakage current (any input 0V ≤ VIN ≤ VDDQ; all other pins not under test = 0V)	IL	-5	—	+5	-5	—	+5	µA	10
Output leakage current (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	—	+5	-5	—	+5	µA	11
Output logic low voltage	VOL(DC)	—	—	0.62	—	—	0.56	V	
External resistor value	ZQ	115	120	125	115	120	125	Ω	

Notes: 1. All voltages are measured at the package pins.
2. GDDR5 SGRAMs are designed to tolerate PCB designs with separate VDDQ and VDD power regulators.
3. AC noise in the system is estimated at 50 mV peak-to-peak for the purpose of DRAM design.
4. Source of reference voltage and control of Reference voltage for DQ and /DBI pins is determined by VREFD, Half VREFD and VREFD Offset Mode Registers.
5. VREFD Offsets are not supported with VREFD2.
6. External VREFC is to be provided by the controller as there is no alternative supply.
7. DB, /DBI input slew rate must be greater than or equal to 3V/ns for POD15 and 2.7V/ns for POD135. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
8. ADR/CMD input slew rate must be greater than or equal to 3V/ns for POD15 and 2.7V/ns for POD135. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
9. VIHX and VILX define the input voltage levels for the receiver that detects x32 mode or x16 mode with /RESET going high.
10. IL is measured with ODT off. Any input 0V ≤ VIN ≤ VDDQ; all other pins not under test = 0V.
11. IOZ is measured with DQs disabled; 0V ≤ VOUT ≤ VDDQ.

Table 10: AC Operating Conditions

Parameter	Symbol	POD15			POD135			Unit	Note
		min.	typ.	max.	min.	typ.	max.		
AC input logic high voltage for address and command inputs	VIHA(AC)	VREFC + 0.20	—	—	VREFC + 0.18	—	—	V	
AC input logic low voltage for address and command inputs	VILA(AC)	—	—	VREFC - 0.20	—	—	VREFC - 0.18	V	
AC input logic high voltage for DQ, /DBI inputs with VREFD	VIHD(AC)	VREFD + 0.15	—	—	VREFD + 0.135	—	—	V	
AC input logic low voltage for DQ, /DBI inputs with VREFD	VILD(AC)	—	—	VREFD - 0.15	—	—	VREFD - 0.135	V	
AC input logic high voltage for DQ, /DBI inputs with VREFD2	VIHD2(AC)	VREFD2 + 0.40	—	—	VREFD2 + 0.36	—	—	V	
AC input logic low voltage for DQ, /DBI inputs with VREFD2	VILD2(AC)	—	—	VREFD2 - 0.40	—	—	VREFD2 - 0.36	V	

Notes: 1. All voltages are measured at the package pins.
2. For optimum performance it is recommended that signal swings are larger than shown in the table.

Table 11: Clock Input Operating Conditions

Parameter	Symbol	POD15		POD135		Unit	Note
		min.	max.	min.	max.		
Clock input mid-point voltage: CK, /CK	VMP(DC)	VREFC - 0.1	VREFC + 0.1	VREFC - 0.1	VREFC + 0.1	V	2,7
Clock input differential voltage: CK, /CK	VIDCK(DC)	0.22	—	0.198	—	V	5,7
Clock input differential voltage: CK, /CK	VIDCK(AC)	0.40	—	0.36	—	V	3,5,7
Clock input differential voltage: WCK, /WCK	VIDWCK(DC)	0.20	—	0.18	—	V	6,8
Clock input differential voltage: WCK, /WCK	VIDWCK(AC)	0.30	—	0.27	—	V	3,6,8
Clock input voltage level for CK, /CK, WCK, /WCK single ended inputs	VIN	-0.3	VDDQ + 0.3	-0.3	VDDQ + 0.3	V	
CK, /CK single ended slew rate	CKslew	3	—	2.7	—	V/ns	10
WCK, /WCK single ended slew rate	WCKSlew	3	—	2.7	—	V/ns	11
Clock input crossing point voltage: CK, /CK	VIXCK(AC)	VREFC - 0.12	VREFC + 0.12	VREFC - 0.108	VREFC + 0.108	V	3,4,7
Clock input crossing point voltage: WCK, /WCK	VIXWCK(AC)	VREFD - 0.10	VREFD + 0.10	VREFD - 0.09	VREFD + 0.09	V	3,4, 8,9

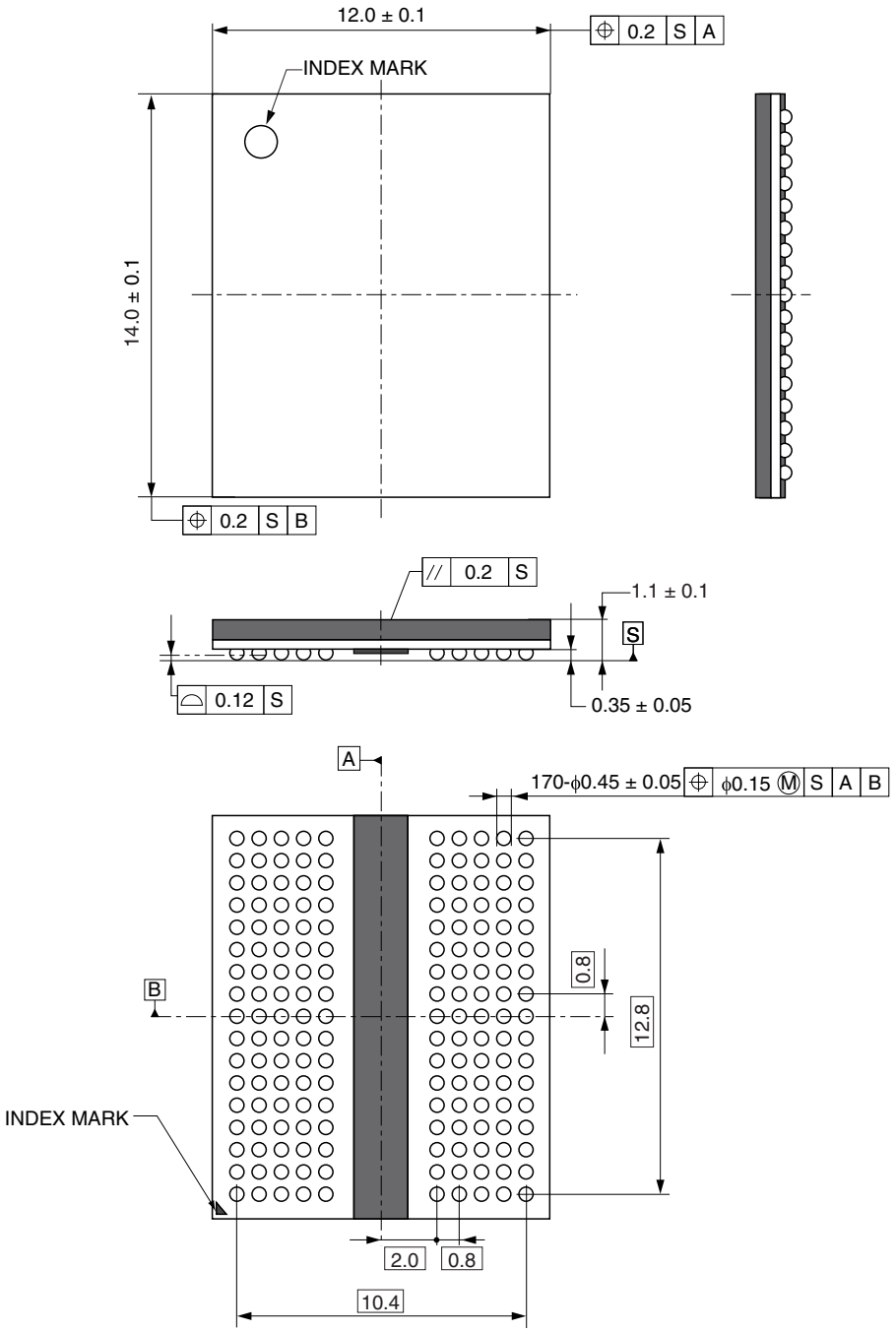
Notes: 1. All voltages are measured at the package pins.
2. This provides a minimum of 0.9V to a maximum of 1.2V, and is nominally 70% of VDDQ with POD15. If POD135, this provides a minimum of 0.845V to a maximum of 1.045V, and is nominally 70% of VDDQ. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.
3. For AC operations, all DC clock requirements must be satisfied as well.
4. The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
5. VIDCK is the magnitude of the difference between the input level in CK and the input level on /CK. The input reference level for signals other than CK and /CK is VREFC.
6. VIDWCK is the magnitude of the difference between the input level in WCK and the input level on /WCK. The input reference level for signals other than WCK and /WCK is either VREFD, VREFD2 or the internal VREFD.
7. The CK and /CK input reference level (for timing referenced to CK and /CK) is the point at which CK and /CK cross. Please refer to the applicable timings in the AC timings table.
8. The WCK and /WCK input reference level (for timing referenced to WCK and /WCK) is the point at which WCK and /WCK cross. Please refer to the applicable timings in the AC Timings table.
9. VREFD is either VREFD, VREFD2 or the internal VREFD.
10. The slew rate is measured between VREFC crossing and VIXCK(AC).
11. The slew rate is measured between VREFD crossing and VIXWCK(AC).

3. Package Drawing

170-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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Revision History

Ver.	Date	Description
1.0	Dec. 2011	Initial version