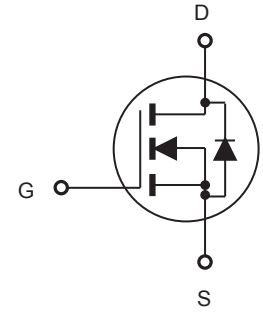
CEP85N75/CEB85N75
CEF85N75

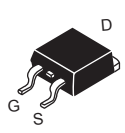
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

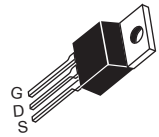
Type	V_{DSS}	$R_{DS(ON)}$	I_D	@V_{GS}
CEP85N75	75V	12mΩ	86A	10V
CEB85N75	75V	12mΩ	86A	10V
CEF85N75	75V	12mΩ	86A [e]	10V

- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 package & TO-220F full-pak for through hole.

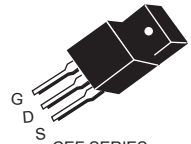




CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F

ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V_{DS}	75		V
Gate-Source Voltage	V_{GS}	±20		V
Drain Current-Continuous	I_D	86	86[e]	A
Drain Current-Pulsed [a]	I_{DM} [f]	344	344[e]	A
Maximum Power Dissipation @ T_C = 25°C	P_D	200	75	W
- Derate above 25°C		1.33	0.026	W/°C
Single Pulsed Avalanche Energy [d]	E_{AS}	325	325	mJ
Single Pulsed Avalanche Current [d]	I_{AS}	50	50	A
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	RθJC	0.75	2	°C/W
Thermal Resistance, Junction-to-Ambient	RθJA	62.5	65	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	75			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 40A		10	12	mΩ
Dynamic Characteristics [c]						
Forward Transconductance	g_{FS}	V_{DS} = 15V, I_D = 40A		45		S
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		3500		pF
Output Capacitance	C_{oss}			715		pF
Reverse Transfer Capacitance	C_{rss}			70		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 37.5V, I_D = 45A, V_{GS} = 10V, R_{GEN} = 4.7Ω		28	56	ns
Turn-On Rise Time	t_r			9	18	ns
Turn-Off Delay Time	$t_{d(off)}$			83	166	ns
Turn-Off Fall Time	t_f			10	20	ns
Total Gate Charge	Q_g	V_{DS} = 60V, I_D = 75A, V_{GS} = 10V		90	119	nC
Gate-Source Charge	Q_{gs}			19		nC
Gate-Drain Charge	Q_{gd}			23		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				86	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 40A			1.5	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.
d.L =0.87mH, I_{AS} =45A, V_{DD} = 38V, R_G = 25Ω, Starting T_J = 25 C .
e.Limited only by maximum temperature allowed .
f .Pulse width limited by safe operating area .

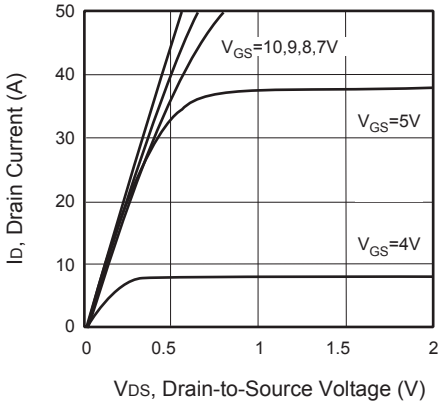


Figure 1. Output Characteristics

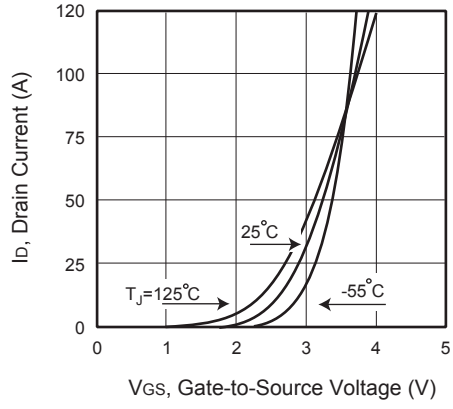


Figure 2. Transfer Characteristics

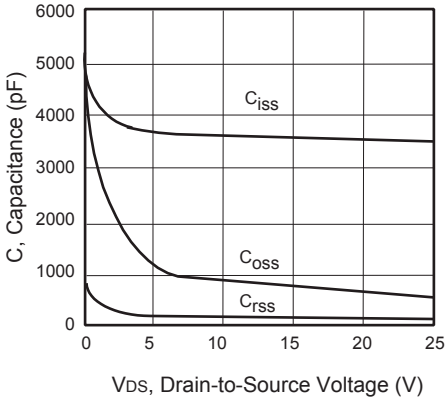


Figure 3. Capacitance

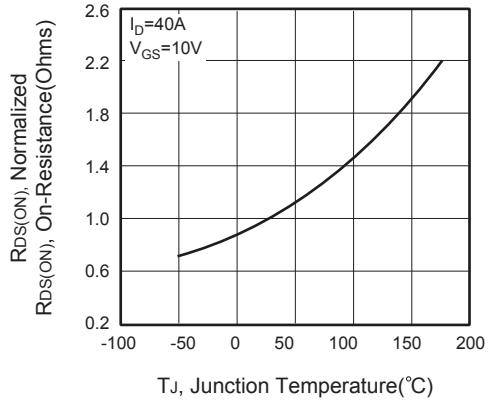


Figure 4. On-Resistance Variation with Temperature

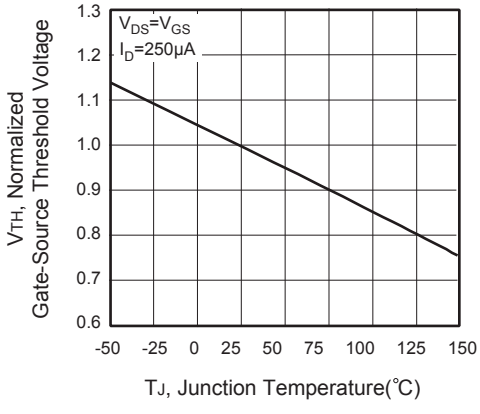


Figure 5. Gate Threshold Variation with Temperature

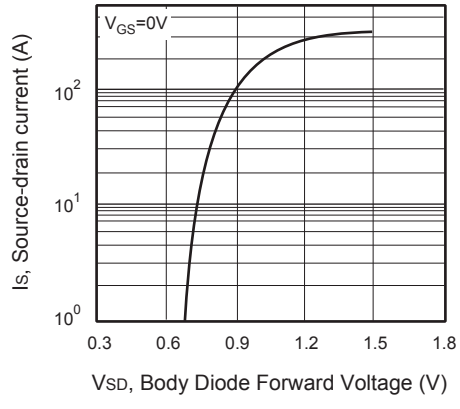


Figure 6. Body Diode Forward Voltage Variation with Source Current

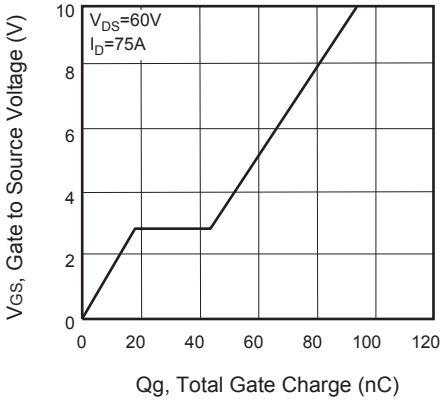


Figure 7. Gate Charge

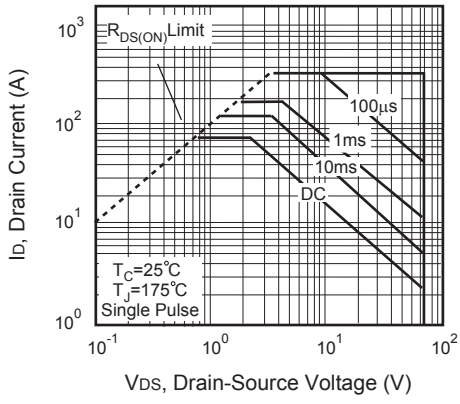


Figure 8. Maximum Safe Operating Area

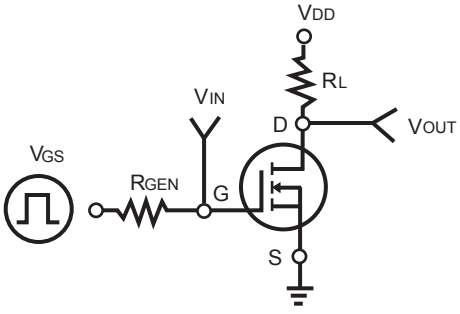


Figure 9. Switching Test Circuit

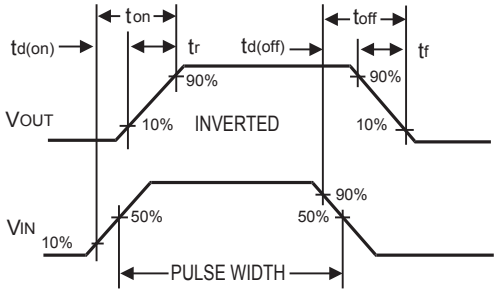


Figure 10. Switching Waveforms

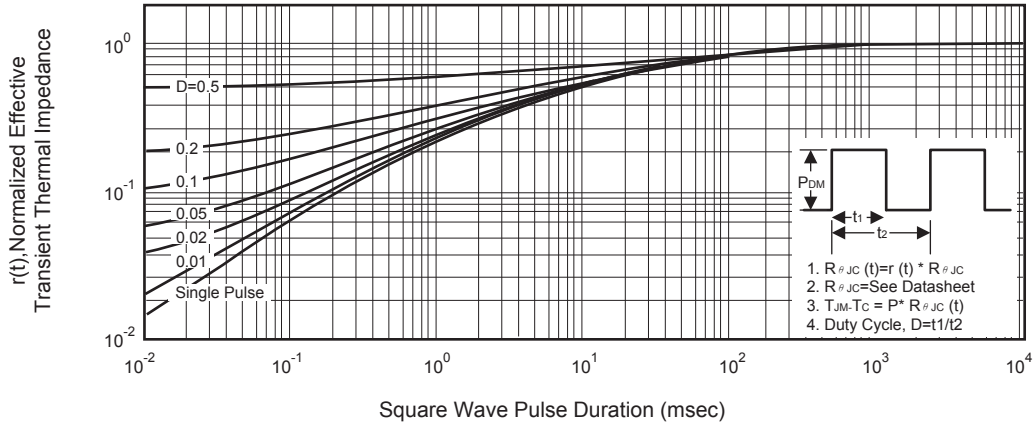


Figure 11. Normalized Thermal Transient Impedance Curve