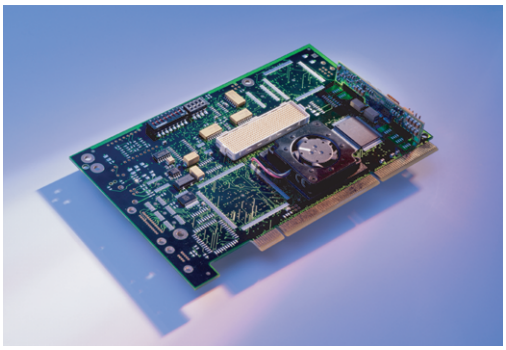
Agilent Technologies E2922B PCI-X Master Target Card

Technical Overview



Key Specifications

- 0 to 133.4 MHz clock speed
- 64 bit data and addressing
- Fully PCI-X compliant
- 53 PCI-X protocol rules
- Controllable in-system through PCI-X
- Exerciser with full capabilities, including split-transactions and 1MB data memory and real-time data generator
- Unidirectional data path verification

Agilent Technologies

Agilent E2922B PCI-X Master Target Test Card

The E2922B PCI-X Master Target Test Card provides validation engineers in the semiconductor industry a fast and predictable way to setup PCI-X traffic and verify PCI-X protocol compliance of first silicon.

The E2922B is a dedicated validation solution for test setups where full population of all available PCI-X slots is required. Operated by the C-API (C Application Interface) through the PCI-X interface itself, the E2922B can be easily integrated into existing test environments. The optionally available Design Verification Test Library offers ready to use standard tests for transaction level and data level stress tests.

Target Application

The E2922B targets validation labs where multiple PCI-X master and targets are needed for validation, e.g. of chip-sets or high-end systems. The dedicated PCI-X exercising and protocol check capabilities combined with its in-system programmability, make the E2922B the ideal test tool for the computer's core logic.

Predictable system and chip validation

The E2922B features a fully controllable master and target (PCI-X Exerciser), real-time data compare and the Agilent patented Protocol Permutation and Randomizing technique. This allows engineers to validate and stress the PCI-X system with specific and fully repeatable test cases.

Ready to use stress tests

The optional available Design Verification Test Library offers a ready to use stress test, which can be fully integrated into existing test frames

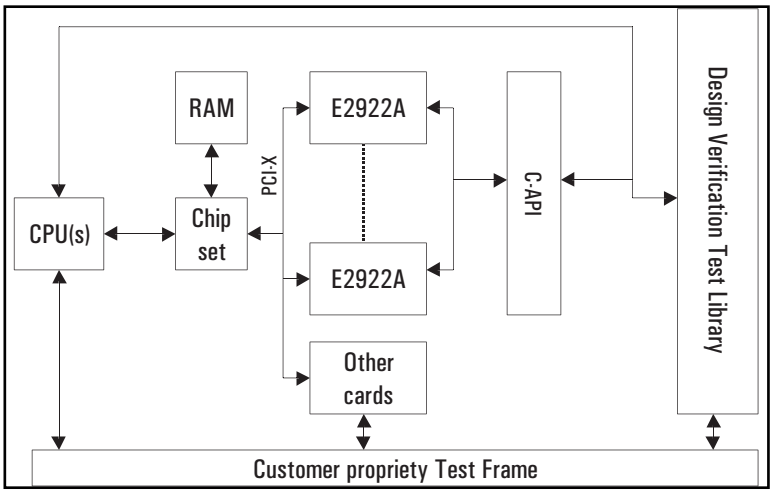


Figure 1: Chip Set Validation using E2922A

Verification of PCI-X protocol compliance

The E2922B features a PCI-X protocol checker, which runs constantly, checking for PCI-X protocol rule violations in real-time. In total, 53 protocol rules are checked concurrently. All rules are derived from the PCI-X specification. Thus, just plugging the E2922B into a PCI-X system and activating the protocol rule checker allows you to check for PCI-X protocol compliance. The E2922B reports a list of all the errors that have occurred. Each individual protocol rule can be masked.

Logic Analyzer Link

The E2922B offers a connector, allowing you to connect your Logic Analyzer. Thus, all PCI-X related signals can be easily acquired using the Logic Analyzer. The connector is compatible with the Future Plus FS2104 logic analyzer link.

System benefits

- Fully programmable traffic behavior.
- Can be easily integrated into existing test frames.
- Predictable setup of transactional and data level test for PCI-X base silicon.
- Stresses corner cases predictably and repeatedly.
- Over 1,000,000 test cases in less than 5 seconds.[1]
- In-system programmable.
- C-Application Programming Interface
- Porting support for Linux, HP-UX, proprietary OS and DOS.

System overview

The E2922B is a short PCI-X card, which can simply be plugged into the system under test. A customer specific C program controls the test setup.

[1] 1 test case @133MHz = (50 clocks delay + avg. 250 clocks for 2k bursts) *7.5ns = 2.5us. Thus, 1,000,000 test cases need = 2.5s + 2s setup time.

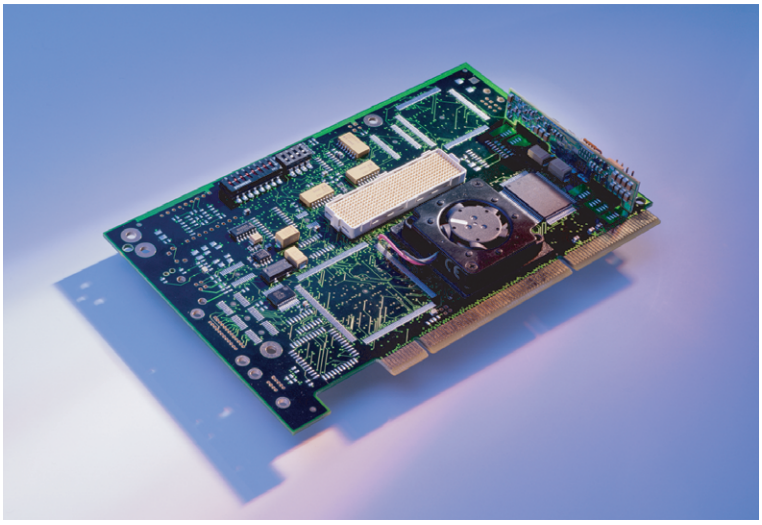


Figure 2: E2922B

PCI-X Protocol Checker

The PCI-X protocol checker checks 53 PCI-X protocol rules in real-time (see table 1 for a detailed list). Each rule can be individually masked to suppress the triggering of known problems. The rules are derived from the PCI-X specification[2], and are designed to find any possible violations of the PCI-X protocol. When a protocol violation is detected, the protocol checker can:

- store the rule number of the first (non-masked) violated rule
- list all found protocol errors
- accumulate the number of violated rules
- assert the protocol violation signal on the expansion connector

Configuration space

The Agilent E2922B provides configuration space, which is fully programmable. Default values (customizable) are stored in an EEPROM on-board and are used to initialize the configuration space when the power is on. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines. Thus, analysis test is possible without having any effect on the device or the system under test.

2 PCI-X Addendum to the PCI Local Bus Specification Revision 1.0, September/22/1999

List of Protocol Rules and Description	Reference
An initiator can terminate a transaction with master abort (deassert FRAME# and IRDY#) 8 clocks after the address phase(s).	PCI-X Spec 2.11.1.2.
If the target inserts wait states on burst write or Split Completion, the initiator must toggle between its first and second data values until the target asserts TRDY# (or terminates the transaction).	PCI-X Spec 1.10.2. Rule 5
The initiator is required to terminate the transaction when the byte count is satisfied.	PCI-X Spec 1.10.2. Rule 6
The initiator is permitted to disconnect a burst transaction (before the byte count is satisfied) only on an ADB.	PCI-X Spec 1.10.2. Rule 7
Burst Write and Split Completion transactions must not be terminated with Split Response. All other target terminations are permitted.	PCI-X Spec 2.6.1.
The target is permitted to signal Single Data Phase Disconnect on the first data phase only (with or without preceding Wait States).	PCI-X Spec 1.10.3. Rule 6
The target is permitted to signal Split Response on the first data phase only (with or without preceding Wait States).	PCI-X Spec 2.11.2.4.
Once the target has signaled Disconnect on Next ADB, it must continue to do so (or signal Target Abort) until the end of the transaction.	PCI-X Spec 2.11.2.2.
The target deasserts DEVSEL#, STOP# and TRDY# one clock after the last data phase (if they are not already deasserted) and floats them one clock after that.	PCI-X Spec 1.10.3. Rule 8
There must be an even number of target initial wait states for a burst write and Split Completion.	PCI-X Spec 2.9.
If a PCI-X target signals Data Transfer (with or without preceding Wait States), the target is limited to disconnecting the transaction on an ADB only (until the byte count is satisfied).	PCI-X Spec 1.10.3. Rule 5
FRAME# cannot be deasserted unless IRDY# was asserted.	PCI Spec Appendix C, Rule 8c
When FRAME# has been deasserted, it cannot be reasserted during the same transaction.	PCI spec Appendix C Rules 8b and 8d
IRDY# must be asserted two clocks after the attribute phase.	PCI-X Spec 1.10.2. Rule 3b
Initiator Wait States are not permitted	PCI-X Spec 1.10.2. Rule 3b
A transaction starts when FRAME# is asserted for the first time. IRDY# must not go low when FRAME# is high.	PCI Spec Appendix C, Rule 7 and 8c
Once asserted IRDY# must stay asserted until the end of transaction or till the target signals a termination.	PCI-X Spec 1.10.2. Rule 3b and PCI-X Spec 2.9.
TRDY# must not be asserted before the attribute phase, but two or more clocks later.	PCI-X Spec 2.8. Table 2-6 and PCI Spec Appendix C Rule 14
Once TRDY# has been asserted, it must not be deasserted and reasserted during the same transaction (no subsequent wait states).	PCI-X Spec 1.10.3. Rule 4
DEVSEL# must be asserted prior to the edge at which the target asserts TRDY#.	PCI-X Spec 2.8. and PCI-X Spec 2.9.1.
DEVSEL# must not be asserted during a special cycle or if a reserved command has been used.	PCI-X Spec 2.4. and PCI-X Spec 2.7.3.
DEVSEL# must not be asserted 1, 5 or more than 6 clocks after the address phase.	PCI-X Spec 2.8.
After a Target asserts DEVSEL#, it cannot be deasserted until the last data phase has completed, except to signal Data Transfer, Wait States, Target Abort, Split Response, Retry and Single Data Phase Disconnect.	PCI-X Spec 1.10.3 Rule 3
DEVSEL# must be deasserted one clock after last transfer.	PCI-X Spec 1.10.3 Rule 8
STOP# must not be asserted without DEVSEL# being asserted, except RST# being asserted.	PCI-X Spec 1.10.1.Rule 12; PCI spec Appendix C, Rule 14, spec 6
If the target signals Split Response, Target-Abort or Retry, the target must do so within eight clocks of the assertion of FRAME#.	PCI-X Spec 1.10.3 Rule 4
If the target signals Single Data Phase Disconnect, Data Transfer or Disconnect on Next ADB, the target must do so within 16 clocks of the assertion of FRAME#.	PCI-X Spec 1.10.3 Rule 4
ACK64# may only be asserted, when REQ64# was asserted before (ACK64# is a response to REQ64#).	PCI Spec 3.8.
A 64-bit initiator asserts REQ64# with the same timing as FRAME# to request a 64-bit data transfer. It deasserts REQ64# with FRAME# at the end of the transaction.	PCI-X Spec 2.12.3. Requirement 4
If a 64-bit target is addressed by a transaction that does have REQ64# asserted with FRAME#, the target asserts ACK64# with DEVSEL# to complete the transaction as a 64-bit target. It deasserts ACK64# with DEVSEL# at the end of the transaction.	PCI-X Spec 2.12.3.
REQ64# must not be used with special cycle or interrupt the acknowledge command. Only burst transactions (memory commands other than Memory read DWORD) use 64-bit data transfers.	PCI-X Spec 2.4. and 2.7.
For DWORD Transactions, REQ64# must be deasserted.	PCI-X Spec 2.12.3. Requirement 2
PERR# may never be asserted three clocks after the address phase (or earlier in a transaction) or during a special cycle. During WRITE, PERR# may be asserted three clocks after IRDY#, during READ, PERR# may be asserted three clocks after TRDY#.	PCI Spec 3.8.2
AD[31::0] address parity error.	PCI Spec Appendix C, Rule 32 b
AD[63::32] address parity error.	PCI Spec Appendix C, Rule 32 c
AD[31::0] data parity error occurred but was not signaled.	PCI-X Spec 5.3.
AD[63::32] data parity error occurred but was not signaled.	PCI-X Spec 5.3.
AD[31::0] data parity error occurred.	PCI Spec Appendix C, Rule 32 b
AD[63::32] data parity error occurred.	PCI Spec Appendix C, Rule 32 c
For I/O and DWORD memory transactions, AD [1:0] and byte enables coding must have a defined relationship in the PCI-X Spec	See table 2.2 in the PCI-X Spec
Reserved commands are reserved for future use.	PCI-X Spec 2.4
DAC is not allowed immediately after a DAC.	PCI Spec 3.9. and PCI-X Spec 2.12.1.
During the data phases C/BE# bus must be driven high for all Burst Transactions except Memory Write.	PCI-X Spec 2.6.
During a Dual Address Cycle, a 64-bit master has to drive the upper half of the address on AD[63::32] in the initial and in the second address phase.	PCI-X Spec 2.12.1.3 a i)
In the second address phase of a Dual Address Cycle, AD [63:32] and AD [31:0] contain duplicate copies of the upper half of the address.	PCI-X Spec 2.12.1.3 a i)
During a Dual Address Cycle, a 64-bit master has to drive the bus command on C/BE [7::4]# in the initial and the second address phase.	PCI-X Spec 2.12.1.3 a ii)
In the second address phase of a Dual Address Cycle, C/BE [7::4]# and C/BE [3::0]# contain duplicate copies of the transaction command.	PCI-X Spec 2.12.1.3 a ii)
DWORD Transactions only support a single data phase.	PCI-X Spec 2.7.
A master that supports 64-bit addressing must generate a SAC instead of a DAC, when the upper 32 bits of the address are zero.	PCI spec 3.9
This rule detects a bus hang. If the bus does not get idle once within 4095 clocks, it *Implementation note*: The counter can be programmed between 1...4095 clocks. A value of 0 for the counter turns the rule	Agilent Rule to detect potential
A master did not respond to a split transaction within 2^{20}-1 clocks. *Implementation note*: The counter can be programmed 1...2^{20}-1 clocks. A value of 0 for the counter turns the rule	Agilent Rule to detect potential
A delayed transaction (retries) has not yet been repeated within 2^{15} clocks.	PCI spec 3.3.3.3.3
A delayed transaction has not terminated within 2^{16} clocks.	Agilent Rule to detect potential

PCI-X Exerciser

The Agilent E2922B features an on-board 64 bit PCI-X exerciser. The exerciser operates at 0 to 133.4 MHz, and can emulate and force practically any behavior of a PCI-X device imaginable- except blatant protocol violations. The exerciser is controlled from a C-API.

The exerciser features:
· two master queues
· one target
· four completer queues to handle independent split-transactions
· one requester-target handling up to 32 open requests

Master, target, completer and requester-target are fully programmable, operate independently of each other and are able to handle:
· 32/64 bit data transfers
· 32/64 bit addressing
· programmable delays between transactions
· block length up to 4Gbyte
· all 14 PCI-X command types

Architectural overview

The exerciser is based on two main ideas. Firstly, defining requester initiator data blocks, describing 'what' data should be transferred and secondly, defining a requester initiator behavior, describing how the transfer should be executed.

For the requester initiator, up to 256 blocks of data transfers can be set up (see figure 3). In addition, requester initiator behaviors are set up, specifying how the requester initiator intends to transfer the data blocks over the PCI-X bus. If any completer target replies to a transfer and requests a split transaction, the requester initiator data block attributes are moved internally to a split transaction maps for further use. The transaction map can manage up to 32 open split transactions. When completing split transactions, the requester target behaviors are used to control the transfer.

The completer target behavior attributes define how the completer target of the E2922B acts. The completer target can manage up to 4 split transaction queues. It is also possible to fully control the initiation of the completion of split transactions. The completer initiator behavior attributes are used to program it. The programmable transaction scheduler decides whether completer or requester transaction is performed.
All data comes or goes through the on-board data memory or from the on-board real-time data generator.

Requester Initiator data block

The requester initiator data block settings define which address space is accessed, and where data is moved. Up to 256 block transfers can be defined and performed in a linear sequence by one of the two transfer queues. Each block specifies:
· the bus command seen on C/BE[3::0] in the address phase. All valid PCI-X commands are supported.
· the 64 bit bus address
· the byte enable value (C/BE[3::0] / C/BE[4::7]
· the start address of the data memory or if the data generator is used
· the number of bytes to be transferred (1 to 4GB)
· if the real-time data compare for incoming data should be activated
· the start condition for the transfer (immediately or wait for event)
· the transfer queue the data is passed through

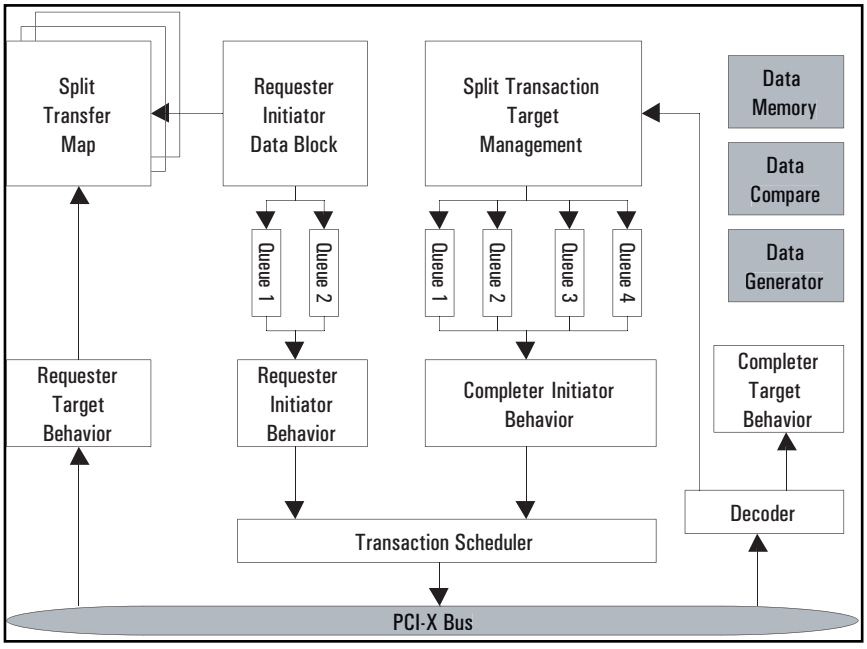


Figure 3: E2922B PCI-X exerciser architecture

Requester Initiator behavior

The requester initiator behaviors are set to specify the PCI-X transfer behavior per address/data phase. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed.
The attributes control:

- 32 or 64 bit data access
- insertion of 1 to 65535 clock cycle delay between transactions
- the next data queue to be used
- if an automatic or customer defined tag (0..31) is used
- the specific burst length for the transfer (1 to 4096 byte) automatically rounded up to the next qword boundary
- the n-th ADB where the requester initiator disconnects (1 to 32)
- perform 0 to 4 address steps
- how many clock cycles after the address phase REQ# is de-asserted (0 to 2047)
- how often the current transfer attributes are used (repeat value 1 to 256)

Latencies between the requester initiator transactions

The latencies between transactions can be varied using requester initiator behavior property. The minimum latency is in general ≤1 clock cycle - including any sequences of read/write where real-time data compare is involved. The only exception is if the most recent transaction is a read/write transfer into data memory and the subsequent transaction is a write out of data memory. In these particular cases, the latency is 10 to 20 clock cycles. Please note that it is assumed that the master does not need to disconnect before the byte count of the current sequence is transferred and that wait cycles are added if required by the PCI-X specification.

Requester target behavior

The requester behavior attributes are set to specify the PCI-X transfer behavior per address/data phase if a target requests the completion of a split transaction from a requester

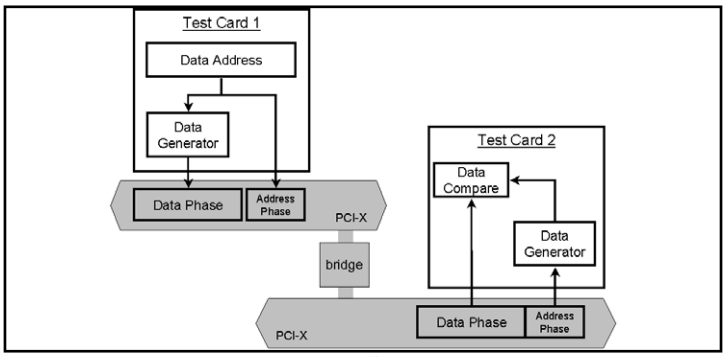


Figure 4: Unidirectional data path verification

initiator. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed.
The attributes control:

- the decode speed used (A[3] /B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (3 to 34)
- the behavior after initial latencies, either accept transfer, disconnect, signal retry or abort
- how often the current behavior is applied (repeat value 1 to 65536)

Completer target behavior attributes

The completer target behavior attributes give full control over the E2928B completer target behavior, and define how the target reacts to a request. Up to 256 attribute entries, which can be setup as linear sequences or repeat loops, are allowed. The attributes control:

- the decode speed used (A[3]/B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (0 to 31)
- the behavior after initial latencies, either accept transfer, signal a single data phase, retry or abort
- the behavior in subsequent data phases, either accept all subsequent data phases, disconnect after 1 to 2047
- data phases or abort after 1 to 2047 data phases
- signaling a split response, either by identifying an address value or range in the address phase, the decoder accessed, or by a subset of all 16 possible PCI-X commands
- the split transaction queue to be used
- how often the current behavior is applied (repeat value 1 to 65536)

Configuration space and decoders

In total, the E2922B features 5 decoders:

- one standard configuration space decoder, fully customer programmable
- 3 programmable target decoders (six bars) that can either hold up to 3 memory spaces (64 bit) or 2 memory spaces and 2 I/O spaces simultaneously
- one decoder to access the 64Kbyte expansion ROM

All decoders can be switched off by a dip-switch on the E2929A, making the card completely invisible to the system under test.

Completer Initiator behavior

The completer behavior attributes are set to specify the PCI-X transfer behavior per address/data phase if a target starts to complete a split transaction. Up to 256 behavior entries, which can be setup as linear sequences or repeat loops, are allowed.
The attributes control:

- the split transaction queue to be served
- the start condition for this transfer
- 32 or 64 bit data transfer

[3] Decode speed A is supported up to 66 MHz

- the number of clock cycles inserted before REQ# is asserted (1 to 65535)
- the number of clock cycles before REQ# is de-asserted (1 to 2047)
- the number of address steps (2 to 6)
- how often the current transfer attributes are used (repeat value 1 to 256)
- disconnect at n-th ADB (2 to 63)

Target latencies

The initial latencies can be programmed with the completer target behavior attributes. Depending on the selected decode speed and address phases, the test card automatically adds the needed number of wait states to achieve the defined initial latency. A minimum of one wait cycles is always added when using decode speed B, C, minimum two wait cycles are needed with decode speed A.
In case the subsequent target access is a 'read from target' and the most recent event was a 'write to target', 'read from other target address', 'master write' or 'master read', the minimum initial latency is 15 clock cycles.

Data memory

The E2922B features a 1MB (128K x 2 dwords) programmable read/write data memory. Master / requester and target/ completer share the memory. The address decoders can selectively address it. The data memory can:

- store data from read/write transfers
- be mapped to any PCI-X address space

Data generator

Instead of using the data memory, the on-board data generator can be used. Without initial latencies, the generator can generate a data pattern, deterministically linked to the data address. Combined with a second exerciser card and the real-time data compare feature, long-time load stressing on any PCI-X to PCI-X data path can be performed while errors are detected in real-time (figure 5).

The generator features the following patterns:

- walking ones or zeros
- ground bounce
- count up (unique data)
- pseudo random pattern (unique data)

The count up and pseudo random pattern are unique up to the length of 1M quad words (4Mb). The data uniqueness is derived out of the lower bit 2 to 22 of the bus address.

Real-time data compare

Real-time data compare can be performed either on:

- Memory:
  when data is written to the memory it is compared against the actual memory content
- Data Generator :
  based on the data address, the generator calculates the expected data and compares it with incoming data.

C-API / PPR

The E2922B comes with a C-Application Programming Interface (C-API) which provides a programming interface for setting up and controlling the master target card.

The test program must run on the system-under-test itself. The PCI-X interface itself is used to control the card.

The library functions are divided into groups, which allow you to set up and control the various capabilities of the Agilent E2922B.

Recommended development environment: MS Visual C++ V. 6.0 or higher.

Protocol Permutation and Randomization (PPR)

The PPR library extends the C-API by offering dedicated functions to setup PCI-X protocol permutation in a pseudo random sequence. It allows easy to set up transfers of contiguous blocks of data with as many protocol variations as possible. Therefore, the PPR software calculates which variations are covered, and after how many data transfers, by permutating the possible protocol variations. It determines whether the coverage, within programmed constraints, can be achieved under given test circumstances, and calculates the test time required to perform the data transfers.

Generating permutations

By specifying lists of protocol variations, which must occur, the user-defined protocol constraints can be easily set. For example, which different burst lengths, wait cycles, memory read/write commands, etc.

Then, PPR automatically moves simultaneously through the lists. With each step, that is, with each permutation, the next value in this list is combined with the next values in the other lists. The hardware based permutation proceeds in this way until each value of each list is combined with all values of the other list, and thus all combinations are covered. In this way, the repetition or omission of combinations is avoided.

Documented test coverage

A printable report tells you to which protocol variation the device has exposed. It explicitly reports which protocol attributes are permutated against which other protocol attributes, and after how many data transfers.

Optimized test time

The values to be varied can be specified for each master and target attribute separately. Thus, focusing on interesting cases can optimize testing time.

By carrying out these protocol permutations in real-time within the exerciser hardware, these tests run much more quickly than any other CPU-based test program.

Effective test generation

The exhaustive C-library makes it simple to focus on test structuring, partitioning and the specification of protocol constraints. This means that an appropriate and valuable test for protocol verification with meaningful results can quickly be obtained.
Once started, the test can easily be extended to incorporate newly gained experiences or to address testing needs of newly invented PCI-X features.

Deterministic test conditions

In contrast to PCI-X traffic generated by other PCI-X cards, the generated variations are completely deterministic and reproducible.

Supported protocol variations

The exerciser and analyzer allows the variation constraints for the PCI-X transfer, PCI-X master/requester and PCI-X target/completer behavior to be specified. All specified constraints can be permutated against each other and up to 100 constraints can be maintained per list.

PCI-X transfer variations

The generator features the following algorithms:

- start address alignment; a list of arbitrary address alignments to start PCI-X transfers at given offsets (e.g. 1 dword) relative to the qword boundaries
- byte enables; a list of selected values for the C/BE lines during the address phase
- block size; a block describes a contiguous range in memory available to be transferred. A list of up to 100 different block sizes (from 1 to 4096 byte) can be selected to be transferred
- bus commands; a list of selected PCI-X bus commands. All selected commands are permutated with other selected constraints, as appropriate, for the specified transfer direction and PCI-X specifications
- permutation of release ordering bit
- permutation of no snoop bit

Target behavior variations

The requester initiator allows for the variation of:

- byte count (1 to 4096)
- disconnect/initiator termination
- delay
- address stepping
- REQ64
- release REQ

The completer initiator allows for the variation of:

- Error message, yes/no
- partitioning
- delay
- address stepping
- REQ64
- release REQ

General Specifications

PCI-X specifications:
PCI-X bus: 32/64 bit
Addressing: 32/64 bit

PCI Clock range:
Exerciser: 0 to 133.4 MHz

Timing specifications:

	Min.	Max.
T_{val}		3.8 ns
T_{on}	0 ns	
T_{off}		7 ns
T_{su}	1.2 ns	
$T_{su(ppt)}$	1.2 ns	
T_{h}	0.5 ns	

@ temperatures of -40°C to +55°C

The E2922A fully meets timing specifications for 133 MHz PCI-X.

Electrical Specifications:

For 3.3V environment, complies with PCI-X Spec. 1.0.

Decoupling: unused 3.3 V power pins are decoupled.

Power requirements: consumes less than 25 W from PCI-X slot.

Trace length limits:
meets PCI-X specifications.

Signal loading:
less than 10 pF, fully PCI-X compliant.

Operating temperature:
-40°C to +55°C.

Mechanical dimensions:
short card, occupying one slot.

Ordering Information

E2922B PCI-X Master Target Test Card
Includes:

- 32/64 bit, 0..133.4 MHz PCI-X protocol checker
- on-board 32/64 bit, 0..133 MHz exerciser hardware
- PPR hardware
- C-API including drivers for Windows NT
- Software media CD

When ordering without base product, S/N of the existing E2922B must be notified on purchase order.

Porting support is available to port C-API to Linux, HP-UX or proprietary operating systems. Contact your local sales offices for detailed information.

Accessories

FuturePlus Analysis Probe[4]
FS2104 for connection of the Agilent logic analyzer. Available from Agilent as resell part FSI 60042

[4] The analysis probe is not an Agilent product. Agilent works closely with Future Plus to ensure quality products, but the vendor is responsible for functionality, pre-sales and post sales support and warranty.

Overview PCI/PCI-X E2920 Series

	PCI Analyzer -protocol checker - 64K state PCI logic analyzer -4MB fast host interface - timing checker -real-time performance measures -GUI - RS-232 interface	**E2940A** compact PCI 32/64 bit 66MHz	**E2925B** PCI 32 bit 33 MHz	**E2928A** PCI 32/64 bit 66 Mhz	**E2929B** PCI-X 32/64 bit 133 MHz -protocol checker -RS-232/USB interface - GUI
Opt.100					**PCI-X Analyzer** - 2M state PCI logic analyzer -4MB fast host interface -real-time performance measures - GUI
Opt.200	**PCI Performance Optimizer**	4M trace memory recommended please order separately		32/64 bit 66 MHz	**PCI-X Performance Optimizer** -post processed and real-time performance analyzer - performance report - GUI
Opt.300	**PCI Exerciser** - master and target -GUI - CLI -512 KB on-board memory	32/64 bit 33 MHz	32 bit 33 MHz	32/64 bit 66 MHz	PCI-X Exerciser - master - target - GUI - 1MB onboard data memory
Opt. 310	**System validation package**	- peer-to-peer test -system memory test - system load test - protocol load test - protocol check - GUI			
Opt.320	**C-API/PPR**	- C-programming interface library -protocol permutation and randomization library			

PCI-PCI-X Bundle:

With the E2997A Agilent aslo offers a great price on the purchase of the E2928A PCI Card and the E2929B PCI-X card.

Master Target Test Card

The E2922B PCI-X Master target Test card provides validation engineers in the semiconductor industry a fast and predictable way to set up PCI-X protocl compliance of first silicon.

Accessories Agilent Products	**E2940A**	**E2925B**	**E2928A**	**E2929B**
E2991A External power supply		•	•	•
E2993A External Agilent Logic Analyzer Adapter		•	•	
E2994A External general purpose Logic Analyzer Adapter		•	•	
E2995A 155 x 4M trace memory		•	•	
E2996A 155 x 4M trace memory	•	•		
System test library	•	•	•	•

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Related Agilent Literature

- Agilent E2925B 32bit, 33 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3501E
- Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3506E
- Agilent E2940A CompactPCI Exerciser & Analyzer, technical specifications, P/n 5968-1915E
- Agilent E2929B PCI-X Exerciser & Analyzer, technical overview, p/n 5968-8984E
- Agilent System Validation Pack, Agilent System Test Library, technical overview, p/n 5968-3500E
- Agilent E2920 Computer Verification Tools, PCI Series, brochure, p/n 5968-9694E
- Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series, case stuy, p/n 5988-0488E
- HP NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study, p/n 5968-6948E
- HP HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI Series, case study, p/n 5968-6949E
- Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study, p/n 5968-4191E

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