

## 4-BIT MAGNITUDE COMPARATOR

## FEATURES

- Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ( $Q_A > B$ ,  $Q_A = B$  and  $Q_A < B$ ). The 4-bit inputs are weighted ( $A_0$  to  $A_3$  and  $B_0$  to  $B_3$ ), where  $A_3$  and  $B_3$  are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table, the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs ( $|A > B$ ,  $|A = B$  and  $|A < B$ ) to the least significant position must be connected as follows:  $|A < B = |A > B = \text{LOW}$  and  $|A = B = \text{HIGH}$ .

For words greater than 4-bits, units can be cascaded by connecting outputs  $Q_A < B$ ,  $Q_A > B$  and  $Q_A = B$  to the corresponding inputs of the significant comparator.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $Q_A > B$ , $Q_A < B$ $A_n, B_n$ to $Q_A = B$ $ A < B$ , $ A = B$ , $ A > B$ to $Q_A < B$ , $Q_A = B$ $ A = B$ to $Q_A = B$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	20 18 15 11	22 20 15 15	ns ns ns ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	18	20	pF

$GND = 0 \text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

## Notes

- CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

- For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

## PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).  
 16-lead mini-pack; plastic (SO16; SOT109A).

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	$ A < B$	$A < B$ expansion input
3	$ A = B$	$A = B$ expansion input
4	$ A > B$	$A > B$ expansion input
5	$Q_A > B$	$A > B$ output
6	$Q_A = B$	$A = B$ output
7	$Q_A < B$	$A < B$ output
8	GND	ground (0 V)
9, 11, 14, 1, 10, 12, 13, 15	$B_0$ to $B_3$ $A_0$ to $A_3$	word B inputs word A inputs
16	$V_{CC}$	positive supply voltage

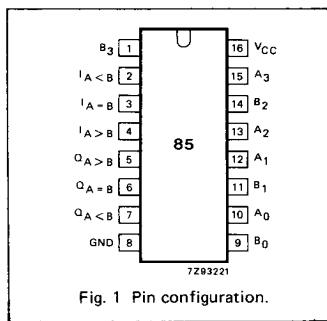


Fig. 1 Pin configuration.

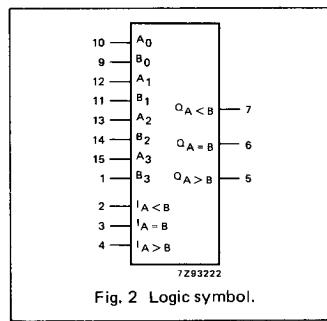


Fig. 2 Logic symbol.

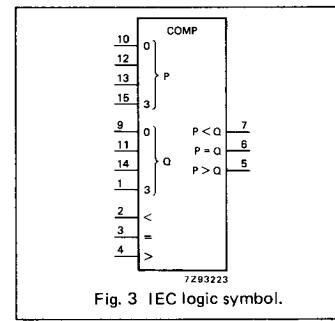


Fig. 3 IEC logic symbol.

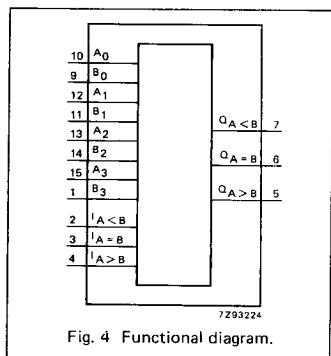


Fig. 4 Functional diagram.

### APPLICATIONS

- Process controllers
- Servo-motor control

### FUNCTION TABLE

COMPARING INPUTS				CASCAADING INPUTS			OUTPUTS		
A <sub>3</sub> , B <sub>3</sub>	A <sub>2</sub> , B <sub>2</sub>	A <sub>1</sub> , B <sub>1</sub>	A <sub>0</sub> , B <sub>0</sub>	I <sub>A&gt;B</sub>	I <sub>A&lt;B</sub>	I <sub>A=B</sub>	Q <sub>A&gt;B</sub>	Q <sub>A&lt;B</sub>	Q <sub>A=B</sub>
A <sub>3</sub> >B <sub>3</sub>	X	X	X	X	X	X	H	L	L
A <sub>3</sub> <B <sub>3</sub>	X	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> >B <sub>2</sub>	X	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <B <sub>2</sub>	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> >B <sub>1</sub>	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> <B <sub>1</sub>	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> >B <sub>0</sub>	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> <B <sub>0</sub>	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	L	L	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	H	L	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	H	L	L	H
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	X	X	H	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	H	L	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	L	H	L	L

H = HIGH voltage level

L = LOW voltage level

X = don't care

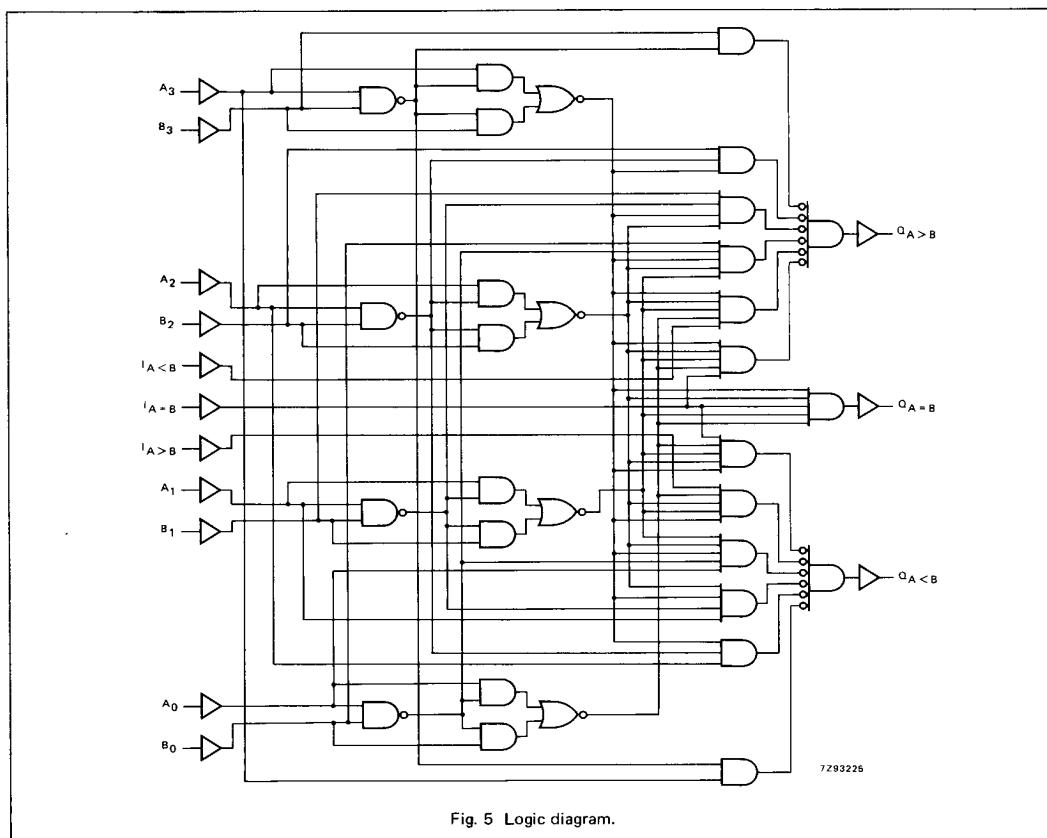


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

ICC category: MSI

**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ 

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	WAVEFORMS		
		+25		−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n, B_n$ to $Q_A > B$ or $Q_A < B$	63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n, B_n$ to $Q_A = B$	58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $I_{A < B}, I_{A=B}, I_{A > B}$ to $Q_A < B, Q_A > B$	50 18 14	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $I_{A=B}$ to $Q_A = B$	39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6		
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6		

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$I_A < B$	1.00
$I_A > B$	1.00
$I_A = B$	1.50
$A_n, B_n$	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_f = t_r = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	WAVEFORMS		
		+25		−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $Q_A > B$ or $Q_A < B$	26	44		55		66	ns	4.5	Fig. 6		
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $Q_A = B$	24	40		50		60	ns	4.5	Fig. 6		
$t_{PHL}/t_{PLH}$	propagation delay $I_A < B, I_A = B, I_A > B$ to $Q_A < B, Q_A > B$	18	31		39		47	ns	4.5	Fig. 6		
$t_{PHL}/t_{PLH}$	propagation delay $I_A = B$ to $Q_A = B$	18	31		39		47	ns	4.5	Fig. 6		
$t_{THL}/t_{TLH}$	output transition time	7	15		19		22	ns	4.5	Fig. 6		

## AC WAVEFORMS

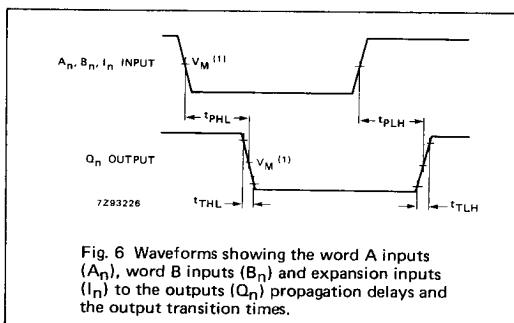


Fig. 6 Waveforms showing the word A inputs ( $A_n$ ), word B inputs ( $B_n$ ) and expansion inputs ( $I_n$ ) to the outputs ( $O_n$ ) propagation delays and the output transition times.

## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND to } 3\text{ V}$ .

## APPLICATION INFORMATION

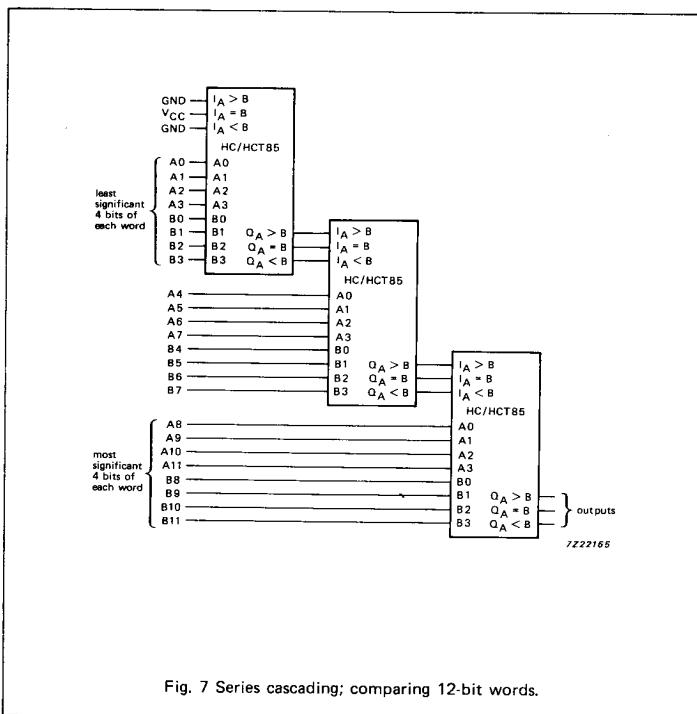


Fig. 7 Series cascading; comparing 12-bit words.

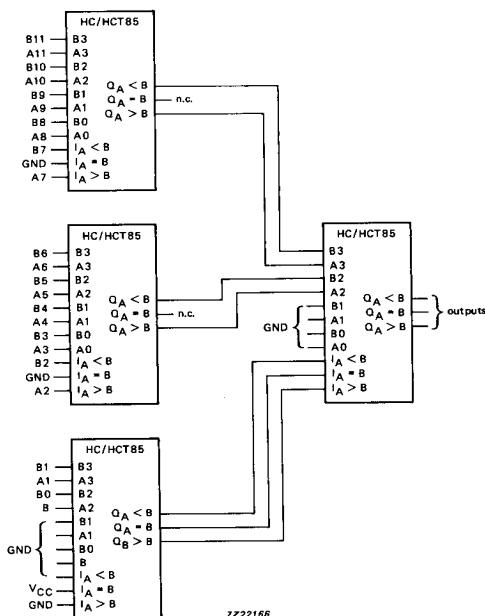


Fig. 8 Parallel cascading; comparing 12-bit words.