

HITJ0302MP

Silicon P Channel MOS FET
Power Switching

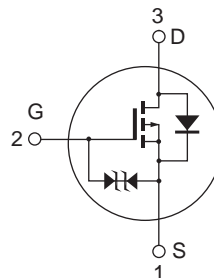
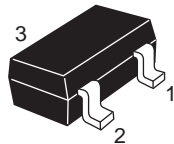
R07DS0477EJ0100
Rev.1.00
Jun 22, 2011

Features

- Low on-resistance
 $R_{DS(on)} = 138 \text{ m}\Omega$ typ ($V_{GS} = -10 \text{ V}$, $I_D = -1.1 \text{ A}$)
- Low drive current
- High speed switching
- 4.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "NG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+10 / -20	V
Drain current	I_D	-2.2	A
Drain peak current	$I_{D(Pulse)}$ ^{Note1}	-5	A
Body - drain diode reverse drain current	I_{DR}	-2.2	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

Electrical Characteristics

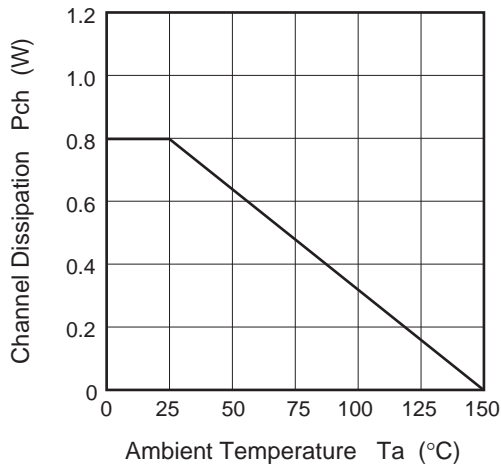
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+10	—	—	V	$I_G = +100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20	—	—	V	$I_G = -100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +8 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -16 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	138	173	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	216	303	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.2	2.1	—	S	$I_D = -1.1 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	195	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	42	—	pF	
Reverse transfer capacitance	C_{rss}	—	29	—	pF	
Turn - on delay time	$t_{d(on)}$	—	19	—	ns	$I_D = -0.5 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_L = 20 \text{ } \Omega$, $R_g = 4.7 \text{ } \Omega$
Rise time	t_r	—	25	—	ns	
Turn - off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	4.6	—	ns	
Total gate charge	Q_g	—	4.2	—	nC	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -2.2 \text{ A}$
Gate to source charge	Q_{gs}	—	0.7	—	nC	
Gate to drain charge	Q_{gd}	—	1.0	—	nC	
Body - drain diode forward voltage	V_{DF}	—	-0.9	—	V	$I_F = -1.5 \text{ A}$, $V_{GS} = 0$ ^{Note3}

Notes: 3. Pulse test

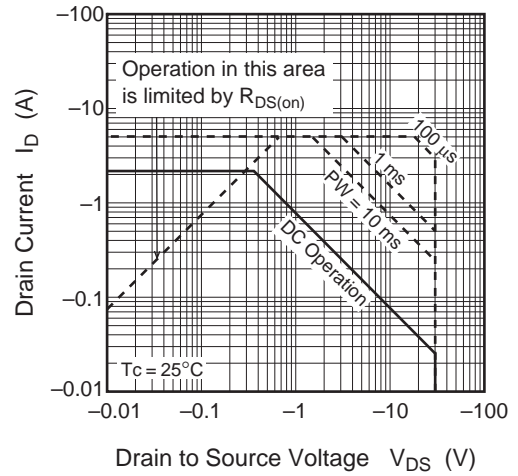
Main Characteristics

Maximum Channel Power Dissipation Curve

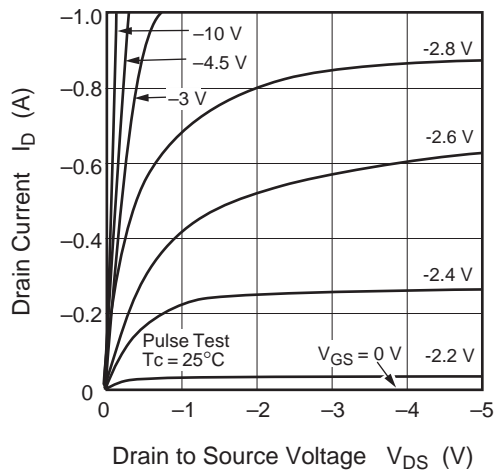


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

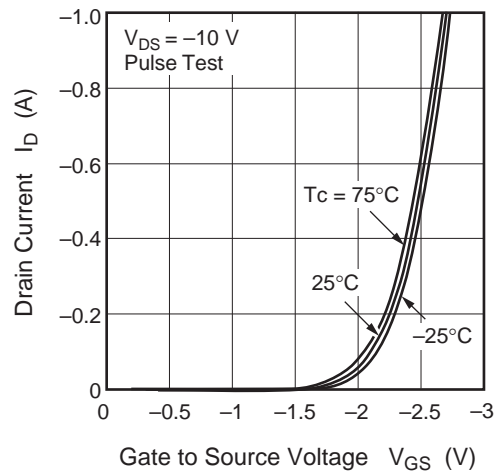
Maximum Safe Operation Area



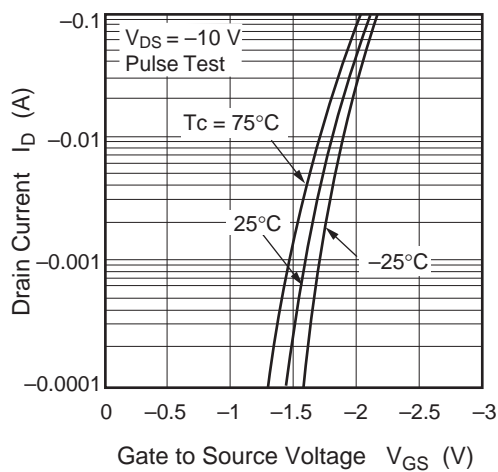
Typical Output Characteristics



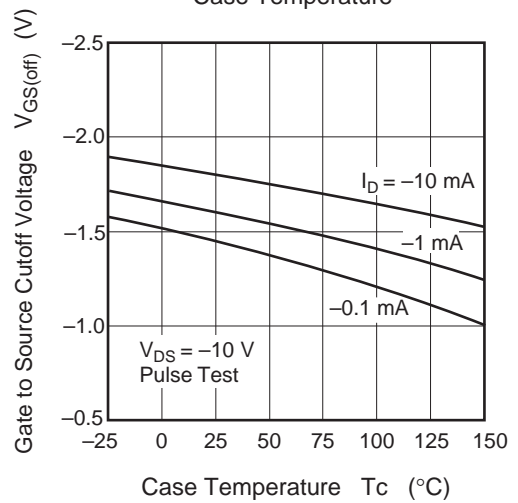
Typical Transfer Characteristics (1)

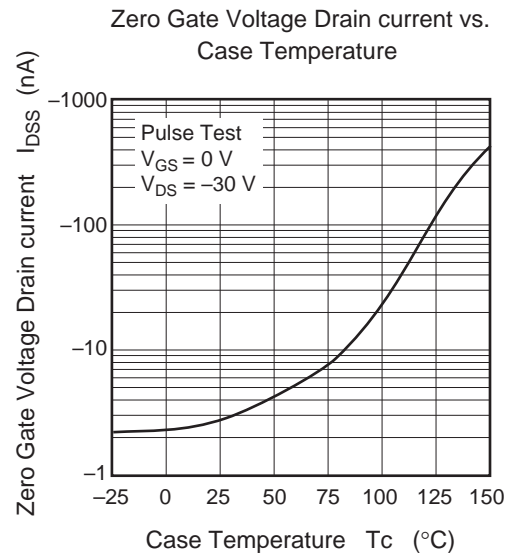
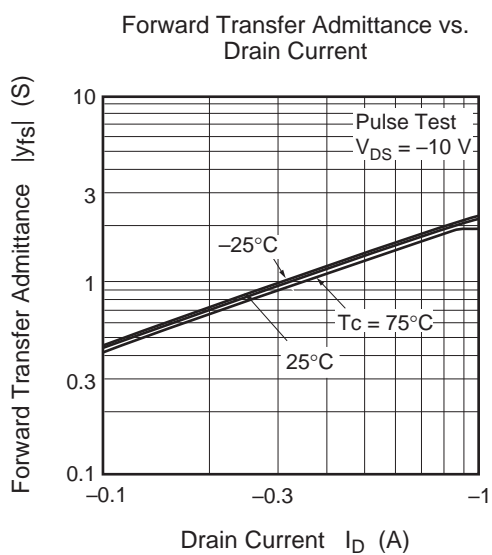
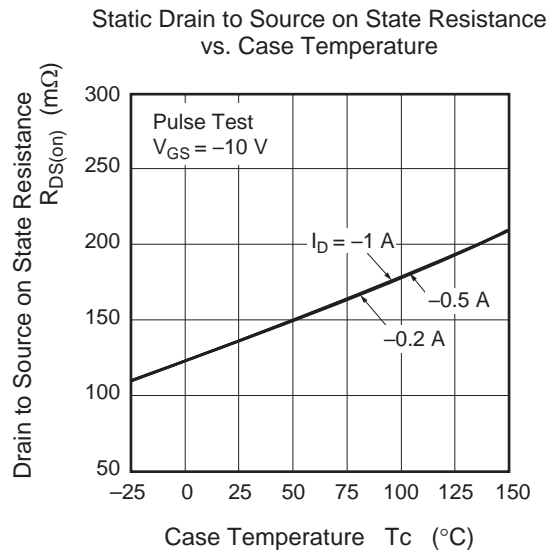
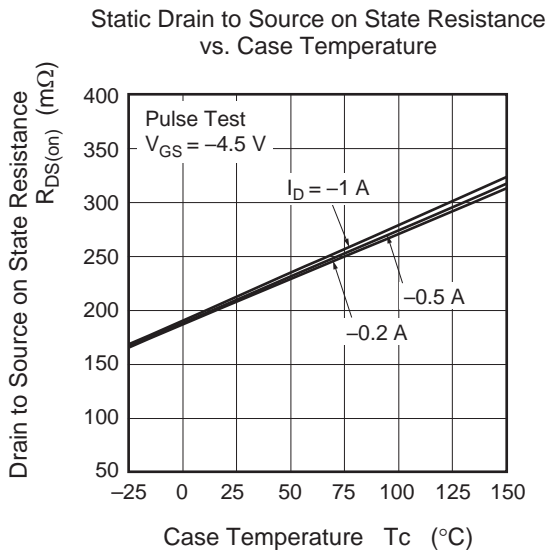
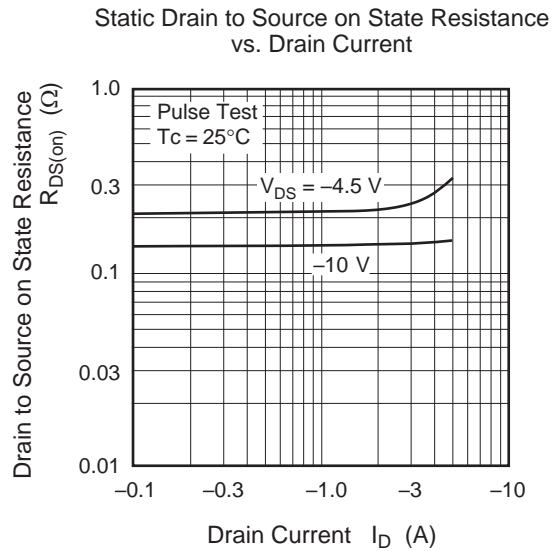
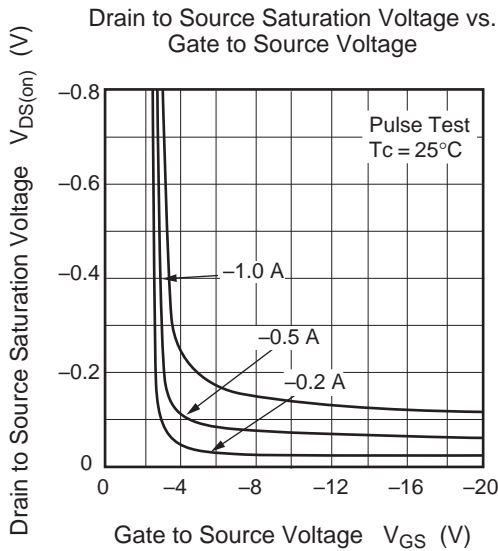


Typical Transfer Characteristics (2)

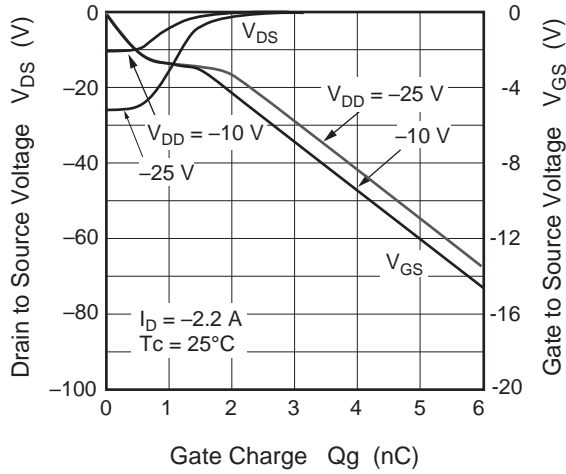


Gate to Source Cutoff Voltage vs. Case Temperature

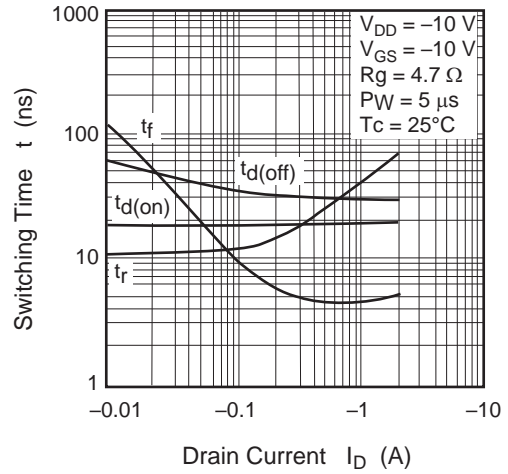




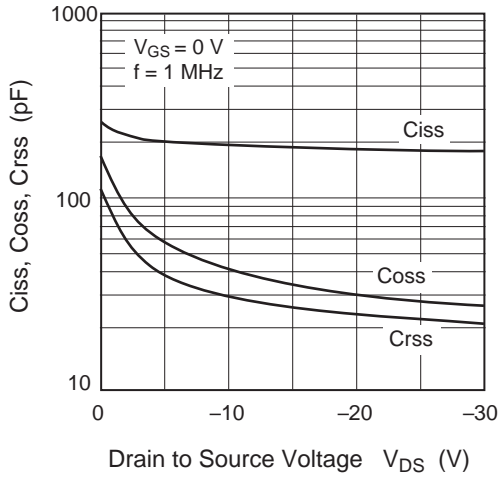
Dynamic Input Characteristics



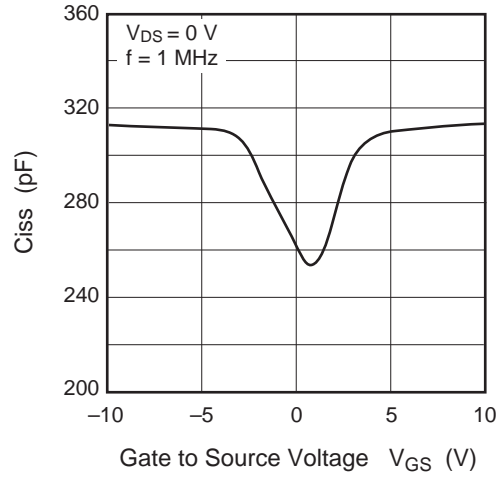
Switching Characteristics



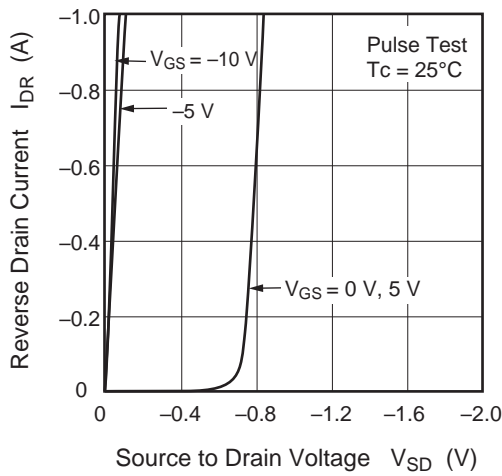
Typical Capacitance vs. Drain to Source Voltage



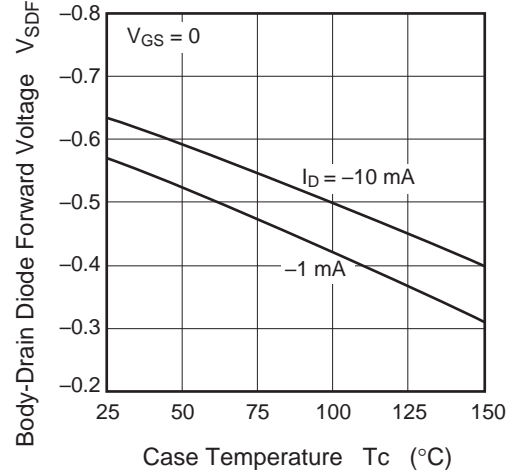
Input Capacitance vs. Gate to Source Voltage



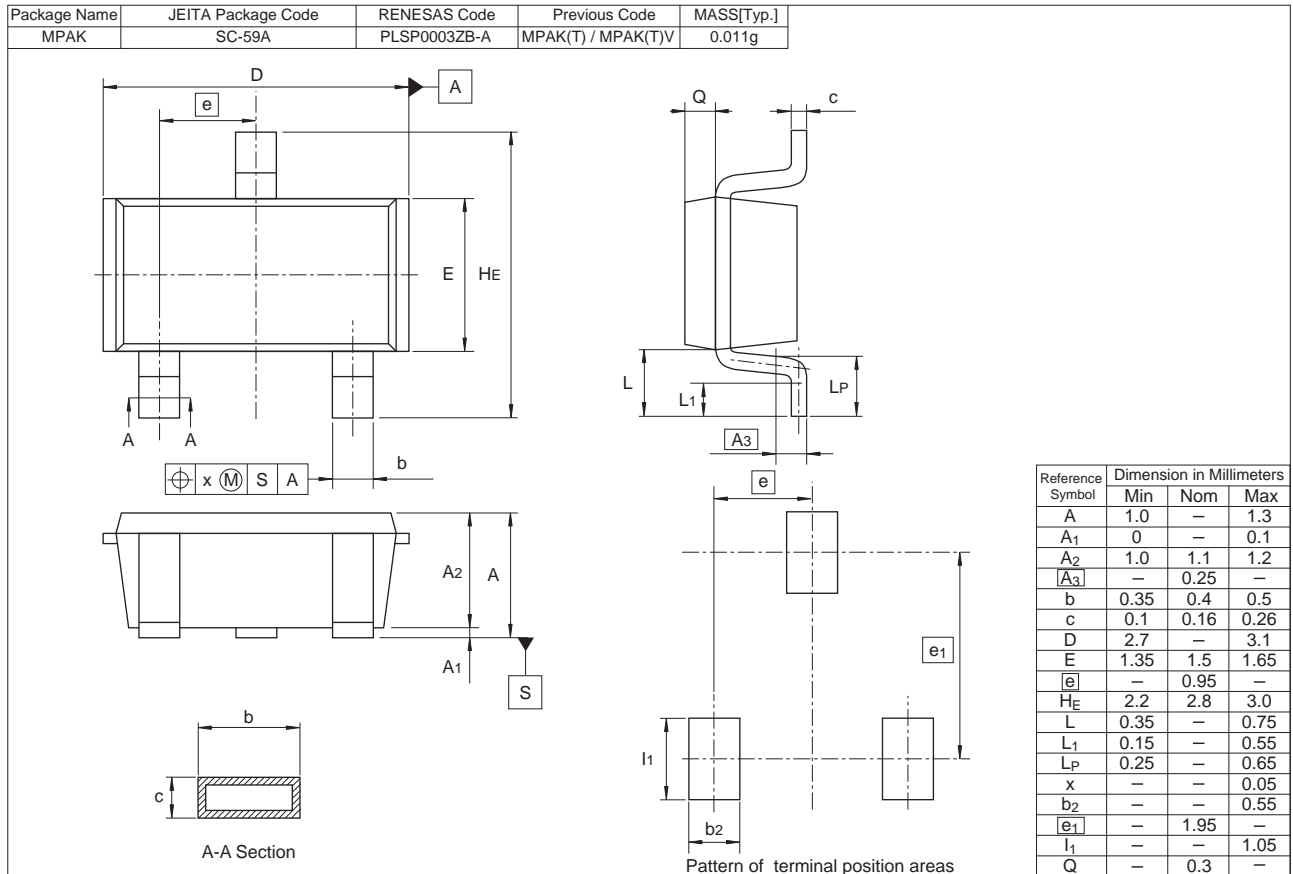
Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
HITJ0302MPTL-HQ	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Note: This product is designed for consumer use and not for automotive.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141