

SOT23 P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVP3306F

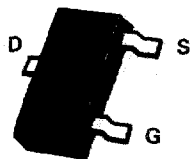
ISSUE 3 - JANUARY 1996

FEATURES

- * 60 Volt V_{DS}
- * $R_{DS(on)}=14\Omega$

PARTMARKING DETAIL - ML

COMPLEMENTARY TYPE - ZVN3306F



SOT23

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	-90	mA
Pulsed Drain Current	I_{DM}	-1.6	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	330	mW
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

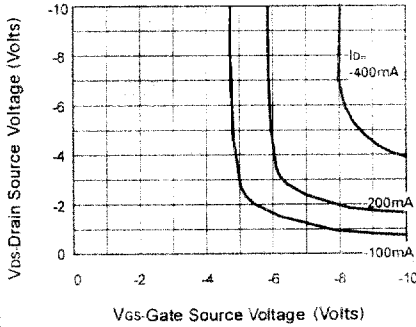
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	-60		V	$I_D=-1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}		20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}		-0.5 -50	μA μA	$V_{DS}=-60V, V_{GS}=0V$ $V_{DS}=-48V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	-400		mA	$V_{DS}=-18V, V_{GS}=-10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		14	Ω	$V_{GS}=-10V, I_D=-200mA$
Forward Transconductance (1)(2)	g_{fs}	60		mS	$V_{DS}=-18V, I_D=-200mA$
Input Capacitance (2)	C_{iss}		50	pF	$V_{DS}=-18V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	C_{oss}		25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	$V_{DD}=-18V, I_D=-200mA$
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		8	ns	
Fall Time (2)(3)	t_f		8	ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.

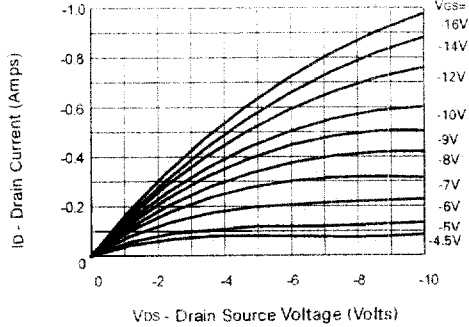
(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator
Spice parameter data is available upon request for this device

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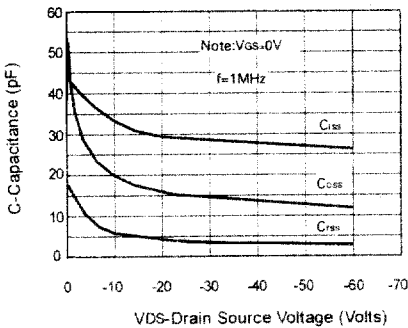
TYPICAL CHARACTERISTICS



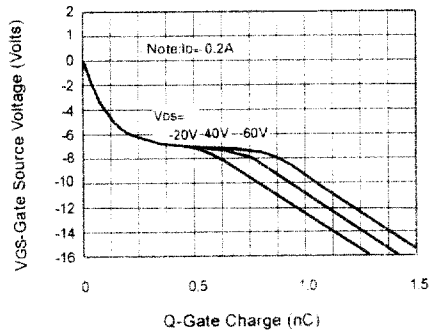
Voltage Saturation Characteristics



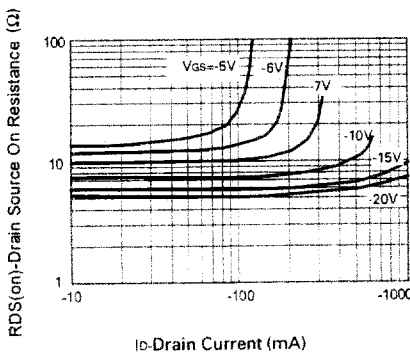
Saturation Characteristics



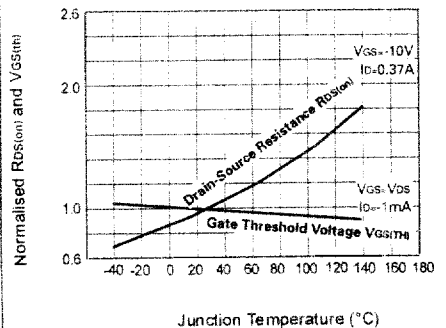
Capacitance v drain-source voltage



Gate charge v gate-source voltage



On-resistance vs Drain Current



Normalised $R_{DS(on)}$ and $V_{GS(th)}$ vs Temperature