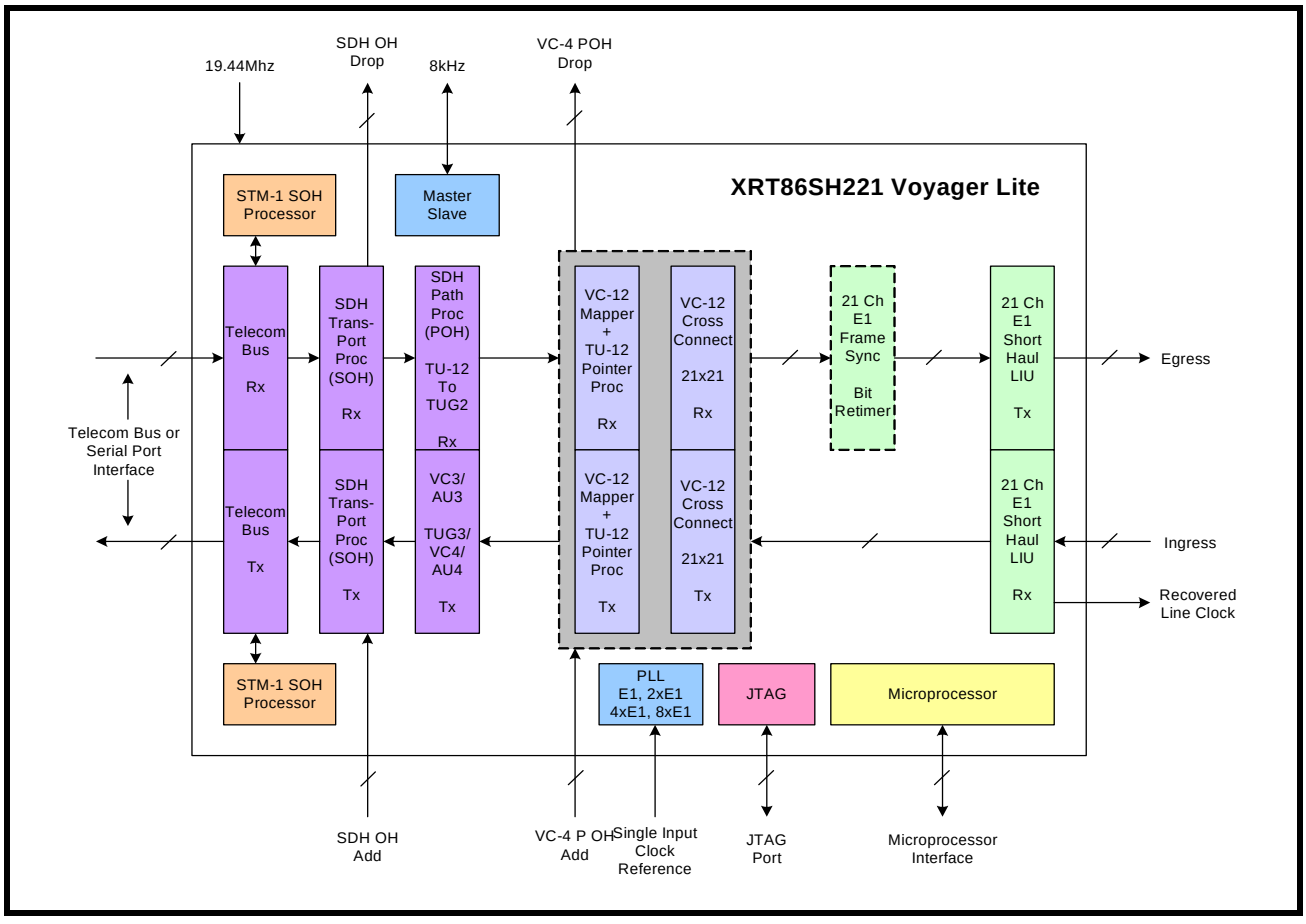
GENERAL DESCRIPTION

The XRT86SH221 (Voyager-Lite) is a physical layer SDH to PDH mapper/demapper which enables E1 aggregation to STM-1 via standard VC-12 to AU-3 and TUG-3/AU-4 mapping protocols. Voyager-Lite supports all the framing, mapping and grooming functions required for STM-1 mapper applications. The device generates and terminates all SDH Regenerator Section, Multiplexer Section and Path Overhead including the low-order Virtual Container (VC) Path Overhead. E1 framing is transparent; therefore, the device neither generates nor terminates the E1 frame.

A single Voyager-Lite performs mapping of 21 asynchronous E1 spans to either VC-12/TU-12/TUG-2/ VC-3/AU-3/STM-0 or VC-12/TU-12/TUG-2/TUG-3/ STM-0. Mapping to STM-1 requires (3) Voyager-Lite devices with one acting as "master" framer and two acting as "slave" framers. In this configuration, Voyager-Lite performs all the necessary framing, pointer processing and mapping functions required for mapping of 63xE1 spans to either VC-12/TU-12/ TUG-2/VC-3/AU-3/STM-1 or VC-12/TU-12/TUG-2/ TUG-3/VC-4/AU-4/STM-1 as shown in the block diagram.

FIGURE 1. SIMPLIFIED BLOCK DIAGRAM



PACKAGE ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT86SH221IB	388 PBGA	-40℃ to +85℃

FEATURES

VT Mapper

- Maps up to 21 synchronous or asynchronous E1 signals to SDH AU-3 via TUG-2 and TU-12, or to SDH STM-0 payload capacity via VT Groups and VT2.
- Dynamic VT/TU size selection.
- Inserts valid V5 bit interleaved parity BIP-2 in the transmit direction.
- Detects and counts V5 BIP-2 errors for performance monitoring.
- Configurable remote error indication REI-V insertion for V5 BIP-2 errors.
- Supports proprietary V5 remote loopcodes.
- Detects and counts remote errors.
- Automatic receive monitor functions include VT/TU remote defect indication RDI-V, VT/TU remote failure indication RFI-V, VT/TU remote error indication REI-V, BIP-2 errors, VT/TU AIS, VT/TU Automatic Protection Switching (APS) signalling for low order path level, and VT/TU loss of pointer LOP-V.
- Automatic receive monitoring functions can be configured to provide an interrupt to the control system, or the device can be operated in a polled mode.
- Test pattern generation and detection/dropping for setup and maintenance.
- User configurable for VT/TU label, AIS-V, RDI-V, RFI-V, REI-V, APS, force BIP-2 errors, or unequipped tributary insertion.

E1 Receive Framing Synchronizer

- Provides a standard compliant 2.048 Mbits PCM30 CRC-4 E1 framer.
- Provides off-line framer.
- Complies with standards such as: ITU-T G.703, G.704, G.706 (including Annex B), G.732, G.735, G.736, G.737, G.761, G.823, I.431 and ETS 300 011, 300 233.
- Supports FAS, Signaling Multiframe, and CRC-4 framing structure.
- FAS reframe time is 625µs maximum.
- Provides Loss Of Frame (LOF), Loss of Multiframe detection.
- Provides Change Of Frame Alignment (COFA) detection.
- Provides Change Of signaling MultiFrame Alignment (COMFA) detection.
- Provides a 2-frame slip buffer for bit retiming.

SDH Transmitter

- Performs standard STM-0/STM-1 transmit processing.
- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253
- Provides a 51.84MHz STM-0 serial interface or 6MHz / 19MHz 8-bit STM-0 / STM-1 parallel interface.
- Performs SDH frame insertion and accepts external frame synchronization.
- Performs optional transmit data scrambling.
- Performs POH, SDH OH generation/insertion.
- Generates transmit payload pointer (H1, H2) (fixed at 522) with NDF insertion.
- Inserts A1/A2 with optional error mask.
- Computes and inserts BIP-8 (B1, B2) with optional error mask.
- Generates AIS-L, REI-L and RDI-L according to receiver state with option of SW or HW insertion.
- Inserts LOS, forces SEF by software.
- Generates RDI-P and REI-P automatically with optional SW or HW override.
- Inserts fixed-stuff columns, calculates and inserts B3 error code.

SDH Receiver

- Performs standard STM-0/STM-1 receive processing.
- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253.
- Provides fully programmable threshold detection for SD and SF conditions.
- Provides a 51.84MHz STM-0 serial interface or 6MHz / 19MHz 8-bit STM-0 / STM-1 parallel interface.
- Provides section trace buffer with mismatch detection and invalid message detection.
- Performs SDH frame synchronization.
- Supports NDF, positive stuff and negative stuff for pointer processor.
- Performs receive data de-scrambling.
- Performs POH, SDH OH interpretation/extraction.
- Interprets payload pointer (H1, H2).
- Detects Out Of Frame (OOF), Loss Of Frame (LOF), Loss Of Signal (LOS), APS failure.
- Detects Line Alarm Indication(L-AIS), Line remote Defect Indication (L-RDI), Loss Of Pointer.
- Detects Path Alarm Indication, Path remote Defect Indication, Path extended RDI.
- Provides signal label monitor with PLM detection.
- Supports path trace buffer with TIM-P and invalid message detection.
- Computes and compares B3, REI-L and REI-P errors.
- Computes and compares BIP-8 (B1, B2) and counts the errors.

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1.0 PIN DESCRIPTIONS

1.1 MICROPROCESSOR INTERFACE PINS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
J26 K25 M23 K26 L25 M26 N25 P26 P24 R25 R24 T25 R23 U25 V25 U24 Y26 U23	L30 M29 M30 N28 N29 P29 R30 R27 R28 T29 T27 U29 U28 V29 W30 W29 V27 AA30	A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I	**Address Input Pins** These address input pins are used for the microprocessor interface to the XRT86SH221. For timing information, please refer to the timing diagrams in the Electrical Specifications section of this datasheet.
L24 L26 N23 N26 R26 U26 V26 W26	N27 P26 P27 R29 T30 T26 U27 U26	D7 D6 D5 D4 D3 D2 D1 D0	I/O	**Bi-Directional Data Bus Pins** These bi-directional data bus pins are used for the microprocessor interface to the XRT86SH221. For timing information, please refer to the timing diagrams in the Electrical Specifications section of this datasheet.
T24	V30	ALE / AS	I	**Address Latch Enable / Address Strobe** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
T26	U30	CS	I	**Chip Select Input**
M24	N30	INT	O	**Interrupt Request Output** This active-low output signal will be asserted any time the XRT86SH221 is requesting interrupt service from the microprocessor. ***NOTE:*** *This output pin is open-drain and requires a 10kΩ pull-up resistor.*
T23	V28	RD / DS / WE	I	**Read Strobe / Data Strobe** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
W25	Y30	WR / R/W	I	**Write Strobe / Read-Write Operation Identifier** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.

1.1 MICROPROCESSOR INTERFACE PINS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
P25	R26	RDY / Dtack / TA	O	**Ready or DTACK Output** The function of this output pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
P2	P1	Reset	I	**Hardware Reset** It is recommended to initiate a HW reset upon power up before configuring the device. This pin must be pulled "Low" for a minimum of 10µS to activate the reset circuitry. During a HW reset, all outputs will be tri-stated and all on-chip registers will be reset to their default values.Note: This pin has an internal 10kΩ pull-up resistor.
P23	T28	PCLK	I	**Microprocessor Interface Clock Input** This input clock signal is only used for the synchronous microprocessor interface modes. This pin is ignored in the asynchronous microprocessor interface mode.Note: The input frequency range of PCLK is 66MHz.
AC3 AB3 AA4	AF3 AG2 AH1	PTYPE2 PTYPE1 PTYPE0	I	**Microprocessor Type Select Inputs** These input pins are used to select the microprocessor mode according to the following table: **PTYPE[2:0] / Microprocessor Interface Mode** 000 – Intel Asynchronous 001 – Motorola Asynchronous 101 – Power PC 403 111 – MPC86x
N24	P30	DBEN	I	**Data Bus Enable** This active-low input pin is used to enable the bi-directional data bus. To disable the data bus, this pin must be pulled "High". For normal operation, this pin should be pulled "Low".
R3 P4	T5 T3	EXT_INT_1 EXT_INT_0	I	**External Interrupt Input [1:0]** These pins can be used to force an interrupt request to the microprocessor by pulling either of these two pins "High". The interrupt will be generated on the INT output pin. ***NOTE:*** *If not used, these pins should be pulled "Low".*
M25	P28	BLAST	I	**Reserved** This pin can be left floating or tied to ground.

1.2 BOUNDARY SCAN AND OTHER TEST PINS

388B BALL	568BALL	PIN NAME	TYPE	DESCRIPTION
JTAG Test Pins				
D2	F4	TCK	I	**Test Clock Input** This pin is used for the boundary scan clock input. For normal operation, this pin should be pulled "Low".
D3	H6	TDI	I	**Test Data Input** This pin is used for the boundary scan input data signal. For normal operation, this pin should be pulled "Low".
E4	E4	TDO	O	**Test Data Output** This pin is used for the boundary scan output data signal.
C2	C2	TMS	I	**Test Mode Select** This pin is used for the boundary scan test mode select input signal. For normal operation, this pin should be pulled "High".
F4	G5	TRST	I	**Test Mode Reset** This pin is used for the boundary scan reset input signal. For normal operation, this pin should be pulled "High".
Analog Continuity and Test Pins				
P3	R4	TESTMODE	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
M3	L1	SCAN_MODE	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
AE2	AD5	SCAN_ENB	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
B15 A15	C15 E15	ATP_RING1 ATP_TIP1	I/O	**Analog Test Point - TIP/RING 1** These pins along with the TMS and TCK boundary scan pins are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with E1 channels 0 through 13. ***NOTE:*** *If not used, these pins should be left floating.*
AF14 AE14	AF15 AJ14	ATP_RING2 ATP_TIP2	I/O	**Analog Test Point - TIP/RING 2** These pins along with the TMS and TCK boundary scan pins are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with E1 channels 14 through 20. ***NOTE:*** *If not used, these pins should be left floating.*
C14 AD14	D15 AH14	ANALOG1 ANALOG2	O	**For Factory Use Only** These pins should be left floating
A13 AC14	A14 AG14	SENSE1 SENSE2	O	**For Factory Use Only** These pins should be left floating

1.3 GENERAL PURPOSE INPUT AND OUTPUT PINS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
GPIO Pins				
F3 E2 C1 H4 AD2 AC2 AE1 Y4	H5 D2 G4 C1 AC5 AD4 AE3 AF2	GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0	I/O	**General Purpose I/O** Each of these pins can be configured to function as either a general purpose input or output pin by programming the GPIO registers outlined in the register map. One register is used to set the direction of each pin, while the other register is used to Read/Write the value of each pin dependent on its direction. ***NOTE:*** *If not used, these pins should be left floating.*

1.4 TIMING AND CLOCK SIGNALS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
Timing and Clock Pins				
G4	E3	MCLK	I	**Master Clock PLL Reference Input Clock** This input functions as the reference input pin to the PLL master clock and can accept any of the following signals by programming the appropriate internal register. 2.048 / 4.096 / 8.192 / 16.384 MHz.
A1	F5	EXT_OSC_ENB	I	**External Oscillator Enable** This pin must be pulled "Low".
R2	R1	EXT_OSC	I	**External Oscillator** This pin must be pulled "Low".

1.4 TIMING AND CLOCK SIGNALS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
R1	R3	TX51_19MHZ	I	**Transmit STM-0/STM-1 Timing Reference Input** The function of this pin depends upon which mode the XRT86SH221 has been configured to operate in. **SDH Over Serial Interface (STM-0 Only)** In this case, the XRT86SH221 will be configured to transmit data at a rate of 51.84MHz on the system side serial interface. Provide a 51.84MHz clock signal to this pin. The Transmit STM-0 POH and SOH Processor blocks will use this clock signal as its timing reference. **SDH Over Telecom Bus Interface** In this case, the XRT86SH221 will be configured to output either an STM-0 or STM-1 signal via the Transmit STM-0/STM-1 Telecom Bus Interface. Provide a 19.44MHz clock signal to this pin for STM-1 or a 6.48MHz clock for STM-0 applications. The Transmit STM-0/STM-1 POH and SOH Processor blocks will use this clock signal as its timing reference.
N4	P5	TxSBFP_IN_OUT	I/O	**Transmit System Bus Frame Pulse Input / Output** The direction of this frame pulse is determined by whether the XRT86SH221 is the Master of Slave device in STM-1 shared Telecom Bus applications whereby three Voyager-Lite devices are connected together. **If the XRT86SH221 (along with two other XRT86SH221 devices) is configured to exchange STM-1 data over a common Telecom Bus, and this particular device is the Master Device - TxSBFP_OUT:** The Master XRT86SH221 will pulse this output pin "High" when it outputs the very first A1 byte (of a given outbound STM-1 frame) via the Transmit STM-1 Telecom Bus Interface. This pin will be kept "Low" at all other times. **If the XRT86SH221 (along with two other XRT86SH221 devices) is configured to exchange STM-1 data over a common Telecom Bus, and this particular device is the Slave Device - TxSBFP_IN:** The Transmit STM-1 SOH Processor Block (within a given slave device) can be configured to initiate its generation of a new outbound STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. The Transmit STM-1 Telecom Bus Interface will begin transmitting the very first byte of a given STM-1 frame, upon sensing a rising edge of the 8kHz signal on this pin.

1.5 LOW SPEED LINE INTERFACE SIGNALS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
E1 Receive Line Interface Signals				
AB23 AC21 AE21 AC17 AE17 AE11 AF8 AC9 AC7 AF1 B2 C6 A5 C10 A11 A18 C18 D19 C22 D24 E25	AG25 AJ26 AG22 AH19 AK18 AH12 AK6 AJ5 AK2 AE5 A1 A2 A5 D10 D12 E17 E18 C22 E23 F23 E27	RTIP20 RTIP19 RTIP18 RTIP17 RTIP16 RTIP15 RTIP14 RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	I	**Receive E1 Line Input - Positive Polarity Signal** RTIP and RRING are differential analog input pins that receive standard E1 Return-to-Zero data, coupled through a 1:1 transformer. The transformer blocks the DC line bias and allows the inputs to be level shifted to mid-power supply.
AC24 AD22 AC19 AD18 AF18 AF10 AE8 AD8 AF2 AD3 D4 D7 D9 A8 B11 B18 B20 A24 C23 E24 C26	AE23 AH25 AF21 AF18 AF17 AJ11 AJ7 AF9 AG6 AE4 B1 B3 B6 E11 A10 A20 C20 D21 C26 D26 D28	RRING20 RRING19 RRING18 RRING17 RRING16 RRING15 RRING14 RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	I	**Receive E1 Line Input - Negative Polarity Signal** RTIP and RRING are differential analog input pins that receive standard E1 Return-to-Zero data, coupled through a 1:1 transformer. The transformer blocks the DC line bias and allows the inputs to be level shifted to mid-power supply.

1.5 LOW SPEED LINE INTERFACE SIGNALS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
AE26 Y23	AF27 AG28	RCLK_REC1 RCLK_REC0	O	**Recovered Line Clock Output** Each of these pins can be internally routed to one of the 21 E1 Recovered Line Clocks to be used as an output clock reference, selected by programming the appropriate registers. By default (or if the recovered line clock is not selected), these output pins are tri-stated.
E1 Transmit Line Interface Signals				

1.5 LOW SPEED LINE INTERFACE SIGNALS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
AE25 AC20 AC18 AD17 AE16 AE12 AF9 AD9 AC8 AC6 D6 B6 D10 B10 A12 A17 A19 C19 A25 C24 D25	AF23 AG23 AJ23 AK19 AK17 AF14 AJ8 AJ6 AJ4 AF4 E5 C5 C8 D11 A11 D17 B20 D20 C25 D25 C28	TTIP20 TTIP19 TTIP18 TTIP17 TTIP16 TTIP15 TTIP14 TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	O	**Transmit E1 Line Output - Posittive Polarity Signal** TTIP and TRING are differential analog output pins that transmit standard E1 Return-to-Zero data. The amplitude of the output pulse is half the nominal E1 standard and level shifted to $V_{CC}/2$ to allow for optimum pulse shaping capability. Therefore, it's necessary to couple these analog outputs to a 1:2 step-up transformer to apply a gain of 2x. It is recommended to connect a 0.1µF capacitor in series with each TTIP signal.
AD24 AE23 AF23 AE19 AC15 AD12 AC11 AF6 AE5 AD4 C4 A3 B7 B9 D13 C16 A20 C20 B24 B25 G23	AJ27 AF22 AK25 AJ19 AH17 AK11 AG10 AK4 AH5 AH2 C3 F8 E10 B9 C12 C18 B21 A24 D24 E24 E26	TRING20 TRING19 TRING18 TRING17 TRING16 TRING15 TRING14 TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	O	**Transmit E1 Line Output - Negative Polarity Signal** TTIP and TRING are differential analog output pins that transmit standard E1 Return-to-Zero data. The amplitude of the output pulse is half the nominal E1 standard and level shifted to $V_{CC}/2$ to allow for optimum pulse shaping capability. Therefore, it's necessary to couple these analog outputs to a 1:2 step-up transformer to apply a gain of 2x.

1.6 HIGH SPEED SERIAL INTERFACE

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
SDH Receive Serial Interface				
T1	T1	RxSTM0CLK	I	**Receive STM-0 Serial Input Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the serial interface is enabled, the XRT86SH221 samples data on the rising edge of this input clock signal.
T2	U1	RxSTM0DATA	I	**Receive STM-0 Serial Input Data** Apply the serial input data to this pin, and it can be sampled on either the rising edge or falling edge of the RxSTM0CLK input pin.
U1	U2	RxSTM0FRAME	I	**Receive STM-0 Serial Frame Pulse** This input pin should be connected to the Frame Pulse to indicate when the first bit of the current STM-0 frame occurs if connected to an external device, where this option is available.
R4	U5	RxSTM0LOS	I	**Receive STM-0 Serial Loss of Signal** If the high speed serial interface is connected to an external LIU (Line Interface Unit), then this input signal can be connected to the LOS output pin from the LIU.
SDH Transmit Serial Interface				
N2	P3	TxSTM0CLK	O	**Transmit STM-0 Serial Output Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the serial interface is enabled, then the XRT86SH221 updates data on the rising edge of this output clock signal. The source of this clock can be a buffered clock derived from the recovered line clock in loop timing mode, or buffered from the internal master clock in local timing mode.
N1	R5	TxSTM0DATA	O	**Transmit STM-0 Serial Output Data** The serial output data can be updated on either the rising edge or falling edge of the TxSTM0CLK output pin.
P1	P2	TxSTM0FRAME	O	**Transmit STM-0 Serial Frame Pulse** This output frame pulse is used to indicate when the first bit of the current STM-0 frame is transmitted if connected to an external device, where this option is available.

1.7 HIGH SPEED TELECOM BUS INTERFACE

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
SDH Receive Telecom Bus Interface				
T3	V2	RxD_CLK	I	**Receive STM-0/STM-1 Telecom Input Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the Telecom Bus is enabled, then all telecom bus signals are sampled on the rising edge of this input clock. This clock should be 6.48MHz for STM-0 or 19.44MHz for STM-1.
V2	V5	RxD_DP	I	**Receive STM-0/STM-1 Telecom Data Polarity** This input pin can be configured to operate as the EVEN or ODD parity value of either the Receive Telecom Data Bus RxD_D[7:0] or the Payload Indicator RxD_PL and Frame Pulse RxD_C1J1V1_FP. ***NOTE:*** *This pin should be pulled "Low" if the part is configured for Re-Phase On.*
U2	V3	RxD_PL	I	**Receive STM-0/STM-1 Telecom Payload Indicator** This input pin is used to indicate when payload bytes within an STM-0/STM-1 frame are being processed. This pin should be pulled "High" for the entire duration of the payload bytes, and pulled "Low" at all other times.
T4	W3	RxD_ALARM	I	**Receive STM-0/STM-1 Telecom Alarm Status** This input pin should be pulled "High" corresponding to any STM-0/VC-3 signal that is carrying either the AU-AIS or TU-AIS indicator. At all other times, this pin should be pulled "Low". If this pin is pulled "High", the XRT86SH221 will automatically declare the AU-AIS or TU-AIS defect for that particular VC-3.
V1	Y1	RxD_C1J1V1_FP	I	**Receive STM-0/STM-1 Telecom Frame Pulse** The XRT86SH221 can be configured for Re-Phase On or Re-Phase Off, meaning that frame synchronization can be externally supplied to this input pin, or the XRT86SH221 can gain frame synchronization from the incoming data. **Re-Phase Off** This pin is ignored and can be tied to ground or left floating. **Re-Phase On** This pin should be pulled "High" during the C1 byte, J1 byte, and V1 byte. At all other times, this pin should be pulled "Low". ***NOTE:*** *When 3 XRT86SH221 chips share the telecom bus in a Master/Slave mode, the C1 bytes must be aligned on all three input pins. The J1 and/or V1 bytes do not have to be aligned.*
Y3 AC1 AB1 AA1 Y2 W2 W1 U3	AE1 AD1 AA4 AC1 AB2 AB1 AA2 Y3	RxD_D7 RxD_D6 RxD_D5 RxD_D4 RxD_D3 RxD_D2 RxD_D1 RxD_D0	I	**Receive STM-0/STM-1 Telecom Input Data Bus** These input pins are sampled on the rising edge of the Receive Telecom Input Clock RxD_CLK. The MSB of the data bus is bit 7, and the LSB is bit 0.

1.7 HIGH SPEED TELECOM BUS INTERFACE

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
SDH Transmit Telecom Bus Interface				
N3	M1	TxD_CLK	O	**Transmit STM-0/STM-1 Telecom Output Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the Telecom Bus is enabled, then all telecom bus signals are updated on the falling edge of this output clock. The source of this clock can be a buffered clock derived from the recovered line clock in loop timing mode, or buffered from the internal master clock in local timing mode. This clock should be 6.48MHz for STM-0 or 19.44MHz for STM-1.
L2	L2	TxD_DP	O	**Transmit STM-0/STM-1 Telecom Data Polarity** This output pin can be configured to operate as the EVEN or ODD parity value of either the Transmit Telecom Data Bus TxD_D[7:0] or the Payload Indicator TxD_PL and Frame Pulse TxD_C1J1V1_FP.
M1	N3	TxD_PL	O	**Transmit STM-0/STM-1 Telecom Payload Indicator** This output pin is used to indicate when payload bytes within an STM-0/STM-1 frame are being transmitted. This pin will be pulled "High" for the entire duration of the payload bytes, and pulled "Low" at all other times.
K1	K1	TxD_ALARM	O	**Transmit STM-0/STM-1 Telecom Alarm Status** This output pin will be pulled "High" corresponding to any STM-0/VC-3 signal that is carrying either the AU-AIS or TU-AIS indicator. At all other times, this pin will be pulled "Low".
M2	M2	TxD_C1J1V1_FP	O	**Transmit STM-0/STM-1 Telecom Frame Pulse** The XRT86SH221 can be configured for Re-Phase On or Re-Phase Off, meaning that frame synchronization can be externally provided to the system or act as a simple Frame Pulse. **Re-Phase Off** This pin is pulled "High" during the A1 byte. At all other times, this pin is pulled "Low". **Re-Phase On** This pin is pulled "High" during the C1 byte, J1 byte, and V1 byte. At all other times, this pin is pulled "Low". ***NOTE:*** *When 3 XRT86SH221 chips share the telecom bus in a Master/Slave mode, all three chips will output this signal.*
H2 K3 L4 J2 J1 K2 L3 M4	G2 J3 H2 G1 J2 H1 J1 K2	TxD_D7 TxD_D6 TxD_D5 TxD_D4 TxD_D3 TxD_D2 TxD_D1 TxD_D0	O	**Transmit STM-0/STM-1 Telecom Output Data Bus** These output pins are updated on the rising edge of the Transmit Telecom Output Clock TxD_CLK. The MSB of the data bus is bit 7, and the LSB is bit 0.

1.8 HIGH SPEED SECTION AND PATH OVERHEAD BUS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive Section and Path Overhead Extraction Bus				
V3	AA3	RxOH	O	**Receive SOH/POH Data Output Port** The extracted SOH/POH overhead bytes will be updated on this output pin on the falling edge of RxOHCLK. Therefore, RxOH should be sampled using the rising edge of RxOHCLK.
Y1	W5	RxOHCLK	O	**Receive SOH/POH Overhead Clock Output** This output clock signal is used as the timing reference for the Receive Overhead Extraction Bus. This clock will update all output extraction bus pins on its falling edge.
V4	Y5	RxOHFRAME	O	**Receive SOH/POH Overhead Frame Boundary Indicator** The Receive SOH/POH Data Output Port will pulse this output pin "High" for one period of RxOHCLK, coincident to whenever it is extracting the very first bit of the STM-0/STM-1 frame in the Section Overhead (A1) and the very first bit of the Path Overhead (J1). If RxPOH_IND is "Low" during this Frame Pulse, then that bit is A1. If RxPOH_IND is "High" during this Frame Pulse, then that bit is J1. This pin will be pulled "Low" at all other times.
U4	Y4	RxOHVALID	O	**Receive SOH/POH Overhead Data Valid Indicator** This output pin will be pulled "High" when the extracted SOH and POH bytes are ready to be sampled from the overhead bus. This pin will be pulled "Low" at all other times. If RxPOH_IND is "Low" while RxOHVALID is "High", then SOH is valid. If RxPOH_IND is "High" while RxOHVALID is "High", then POH is valid. This pin will be pulled "Low" at all other times.
W3	AB3	RxPOH_IND	O	**Receive POH Indicator** The Receive Path Overhead Indicator will pull "High", coincident to whenever it is extracting Path Overhead data via the RxOH output pin. Conversely, this pin will pull "Low", coincident to whenever it is extracting Section Overhead data via the RxOH output pin. This pin will be updated on the falling edge of RxOHCLK.
Transmit Section and Path Overhead Insertion Bus				
K4	E1	TxOHEN	O	**Transmit SOH/POH Overhead Port Enable Output** The state of this output pin determines the time period when the XRT86SH221 can accept SOH/POH overhead bytes. The Overhead Insertion Bus is active when this pin is pulled "High".
G2	F2	TxOH	I	**Transmit SOH/POH Data Input Port** If the System Side Terminal Equipment intends to insert its own value for a given overhead SOH or POH byte into the outbound STM-0 or STM-1 data-stream, then the System Side Terminal Equipment is expected to apply the overhead bytes to this input pin while asserting the TxOHINS input pin. This input pin is sampled upon the rising edge of TxOHCLK.
G1	H3	TxOHCLK	O	**Transmit SOH/POH Overhead Clock Output** This output clock signal is used as the timing reference for the Transmit Overhead Insertion Bus. This clock will sample all input insertion bus pins on its rising edge.

1.8 HIGH SPEED SECTION AND PATH OVERHEAD BUS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
J3	J4	TxOHFRAME	I/O	**Transmit SOH/POH Overhead Frame Boundary Indicator** The Transmit SOH/POH Data Input Port will pulse this output pin "High" for one period of TxOHCLK, coincident to whenever it is processing the very first SOH byte of a given outbound STM-0/ STM-1 frame in the Section Overhead (A1) and the very first bit of the Path Overhead (J1). If TxPOH_IND is "Low" during this Frame Pulse, then that bit is A1. If TxPOH_IND is "High" during this Frame Pulse, then that bit is J1. This pin will be pulled "Low" at all other times.
H1	F1	TxOHINS	I	**Transmit SOH/POH Overhead Insertion Input** If the System Side Terminal Equipment intends to insert its own value for a given overhead SOH or POH byte into the outbound STM-0 or STM-1 data-stream, then this input pin should be pulled "High" coincident with the SOH or POH bytes. This input pin is sampled upon the rising edge of TxOHCLK.
F1	K5	TxPOH_IND	I/O	**Transmit POH Indicator** The Transmit SOH/POH Data Input Port will toggle and hold this output pin "High", coincident to whenever it is ready to accept POH data via the TxOH input pin. Conversely, this pin will hold this pin "Low", coincident to whenever it is ready to accept SOH data via the TxOH input pin. This pin will be updated on the falling edge of TxOHCLK as an output (or sampled on the rising edge as an input).

1.9 HIGH SPEED TU POH OVERHEAD BUS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive TU POH Extraction Bus				
W4	AA5	RxTUPOH	O	**Receive TU POH Data Output Port** This output pin will output the contents of the VC-4 POH bytes within the incoming STM-1 data-stream. This output is updated on the falling edge of RxTUPOHCLK.
AA2	AB4	RxTUPOHCLK	O	**Receive TU POH Overhead Clock Output** If the XRT86SH221 along with two other devices has been configured to operate in the STM-1/TUG-3 Mode, this output clock signal is used as the timing reference for the Receive VC-4 POH Overhead Extraction Bus. This clock will update all output extraction bus pins on its falling edge.
AD1	AD2	RxTUPO-HFRAME	O	**Receive TU POH Data Output Port - Frame Boundary Output** The Receive TU POH Data Output Port will pulse this output pin "High" for one period of RxTUPOHCLK, coincident to whenever it is extracting the very first bit of the VC-4 POH. This pin will be pulled "Low" at all other times.
AA3	AB5	RxTUPOHVALID	O	**Receive TU POH Data Output Port - Overhead Indicator Output** This output pin will be pulled "High" when the extracted VC-4 POH bytes are ready to be sampled from the overhead bus. This pin will be pulled "Low" at all other times.

1.9 HIGH SPEED TU POH OVERHEAD BUS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
Transmit TU POH Insertion Bus				
J4	D1	TxTUPOHEN	O	**Transmit TU POH Overhead Port Enable Output** The state of this output pin determines the time period when the XRT86SH221 can accept VC-4 POH overhead bytes. The Overhead Insertion Bus is active when this pin is pulled "High".
F2	F3	TxTUPOH	I	**Transmit TU POH Data Input Port** If the System Side Terminal Equipment intends to insert its own value for a given VC-4 POH byte, then the System Side Terminal Equipment is expected to apply the overhead bytes to this input pin while asserting the TxTUPOHINS input pin. This input pin is sampled upon the rising edge of TxTUPOHCLK.
H3	H4	TxTUPOHCLK	O	**Transmit TU POH Overhead Clock Output** This output clock signal is used as the timing reference for the Transmit Overhead Insertion Bus. This clock will sample all input insertion bus pins on its rising edge.
E1	G3	TxTUPO-HFRAME	I/O	**Transmit TU POH Overhead Frame Boundary Indicator** The Transmit TU POH Data Input Port will pulse this output pin "High" for one period of TxTUPOHCLK, coincident to whenever it is processing the very first VC-4 POH byte. This pin will be pulled "Low" at all other times.
D1	J5	TxTUPOHINS	I	**Transmit TU POH Overhead Insertion Input** If the System Side Terminal Equipment intends to insert its own value for a given overhead VC-4 POH byte, then this input pin should be pulled "High" coincident with the TU POH bytes. This input pin is sampled upon the rising edge of TxTUPOHCLK.

1.10 POWER AND GROUND PINS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
Power Supply				
B1, AB2, AB25, M15, P15, N15, A2, R15, M14, M13, P14, P13, N14, N13, R14, R13, M12, P12, N12, R12, G3	J6, AD3, AB25, E25, E20, P17, T17, R17, C4, U17, P16, P15, T16, T15, R16, R15, U16, U15, P14, T14, R14, U14, K6	1.8V Digital	-	**1.8V Digital Power Supply**
AC12, AF15, AE20, B22, B14, A10, AF13, D14	AF12, AK13, AG19, B26, B15, B10, AJ16, B17	1.8V Analog	-	**1.8V Analog Power Supply**
J23, P16, N16, L14, L13, T14, T13, P11, N11	J25, T18, R18, N16, AJ30, N15, V16, V15, T13, R13	3.3V Digital	-	**3.3V Digital Power Supply**
AE4, AD7, AF7, AD11, AD13, AD15, AE18, AF21, AE22, AD23, F23, D22, C21, A22, D16, A16, B13, D12, B8, A4, B4, AD5, AF3, AE7, AE9, AC13, AF17, AF19, AD19, AF25, AC23, B26, D23, B23, A23, B19, D15, B12, A9, C9, D8, C5	AG4, AK3, AK5, AG11, AK12, AH16, AJ18, AF20, AJ25, AG24, B29, F22, E22, B22, D18, A18, D13, A9, A7, A3, F7, AG3, AF8, AH7, AH9, AJ12, AJ17, AG18, AK24, AE21, AK28, D27, B28, A28, E19, A21, A19, E13, C10, D9, D6, D4	3.3V Analog	-	**3.3V Analog Power Supply**
Ground Pins				
C3, E3, AB4, AC4, H23, M16, L16, L15, T16, T15, R16, M11, L12, L11, T12, T11, R11, AE3, AE6, AC10, AE10, AF12, AF16, AC16, AF22, AD21, AC22, C25, A26, D20, D18, C17, B16, C13, C11, A7, C7, B3, AC5, AD6, AF5, AD10, AF11, AD16, AF20, AD20, AE24, AF26, F24, E23, D21, B21, D17, B17, C12, D11, A6, B5, D5, AF4, AE15, AF24, A21, A14, C8, AE13, C15	G6, D3, AC6, AD6, AD25, G25, P18, N18, N17, V18, V17, U18, P13, N14, N13, V14, V13, U13, AF5, AG7, AF10, AK7, AH13, AK16, AH18, AG21, AH24, AE22, F24, A29, F21, C21, C19, B18, B12, E12, A6, B4, D5, AJ1, AE9, AG8, AF11, AG13, AG17, AK20, AJ24, AK27, AH26, F26, C27, B27, B23, D19, B19, B11, A8, B7, E7, B2, AE10, AJ13, AH23, A22, A15, C7, AF16, C17	GND	-	**Ground**

1.10 POWER AND GROUND PINS

388 BALL	568 BALL	PIN NAME	TYPE	DESCRIPTION
No Connect Pins				
AB24, AA23, AD25, AC25, AA24, AD26, W23, AA25, Y24, AC26, W24, V23, AB26, AA26, Y25, V24, J25, L23, K24, H26, H25, G26, K23, J24, G25, F26, E26, H24, D26, G24, F25, L1	E2, L5, K4, M5, L4, K3, L3, N5, M4, M3, P4, N2, N1, R2, T4, T2, U3, U4, V1, W1, V4, W2, Y2, W4, AA1, AC2, AC3, AF1, AE2, AA6, AC4, AG1, AB6, AF24, AK29, AJ28, AH27, AG26, AE24, AG27, AH28, AJ29, AE26, AK30, AC25, AE27, AJ30, AF28, AC26, AG29, AD27, AH30, AE28, AF29, AC27, AG30, AD28, AA26, AE29, AB27, AF30, AC28, AD29, Y26, AB28, AC29, AD30, W26, Y27, AA28, AB29, AC30, AB30, Y28, V26, W27, AA29, Y29, W28, N26, M28, L29, M27, K30, L28, K29, J30, K28, J29, H30, K27, L26, J28, H29, G30, F30, H28, J27, K26, G29, E30, F29, G28, K25, J26, E29, F28, G27, H26, C30, D29, E28, F27, H25, G26, B30, C29, A25, N4, AF25, AF26, AD26, AH29, AA25, AB26, AE30, AA27, M26, L27, H27, D30, AH3, AE7, AJ2, AF6, AK1, AG5, AH4, AE8, AF7, AJ3, AH6, AH10, AJ9, AK8, AK9, AJ10, AG12, AF13, AH11, AK10, AG16, AK15, AJ15, AH15, AG15, AK14, AJ20, AK21, AH20, AJ21, AK22, AF19, AG20, AH21, AJ22, AK26, B14, C14, D14, A13, E14, B13, C13, A12, C9, D23, A27, C24, E21, B25, D22, A26, C23, B24, A23, A17, D16, C16, B16, A16, C11, F10, E9, D8, A4, B5, C6, D7, F9, E8, E6, E16, A30	NC	-	**No Connect**

2.0 APPLICATIONS AND PHYSICAL INTERFACE GENERAL OVERVIEW

The XRT86SH221 (Voyager-Lite) is a highly integrated, monolithic device designed for cost-sensitive SDH to PDH mapper applications. Voyager-Lite supports all the framing, mapping and grooming functions required for E1 aggregation to STM-1 via standard VC-12 to AU-3 and AU-4/TUG-3 mapping protocols. The device generates and terminates all SDH Regenerator Section, Multiplexer Section and Path Overhead including the low-order Virtual Container (VC) Path Overhead. E1 framing is transparent; therefore, the device neither generates nor terminates the E1 frame.

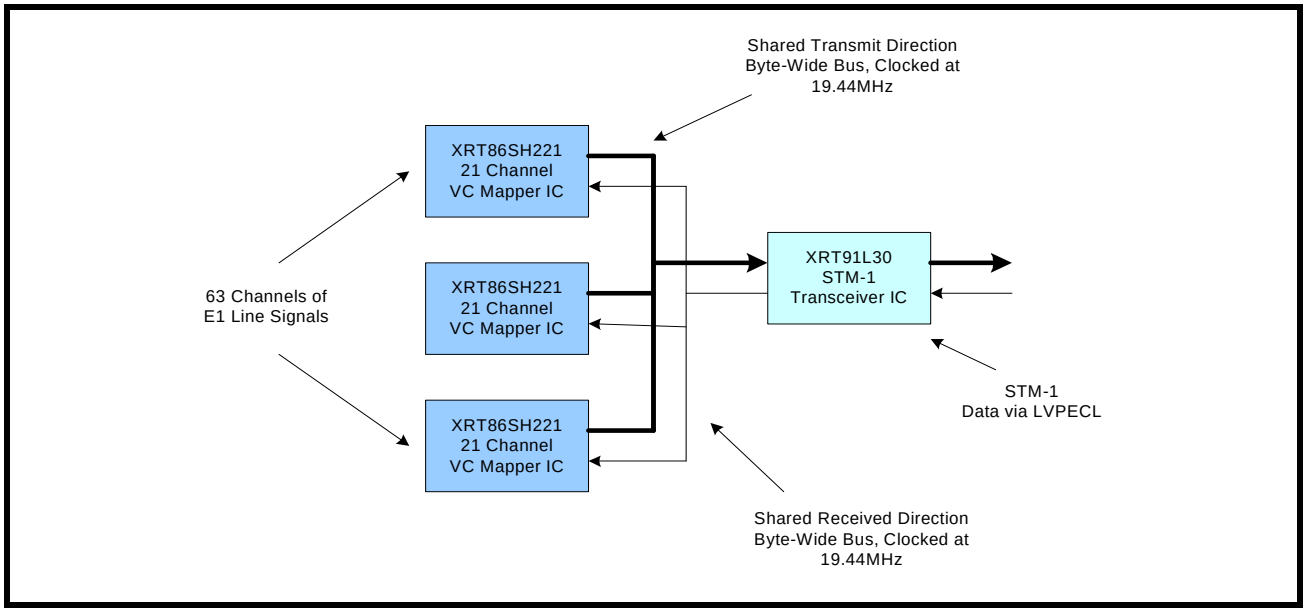
Voyager-Lite includes a standard Telecom Bus interface to an SDH (STM-0/STM-1) Framer /Mapper with SDH-to-PDH Desynchronizer, VC-12/TU-12 Mapper, VC-12 Cross-Connect and a 21-channel E1 Short Haul LIU with integrated egress frame synchronizer for E1 bit-retiming. Voyager-Lite also provides alarm and performance monitoring for all STM-1 and VC-12 overhead in compliance with ITU-T G.783 standards. Section and Path overhead may be inserted/extracted via serial interfaces provided in transmit and receive directions.

The 21-channel E1 Short Haul LIU provides line termination and generation in compliance with G.703 standards, supporting E1 (2.048Mbps) 75Ω and 120Ω applications. The LIU receiver includes adaptive equalizer, clock and data recovery, and HDB3 decoding with performance monitoring of Loss of Signal, Line Code Violations and Excessive Zeros. The LIU transmitter includes HDB3 encoder, transmit pulse shaping and line driver. The LIU also provides a half-duplex jitter attenuator which may be applied in either the transmit or receive data path.

E1 spans are mapped to VC-12/TU-12 via the Virtual Container (VC) and Tributary Unit (TU) mapper. VC-12 grooming support provided for both transmit and receive directions on a per E1 basis via the integrated, full-duplex 21x21 VC-12 Cross-Connect. The SDH framer/mapper supports generation and termination of STM-1 Section and Path overhead and also performs SDH to PDH desynchronization.

A single Voyager-Lite performs mapping of 21 asynchronous E1 spans to either VC-12/TU-12/TUG-2/VC-3/AU-3/STM-0 or VC-12/TU-12/TUG-2/TUG-3/STM-0. VC mapping to STM-1 requires (3) Voyager-Lite devices with one acting as "master" framer and two acting as "slave" framers. In this configuration, Voyager-Lite performs all the necessary framing, pointer processing and mapping functions required for mapping of 63xE1 spans to either VC-12/TU-12/TUG-2/VC-3/AU-3/STM-1 or VC-12/TU-12/TUG-2/TUG-3/VC-4/AU-4/STM-1.

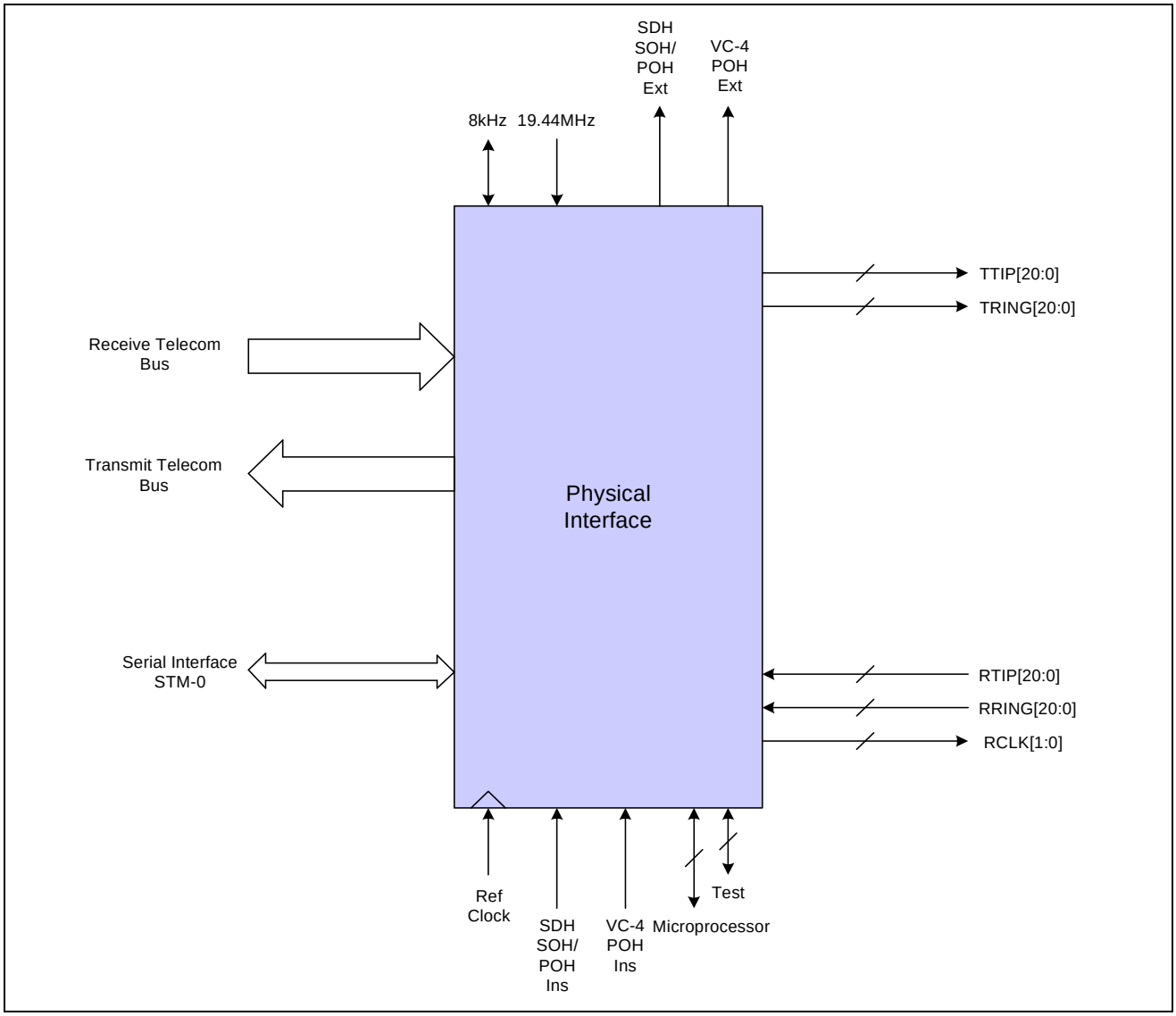
FIGURE 2. APPLICATION DIAGRAM



2.1 Physical Interface

Voyager-Lite consists of several physical interfaces supporting the E1 Line Interface, STM-0/STM-1 Line Interface, SDH SOH/POH and TU-POH Overhead Insertion and Extraction Interfaces, Timing and Synchronization Interfaces, Microprocessor Interface and JTAG/Testability Interfaces. The diagram shown in Figure 3 illustrates organization and applied nomenclature of these interfaces.

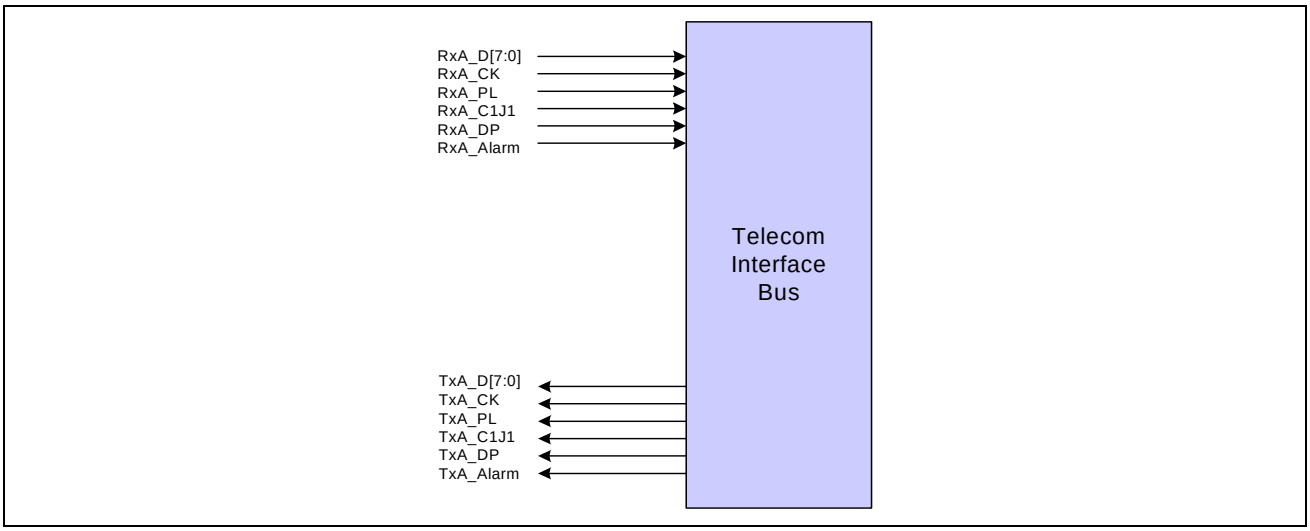
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE PHYSICAL INTERFACE



2.2 Telecom Bus Interface

Voyager-Lite applications typically require transport of STM-1 signals over optical networks. Therefore, Voyager-Lite provides a standard Telecom Bus which supports direct connection to STM-1 optical transceivers such as the XRT91L30, STM-1 Transceiver (CDR+SERDES). The signaling protocol defined for the Voyager-Lite Telecom Bus supports the multiplexing of STM-0 data streams required to create an aggregate STM-1 signal. However, the Telecom Bus also provides direct output of a single STM-0 data stream at 6.48MHz to support STM-0 mapping applications.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE TELECOM BUS INTERFACE



- The Transmit Telecom Bus Interface provides the ingress STM-0/STM-1 data stream output
- The Receive Telecom Bus Interface provides the egress STM-0/STM-1 data stream input

The Telecom Bus interface consists of the following input/output signal.

Transmit Telecom Bus Interface

•TxA_D[7:0] 8-bit parallel telecom data bus
•TxA_CK 19.44/6.48 MHz telecom bus clock
•TxA_PL Payload location indicator
•TxA_C1J1 C1/J1/V1 byte location indicator
•TxA_DP Telecom data bus parity indicator
•TxA_Alarm AU-AIS/TU-AIS alarm indicator

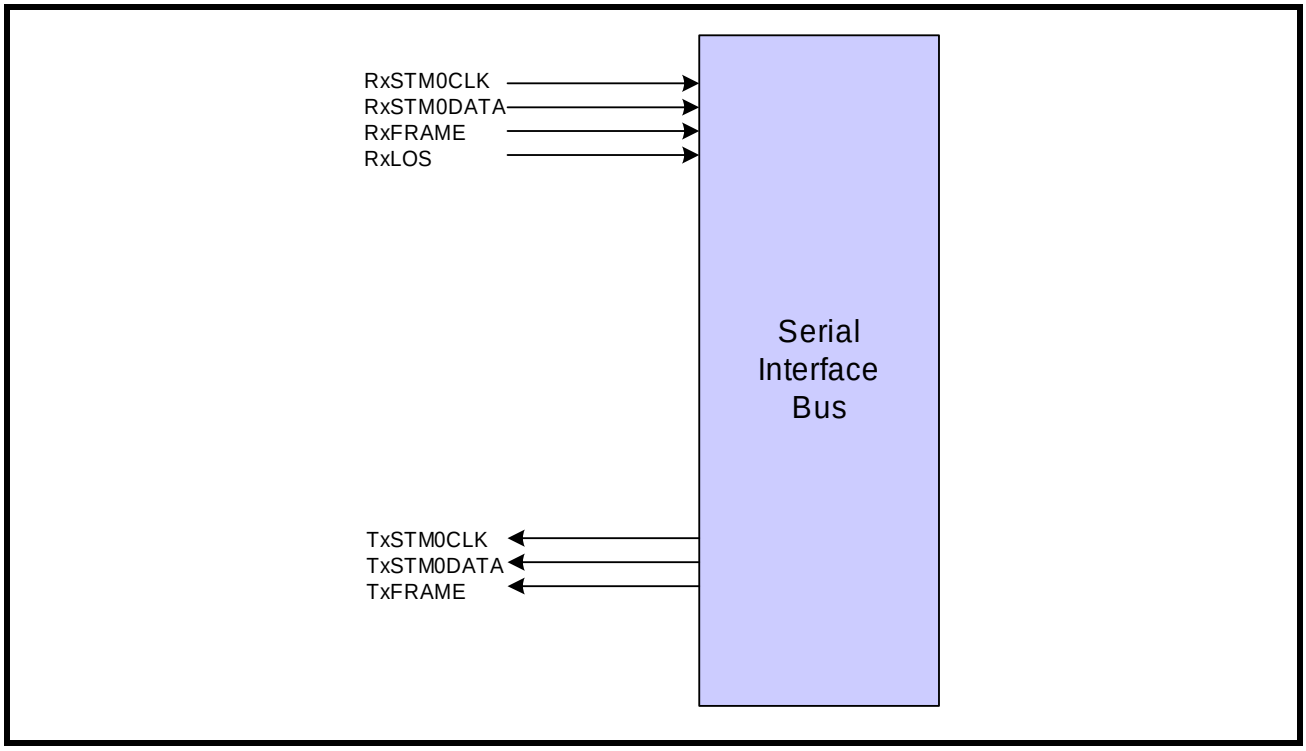
Receive Telecom Bus Interface

•RxA_D[7:0] 8-bit parallel telecom data bus
•RxA_CK 19.44/6.48 MHz telecom bus clock
•RxA_PL Payload location indicator
•RxA_C1J1 C1/J1/V1 byte location indicator
•RxA_DP Telecom data bus parity indicator
•RxA_Alarm AU-AIS/TU-AIS alarm indicator

2.3 STM-0 Serial Interface SDH Frame Synchronization and Timing Interface

In addition to the parallel telecom bus, the high speed interface has the option to transmit and receive data through an STM-0 interface. STM-1 is NOT supported with the serial interface.

FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL PORT INTERFACE



- The Transmit Serial Interface provides the ingress STM-0 data stream output
- The Receive Serial Interface provides the egress STM-0 data stream input

The Serial Interface consists of the following input/output signal.

Transmit Serial Interface

•TxSTM0CLK Transmit serial interface clock
•TxSTM0DATA Transmit serial interface data
•TxSTM0FRAME Transmit serial interface frame pulse

Receive Serial Interface

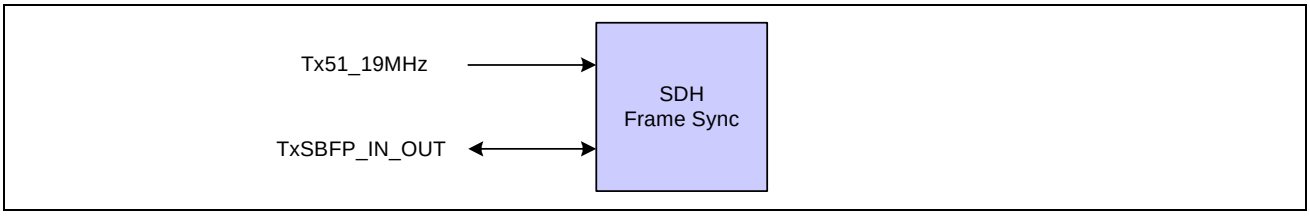
•RxSTM0CLK Receive serial interface clock
•RxSTM0DATA Receive serial interface data
•RxSTM0FRAME Receive serial interface frame pulse
•RxSTM0LOS Receive serial interface loss of signal

2.4 SDH Frame Synchronization and Timing Interface

SDH Section layer processing at the STM-1 level is managed by a combination of overhead processing performed in the "master" framer as well as through synchronization of the SDH framing engines within the "master" and "slave" framers. The "master" device supports insertion and monitoring of B1 BIP-8 overhead and also distributes an 8kHz frame sync to the "slave" devices. The "slave" devices source this frame sync as the reference for all SDH framer/mapper blocks. In particular, the SDH framing, scrambling and descrambling blocks rely upon this frame sync to ensure the "master" and "slave" devices remain synchronized at all times.

The XRT86SH221 requires a 19.44MHz input clock reference for timing of the Telecom Bus, SDH Framers, SDH Overhead processors, VC-12 Mapper and VC-12 Cross-Connects for STM-1 applications. The same 19.44MHz reference should be applied to all three Voyager-Lite device when operating in STM-1 mapper mode. In the case of STM-0 applications, the device will accept a 6.48MHz reference input.

FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF THE SDH FRAME SYNCHRONIZATION



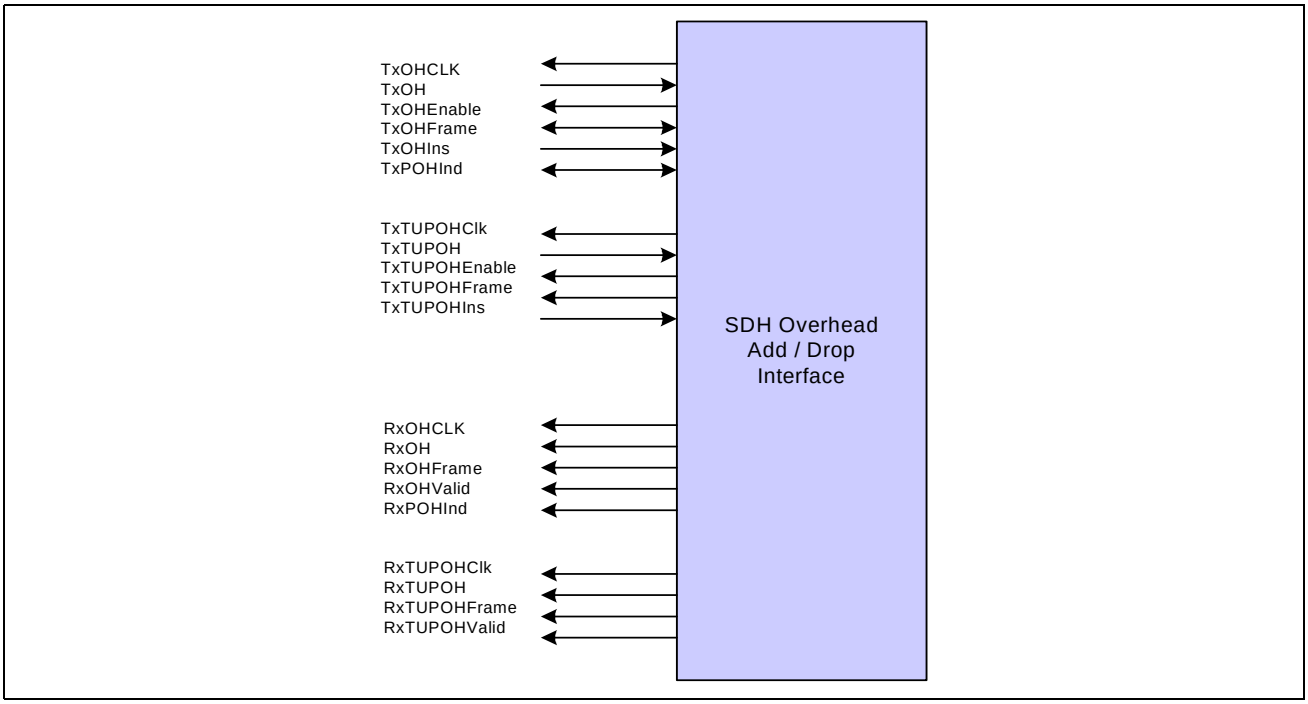
The SDH Frame Synchronization and Timing Interface consists of the following signals.

- Tx51_19MHz Transmit STM-1/STM-0 Timing Reference Input
- TxSBFP_IN_OUT System Frame Pulse (Frame Synchronization Signal)

2.5 SDH Overhead Add-Drop Interfaces

SDH Overhead Add-Drop Interfaces provide access to the SDH Regenerator Section, Multiplexer Section and Path Overhead. Please note there is no external interface providing access to the VC-12 Low-Order Path Overhead. These interfaces allow flexible insertion and extraction of overhead and alarm data, thereby enabling proprietary processing of the SDH frame.

FIGURE 7. SIMPLIFIED BLOCK DIAGRAM OF THE SDH OVERHEAD ADD-DROP INTERFACE



- The Transmit SDH SOH/POH Overhead Interface allows insertion of Regenerator Section, Multiplexer Section and Path overhead data within the transmit STM-1/STM-0 data stream.
- The Transmit TU POH Overhead Interface allows insertion of Low-Order Path overhead data within the transmit TU-12/VC-12 data stream.
- The Receive SDH SOH/POH Overhead Interface allows extraction of Regenerator Section, Multiplexer Section and Path overhead data from within the receive STM-1/STM-0 data stream.
- The Receive TU POH Overhead Interface allows extraction of Low-Order Path overhead data from within the receive TU-12/VC-12 data stream.

The SDH Overhead Insertion/Extraction Interfaces consist of the following signals.

Transmit SDH SOH/POH Insertion Bus (TxOH)

- TxOHCLK Transmit overhead clock
- TxOH Transmit overhead data
- TxOHEnable Transmit overhead bus enable
- TxOHFrame Transmit overhead frame boundary indicator
- TxOHIns Transmit overhead Insertion Control
- TxPOHInd Transmit overhead SOH/POH Indicator

Transmit TU POH Insertion Bus (TxTUPOH)

- TxTUPOHClk TxTUPOH clock
- TxTUPOH TxTUPOH data
- TxTUPOHEnable TxTUPOH bus enable
- TxTUPOHFrame TxTUPOH frame boundary indicator
- TxTUPOHIns TxTUPOH insertion control

Receive SDH SOH/POH Overhead Extraction Bus (RxOH)

- RxOHClk Receive overhead clock
- RxOH Receive overhead data
- RxOHFrame Receive frame boundary indicator
- RxOHValid Receive valid indicator
- RxPOHInd Receive overhead SOH/POH indictor

Receive TU POH Extraction Bus (RxTUPOH)

- RxTUPOHClk RxTUPOH clock
- RxTUPOH RxTUPOH data
- RxTUPOHFrame RxTUPOH frame boundary indicator
- RxTUPOHValid RxTUPOH valid indicator

2.6 E1 Short Haul Line Interface

Voyager-Lite's E1 Short Haul LIU provides the physical interface for 75Ω Coax and 120Ω Twisted Pair applications. With selectable 75Ω/120Ω internal termination and option for high impedance on both transmit and receive LIU interfaces, the device supports 1:1 and 1+1 redundancy with hitless hot-swapping for Coax and Twisted pair designs with a single Bill-of-Materials. The E1 transmit driver and receive equalizer are designed specifically to meet G.703 E1 Short Haul transport requirements.

The E1 Short Haul Line Interfaces consist of the following signals.

Transmit Line Output Signals

- TTIP[0:20] E1 Transmit TIP data
- TRING[0:20] E1 Transmit RING data

Receive Line Input Signals

- RTIP[0:20] E1 Receive TIP data
- RRING[0:20] E1 Receive RING data

Note: TTIP/TRING and RTIP/RING pins are grouped in pairs such as TTIP0/TRING0.

2.7 E1 Timing Interface

Timing support within the 21-channel LIU includes sourcing of an external reference input clock and recovery of the incoming receive E1 Line clock. This reference clock input frequency should be either 2.048MHz, 4.096MHz, 8.192MHz, or 16.386Mhz. The E1 LIU includes a Master Clock Synthesizer which accepts this input clock reference and derives a 2.048MHz reference functions such as Clock and Data Recovery as well as timing of the E1 transmit output data stream. The Clock and Data Recovery circuit recovers the incoming receive E1 Line clocks, which can be multiplexed to one of the two dedicated output pins, RCLK_REC[1:0]. Either the E1 LIU reference clock input or the recovered receive E1 Line clock may be used as the timing source for the transmit E1 data stream bit-retiming function.

The E1 Timing Interface consists of the following signals.

- MCLK 2.048/4.096/8.192/16.384MHz reference clock input
- RCLK_REC[1:0] Recovered E1 (Receive) line clock outputs

2.8 Microprocessor Interface

Voyager-Lite provides a standard microprocessor interface supporting Intel, Motorola, PowerPC and Mips synchronous/asynchronous PIO bus interfaces. The microprocessor interface provides an 18-bit address and 8-bit data bus interface for configuration, control, status monitoring with up to 66 MHz read/write access. The device allows a noon-multiplexed address and data bus, supports reset-upon-read/write-clear for control of status registers and provides programmable interrupt signal.

The Microprocessor Interface consists of the following signals.

- A[0:17] 18-bit Address Bus
- D[7:0] 8-bit Data Bus
- ALE/AS Address Latch Enable/Address Strobe
- CS Chip Select
- INT Interrupt
- RD/DS/WE Read Strobe/Data Strobe/Write Enable
- RDY'/DTACK/RDY/TA Ready, DTACK, or Transfer Acknowledge
- RESET Hardware Reset Input
- mPCLK Microprocessor Interface Clock Input
- WR'/RW Write Strobe/Read-Write Operation Identifier
- PTYPE[2:0] Microprocessor Interface Type Selector
- DBEN/OE Bi-Directional Data Bus Enable

3.0 FUNCTIONAL DESCRIPTION

The XRT86SH221 includes the following functional blocks

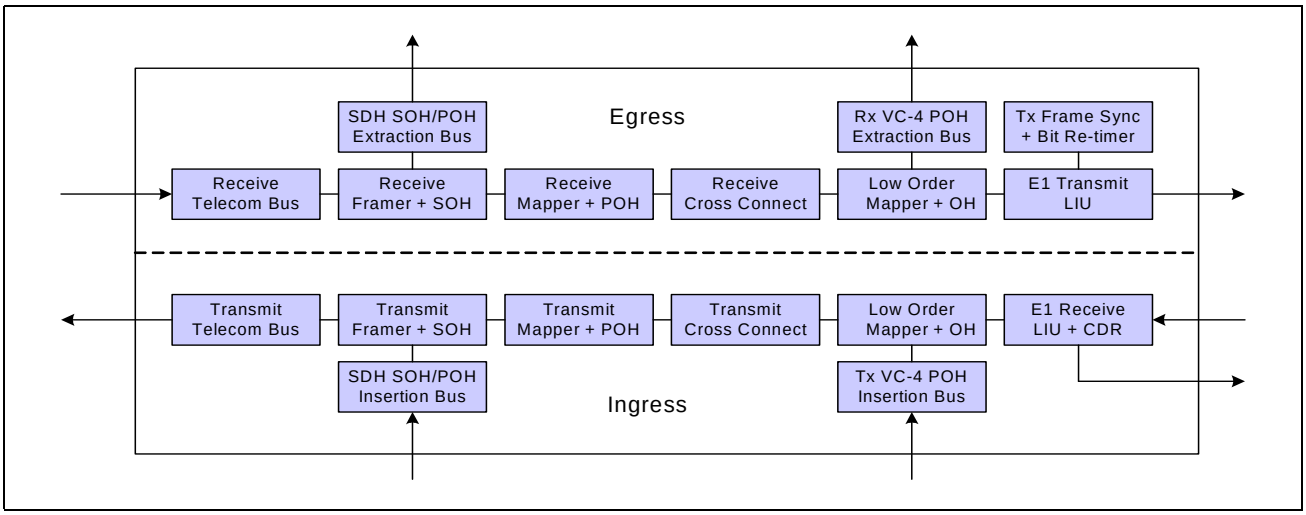
Ingress Data Path Functional Blocks

- E1 Receive LIU plus Clock and Data Recovery (RxE1LIU)
- Transmit TU POH Insertion Bus (TxTUPOH)
- VC-12/TU-12 Transmit Low-Order Mapper and Overhead Processor (TxLOPOHProc)
- VC-12 Transmit Cross-Connect (TxVC12XC)
- Transmit SDH SOH/POH Insertion Bus (TxTPOH)
- SDH Transmit Mapper and Path Overhead Processor (TxPOHProc)
- SDH Transmit Framer and Section Overhead Processor (TxSOHProc)
- Transmit Telecom Bus (TxTBus)

Egress Data Path Functional Blocks

- Receive Telecom Bus (RxTBus)
- SDH Receive Framer and Section Overhead Processor (RxSOHProc)
- SDH Receive Mapper and Path Overhead Processor (RxPOHProc)
- SDH Receive SOH/POH Overhead Extraction Bus (RxTPOH)
- VC-12/TU-12 Receive Low-Order Overhead Processor (RxLOPOHProc)
- Receive TU POH Extraction Bus (RXTUPOH)
- VC-12 Receive Cross-Connect (RxVC12XC)
- E1 Transmit Frame Synchronizer and Bit-Retimer (TxE1Frm)
- E1 Transmit LIU (TxE1LIU)

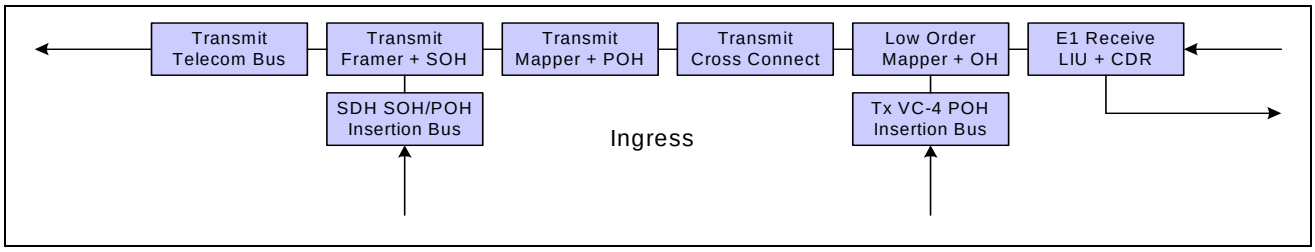
FIGURE 8. FUNCTIONAL BLOCK DIAGRAM



3.1 Ingress Data Path Functional Blocks

The Ingress data path is defined as the flow of data from the E1 LIU Receiver input through the VC Mapper and SDH Framer/Mapper to the Transmit Telecom Bus. The following sections describe the general functions and detailed features for each block within the ingress data path.

FIGURE 9. SIMPLIFIED BLOCK DIAGRAM OF THE INGRESS DATA PATH



3.2 E1 Receive LIU (RxE1LIU)

- Loss of signal (RLOS) according to ITU-T G.775 and ETS300233
- Internal impedance matching on receive for 75Ω or 120Ω
- Power down on a per channel basis
- Selectable crystal-less digital jitter attenuators (JA) with 32-bit or 64-bit FIFO that can be selected in the receive path
- Receive inputs may be set to high impedance for protection or redundancy applications on a per channel basis
- R3 Technology for 1:1 or 1+1 redundancy without relays
- On chip digital clock and data recovery for high input jitter tolerance
- QRSS, TAOS, and Network Loop Codes for receive diagnostics
- Supports remote loop back modes

3.3 Transmit Low-Order (TU) Overhead Insertion Bus (TxTUPOH)

The SDH Transmit Low-Order (TU) Overhead Insertion Bus provides capability to receive the TU-12/VC-12 Low-Order Path Overhead (LOPOH) from an external processor. Data received by the TxTUPOH block may be optionally inserted into the outgoing TU-12/VC-12 overhead during generation of the corresponding overhead byte within the TxLOPOHProc block.

3.4 VC-12/TU-12 Transmit Low-Order Mapper and Overhead Processor (TxLOPOHProc)

The VC-12/TU-12 Transmit Low-Order Overhead Processor performs asynchronous mapping of E1 spans into TU-12/VC-12 payloads. The TxLOPOHProc receives 21 independent E1 data streams from the Receive E1 LIU block and maps these E1 spans to TU-12/VC-12. This block generates all the necessary Low-Order Path Overhead including functions supported within the V5, J2, N2, and K4 bytes.

The primary features of the TxLOPOHProc block include the following functions

- •Maps (21) independent E1 spans into TU-12/VC-12 payloads
- •Generates the TU-12/VC-12 Low-Order Path Overhead
- •Supports Low-Order Path Overhead Generation including V5, J2, N2, and K4
- •V5 overhead generations support includes:
- •BIP-2 Parity
- •Low-Order Path Signal Label
- •Low-Order Path Remote Error Indicator (LO-REI)
- •Low-Order Path Remote Failure Indicator (LO-RFI)
- •Low-Order Path Remote Defect Indicator (LO-RDI)
- •J2 overhead generation supports Low-Order Access Path Identifier (LO-API) Messaging
- •N2 overhead generation supports for Low-Order Tandem Connection Monitoring (LO-TCM)
- •K4 overhead support for Low-Order APS Signaling
- •Generates VC-12 stuff bits, overhead bits, justification opportunity bits, and justification control bits to support rate adaptation between the incoming E1 signals and the SDH transmit timing reference
- •Low-Order Path overhead may be optionally forced to reflect values configured within the software register map or those received by the TxTUPOH Insertion Bus.

3.5 VC-12 Transmit Cross-Connect (TxVC12XC)

The VC-12 Transmit Cross-Connect operates in parallel with the VC-12/TU-12 Transmit Low-Order Path Overhead Processor to support grooming of the ingress VC-12 paths. The TxVC12XC block provides a 21x21 VC-12 cross-connect which performs grooming of the VC-12 signals to support rearrangement, or reordering, of the E1 traffic received from the E1 Line Interface before mapping within the STM-0/STM-1 payload.

3.6 Transmit SDH SOH/POH Insertion Bus (TxOH)

The SDH Transmit SOH/POH Overhead Insertion Bus receives section and path overhead data from an internal processor for the purpose of insertion within the corresponding byte of the outgoing STM-0/STM-1 signal. This block receives the section and path overhead from external pins and provides this data to the TxPOHProc and TxSOHProc.

3.7 SDH Transmit Mapper and Path Overhead Processor (TxPOHProc)

The SDH Transmit Mapper and Path Overhead Processor receives TU-12/VC-12 overhead and payload data stream from the TxLOPOHProc block and maps this data to either VC-3/AU-3 or TUG-3/VC-4/AU-4. The TxPOHProc block performs all the mapping and overhead generation functions required at the High-Order Path layer. The TxPOHProc provides fixed pointer generation with a pointer value of "522" and also supports B3 parity calculation/insertion and High-Order Path alarm generation. Data received by the TxOH block may be optionally inserted into the outgoing path overhead during generation of the corresponding overhead byte within the TxPOHProc block.

The primary features of the TxPOHProc block include the following functions

Payload Pointer Overhead

- Fixed payload pointer (H1, H2, H3) generation with user programmable value (default = "522")
- Supports NDF insertion within H1/H2 pointer
- Performs mapping of TU-12/VC-12 data streams into either VC-3/AU-3 or TUG-3/VC-4/AU-4
- Supports insertion of Alarm Indication Signal - Path (AU-AIS or AIS-P) based on alarm and defects detected within the incoming egress STM-0/STM-1 signal
- Performs B3 parity calculation and Insertion
- C2 Signal Label Insertion
- Remote Defect Indication - Path (RDI-P) alarm insertion
- Remote Error Indication - Path (REI-P) alarm insertion
- Supports H4 Tributary Unit Multiframe Indicator insertion
- F3 User Channel overhead generation
- Supports K3 APS signaling
- Supports N1 High-Order Path Tandem Connection signaling
- Path overhead may be optionally forced to reflect values configured within the software register map or those received by the TxOH Insertion Bus.

3.8 SDH Transmit Framer and Section Overhead Processor (TxSOHProc)

The SDH Transmit Framer and Section Overhead Processor receives the data from the TxPOHProc and completes the multiplexing and overhead generation process to create the STM-0/STM-1 signal output to the Transmit Telecom Bus. The TxSOHProc performs all the overhead processing required for Regenerator and Multiplexer Section. The block includes supports or A1A2 frame generation, B1/B2 parity calculation, Section Trace Messaging, DCC Messaging, and K1/K2 APS support. Data received by the TxOH block may be optionally inserted into the outgoing section overhead during generation of the corresponding overhead byte within the TxSOHProc block.

The primary features of the TxSOHProc block include the following functions compliant

Regeneration Section Overhead

- Frame Generation with the A1/A2 bytes with optional alignment to external 8 kHz frame sync
- Provides optional error mask for A1/A2 frame bit error generation
- Optional support for generation of LOS and SEF condition
- Scrambling
- Insertion of J0 Section Trace Message
- B1 Parity calculation and insertion with optional error mask
- E1 Orderwire and F1 User Channel overhead insertion
- Data communication channels (DCC messaging) insertion within D1-D3 and D4-D12

Multiplexer Section Overhead

- B2 Parity calculation and insertion with optional error mask
- K1/K2 signaling for APS, Alarm Indication and Remote Device Indication
- Alarm Indication Signal - Line (AIS-L) alarm generation
- Remote Defect Indication - Line (RDI-L) alarm generation
- Remote Error Indicator - Line (REI-L) alarm generation
- Alarm generation based on incoming upstream defects and optional software/hardware control
- Data communication channels (DCC messaging) insertion within D4-D12
- S1 processing for Synchronization Status Monitor
- M0/M1 generation for reporting of B2 bit/block error counts to upstream equipment
- E2 Orderwire overhead insertion

3.9 Transmit Telecom Bus (TxTBus)

The Transmit Telecom Bus provides the ingress data path STM-0/STM-1 physical interface for connection to an STM-0/STM-1 transceiver module, downstream processor or backplane connection.

- STM-0 Mode: 8-bit parallel bus operating at 6.48MHz
- STM-1 Mode: 8-bit parallel bus operating at 19.44MHz

The Transmit Telecom Bus provides a physical interface between the optical transceiver module and Voyager-Lite for the ingress data path. This bus operates at 19.44Mbps for STM-1 applications and 6.48Mpbs for STM-0 applications using an 8-bit parallel data bus. The primary function of this block is transmission of data to the optical transceiver, or other upstream processor. Data received from the SDH Transmit Framer and Section Overhead Processor is sent out on the TxTBus. STM-0 timeslots for the aggregate STM-1 signals are previously byte-aligned. Therefore, the TxTBus performs and STM-1 multiplex function in order to create the aggregate STM-1 output signal.

For STM-1 applications, the TxTBus within the "slave" devices will send the STM-0 time slot for the appropriate STM-0. The TxTBus within the 'master" device will send the STM-0 for time slot "0". The result is a time domain multiplexing of STM-0 signals at the TxTBus which creates the aggregate STM-0 signal. The "master" device monitors the TxTBus data during the "slave" device output timeslots for the purpose of B1 parity calculation.

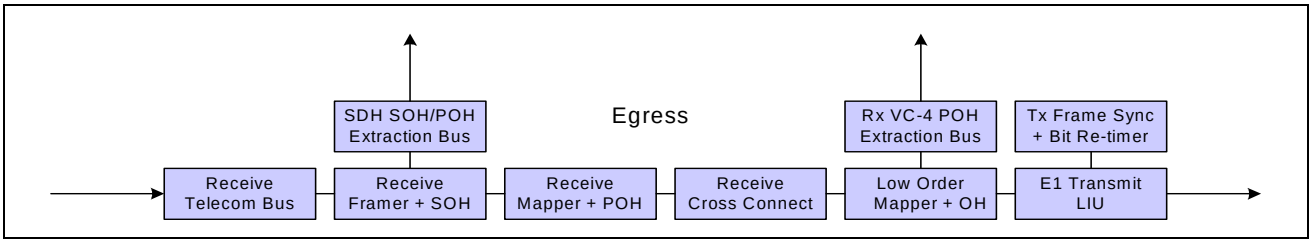
The TxTBus supports the following features:

- Optional configuration for the TxTBus Clock polarity (positive/negative polarity)
- Optional Parity calculation for either the data bus only or the combination of the data bus, PL, C1J1 and Alarm signals.
- Optional configuration of the TxTBus Data Parity polarity (positive/negative polarity
- Optional configuration of the TxTBus C1J1 indicator for frame phase indication, payload phase indication or both

3.10 Egress Data Path Functional Blocks

The Egress data path is defined as the flow of data from the Receive Telecom Bus input through the SDH Framer/Mapper and VC Mapper to the E1 LIU Transmit output as shown below in **Figure 10**. The following sections describe the general function and detailed features for each block within the egress data path.

FIGURE 10. SIMPLIFIED BLOCK DIAGRAM OF THE EGRESS DATA PATH



3.11 Receive Telecom Bus (RxTBus)

The Receive Telecom Bus provides the physical interface between the optical transceiver module and Voyager-Lite for the egress data path. This bus operates at 19.44Mbps for STM-1 applications and 6.48Mpbs for STM-0 applications using an 8-bit parallel data bus. The primary function of this block is reception of data from the optical transceiver, or other upstream processor. Data received by the RxTBus is byte-aligned and passed to the SDH Receive Framer and Section Overhead Processor.

For STM-1 applications, the RxTBus within the "slave" devices will sense only the STM-0 time slot for the appropriate STM-0. The RxTBus within the 'master" device will sense all STM-0 time slots for the aggregate STM-1 signal in order to support the appropriate monitoring of section overhead functions such as B1 parity.

The RxTBus supports the following features:

- Optional configuration for the RxTBus Clock polarity (positive/negative polarity)
- Optional Parity monitoring for either the data bus only or the combination of the data bus, PL, C1J1 and Alarm signals.
- Optional configuration of the RxTBus Data Parity polarity (positive/negative polarity
- Optional configuration of the RxTBus C1J1 indicator for frame phase detection, payload phase detection or both
- Byte-Alignment of incoming STM-0/STM-1 data
- Automatic Insertion of downstream AIS-P based on incoming RxD_Alarm pin status

3.12 SDH Receive Framer and Section Overhead Processor (RxSOHProc)

The SDH Receive Framer and Section Overhead Processor receives the STM-0/STM-1 data stream from the RxTBus and performs all the overhead processing required for Regenerator and Multiplexer Section termination. The RxSOHProc supports performance, defect and alarm monitoring for all section overhead data. The RxSOHProc allows user access to the incoming SOH data through microprocessor accessed registers or via the Receive SDH SOH/POH Overhead Extraction Bus (RxOH).

The primary features of the RxSOHProc block include the following functions

Regeneration Section Overhead (aka - Section Overhead)

- Loss of Signal alarm detection
- Frame-Alignment of A1/A2 bytes
- Severely Errored Frame (SEF), or Out-of-Frame (OOF) alarm detection
- Loss of Frame (LOF) alarm detection
- Descrambling
- Detects J0 Section Trace Message and provides indication of
- J0 Section Trace Message: Mismatch
- J0 Section Trace Message: Invalid
- B1 Parity monitoring with Signal Degrade (SD) and Signal Fail (SF) alarm detection
- Includes programmable thresholds for declaration of SD and SF conditions
- Extracts E1 Orderwire and F1 User Channel overhead
- Extracts data communication channels (DCC messaging) from D1-D3 and D4-D12

Multiplexer Section Overhead (aka - Line Overhead)

- B2 Parity monitoring with Signal Degrade (SD) and Signal Fail (SF) alarm
- Includes programmable thresholds for declaration of SD and SF conditions
- K1/K2 processing for APS, Alarm Indication and Remote Device Indication
- Detects APS failure indicated within the K1/K2 bytes
- Alarm Indication Signal - Line (AIS-L) alarm detection
- Remote Defect Indication - Line (RDI-L) alarm detection
- Extracts data communication channels (DCC) messaging from D4-D12
- S1 processing for Synchronization Status Monitor
- Remote Error Indicator - Line (REI-L) alarm detection
- M0/M1 processing for collection of upstream B2 bit/block error counts
- Extracts E2 Orderwire overhead

Regenerator and Multiplexer Section Error Counters:

- Provides 32-bit saturating counter of OOF/SEF errors
- Provides 32-bit saturating counter of LOF errors
- Provides 32-bit saturating counter of LOS errors
- Provides 32-bit saturating counter of SD errors
- Provides 32-bit saturating counter of SF errors
- Provides 32-bit saturating counter of RDI-L errors
- Provides 32-bit saturating counter of REI-L errors
- Provides 32-bit saturating counter of BIP-8 B1 errors
- Provides 32-bit saturating counter of BIP-8 B2 errors

3.13 SDH Receive Mapper and Path Overhead Processor (RxPOHProc)

The SDH Receive Mapper and Path Overhead Processor receives the Path Overhead and payload data stream from the RxSOHProc and performs all the overhead processing required for High-Order Path termination. The RxSOHProc supports performance, defect and alarm monitoring for all High-Order Path overhead data. This block also performs pointer interpretation and demapping of the STM-0/STM-1 payload. The RxPOHProc terminates the AU-4/VC-3/TUG-3/TUG-2 or AU-3/VC-3/TUG-2 overhead, and passes the TU-12/VC-12 mapped data to the Receive TU-12/VC-12 Low-Order Overhead Processor. The block supports user access to the incoming High-Order POH data through microprocessor accessed registers or via the Receive SDH SOH/ POH Overhead Extraction Bus (RxOH).

The primary features of the RxPOHProc block include the following functions compliant with ITU-T …

Payload Pointer Overhead

- Interprets payload pointer (H1, H2, H3), performs payload extraction and provides monitoring for
- Loss of Pointer (LOP) alarm detection
- New Data Flag (NDF)
- Alarm Indication Signal detection (AU-AISP)
- New Data Flag (NDF)
- Positive and Negative stuff events
- Alarm Indication Signal - Path (AU-AIS or AIS-P) alarm detection

High-Order Path Overhead

- Detects J1 Path Trace Message and provides indication of
- J1 Path Trace Message: Trace Identifier Mismatch - Path (TIM-P)
- J1 Path Trace Message: Invalid
- B3 Parity monitoring
- C2 Signal Label Monitoring within indication of Invalid, Unequipped, and Payload label mismatch status
- Remote Defect Indication - Path (RDI-P) alarm detection
- Remote Error Indication - Path (REI-P) alarm detection
- Supports H4 Tributary Unit Multiframe Indicator
- Extracts F3 User Channel overhead
- Supports K3 APS signaling
- Supports N1 High-Order Path Tandem Connection Signaling

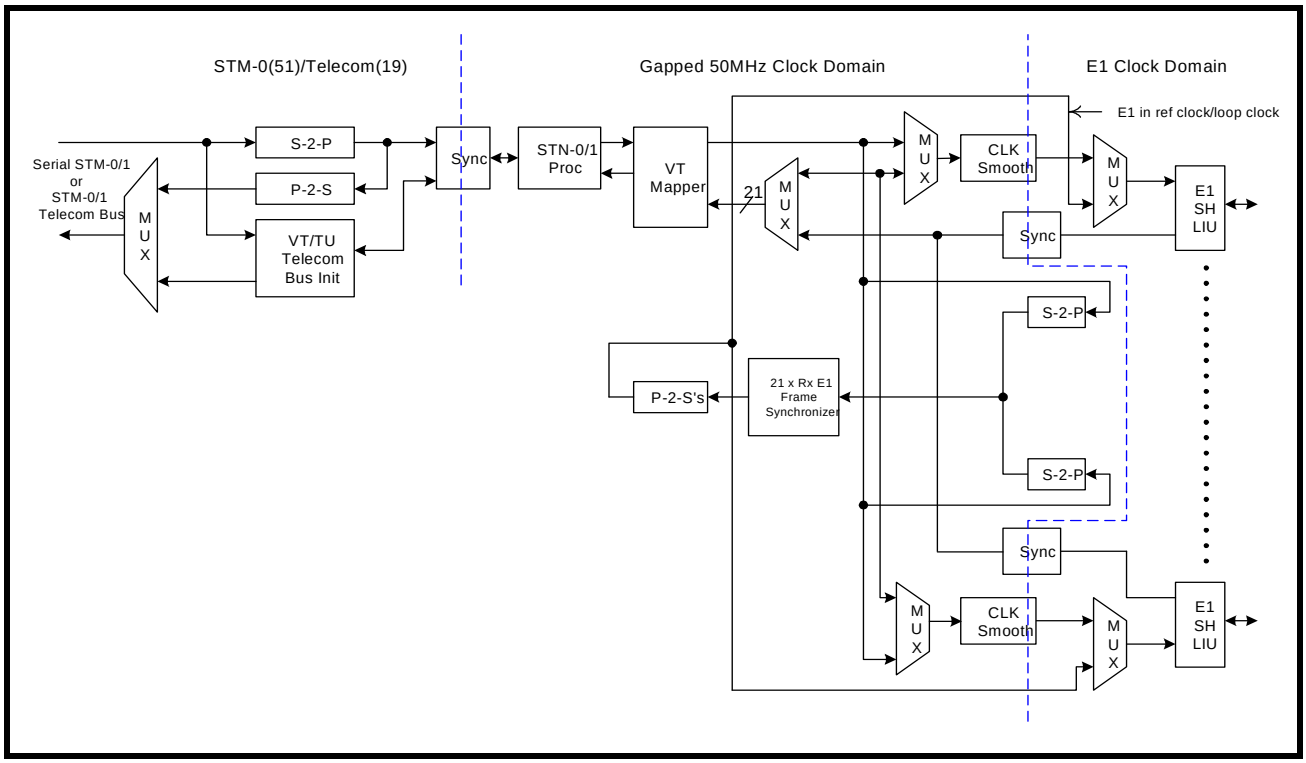
Error Counters include the following:

- Provides 32-bit saturating counter of LOP
- Provides 32-bit saturating counter of AIS-P errors
- Provides 32-bit saturating counter of BIP-8 B3 errors
- Provides 32-bit saturating counter of REI-P errors

4.0 VOYAGER-LITE HARDWARE ARCHITECTURE AND ALGORITHMS

This section intends to provide a description of the overall Voyager-Lite architecture and functions of each module inside the chip. The detailed information about each module will be addressed in the following subsections. **Figure 11** represents a simplified block diagram of this device.

FIGURE 11. VOYAGER-LITE ARCHITECTURE

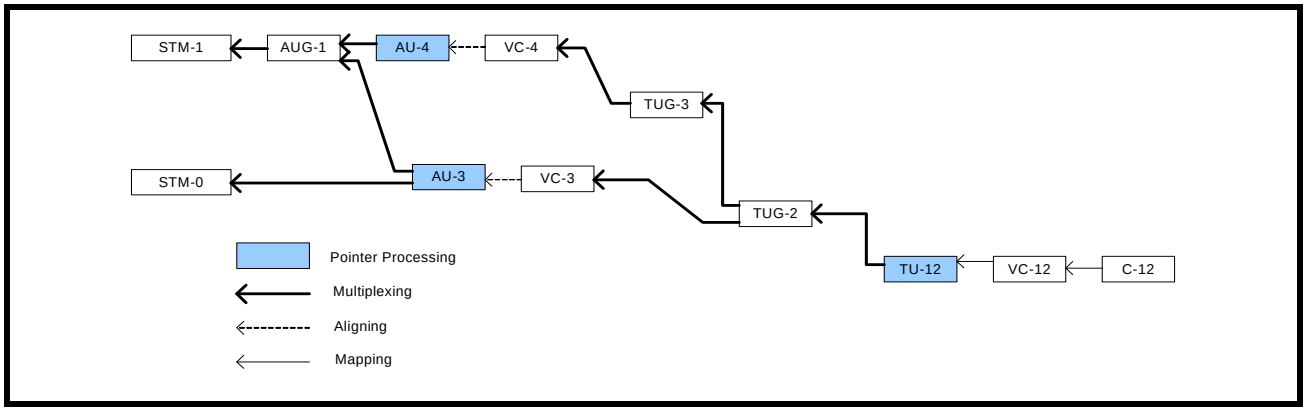


4.1 MULTIPLEXING STRUCTURE

Figure 12 shows the relationship between various multiplexing elements that are defined and illustrates possible multiplexing structures.

VC TYPE	VC BANDWIDTH	VC PAYLOAD
VC-12	2 240 kbit/s	2 176 kbit/s

FIGURE 12. MULTIPLEXING STRUCTURE



4.2 FUNCTIONAL BLOCKS

The Voyager-Lite device is functionally, as well as architecturally, divided into the following blocks and modules:

- Transceiver Interface
- STM-0/1 Transmit Framer (Tx Transport Overhead Processor)
- STM-0/1 Transmit TOH (Transport OverHead) Interface
- STM-0/1 Receive Framer (Rx Transport Overhead Processor)
- STM-0/1 Receive Overhead Interface
- STM-0/1 Transmit Pointer Processor (Tx Path Overhead processor)
- STM-0/1 Transmit POH (Path OverHead) Interface
- STM-0/1 Receive Pointer Processor (Rx Path Overhead Processor)
- STM-0/1 Receive POH (Path Overhead) Interface
- VT Mapper
- 21 Port Cross Connect
- E1 Receive Framing Synchronizer
- LIU Control Interface
- LIU Modules
- Microprocessor Interface
- Interrupt Controller
- Performance Monitor

The operations and functions of these blocks are discussed in detail in the following sections. This section gives an overview of the operation of this device.

4.3 SDH TRANSMIT DATA FLOW

The SDH transmit blocks allow flexible insertion of transport and path overhead bytes through both hardware and software. The blocks also perform primitive SDH tasks such as data scrambling, BIP-8 calculation and insertion, and fixed stuff columns insertion. The blocks are used to transmit an SDH STM-1 stream with any legal concatenation composition. The location of the SPE within the STM-1 frame is fixed with a pointer offset of 522, which results in the J1 byte immediately trailing the last Z0 byte in the transport overhead.

Figure 13 shows the general structure of an SDH transmitter. As in the case of SDH receive blocks, the SDH transmit blocks are reusable blocks that are configured to transmit any compositions of any STM-N stream (3c and 1). The SDH transmit block consists of a transport section (txspoh_proc and txspoh_cont blocks) and 5 path sections.

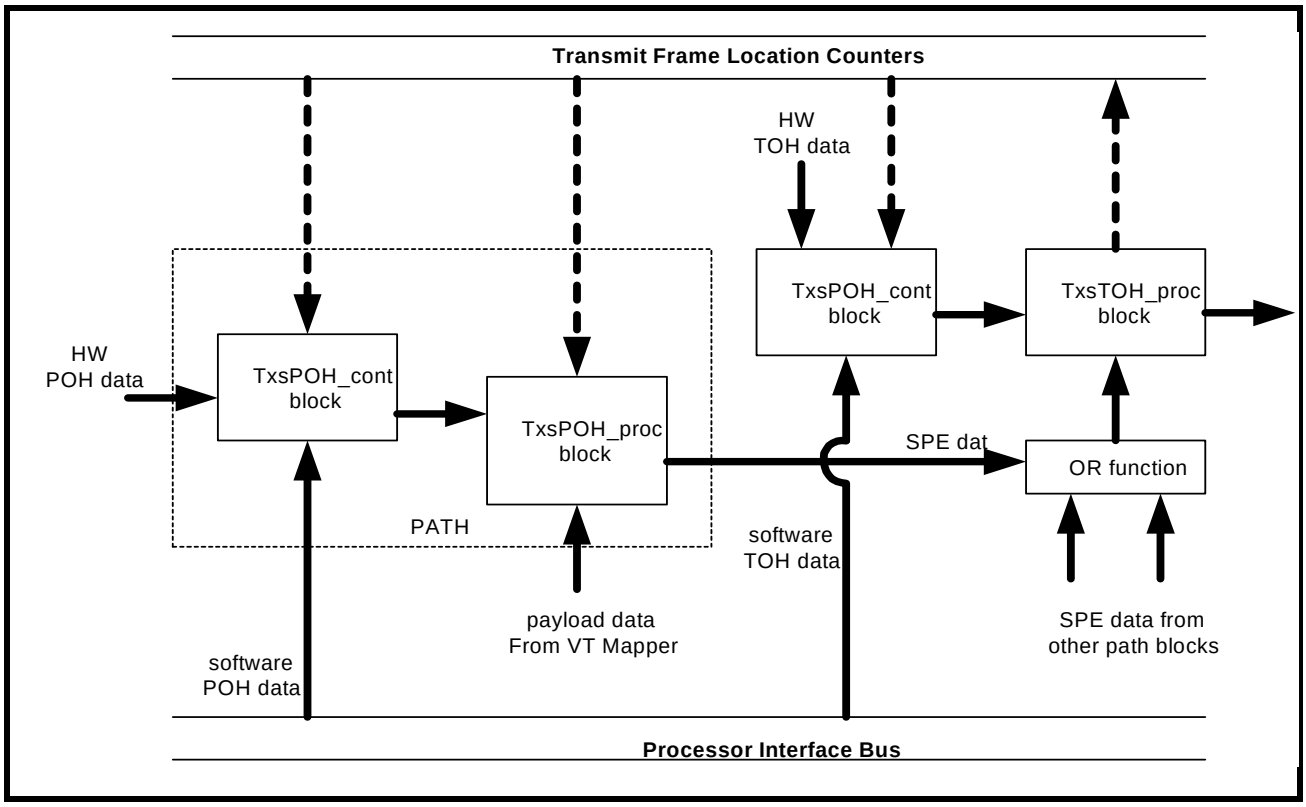
The txspoh_cont path overhead block receives path overhead data from both software and hardware and allows software to select the version that is forwarded to the txspoh_proc path processor block. Software can also specify actions on the SPE data such as AIS-P insertion and RDI-P insertion.

The txspoh_proc block receives payload data from the VT Mapper interface and path overhead data from the txspoh_cont block and performs a multiplexing function using the location information from the txspoh_proc transport processor block. The txspoh_proc block also generates the H1/H2 pointer bytes and provides them on its output data port at the appropriate instances in the transport overhead. Since there can be multiple path blocks for a SDH transmitter, the txspoh_proc block only puts bytes onto its output data ports when the current transmit time slot belongs to its path. Otherwise, zeros are placed on the output data port. The data from all the txspoh_proc blocks are ORed together before being forwarded to the txstoh_proc block.

The txstoh_cont transport control block receives transport overhead data from both software and hardware and allows software to specify the version that is forwarded to the txstoh_proc block. Software also specifies actions such as AIS-L insertion, LOS insertion, and BIP-8 error insertions.

The txstoh_proc block accepts SPE data from the txspoh_proc blocks and transport overhead data from the txstoh_cont block. The txstoh_proc block generates transmit location signals and chooses from the appropriate input data stream for each byte location in the frame. The txstoh_proc also generates time advanced versions of the location signals for the other SDH transmit blocks to facilitate pipelining.

FIGURE 13. SDH TRANSMITTER GENERAL STRUCTURE



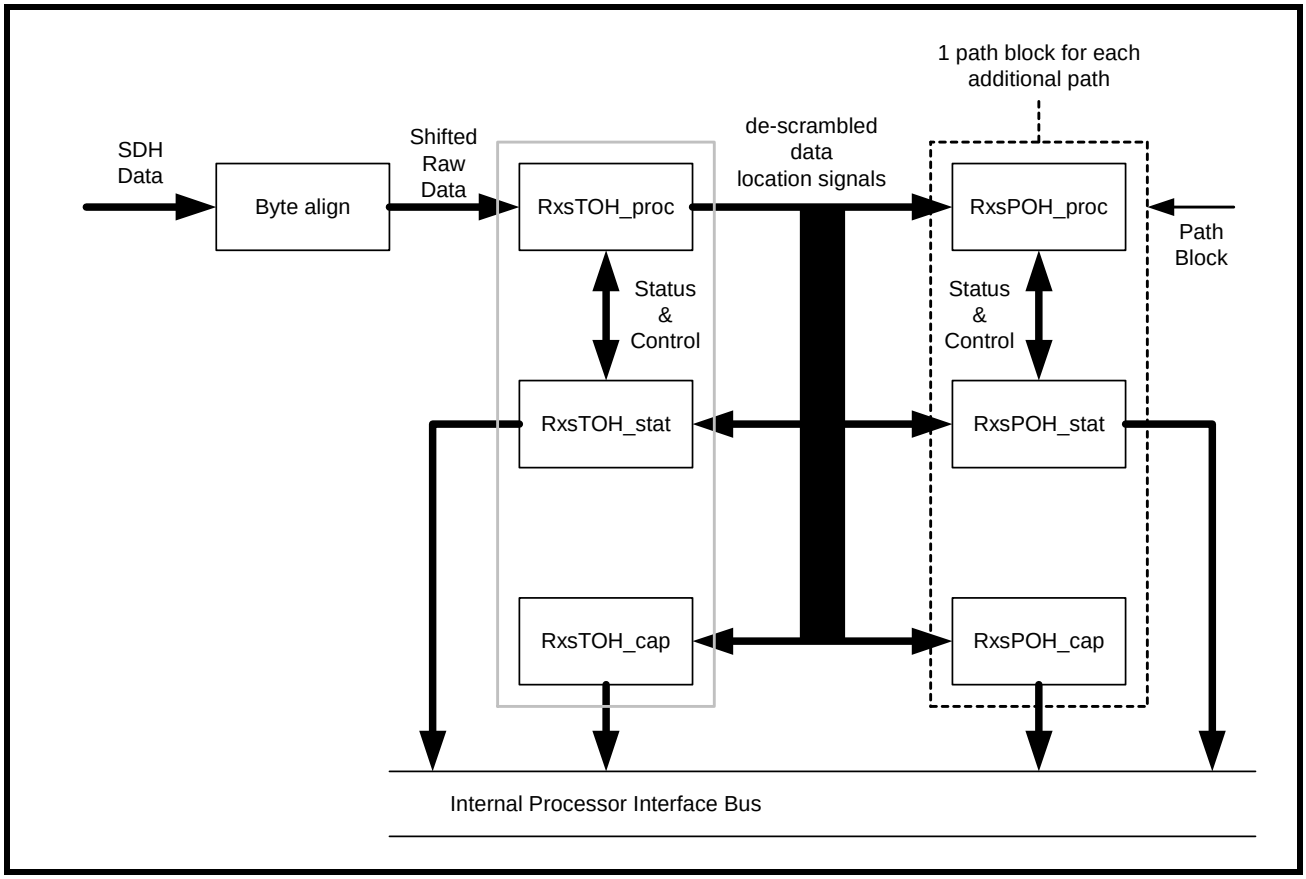
4.4 SDH RECEIVE DATA FLOW

The SDH receive blocks receive SDH STM-1 signals with various concatenation compositions and perform the necessary transport and path overhead processing. Strobe signals are generated for downstream circuitry to extract the payload data.

Figure 14 shows the general composition of an SDH STM-1 receiver. The receiver consists of a transport section and a path section. The receive transport section consists of one rxstoh_proc block which finds frame synchronization, performs error checking, de-scrambles the data, contains one rxstoh_stat block which provides the register file for the SDH receive transport section, maintains some counters and buffers, and contains one rxstoh_cap block which captures all the transport overhead bytes for possible processing by the software. The receive path section consists of 5 path blocks. Each path block consists of one rxspoh_proc block which does pointer processing and error checking, one rxspoh_stat block which provides the register file for the receive path section and maintains some counters and buffers, and one rxspoh_cap block which captures all the path overhead bytes for processing by software. The SDH receive (and transmit) blocks support a 32 bit internal data bus width. The wider data width allows the SDH receiver/transmitter to limit the internal clock speed to a reasonable number for high bandwidth STM-1 streams.

The byte align block is an auxiliary block acting as a simple barrel shifter to align the incoming bytes according to the rxstoh_proc block's requests.

FIGURE 14. GENERAL COMPOSITION OF A SDH STM-N RECEIVER

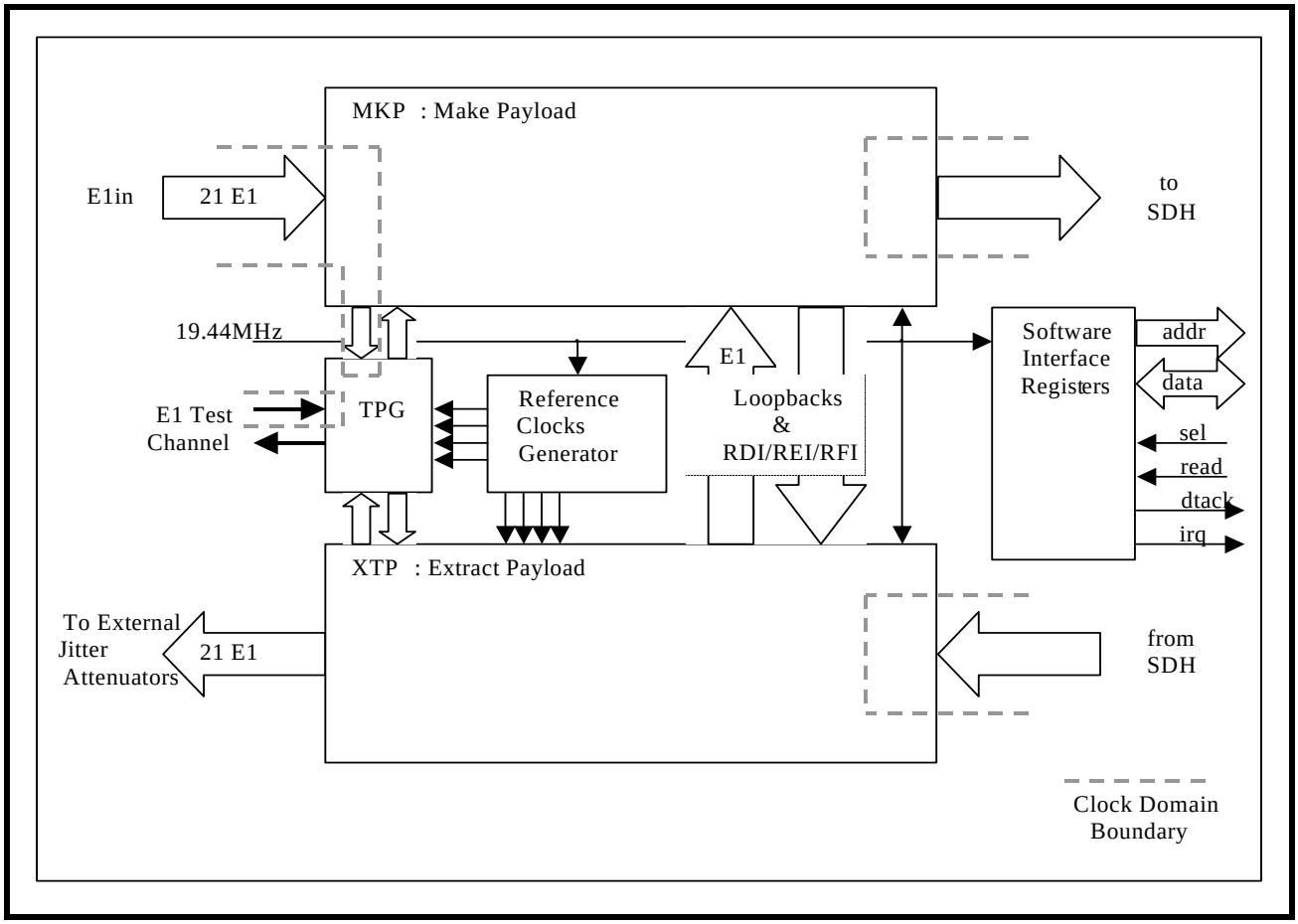


4.5 VT MAPPER

The VTM VT/TU Mapper block is designed to map E1 signals into an SDH VC-3/TUG-3 which in turn can be mapped respectively into an STM-0 or into an STM-1. This reusable block provides all of the functions necessary to insert and drop any valid combination of up to 21 asynchronous E1signals to or from an STM-0 Payload Capacity or an SDH VC-3.

On the STM-0/STM-1 side, the reusable block has an 8-bit data bus. This allows it to interface to the other blocks that will process the higher layers of overhead. On the E1 side, this block has bit serial data inputs and outputs. The VTM contains built-in test pattern insertion and drop capabilities that allow end-to-end testing for initial setup or maintenance without the need for external test equipment. Built-in loopbacks on both sides provide maximum flexibility for use in a number of SDH or E1 products including terminal multiplexers, add/drop multiplexers, or digital cross connects. A high-speed microprocessor interface and full user programmability for VT/TU slot insertion and drop control provide maximum flexibility for E1 configuration.

FIGURE 15. TOP LEVEL BLOCK DIAGRAM



The E1 to SDH section shown in the top part of **Figure 15**, handles the deserialization of the up to 21 incoming signals. It handles the VT Path Overhead (SDH: VC Path Overhead) processing and Fixed Stuff insertion to generate a byte-serial stream on the 8-bit mid bus ready to be processed by the Path, Line and Section Overhead processing blocks to produce an STM-0 or STM-1 signal.

The SDH to E1 section shown in the bottom part of **Figure 15** accepts a byte-serial stream on the mid bus, removes the Fixed Stuff and extracts the virtual tributaries (SDH: Tributary Units) to create up to 21 E1 signals with gapped clocks.

4.6 INTERRUPTS AND STATUS

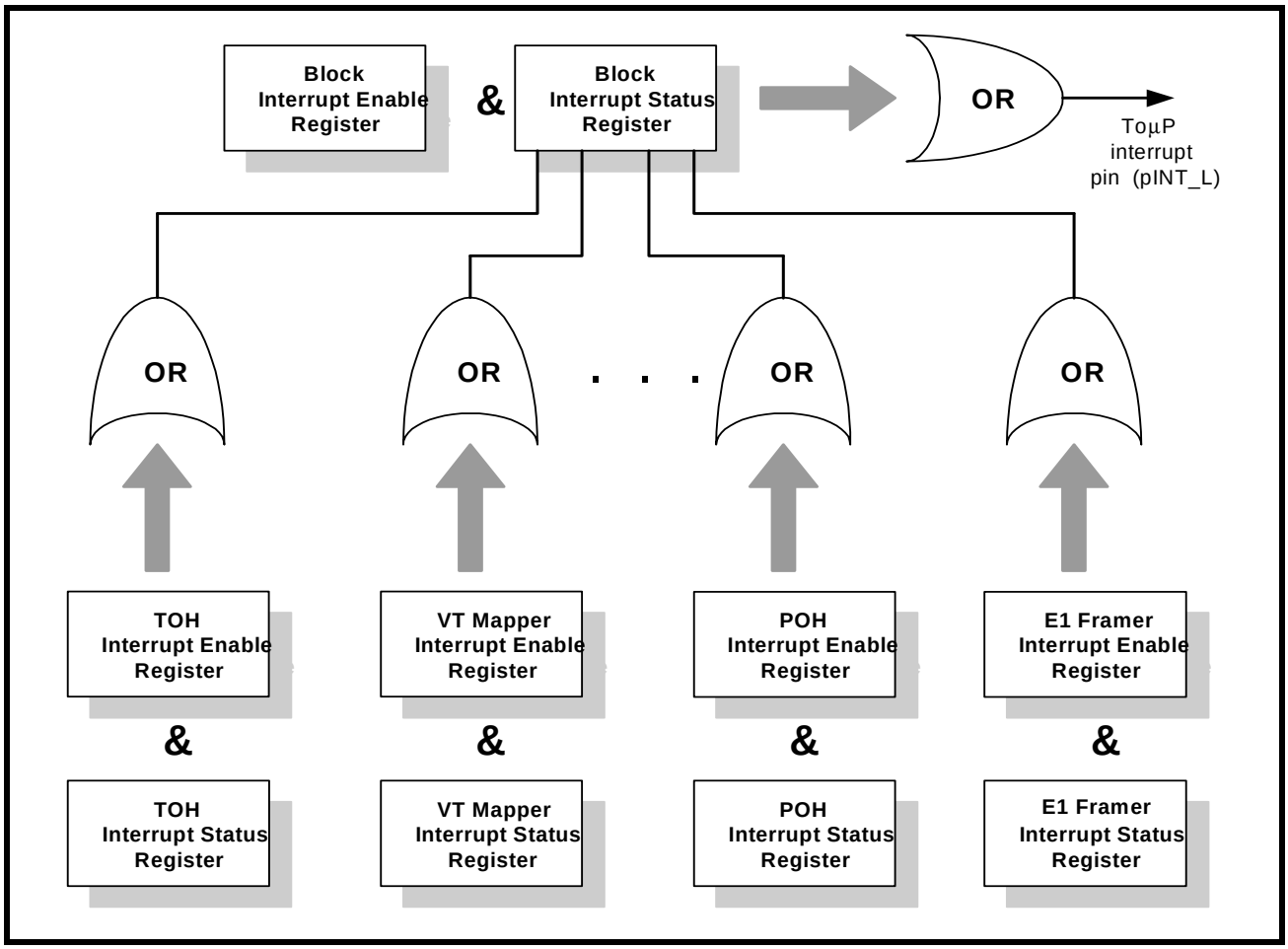
An interrupt pin (INT) is provided for microcontroller interface. This interrupt pin provides interrupts in response to alarm conditions, error events, messages received, error counter overflows, synchronization indication, and parity errors. The interrupt scheme is organized in a Hierarchical Status Reporting architecture to provide a means for a microcontroller to identify the source of interrupt. Status registers record the latest situation of condition events. An interrupt will be generated if the ENABLE bit corresponding to a given status is set in the interrupt enable register.

Each block contains several sources of interrupts. These interrupts are first multiplexed at the block level. Then the interrupts from different blocks are integrated to generate an interrupt signal on the INT pin. The multiplexing of these interrupts is thus at two levels:

1. Source Level.
2. Block Level

At the source level, interrupts may be individually enabled or disabled. All interrupts in a block are multiplexed to produce a block level interrupt. These block level interrupts may then be separately enabled or disabled. Figure 16 is a simplified block diagram of the status reporting hierarchy.

FIGURE 16. INTERRUPT HIERARCHY



4.7 INTERRUPT PROCESSING AND CONTROL

Each time an interrupt occurs, a microprocessor can identify the source of the interrupt by searching through the status hierarchy. The search will cause the status register on the search tree to be read. Reading of the leaf status register will clear the ENABLE bit(s) associated with the interrupting status bit(s) if the ENBCLR bit in Interrupt Control Register is set. This will prevent continuous interrupts to be generated once the microcontroller services the status register. Reading of the leaf status register will also reset the status bit(s) if the Reset Upon Read (RUR) option in the Interrupt Control Register has been enabled. Otherwise, a write is required to clear the bit(s) in the status registers. To clear the bit(s) in the status registers, the microcontroller needs to write a mask (0 to mask and 1 to clear) to this register to identify the bit that it wants to clear.

STATUS POLLING

The SDH framer supports status polling capability for all status registers. The operation is executed by preceding a read of these registers with a write. When a one is written to a bit position, the read register will be updated with the current value and the status bit will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. This scheme allows an external microcontroller to individually poll certain bits without disturbing the other bits in the register.

4.8 STM-0/1 RECEIVE TRANSPORT PROCESSOR

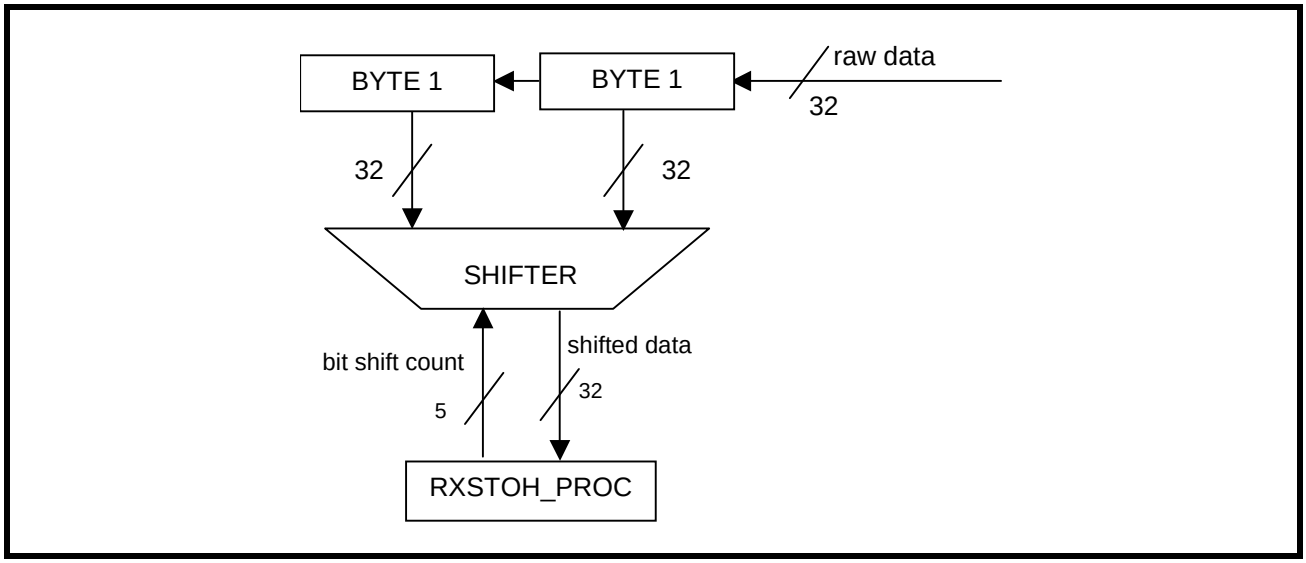
RXSTOH_PROC BLOCK

The rxstoh_proc block has an 8 bit internal interface bus. The rxstoh_proc block performs the following functions: Byte alignment, LOS detection, frame alignment, de-scrambling, BIP processing, and line RDI and AIS detection. The rxstoh_proc block also generates location signals for the rest of the SDH receive blocks.

BYTE_ALIGN BLOCK

The byte_align block acts as a barrel shifter which shifts the parallel SDH input stream according to requests from the framer in the rxstoh_proc block. Figure 17 shows the functional diagram of the byte_align block.

FIGURE 17. BYTE_ALIGN BLOCK FUNCTIONAL DIAGRAM



LOS DETECTION

The rxstoh_proc block monitors the incoming scrambled data for the absence of 1's. The SDH standard has the following two rules for handling LOS defects which are observed by the rxstoh_proc block.

- An SDH NE shall monitor all incoming SDH signals (before de-scrambling) for an "all-zeros pattern," where an all-zeros pattern corresponds to no light pulses for OC-N optical interfaces and no voltage transitions for STM-0 and STM-1 electrical interfaces. A LOS defect shall be detected when an all-zeros pattern on the incoming SDH signal lasts 100µs or longer. If an all-zeros pattern lasts 2.3µs or less, a LOS defect shall not be detected.
- An SDH NE shall terminate a LOS defect when the incoming signal has two consecutive valid framing alignment patterns and during the intervening time (one frame), no all-zeros pattern qualifying as a LOS defect exists.

The rxstoh_proc block allows the software to specify the number of all zero bytes before a LOS defect is declared and clears the LOS defect when the conditions stated are satisfied.

The rxstoh_proc block also monitors the LOPC (loss of optical carrier) input which when asserted, causes the rxstoh_proc block to automatically assert AIS downstream (this feature is programmable by software). This feature is useful when the off-chip optical instrument has detected a loss of carrier but the amplifier data output to the chip still contains random transitions.

FRAME ALIGNMENT

The rxstoh_proc block monitors the incoming stream for A1 and A2 patterns to determine frame alignment. The following SDH standard rules concerning finding frame alignment are observed by the rxstoh_proc block.

- The A1 byte shall be set to '11110110' (Hex F6) and the A2 byte shall be se to '00101000' (Hex 28) in all STM-0s within an STM-N.
- The framing pattern observed by an SDH NE shall include a subset of the A1 and A2 bytes contained in the incoming STM-N electrical or OC-N signal.
- An SEF defect shall be detected when the incoming signal has a minimum of 4 consecutive erred framing patterns. The maximum SEF detection time shall be 625µs for a random signal.
- The framing algorithm used to check the alignment shall be such that an SEF defect is not detected more than an average of once every 6 minutes while the BER of the STM-N electrical or OC-N signal is 10^{-3}.
- Once an SEF defect has been detected, the SDH NE shall terminate the SEF defect upon detecting two successive error-free framing patterns.
- All incoming SDH signals shall be monitored for LOF. A SDH NE shall detect an LOF defect when an SEF defect on the incoming SDH signal persists for 3ms.
- The SDH NE shall terminate an LOF defect 1ms to 3ms after terminating the SEF defect on the incoming SDH signal, if the SEF defect is not (re)detected before the LOF defect is terminated.

The rxstoh_proc block implements the optional 3ms integration timer to deal with SEF and LOF defects. The integration timer consists of an SEF timer and an in-frame timer that operates as follows:

The in-frame timer is activated (accumulates) when an SEF defect is absent. It stops accumulating and is reset to zero when an SEF defect is detected. The SEF timer is activated (accumulates) when an SEF is present. It stops accumulating when the SEF defect is terminated. It is reset to zero when the SEF defect is absent continuously for 3ms (i.e., the in-frame timer reaches 3ms). An LOF defect is detected when the accumulated SEF timer reaches the 3ms threshold. Once detected, the LOF defect is terminated when the in-frame timer reaches 3ms (24 frames).

When SEF is low (i.e., the framer currently has frame alignment), the rxstoh_proc block allows the software to specify the number of correct A1 fields that must be followed by the same number of correct A2 fields for the framing pattern to be considered correct. When the rxstoh_proc is searching for frame (i.e., the SEF defect has been declared), all bits of all the A1 and A2 bytes must be correct in order for the A1 or A2 byte to be considered valid.

Once a frame has been located, the rxstoh_proc block outputs the current row, column, and time slot of the de-scrambled data. Note that for the 8-bit version of rxstoh_proc, a time slot is the same as an STS slot where as for the 32-bit version of rxstoh_proc, each time slot contains 4 STS slots (byte lanes). The software can also force the SEF condition which causes the rxstoh_proc to re-find frame.

Alternatively, the SDH framer also monitors a frame pulse input. When the frame pulse input is asserted, the framer automatically assumes the current byte on the input data bus is the first A1 byte.

The software can force the SEF condition in the framer in the rxstoh_proc block by writing a "1" to the appropriate register file bit. This causes the rxstoh_proc block to declare an SEF alarm and re-find frame. The bit is cleared after the rxstoh_proc block has rediscovered frame alignment (after at least 1 frame) and the SEF alarm has been removed.

De-scrambling

The rxstoh_proc de-scrambles all bytes of the incoming stream except for theA1, A2, and J0/Z0 bytes. The following SDH standard rule is observed by rxstoh_proc. De-scrambling can be disabled via software.

SDH interface signals shall be scrambled (i.e., scrambled at the transmitter and de-scrambled at the receiver) using a frame synchronous scrambler of sequence length 127, operating at the line rate. The generating polynomial for the scrambler shall be 1+x6+x7. The scrambler shall be reset to '1111111' on the most-significant bit of the byte following the Z0 byte in the Nth STM-0 (i.e., the byte following the last Z0 byte). That bit and all subsequent bits to be scrambled shall be added, modulo 2, to the output from the x7 position of the scrambler. The scrambler shall run continuously from that bit on throughout the remainder of the STM-N frame.

BIP Processing

The rxstoh_proc block calculates BIP-8 over the pertinent bytes of the incoming stream for comparison with both the B1 and B2 fields of the transport overhead. The B1 and B2 values are calculated according to the following SDH standard rules:

- The B1 byte in a line-side signal shall carry a BIP-8 code, using even parity. The section BIP-8 shall be calculated over all bits of the previous STM-N frame after scrambling and placed in the B1 byte of the current STM-N frame before scrambling.
- The B2 byte shall be provided in all STM-0s within an STM-N to carry a Line BIP-8 code, using even parity. The Line BIP-8 shall be calculated over all bits of the Line Overhead and the envelop capacity of the previous STM-0 frame before scrambling, and placed in the B2 byte of the current STM-0 frame before scrambling.

The rxstoh_proc block outputs an error mask to the rxstoh_stat block after each comparison with B1/B2. Note that only the first B1 byte of an STM-N stream contains the BIP-8 bits. The second through the Nth B1 bytes are all undefined. The number of B2 bytes is equal to the number of STM-0's within the STM-N signal. Two memories are used in the B2 error code calculations. One memory is used to store the running value of the B2 error calculations. This memory is a 12x8/32 dual port RAM with one port for reads and one port for writes. This is necessary because as the hardware is calculating the B2 code for each STM-0, it needs to store the new value into the memory and at the same time fetch the current code for the next STM-0 from memory. The second memory is a single port 12x8/32 RAM used to store the final B2 codes for all the STM-0's. This memory is read at the B2 byte locations for comparisons and written into the A1 byte locations to store the final B2 codes for the previous frame. For the 8 bit version of the rxstoh_proc block, the B2 RAM widths are 8 bits. For the 32 bit version of rxstoh_proc block, the B2 RAM widths are 32 bits.

LINE RDI AND AIS DETECTION

The rxstoh_proc block monitors the 3 least significant bits of the first K2 byte for RDI_L and AIS_L detection. The AIS_L detection algorithm follows the following SDH standard rules:

- LTE shall detect an AIS-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte contain the '111' pattern in 5 consecutive frames
- LTE shall terminate the AIS-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte have any pattern other than '111' in five consecutive frames.

NOTE: The number of consecutive observations is 5. Also, bits 6, 7 and 8 in the SDH standard refer to the least significant 3 bits. The RDI_L detection algorithm follows the following SDH standard rules:

- LTE shall detect an RDI-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte contains the '110' pattern in 5 to 10 consecutive frames
- LTE shall terminate the RDI-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte have any pattern other than '110' in five to 10 consecutive frames.

DOWNSTREAM AIS INSERTION

The rxstoh_proc block will insert path AIS in the downstream data when prompted by the rxstoh_stat block.

RXSTOH_STAT BLOCK

The rxstoh_stat block has an 8 bit internal bus. The rxstoh_stat block contains the status and control registers for the transport overhead blocks. In addition, the rxstoh_stat block monitors the S1, REI-L, and K1/K2 fields of the transport overhead. The rxstoh_stat block also monitors the B1 and B2 error masks and accumulates the bit or word error events.

SYNCHRONIZATION STATUS (S1) MONITOR

The rxstoh_stat block extracts the synchronization status (S1) byte from the line overhead and monitors it for change. The S1 byte is only defined for the first STM-0 in an STM-1 signal. The extraction algorithm is defined by the SDH standard as:

- A change in the S1 synchronization status message shall be detected if at least 8 consecutive samples (these may or may not be consecutive SDH frames) of bits 5-8 (least significant 4 bits) of the S1 byte have the same (new) value. The sampling rate shall be such that the maximum time to detect a change (assuming no transmission errors) is 1 second.
- For S1 messages, if no validated synchronization status message is detected (e.g., due to transmission errors or the receipt of an undefined message) for a period of greater than 10 seconds, the NE shall consider the reference failed.

The rxstoh_stat block monitors the S1 byte for 8 consecutive identical values after which the new value is stored in a register for access by software. The rxstoh_stat block also implements a counter for an unstable S1. This counter is incremented for each byte that differs from the previously received byte. An invalid S1 condition is declared when the S1 counter reaches 32. The S1 counter is cleared to 0 when 8 consecutive identical S1 bytes are received. Upon detection of an invalid S1 condition, the software can then set up a 10s timer to detect for S1 reference failure.

REI-L (M0/M1) MONITOR

The M0/M1 field contains the line remote error indicator (REI-L) count. For an STM-0 stream, the count is contained in the first REI-L byte (M0 byte) whereas for an STM-1 or higher stream, the count is contained in the third REI-L byte (M1 byte). The rxstoh_stat block interprets the REI-L field according to the following SDH standard rules:

- LTE terminating an OC-1 or STM-0 electrical signal shall set bits 5 through 8 of the M0 byte to indicate (to the upstream LTE) the count of the interleaved-bit block errors that it has detected based on the BIP-8 (B2) byte. The error count shall be a binary number from zero (i.e., 0000) to 8 (i.e., 1000). The remaining seven values represented by the four REI-L bits (i.e., 1001 through 1111) shall not be transmitted, and shall be interpreted by receiving LTE as zero errors.
- LTE terminating an OC-N or STM-N electrical signal (N greater than or equal to 3) shall set the M1 byte to indicate (to the upstream LTE) the count of the interleaved-bit block errors that it has detected using the B2 bytes. For values of N below 48, the error count shall be a binary number from zero to 8xN. The remaining possible values [i.e., 255-(8xN)] represented by the eight REI-L bits shall not be transmitted and shall be interpreted by the receiving LTE as zero errors. For N equal to 48, the count shall be truncated at 255.

The rxstoh_stat accumulates the REI-L counts in a 20 bit saturation counter. The count is transferred to a holding register and reset by software request. The rxstoh_stat also flags any non zero REI-L counts. The

software can configure the rxstoh_stat block to accumulate either bit errors or error events. An error event is defined as any non-zero REI-L count.

Since 8000 frames are received each second and the maximum REI-L count of each frame is 255, the software should poll (and clear) the M1 counter at least once every 232/(8000x255) = 2105 seconds.

K1/K2 MONITOR

The rxstoh_stat block filters and captures the first K1 and K2 bytes of the STM-N stream for APS processing by the software. The filtering is done based on the following SDH standard rule:

- A new code on the received K1 and K2 bytes shall replace the current received code if it is received identically in five consecutive frames.

In addition, rxstoh_stat also monitors the K1 byte for inconsistent APS byte error according to the following definition of the SDH standard.

"An inconsistent APS byte occurs when no three (five) consecutive K1 bytes of the last 12 successive frames are identical, starting with the last frame containing a previously consistent byte."

When an inconsistent APS byte occurs, a flag is set to notify the software. When a new K1/K2 code is detected, a flag is set to notify the software.

B1 ERROR MONITOR

The rxstoh_stat block monitors the B1 error mask from the rxstoh_proc block and accumulates the error count in a 16 bit saturation counter. Upon software request, the count is transferred to a holding register and reset. The software specifies whether to accumulate B1 error bits or events where an error event is defined as any non-zero B1 error mask received from the rxstoh_proc block. A flag is set to notify the software whenever a B1 error event occurs.

Since 8000 frames are received each second and the maximum B1 error count of each frame is 8, the counter will saturate after 232/(8000x8) = 67108 seconds

B2/SD/SF ERROR MONITOR

The rxstoh_stat block accumulates the B2 error count using a 32 bit counter in the same manner as the B1 error counter. Since 8000 frames are received each second and the maximum B2 error count of each frame is 384, the software should poll (and clear) the M1 counter at least once every 232/(8000x384) = 1398 seconds.

In addition, the rxstoh_stat block monitors BIP-2 codes for Signal Fail (SF) and Signal Degrade (SD) conditions. The SD/SF monitoring is done using a discretized sliding window protocol in which the sliding window size is de-composed into 8 sub-intervals. SD/SF is declared if the total B2 error count of all the sub-intervals exceeds a given threshold. Similarly, SD/SF is cleared when the total B2 error count is below a given threshold. In addition, the user can specify a burst tolerance threshold for each sub-interval. The B2 error count for each sub-interval is saturated at the burst tolerance threshold. The window size and thresholds for declaring and clearing SD/SF alarms are specified separately. The window size and thresholds for SD and SF are also specified separately. As a result, 4 sliding windows are needed. The sliding window is implemented by the rxstoh_berm block, 4 of which are instantiated by the rxstoh_stat block.

The setting and clearing of the SF and SD signals adhere to the following SDH standard rules and recommendations:

- Loss of Signal, Loss of Frame, AIS-L defects, and a Line BER exceeding 10^{-3} on an incoming OC-N shall be detected as SF conditions on that line.
- The BER threshold for an SF condition may be required to be user-provisionable over the range of 10^{-3} to 10^{-5}
- A BER exceeding the SD threshold on an incoming OC-N shall be detected as an SD condition on that line
- The BER threshold for an SD condition shall be user-provisionable over the range of 10^{-5} to 10^{-9}

The rxstoh_stat block lets software specify the time interval over which to monitor the B2 error counts and the thresholds over/under which to set/clear the SF and SD conditions.

SEF FORCE

Software can force the SEF condition in the frame finder in the rxstoh_proc block by writing a "1" to the appropriate register file bit. This causes the rxstoh_proc block to re-find frame. The bit is cleared after the rxstoh_proc block has rediscovered frame alignment (after at least 1 frame).

SECTION TRACE (J0) MONITOR

The SDH standard has defined the J0 byte as a 1 byte or 16 byte message in the following manner:

This byte is used to transmit repetitively a Section Access Point Identifier so that a section receiver can verify its continued connection to the intended transmitter. Within a national network, or within the domain of a single operator, this Section Access Point Identifier may use either a single byte (containing the code 0-255) or the Access Point Identifier format as defined in clause 3/G.831. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport.

A 16-byte frame is defined for the transmission of Section Access Point Identifiers where these conform to the definition contained in clause 3/G.831. The first byte of the string is a frame start marker and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 T.50 characters (international Reference Version) required for the Section Access Point Identifier. The 16 byte frame description is given in the table below:

TABLE 1: 16-BYTE FRAME FOR TRAIL APID

BYTE #	VALUE (BIT 1, 2, … ,8)							
1	1	C1	C2	C3	C4	C5	C6	C7
2	0	X	X	X	X	X	X	X
3	0	X	X	X	X	X	X	X
:	:				:			
16	0	X	X	X	X	X	X	X

NOTES:

1. *C1 to C7 is the result of the CRC-7 calculation over the previous frame. C1 is the MSB. The description of this CRC-7 calculation is given in Annex B*
2. *0XXXXXXX represents a T.50 character.*

.2

In the case of inter-working of equipment implementing the STM identifier functionality and equipment employing the Regenerator Section Trace function, the latter shall interpret the pattern "0000001" in J0 as "Regenerator Section Trace - unspecified". This unspecified Regenerator Section Trace can also be used if no use of the Regenerator Section Trace is made.

The rxstoh_stat block enables software to specify the length of the J0 section trace message. This length could be 1 or 16 for SDH, and 64 should the SDH standard in the future specify the J0 byte as a section trace byte. The software also specifies whether to look for an LF or a starting "1" bit when the rxstoh_stat block is trying to locate the start of the message. The software also specifies the number (3 or 5) of consecutive consistent section trace messages that must be observed before it is accepted.

An interrupt is generated when a new section trace message is accepted as valid. The valid section trace message is compared with an expected section trace message downloaded to memory by software. A J0 mismatch (J0_MIS) flag is raised if the 2 messages are not identical. The rxstoh_stat block also implements a J0 unstable counter. The J0 unstable counter is incremented for each byte that differs from the previously

received byte. An invalid J0 condition is declared when the J0 unstable counter reaches 8. The J0 unstable counter is cleared to 0 when a valid J0 is accepted.

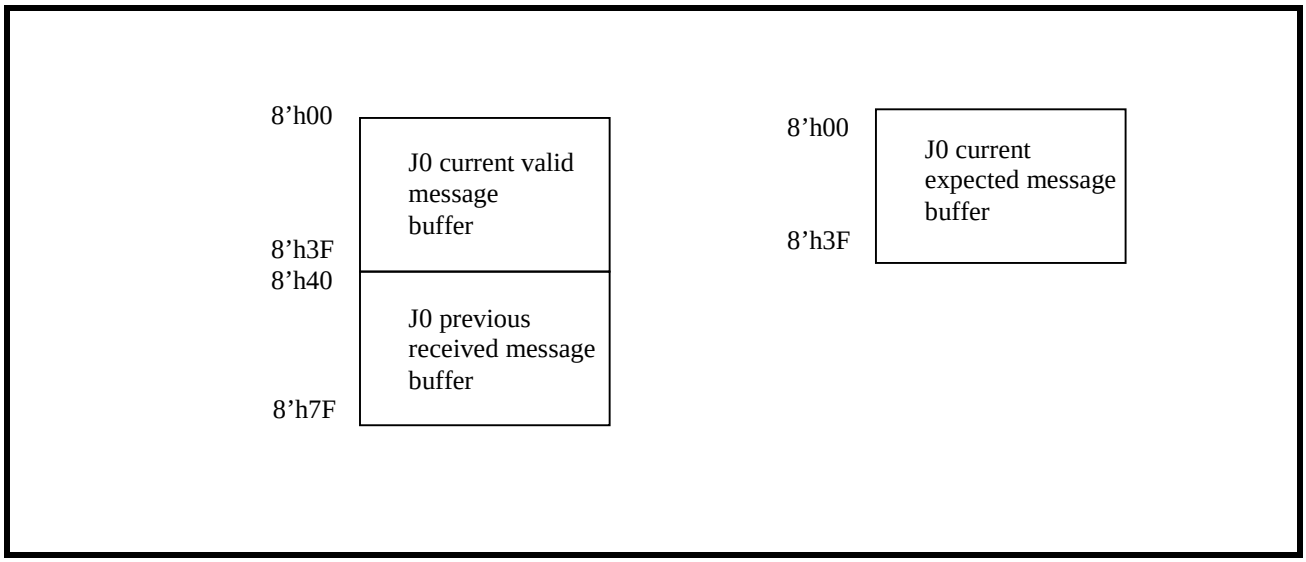
The SDH receive section trace buffer uses a 128x8 single port memory and a 64x8 single port memory. The memories are organised as shown in **Figure 18**. The 128x8 single port ram has 2 segments:

- One segment stores the current accepted trace message
- One segment stores the previous received trace message

The 64x8 single port ram stores the expected trace message which is downloaded by the CPU.

Whenever a new trace message is accepted as valid, the valid message buffer and the previous message buffer swap in the sense that what used to be the valid message buffer segment is now the segment for storing the previous received message and vice versa. The CPU downloads new expected trace messages to the new expected message buffer. Since comparisons between the expected trace message buffer and the accepted trace message buffer are not valid when the CPU is downloading to the expected trace message buffer, the J0 mismatch interrupt should be disabled during downloading of the expected trace message buffer.

FIGURE 18. RECEIVE TRACE BUFFER MEMORY



DOWNSTREAM AIS INSERTION CONTROL

The rxstoh_stat block can be configured to cause downstream AIS insertion when any of the following conditions are detected: AIS-L, LOS, LOF, LOPC, SD, SF, J0 mismatch, and J0 unstable. Downstream AIS insertion to the path section is done according to the following SDH rule:

- LTE shall generate AIS-P downstream for the affected STS paths within 125µs of detecting an AIS-L defect (or a lower layer, traffic-related, near-end defect) or (if the STS pointer is processed) an LOP-P defect on the incoming signal, or the failure of STS PTE supporting provisioned path origination functions. The AIS-P shall be generated as all-ones in the H1, H2 and H3 bytes, and the entire STS SPE.
- LTE shall deactivate the AIS-P within 125µs of terminating the defect that caused it to be sent, or in the case of a local equipment failure, within 125µs of clearing the failure or determining that standby equipment has been switched in. LTE that performs STS pointer processing shall deactivate AIS-P by constructing a correct STS pointer with a set NDF, followed by normal pointer operations, as well as ceasing to insert the all ones pattern in the STS SPE. LTE that does not perform STS pointer processing shall deactivate AIS-P by ceasing the insertion of all ones in the H1, H2 and H3 bytes, and the STS SPE.

The software can enable or disable the insertion of path AIS-P on detection of any of the aforementioned conditions. If path AIS insertion is necessary, then an enable signal to the rxstoh_proc block is activated which causes the rxstoh_proc block to insert all ones in the pertinent bytes.

RXSTOH_CAP BLOCK

The rxstoh_cap block has an 8 bit internal interface bus. The rxstoh_cap block captures the contents of the SDH overhead for up to 3 STM-0 slots and stores them for access by the external processor. On a read access from the processor interface, the bit rxstoh_cap block accepts a 9 bit address of the form: xxxxxyyyy where xxxxx specifies the field number and yyyy specifies the time slot number of the 4 bytes that are requested.

One 944x8 (STM-1) or 256x8 (STM-0) single port RAM is used to capture and hold the SDH OH contents for the processor of each byte-slice module. The memory is divided into one 512 x 8 (only 432 is used) and one 432 x 8 segments. One segment captures the SDH overhead bytes from the current frame while the other segment stores the transport overhead bytes from the previous frame. The two segments are swapped after every frame in the sense that what used to be the current SDH OH byte capture segment is now the holding segment for the previous frame and vice versa.

When the last SDH overhead byte of the current frame has been written into memory, an interrupt is generated to notify the software. The contents of the SDH overhead memory will be preserved for one frame (i.e., until the next SDH OH capture generates an interrupt) for access by the software.

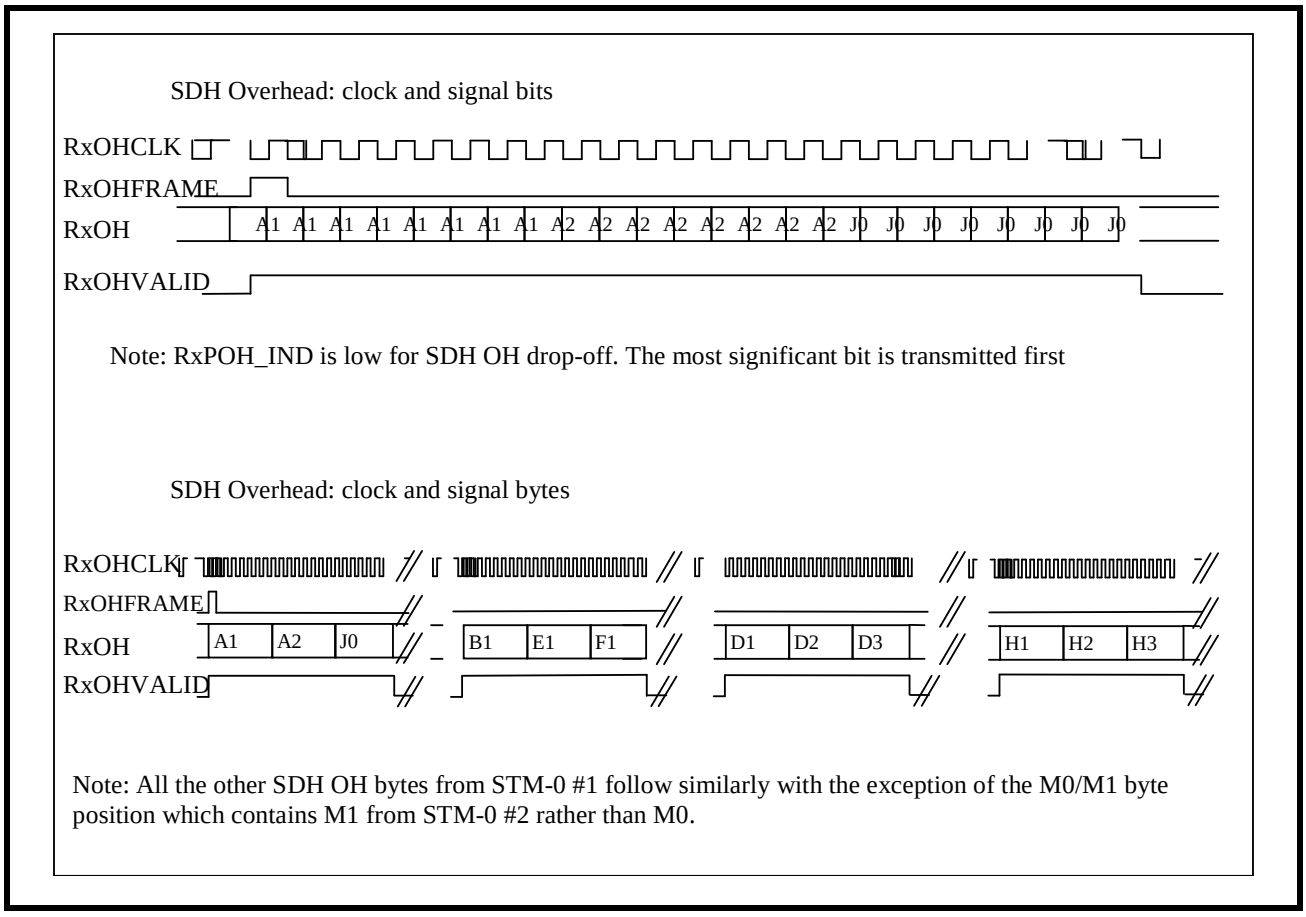
The captured SDH OH bytes are available to the processor via indirect memory registers. The addressing scheme used to access the SDH OH bytes is shown in Table 2. Each access to a captured SDH OH byte consists of writing the corresponding address into the SDH OH capture indirect address register followed by a read/write to/from the SDH OH capture indirect data register.

TABLE 2: ADDRESSING SCHEME USED TO ACCESS THE SDH OH BYTES

ADDR[9:2]	Byte 3 (MSB)	Byte 2	Byte 1	Byte 0 (LSB)
{5'h00, 2'h0}	A1 (STS-0)	A1 (STM-0)	A1 (STS-2)	A1 (STM-1)
{5'h00, 2'h1}	A1 (STS-4)	A1 (STS-5)	A1 (STS-6)	A1 (STS-7)
{5'h00, 2'h2}	A1 (STS-8)	A1 (STS-9)	A1 (STM-00)	A1 (STM-01)
{5'h00, 2'h3}	unused	unused	unused	Unused
{5'h01, 2'h0}	A2 (STS-0)	A2 (STM-0)	A2 (STS-2)	A2 (STM-1)
{5'h01, 2'h1}	A2 (STS-4)	A2 (STS-5)	A2 (STS-6)	A2 (STS-7)
{5'h01, 2'h2}	A2 (STS-8)	A2 (STS-9)	A2 (STM-00)	A2 (STM-01)
{5'h01, 2'h3}	unused	unused	unused	Unused
. . .	. . .	. . .	. . .	. . .
{5'h1A, 2'h0}	E2	byte 26 (STM-0)	Byte 26 (STS-2)	byte 26 (STM-1)
.	.	.	.	.
{5'h1A, 2'h2}	byte 26 (STS-8)	byte 26 (STS-9)	byte 26 (STM-00)	byte 26 (STM-01)
{5'h1A, 2'hC}	unused	unused	unused	unused
. .	. .	. .	. .	..

When this module is used for the STM-0 or STM-1 port, the captured SDH overhead bytes are serialized and sent as outputs from the chip (with the exception of the M0 byte which is replaced by the more useful M1 byte from the third STM-0). The bytes are multiplexed onto a single bit stream as shown in **Figure 19**. The RxOH, RxOHFRAME, and RxOHVALID signals are updated on the falling edge of RxOHCLK. When used on the STM-0/STM-1 side, the bytes captured are sent out to the external interface through an 8-bit bus.

FIGURE 19. RECEIVE TRANSPORT OVERHEAD INTERFACE TIMING



STM-0/1 RECEIVE PATH PROCESSOR

RXSPOH_PROC BLOCK

The pointer processing operation of the rxspoh_proc block is described by the following SDH standard rules:

- The pointer value shall be a binary number with a range of 0 to 782, and shall indicate the offset between the pointer word (the last byte of the H3 field) and the first byte of the STS SPE.
- A pointer increment operation shall be indicated by inverting the I-bits of the pointer word. The positive stuff byte shall appear immediately after the H3 byte in the frame containing the inverted I-bits.
- A pointer decrement operation shall be indicated by inverting the D-bits of the pointer word. The H3 byte shall be used as the negative stuff byte, (i.e., it is used to carry an SPE byte in the frame containing the inverted D-bits).
- The increment/decrement decision should be made at the receiver by a match of 8 or more of the 10 I- and D-bits to either the increment or decrement indication.
- A normal NDF shall be indicated (during normal operation) by a '0110' code in the N-bits. The NDF shall be set by inverting the N-bits to '1001'. The new alignment of the STS PSE shall be indicated by the pointer value accompanying the set NDF and takes effect at the offset indicated.
- The decoding at the pointer processor shall be performed by majority voting (i.e., the NDF shall be detected as being set if three or four of the N-bits match the '1001' code). If a set NDF is detected, then the coincident pointer value shall replace the current value at the offset indicated by the new pointer value.
- The first STM-0 within an STM-Nc shall have a normal pointer word
- All subsequent STM-0s within the STM-Nc shall have their pointer values (i.e., bits 7 through 16) set to all-ones, and their N-bits set to '1001' (i.e., set NDFs).
- A pointer processor in an NE that is transmitting or receiving an STM-Nc SPE shall perform the operations indicated by the pointer in the first STM-0 of the STM-Nc on all N of the STM-0s in that STM-Nc.
- During normal operation, the pointer value locates the start of the STS SPE within the STS Envelop Capacity.
- Any variation from the current pointer value shall be ignored unless a consistent new value is received three times consecutively, or the variation is one of the operations in rules 4, 5, or 6.
- Any consistent new value received three times in succession shall replace the current value at the offset indicated by the new pointer value.
- If the pointer word contains the concatenation indicator, then the operations performed on that STM-0 are identical to those performed on the first STM-0 within the STM-Nc. Rules 4 and 5 do not apply to this pointer word.
- If an increment is detected, then the byte following H3 shall be considered a positive stuff byte, and the current pointer value shall be incremented by one.
- If a decrement is detected, then H3 shall be considered a negative stuff byte, and the current pointer value shall be decrement by one.
- If a set NDF is detected, then the coincident pointer value replaces the current value at the offset indicated by the new pointer value.
- STS PTE and LTE that processes the STS pointer shall monitor for LOP-P. An LOP-P defect shall be detected if a valid pointer is not found in N consecutive frames (where 8 is less than or equal to N less than or equal to 10), or if N consecutive NDFs (other than in a concatenation indicator) are detected. An LOP-P defect shall not be detected when LTE is receiving and relaying an all-ones STS pointer, or when STS PTE is receiving pointers that qualify as those necessary to cause the detection of an AIS-P defect (i.e., three or more consecutive all-ones pointers)
- STS PTE and LTE that processes the STS pointers shall terminate an LOP-P defect when the STS has a valid pointer with a normal NDF, or a valid concatenation indicator, in three consecutive frames.
- STS PTE shall terminate an LOP-P defect when it detects an AIS-P defect.

- STS PTE shall detect an AIS-P defect when the H1 and H2 bytes for an STS path contain an all-ones pattern in three consecutive frames. For an STM-Nc path, only the H1 and H2 bytes of the first STM-0 need to be observed.
- STS PTE shall terminate an AIS-P defect when the H1 and H2 bytes for the STS path contain a valid STS Pointer with a set NDF, or when they contain valid, identical STS Pointers with normal NDFs for three consecutive frames. For an STM-Nc path, the concatenation indicators must also be valid.
- STS PTE should terminate an AIS-P defect when it detects an LOP-P defect.

The rxspoh_proc block chooses N as 8. Note that for a pointer to be considered valid, the following two conditions from the SDH standard need to be satisfied:

"A pointer with an in-range value, the N-bits are set to their normal value."

The SDH standard also provides the following recommendation:

"If a pointer processor detects an increment or decrement operation within three frames after another pointer change operation (e.g. due to transmission errors), it can either ignore that operation or interpret it as a valid operation.

In addition, if the rxspoh_proc is operating in an SDH environment, then the ss bits of the pointer word must be '10'. The above rules can be concisely summarized by the FSM in **Table 3**.

In **Table 3**, the label *n x event_type* denotes an event of event_type occurring in n consecutive pointers. The event types are defined in **Table 3**.

FIGURE 20. POINTER PROCESSING FSM

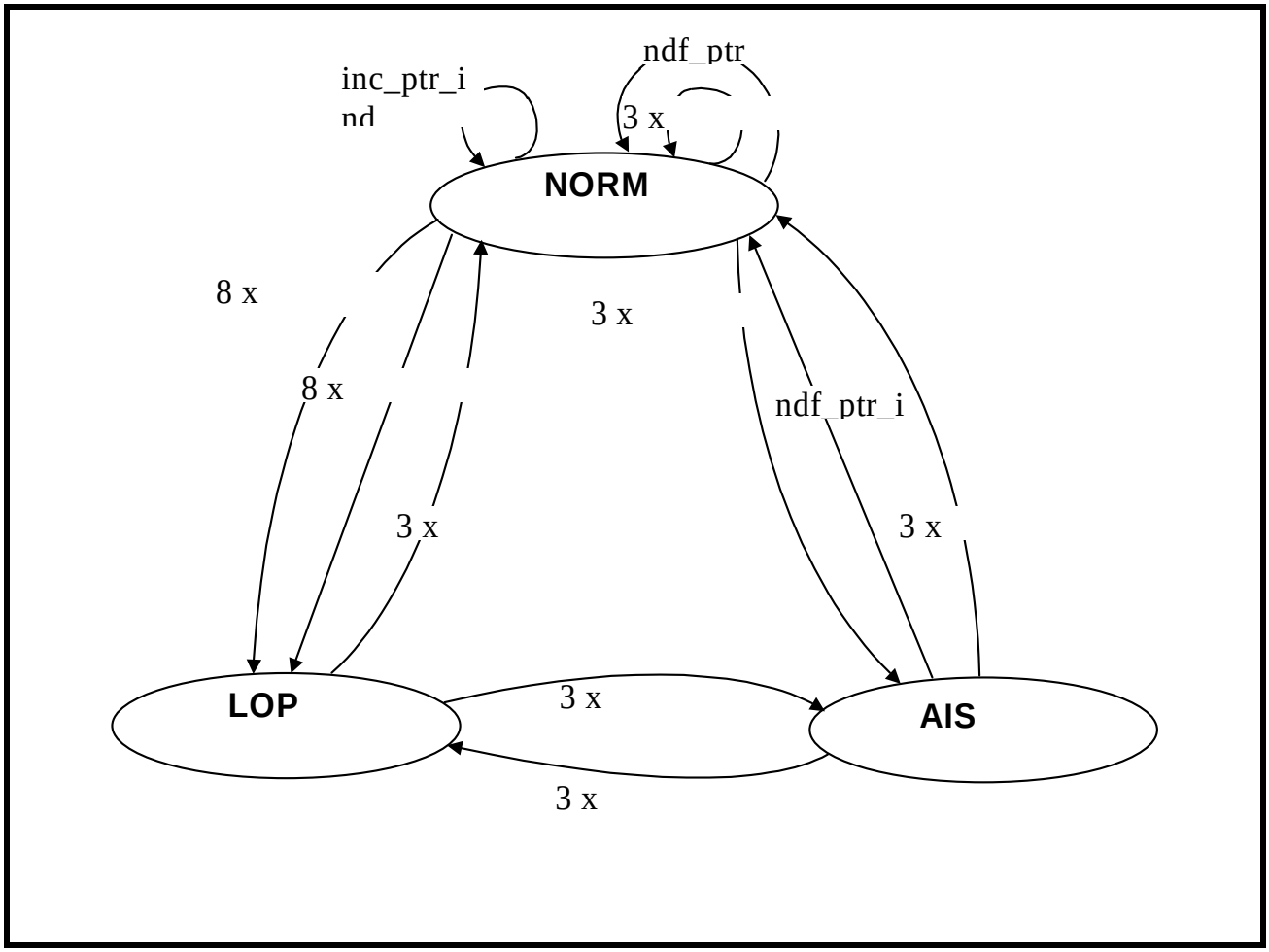


TABLE 3: SDH POINTER EVENT TYPES

EVENT (INDICATION)	DESCRIPTION
norm_ptr_ind	disabled NDF + ss + offset value equal to active offset
ndf_ptr_ind	enabled NDF + ss + offset value in range of 0 to 782.
ais_ptr_ind	H1 = 'hFF', H2 = 'hFF'
inc_ptr_ind	disabled NDF + ss+ majority of I bits inverted + no majority of D bits inverted + previous ndf_ptr_ind, inc_ptr_ind, or dec_ptr_ind more than 3 frames ago
dec_ptr_ind	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous ndf_ptr_ind, inc_ptr_ind, or dec_ptr_ind more than 3 frames ago
inv_ptr_ind	not any of the above
new_ptr_ind	disabled NDF + ss + offset in range of 0 to 782 but no equal to active offset.

B3 PROCESSING

The rxspoh_proc block calculates the path BIP-8 over the pertinent bytes of the incoming stream for comparison with the B3 field of the path overhead. The B3 value is calculated according to the following SDH standard rule:

- The B3 byte shall carry a BIP-8 code, using even parity. The STS Path BIP-8 shall be calculated over all bits (783 bytes for an STM-0 SPE or Nx783 bytes for an STM-Nc SPE, regardless of any pointer adjustments) of the previous STS SPE before scrambling and placed in the B3 byte of the current STS SPE before scrambling.

The rxspoh_proc block outputs an error mask to the rxspoh_stat block after each comparison with B3.

PAYLOAD EXTRACTION

The rxspoh_stat block determines the positions of the payload bytes within each frame and generates the appropriate byte lane enables for the VT Mapper interface.

In an STM signal, the fixed columns are defined as the 3 columns following the POH column . The rxspoh_stat block will detect the arrival of the fixed stuff bytes and will not generate any byte lane enables for the VT Mapper interface during the fixed stuff bytes.

DOWNSTREAM AIS INSERTION

The rxspoh_proc block will insert path AIS in the downstream data when prompted by the rxspoh_stat block.

RXSPOH_CONCAT BLOCK

The rxspoh_concat block has an 8 bit internal bus. The concatenated pointer indicator has the value 1001_1111_1111_1111. The SDH standard gives a recommendation on concatenated pointer processing similar to that of **Figure 21**. In **Figure 21**, the following events are defined:

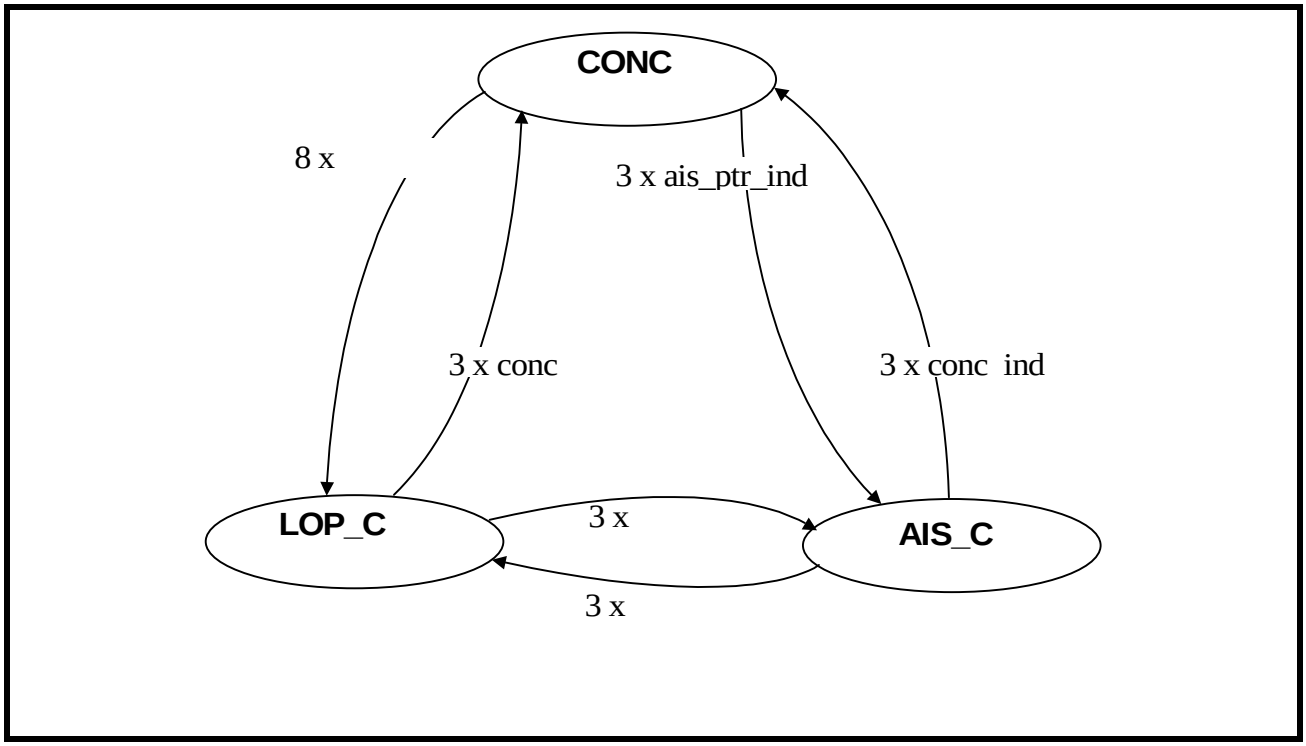
conc_ind: NDF enabled + ss1111111111

ais_ptr_ind: 11111111 11111111

inv_ptr_ind: Any other.

The rxspoh_concat block processes the concatenation pointer indicator for each STS slot according to **Figure 21** and provides the current concatenated pointer indicator FSM state of each slot via registers.

FIGURE 21. CONCATENATED POINTER INDICATOR PROCESSING FSM



RXSPOH_STAT BLOCK

The rxspoh_stat block captures the status signals from the path overhead blocks and stores them in registers. The rxspoh_proc block also accumulates REI-P counts from the G1 field and stores them in a 32 bit counter.

B3 MONITOR

The rxstoh_stat block monitors the B3 error mask from the rxspoh_proc block and accumulates the error count in a 16 bit saturation counter. Upon software request, the count is transferred to a holding register and reset. The software specifies whether to accumulate B3 error bits or B3 error events where an error event is defined as any non-zero B3 error mask received from the rxspoh_proc block. An interrupt is flagged to notify software whenever a B3 error event occurs.

RDI-P MONITOR

There have been two versions of definition for the path RDI defect in the SDH standard. The older version is called single-bit RDI-P (SRDI-P) and uses only bit 5 (4th least significant bit) of the G1 byte. The current version is called the enhanced RDI-P (ERIP-P)and uses bits 5, 6 and 7 of the G1 byte. The ERDI-P is declared when bits 5, 6, and 7 of the G1 byte contain anything other than '011, 000, 001'. The SDH standard has the following standard with respect to receiving the RDI-P signal:

- STS PTE shall generate an appropriate RDI-P signal, as specified in Table 4, within 100ms of detecting a listed defect.
- When STS PTE generates a particular type of RDI-P signal, it shall generate it for at least 10 frames.
- STS PTE that does not support ERDI-P shall detect a one-bit RDI-P defect when a "1" is received in bit 5 of G1 for 10 consecutive frames
- STS PTE that supports ERDI-P shall detect an RDI-P defect when one of the RDI-P defect codes shown in Table 4 (one-bit or enhanced) is received for 5 to 10 consecutive frames
- STS PTE that does not support ERDI-P shall terminate the one-bit RDI-P defect when a "0" is received in bit 5 of G1 for 10 consecutive frames.

- STS PTE that supports ERDI-P shall terminate a particular type of RDI-P defect (one-bit or enhanced) when a code other than the code corresponding to that defect is received for 5 to 10 consecutive frames

TABLE 4: RDI-P SETTINGS AND INTERPRETATION

G1 BITS 5, 6 AND 7	PRIORITY OF ERDI-P CODES	TRIGGER	INTERPRETATION
0xx	not applicable (for SRDI-P only, bits 6 and 7 should be '00')	No defects	No RDI-P defect
1xx	not applicable (for SRDI-P only, bits 6 and 7 should be '00')	AIS-P, LOP-P	one-bit RDI-P defect
001	4	No defects	No RDI-P defect
010	3	PLM-P, LCD-P	ERDI-P Payload Defect
101	2	AIS-P, LOP-P	ERDI-P Server Defect
110	1	UNEQ-P, TIM-P	ERDI-P Connectivity defect

The rxspoh_stat block allows software to specify the type of RDI-P error to monitor. The software also programs the number of consecutive consistent RDI-P codes that must be observed before it is accepted as valid. When a new valid RDI-P is detected, a flag is set for software and the RDI-P code that caused the condition is captured in a register. The rxspoh_stat block also implements a RDI-P unstable counter. The RDI-P unstable counter is incremented for each byte that differs from the previously received byte. An invalid RDI-P condition is declared when the RDI-P unstable counter reaches the software specified threshold. The RDI-P unstable counter is cleared to 0 when a valid RDI-P code is accepted.

REI-P MONITOR

Bits 1 through 4 (most significant 4 bits) of the G1 byte are allocated to convey the path REI (REI-P) function and are defined in the SDH standard as:

- STS PTE shall set bits 1 through 4 of the G1 byte to indicate (to the upstream STS PTE) the count of interleaved-bit block errors that it has detected based on the STS Path BIP-8 byte (B3). The error count shall be a binary number from zero to 8. The remaining seven values shall not be transmitted and shall be interpreted by receiving STS PTE as zero errors.

The rxspoh_stat accumulates the REI-P counts in a 16 bit saturation counter. The count is transferred to a holding register and reset by software request. The rxspoh_stat also flags any non zero REI-L counts. The software can configure the rxstoh_stat block to accumulate either bit errors or error events. An error event is defined as any non-zero REI-P count.

SIGNAL LABEL (C2) MONITOR

The C2 byte is allocated to indicate the contents of the STS SPE and is treated as a signal label. The rxspoh_stat block monitors the C2 byte for several conditions according to the SDH standard.

- STS PTE shall detect an STS Payload Label Mismatch (PLM-P) defect within 250ms of the onset of at least five consecutive samples (which may or may not be consecutive frames) of mismatched STS Signal Labels (C2 byte), as specified in **Table 5**.
- STS PTE should detect a PLM-P defect immediately upon receipt of five contiguous frames with mismatched STS Signal Labels, as specified in **Table 5**.
- STS PTE shall terminate a PLM-P defect within 250ms of detecting the onset of at least five consecutive samples (which may or may not be consecutive frames) of matched STS Signal Labels.
- STS PTE should terminate a PLM-P defect immediately upon receipt of five contiguous frames with matched STS Signal Labels, as specified in **Table 5**.
- STS PTE shall terminate a PLM-P defect upon detecting an UNEQ-P defect.

- STS PTE shall detect an STS Path Unequipped (UNEQ-P) defect within 10ms of the onset of at least 5 consecutive samples (which may or may not be consecutive frames) of unequipped STS Signal Labels (C2 byte = 00hex)
- STS PTE should detect an UNEQ-P defect immediately upon receipt of five contiguous frames with unequipped STS Signal Labels, as specified in Table 5.
- STS PTE shall terminate an UNEQ-P defect within 10ms of the onset of at least five consecutive samples (which may or may not be consecutive frames) of STS Signal Labels that are not unequipped.
- STS PTE should terminate an UNEQ-P defect immediately upon receipt of five contiguous frames with STS Signal Labels that are not unequipped, as specified in Table 5.

TABLE 5: STS SIGNAL LABEL MISMATCH DEFECT CONDITIONS

PROVISIONED STS PTE FUNCTIONALITY	RECEIVED PAYLOAD LABEL (C2 BYTE, IN HEX FORMAT)	DEFECT
Any Equipped functionality (C2 = anything except H00)	Unequipped (00)	UNEQ-P
Any Equipped functionality	Equipped - Non Specific (01)	none (Matched)
Equipped - Non Specific (C2 = H01)	A value corresponding to any Payload Specific functionality	none (Matched)
Any Payload Specific functionality (C2 = anything except H00 or H01)	A value corresponding to the same payload specific functionality as the provisioned functionality	none (Matched)
Any Payload Specific functionality	A value corresponding to a different payload specific functionality as the provisioned functionality	PLM

The rxspoh_stat block allows software to specify the expected signal label and compares it with the observed value. If the values mismatch, then a path label mismatch (PLM) error is declared. If the observed value is 00hex, then a path unequipped (UNEQ) error is declared (and PLM cleared). If the observed value matches the expected value, then PLM is cleared. If the observed value changes, then a flag is set for software. For a C2 label to be considered valid, it must be received in 5 consecutive frames. The rxspoh_stat blocks also implements a C2 unstable counter. The C2 unstable counter is incremented for each byte that differs from the previously received byte. An invalid C2 condition is declared when the C2 unstable counter reaches 5. The C2 unstable counter is cleared to 0 when 5 consecutive identical C2 bytes are received. The rxspoh_stat block implements a mismatch mechanism that can be summarised in Table 6.

TABLE 6: TRUTH TABLE FOR PATH LABEL ERROR CONDITIONS

EXPECTED VALUE	RECEIVED VALUE	ACTION
00	00	match
00	01	mismatch
00	XX	mismatch
01	00	UNEQ-P
01	01	match
01	XX	match
XX	00	UNEQ-P
XX	01	match
XX	XX	match
XX	YY	mismatch

PATH TRACE (J1) MONITOR

The J1 byte of the path overhead is used as a path trace identifier. The path trace identifier is monitored using the following SDH standard rules:

- An SDH NE that contains STS PTE shall allow the user to provision, on a per-path basis, the contents of the STS Path Trace carried in the J1 byte of the STS path overhead originated by the PTE. The transmitted STS Path Trace string shall be 64 bytes in length.
- An SDH NE that contains STS PTE shall support a feature that allows the contents of the STS Path Traces to be provisioned as ASCII characters. In addition, the following apply:
- The feature shall allow the user to enter a string of up to 62 characters
- The feature shall place no restriction on the content of the string except that the characters shall be ASCII printable characters
- The NE shall automatically pad the string entered by the user to 62 characters using ASCII NULL characters, and then add <CR> and <LF> characters (i.e., 'OD' and '0A' for a total of 64 characters
- Each 8 bit ASCII character shall be loaded into one J1 byte.
- An SDH NE shall support a feature to allow the user to provision the expected ASCII-based path trace for each STS path that it terminates and for which TIM-P detection has been activated. In addition, the following apply:

  1. The feature shall allow the user to enter a string of up to 62 characters
  2. The feature shall place no restriction on the contents of the string, except that
  3. The characters shall be ASCII printable characters.

- STS PTE shall detect a TIM-P defect within 30 seconds (or less) when none of the sampled 64-byte STS path trace strings match the provisioned expected value.
- STS PTE shall terminate a TIM-P defect within 30 seconds (or less) when four-fifth (or more) of the sampled STS path trace strings match the provisioned expected value
- An SDH NE that is monitoring for changes of the incoming path trace shall detect when a sustained change in the path trace content occurs. Upon detecting a sustained change, the NE shall send a message to an OS. The level of the message shall be Not Alarmed, and it shall include both the previously received path trace, and the new path trace (assuming they are ASCII-based).
- An SDH NE that is monitoring for a mismatch between the incoming path trace and an expected path trace for diagnostics purposes shall detect when a sustained mismatch occurs. Upon detecting a sustained mismatch, the NE shall set an indication for that path and send a message to an OS. The level of the message shall be Not Alarmed, and it shall include both the expected path trace, and the new path trace (assuming they are ASCII-based).
- An SDH that is monitoring the incoming path trace for diagnostic purposes and that has detected a sustained mismatch shall detect when the incoming path trace matches the expected path trace. Upon detecting a match, the NE shall clear the indication for that path and send a clear message to the OS (if the mismatch was reported to an OS).

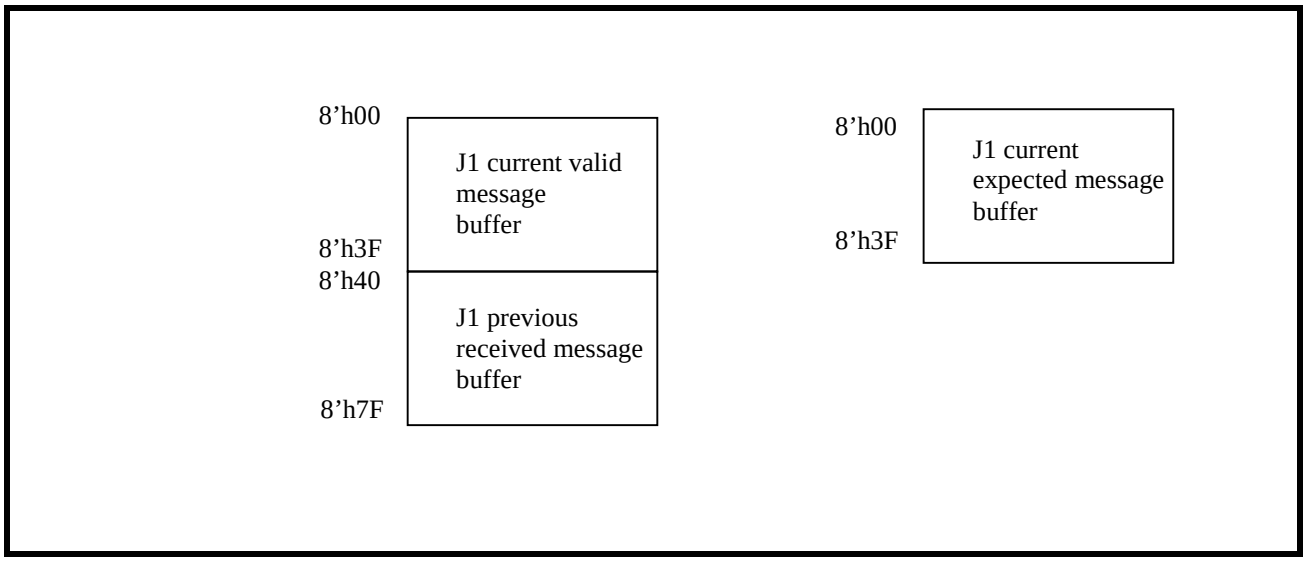
The SDH standard defines the path trace message length to be a 16 byte message. The message format is such that the first byte of the message always has a "1" in its most significant bit while the subsequent bytes in the message all have a "0" in their most significant bits.

The rxspoh_stat block allows software to specify the length of the J1 section trace message. This length could be 1 or 16 for SDH. The software also specifies whether to look for a <LF> or a starting "1" bit when the rxspoh_stat block is trying to locate the start of the message. Software also specifies the number (3 or 5) of consecutive consistent section trace messages that must be observed before it is accepted.

An interrupt is generated when a new section trace message is accepted as valid. The valid section trace message is compared with an expected section trace message downloaded to memory by software. A J1 mismatch (J0_MIS) flag is raised if the 2 messages are not identical. The rxspoh_stat block also implements a J1 unstable counter. The J1 unstable counter is incremented for each byte that differs from the previously

received byte. An invalid J1 condition is declared when the J1 unstable counter reaches 8. The J1 unstable counter is cleared to 0 when a valid J0 is accepted.

The SDH receive path trace buffers use a 128x8 single port memory and a 64x8 single port memory as in the case of the SDH receive section trace buffers.



DOWNSTREAM AIS INSERTION CONTROL

The rxspoh_stat block can be configured to cause downstream AIS insertion to the cell processor when any of the following conditions are detected: AIS-P, LOP-P, TIM-P, J1 unstable, PLM-P, UNEQ-P and C2 unstable. Downstream AIS insertion to the cell processor is done by sending all ones in all the extracted payload bytes.

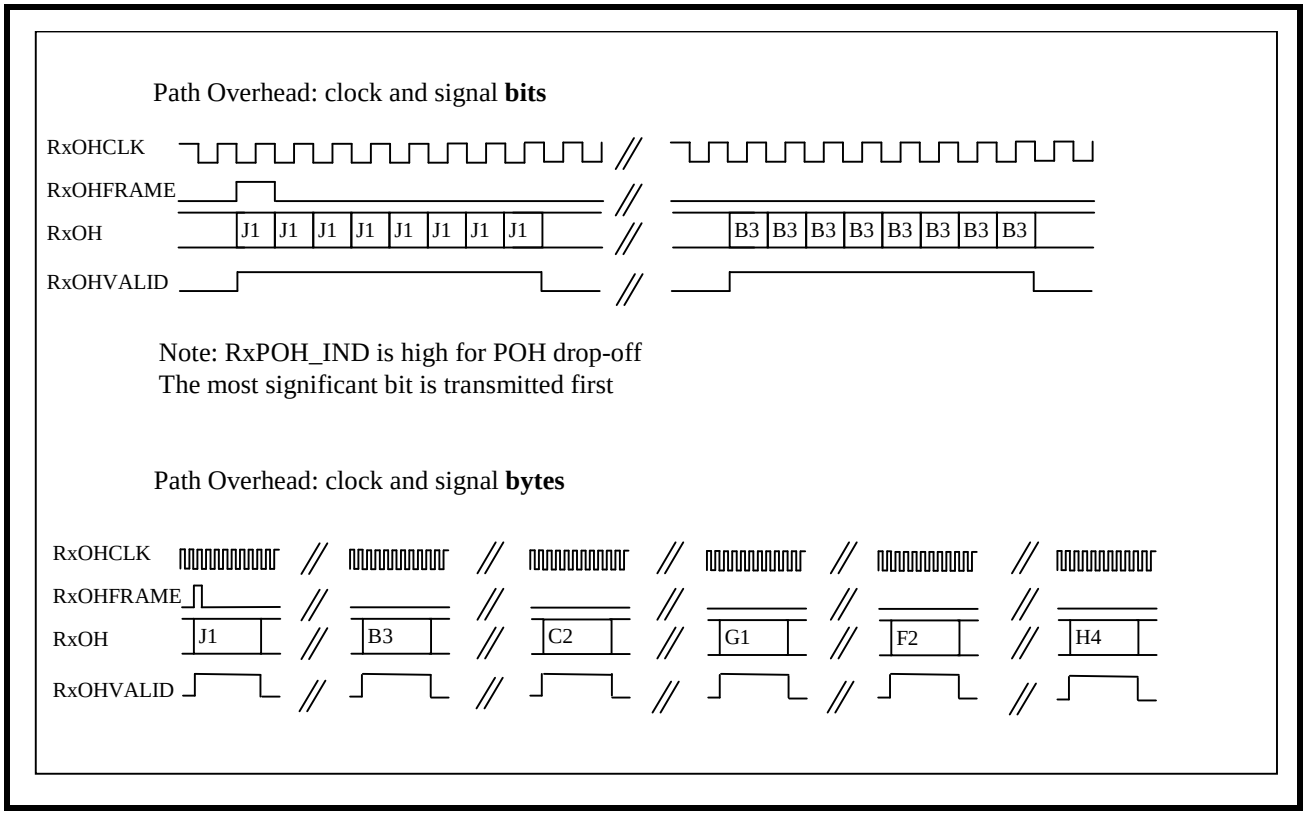
The software can enable or disable the insertion of path AIS to the cell processor on detection of any of the aforementioned conditions. If AIS insertion is necessary, then an enable signal to the rxspoh_proc block is activated which causes the rxspoh_proc block to insert all ones in the payload bytes on the 'rbyte' port to the VT Mapper cell processor.

RXSPOH_CAP BLOCK

The rxspoh_cap block captures the contents of the path overhead and stores them for access by the external processor. The nine path overhead bytes are stored in registers. The rxspoh_cap block issues an interrupt once all the path overhead bytes (9 bytes) for the current frame have been captured. When the last path overhead byte of the current frame has been written to its register, an interrupt is raised to notify the software. The contents of the captured path overhead bytes are preserved for one frame (i.e., until the next capture interrupt) for access by the software.

The captured path overhead bytes are serialized and sent as outputs from the chip as shown in **Figure 22**. RxOHFRAME, RxOH, and RxOHVALID are updated on the falling edge of RxOHCLK. The rate of RxOHCLK is programmable in the range from 1.215MHz to 38.88MHz.

FIGURE 22. PATH OVERHEAD INTERFACE TIMING



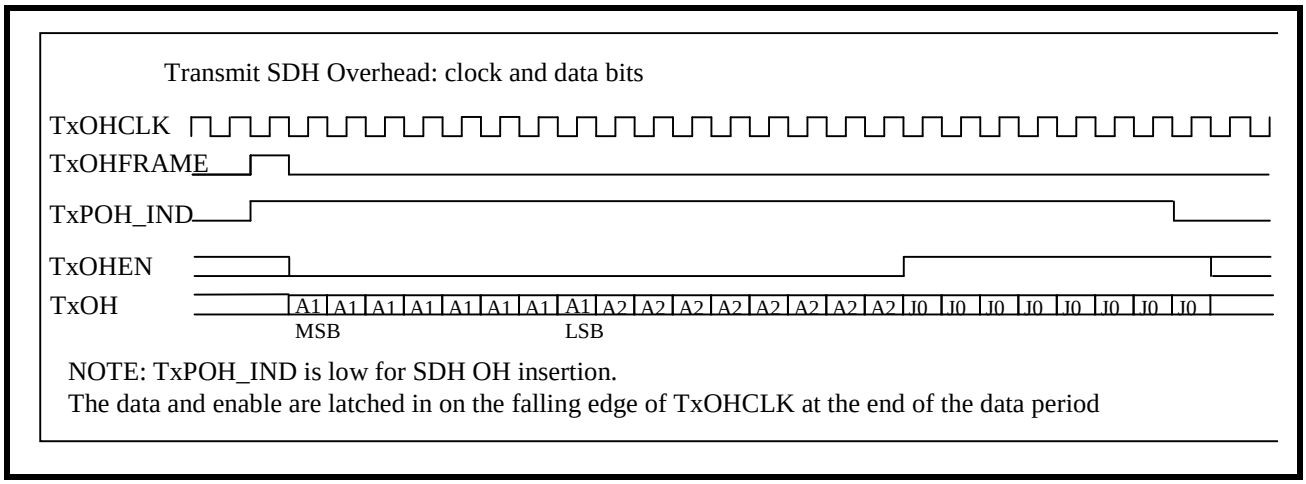
STM-0/1 TRANSMIT TRANSPORT PROCESSOR

TXSTOH_INS BLOCK

The txstoh_ins block provides a serial port for hardware insertion of the transport overhead bytes. The hardware inserted SDH OH bytes, if enabled, override the contents of the SDH OH software registers during transmission. The hardware inserted SDH OH bytes are forwarded to the txstoh_cont block along with the enable signal. The SDH OH port also has an enable input which allows hardware to override the contents of the SDH OH software registers without going through the processor interface. The following picture shows the transport overhead J0 byte being enabled. The TxOHFRAME and TxOHEN signals are updated on the falling edge of TxOHCLK while the TxOHINS and TxOH signals are sampled on the second rising edge of TxOHCLK following the assertion of TxOHEN.

The rate of TxOHCLK is programmable within the range from 2.43 MHz to 38.88 MHz.

FIGURE 23. TRANSMIT TRANSPORT OVERHEAD INTERFACE TIMING



HARDWARE RDI-L INSERTION

Hardware can enable RDI-L insertion by setting the most significant bit of the B2 byte to "1" on the TTOH serial input line. Note that software must first enable hardware RDI-L insertion. The state of the TTOHIns pin has no effect during the B2 slots.

TXSTOH_CONT BLOCK

The txstoh_proc has one 8 bit internal data bus interface. The txstoh_cont block provides the register file and internal processor interface for the transport section of the SDH transmitter. It selects the value of the transport overhead bytes from either hardware or software according to the control registers and forwards them to the txstoh_proc block for transmission. The hardware value is specified through a parallel data input port. If the transport overhead bytes are serially entered into the chip, it is assumed that a serial to parallel data converter has converted the data to parallel format and has placed the data on the input of the txstoh_cont block at the appropriate instances during transmission. The txstoh_cont also provides control for the transmission of a section trace message (J0 byte).

A1/A2 GENERATION

The txstoh_cont block generates alternate A1 and A2 values based on hardware or software requests and sends them to the txstoh_proc block via the tx_toh_data lines. The txstoh_cont block accepts A1/A2 values from the hardware input, or alternatively, software can specify an error mask indicating the A1/A2 bytes in which errors should be inserted for diagnostic purposes. A1/A2 errors are always inserted on frame boundaries, i.e., the A1/A2 error mask is only sampled at the start of every frame.

B1 ERROR MASK GENERATION

The txstoh_cont block allows software to insert errors into the B1 value calculated and transmitted by the txstoh_proc block. By writing to an appropriate register bit, a software controlled error mask is used to insert errors into the B1 byte.

B2 ERROR MASK GENERATION

The txstoh_cont block allows software to control B2 BER generation through two registers: A byte error mask register and a bit error mask register. The byte error mask specifies which of the B2 bytes are to be corrupted and the bit error mask specifies which bits are to be inverted in the B2 bytes that are to be corrupted. In the case of an 8 bit internal data bus, each bit in the B2 byte error mask corresponds to 4 bytes (i.e., one time slot). The B2 byte and bit error masks are sampled before the first B2 byte of each frame if B2 error insertion is enabled by software.

SCRAMBLING

The txstoh_cont block allows software to disable scrambling by setting a bit in the control register. Otherwise, the SDH data is scrambled using the identical algorithm as the de-scrambling process.

K1/K2 CONTROL

The K1/K2 bytes contain the APS code. The APS code transmitted either come from software registers or from hardware via the TxOH serial pin. Note that the 3 least significant bits of the K2 byte (bits 6, 7 and 8) may be overridden by an RDI-L alarm.

RDI-L CONTROL (K2 BITS 6, 7, AND 8)

The RDI-L indication bits consist of the 3 least significant bits of the K2 byte. The bits usually contain portions of the transmitted APS code. However, they are overridden with the RDI-L pattern 3'b110 if any of the following software configurable conditions occur: LOS, LOF, or AIS-L. RDI-L can also be inserted from hardware via the TxOH serial pin or forced by software. RDI-L insertion is done according to the following SDH rules:

- TE shall generate RDI-L within 125µs of detecting an AIS-L defect (or a lower-layer, traffic-related, near-end defect). The LTE shall generate RDI-L by inserting the code '110' in bits 6, 7, and 8 of the K2 byte.

The lower-layer, traffic-related, near-end defects referred to by R6-200 are LOS and LOF from the receiver blocks.

- If bits 6 through 8 of the K2 byte are not used for other purposes (e.g., the linear APS mode indication), the LTE shall deactivate RDI-L by inserting the code '000' in bits 6, 7, and 8 of the K2 byte within 125µs of terminating the defect that caused it.
- If bits 6 through 8 of the K2 byte are used for other purposes, the LTE shall deactivate RDI-L by inserting an appropriate code in bits 6, 7, and 8 of the K2 byte within 125µs of terminating the defect that caused it to be sent (assuming it has been sent for any minimum RDI-L assertion time supported by the NE).
- When LTE generates RDI-L, it should generate it for at least 20 frames.

SECTION TRACE GENERATION (J0/Z0)

The txstoh_cont block allows three methods in the transmission of the J0/Z0 bytes:

Method 1: The J0 byte is set to all 1 in accordance with the SDH standard rule.

- Unless it is being used for a defined purpose (e.g., to carry a section trace message once the details of that feature are defined) each J0 and Z0 byte shall be set to a binary number corresponding to its order of appearance in the STM-N frame (i.e., the J0 byte shall be set to 00000001, the first Z0 byte shall be set to 00000010, etc.).

Method 2: The J1 byte is obtained from the hardware input

Method 3: The J1 byte is obtained from the message written by software into the J1 message buffer

Method 1 is the default unless the software control specifies otherwise. The Z0 bytes are always generated according to the above rules.

The section trace (J0) transmit buffers use a 64x8 single port ram as in the case of the path trace transmit buffers. The memory segments contain the J0 section trace buffers and operate in the same way as the J1 transmit path trace buffers.

REI-L GENERATION (M0/M1)

The txstoh_cont block allows three methods in the transmission of the M0/M1 bytes:

Method 1 : The REI-L signal is set according to the B2 error count by the receiver blocks from the most recently received frame

Method 2 : The REI-L signal is obtained from the hardware input

Method 3 : The REI-L signal is obtained from software

Method 1 is the default unless software chooses to enable either method 2 or 3.

S1/F1/E1/E2 SELECTION

The txstoh_cont block allows either hardware or software insertion of the S1, F1, E1, and E2 bytes. The default generation method for the S1 byte is reading from the software registers. The default generation method for the E1, F1, and E2 bytes is hardware insertion. The registers contain all zeros upon reset.

DATACOM (D1-D12) SELECTION

The data communication bytes are inserted via hardware only.

UNDEFINED SDH OH BYTES

The remaining bytes of the STM-N transport overhead are all currently undefined. The txstoh_cont block inserts all zeros in those bytes in accordance with the SDH standard.

- An SDH NE shall have the capability to ignore the values contained in all undefined and unused bits and bytes [except for BIP-8 calculations] to prevent misinterpretation of the received patterns.
- An SDH NE should send an all-zeros pattern (before scrambling) in undefined bits and bytes. All-zero patterns should also be sent in defined bits and bytes if the NE does not support the defined function or if the function has been disabled by the user.

AIS-L CONTROL

The txstoh_cont provides AIS-L insertion capabilities according to the SDH standard:

- STE shall generate AIS-L downstream within 125µs of detecting an LOS or LOF defect on the incoming signal or the failure of LTE supporting provisioned line origination functions. The AIS-L shall be generated as an STM-N electrical signal that contains valid section overhead and a scrambled all-ones pattern for the remainder of the signal.

The txstoh_cont allows software to insert an AIS-L condition on the transmitted data by writing to an appropriate bit in the register file. The AIS-L condition is set/unset on frame boundaries. AIS-L insertion overrides all other frame data insertion schemes with the exception of LOS insertion.

LOS INSERTION

The txstoh_cont block allows software to specify an LOS condition on the transmitted data which sets all data bytes to zero after scrambling. LOS insertion is enabled by writing a "1" to the appropriate register file bit. LOS insertion, if specified, overrides all other transmit frame data insertion schemes.

TXSTOH_PROC BLOCK

The txstoh_proc has one 8 bit internal data bus interface. The txstoh_proc multiplexes transport overhead data from the txstoh_cont block and SPE data from the txspoh_proc block and inserts them into the data stream. The txstoh_proc block generates timing and location signals for the other transmitter blocks and performs primitive SDH tasks such as scrambling, B1/B2 calculation and insertion, and start of frame (A1/A2) insertion using control signals from the txstoh_cont block.

LOCATION STROBE GENERATION

The txstoh_proc block maintains the location of the current byte (byte lanes) being transmitted and outputs time-advanced row, column, and time slot numbers of the data on the byte lane(s) for the other SDH transmitter blocks. The time-advanced location signals allow for pipeline delays necessary to move the data from the other transmit blocks to the txstoh_proc block.

A1/A2 INSERTION

During normal operation, the txstoh_proc block inserts the SDH framing pattern F628 (hex) for the A1 and A2 bytes respectively. This can be overridden by non-zero values from the tx_toh_data input from the txstoh_cont block at the time of insertion.

B1 CALCULATION AND INSERTION

The txstoh_proc block calculates the BIP-8 B1 error code on the scrambled data of the current frame and inserts it into the B1 byte of the next frame before scrambling. Errors can be inserted for diagnostic purposes from the tx_toh_data input from the txstoh_proc block.

B2 CALCULATION AND INSERTION

The txstoh_proc block calculates the BIP-8 B2 error code on the unscrambled data of the current frame except for the section overhead bytes and inserts it into the B2 bytes of the next frame before scrambling. Errors can be inserted for diagnostic purposes from the tx_toh_data input from the txstoh_proc block.

Two memories are used in the B2 error code calculations for the txstoh_proc block. One memory is used to store the running value of the B2 error calculations. This memory is a 12x8 dual port RAM with one port for reads and one port for writes. This is necessary because as the hardware is calculating the B2 code for each STS, it needs to store the new value into the memory and at the same time fetch the current code for the next STS from memory. The second memory is a single port 12x8 RAM used to store the final B2 codes for all the STS's. This memory is read at the B2 byte locations for comparisons and written into in the A1 byte locations to store the final B2 codes for the previous frame. For the 8 bit version of the rxstoh_proc block, the B2 RAM widths are 8 bits.

SCRAMBLING

The txstoh_proc block scrambles all the bytes of the SDH frame except for the A1, A2, and J0/Z0 bytes. Scrambling may be disabled by software. Scrambling is controlled on frame boundaries. That is, the txstoh_proc block will sample the scram_enable input at the beginning of each frame and scrambling is performed on the entire frame if the scram_enable is "High".

SDH OH DATA INSERTION

For the rest of the SDH OH bytes, the txstoh_proc simply takes the data on the TxOH input at the time of transmission, and inserts it into the corresponding location in the SDH frame. The SDH OH bytes intended to be inserted in this manner are: M0/M1, J0, S1, K1, K2, F1, E1, E2, the data communication bytes (D1-D12) and the undefined and growth bytes.

SPE DATA INSERTION

The txspoh_proc block places SPE data on the tx_path_data input of the txstoh_proc according to the location signals generated by the txstoh_proc block. The txstoh_proc takes the SPE data and inserts it into the transmit SDH frame at the appropriate instances in time.

AIS-L/LOS INSERTION

The txstoh_proc can apply either an AIS-L or a LOS condition as described in previous sections according to control signals from the txstoh_cont block.

4.9 TELECOM BUS INTERFACE

The device's Telecom Bus interface supports the following features:

Option to enable/disable parity generation.

Option to select if parity is generated over data only or data and PL and C1J1 and Alarm signals.

Option to select if odd or even parity is used.

Accepts 8 kHz transmit frame pulse and complementary transmit reference clock to synchronize transmit data.

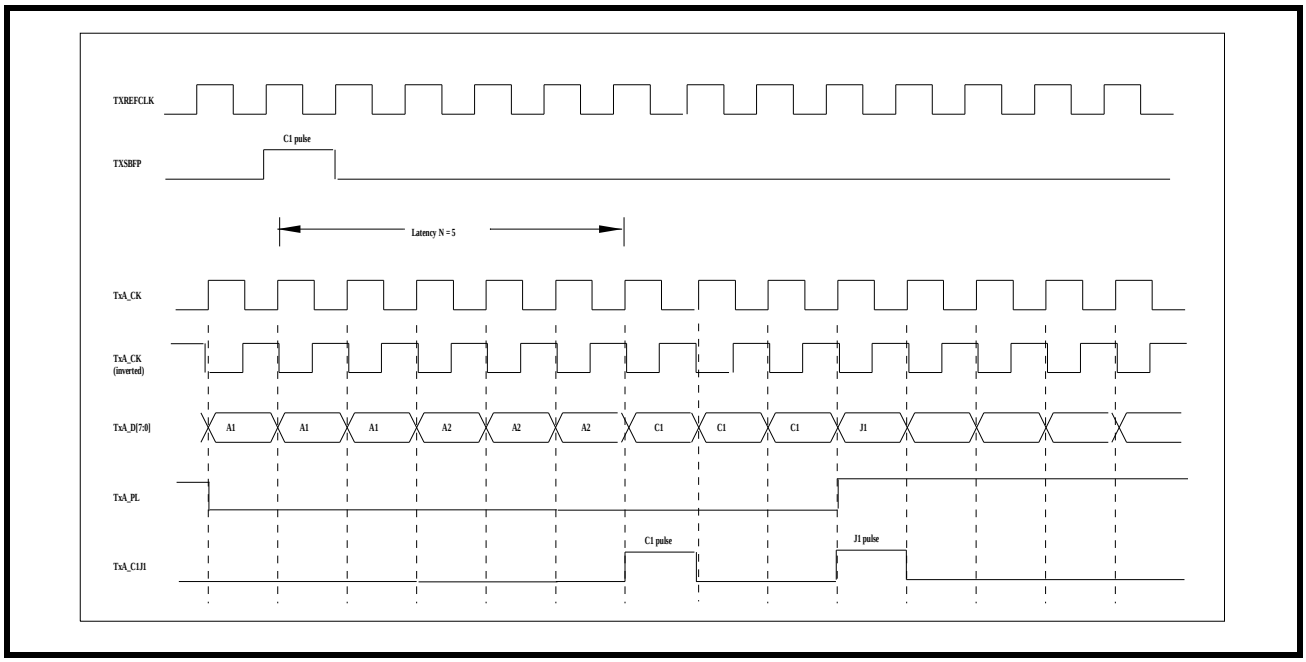
4.9.1 TRANSMIT TELECOM BUS

The Tansmit Telecom Bus interface consists of the following outputs: 8-bit data bus TxD_D[7:0], clock TxD_CLK, payload indication TxD_PL, timing indication TxD_C1J1V1_FP, parity TxD_DP, and a alarm indication TxD_ALARM. The device also allows a common set of reference timing signals for synchronizing the data input to each of the Telecom Bus ports for the cases where transmit re-phase is not available on the other side. The Telecom Bus port operates at 19.44 MHz on STM-1 and 6.28 Mhz on STM-0.

The subsections below summarize the functionality of the Telecom Bus interface signals. Tx51_19Mhz is provided as a reference clock to put data out onto the Telecom Bus ports. These signals are 19.44/6.28 MHz. This clock must be used to source the data to be transmitted on the appropriate Telecom Bus.

An 8kHz pulse (TxSBFP_IN_OUT) is input on the falling edge of Tx51_19Mhz once every frame period and is one Tx51_19Mhz clock cycle wide. It is used to synchronize the data arriving at the TxD_D[7:0] outputs. A 16-bit latency counter can be configured to determine the latency between the frame pulse and the associated input data (C1). Figure 24 shows the relationship between the Input Telecom Bus Data and the TxSBFP_IN_OUT signal.

FIGURE 24. TRANSMIT TELECOM BUS INTERFACE TIMING



The transmit Telecom Bus clock output (TxD_CLK) is used to clock the transmit Telecom Bus output signals. It must be synchronous with the Tx51_19Mhz clock. Also, no phase relationship is required between Tx51_19Mhz and the TxD_CLK. The TxD_D[7:0] stream must contain valid Pointer Bytes and the POH.

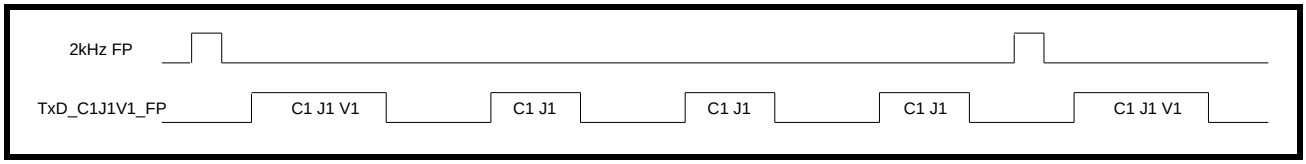
The Telecom Bus also generates the value of the transmit Telecom Bus parity output (TxD_DP). The parity calculations can be configured through the use of the control bits in the interface control registers. The

transmit Telecom Bus Alarm output (TxA_Alarm) is generated to tell the external device to generate AIS-P in the STM-0/STM-1 for which the alarm occurs.

4.9.2 2kHz Mode in STM-1

To align the V1 bytes with H4 in STM-1, the part must be configured for 2kHz. With a 2kHz frame pulse applied to each of the Voyager Lite devices, the parts can align VT Superframe boundaries. This will allow V1 bytes within each device to match one another. The TxD_C1J1V1_FP will pulse "High" for all C1J1 bytes. However, it will only pulse "High" during the V1 byte. V2, V3, and V4 will not be indicated by the external frame pulse.

FIGURE 25. C1J1V1 PULSE IN STM-1 2KHZ MODE

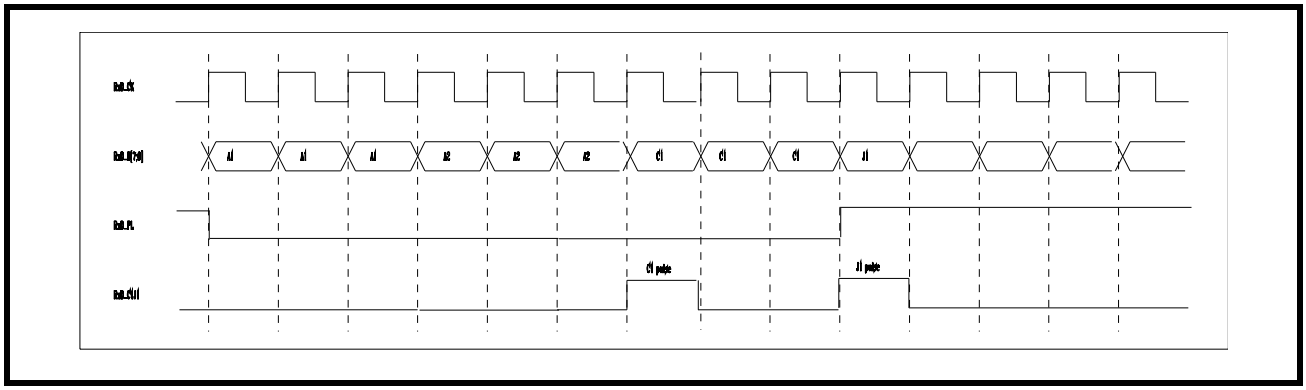


4.9.3 RECEIVE TELECOM BUS

The receive Telecom Bus interface consists of the following inputs: 8-bit data bus RxD_D[7:0], clock (RxD_CLK), SPE indication (RxD_PL), C1J1 indication (RxD_C1J1V1_FP), parity (RxD_DP), and a alarm indication (RxD_ALARM). All of the receive Telecom Bus ports operate at 19.44/6.28 MHz.

The subsections below summarize the functionality of the receive Telecom Bus interface signals. The receive Telecom Bus clock input RxD_CLK is used to clock in the receive Telecom Bus input signals from an external device. The clock edge on which the Telecom Bus signals are clocked is programmable via the CKINV control bits. **Figure 26** shows the functional relationship of the receive Telecom Bus signals.

FIGURE 26. RECEIVE TELECOM BUS INTERFACE TIMING



Each receive Telecom Bus port has an 8-bit wide data bus that inputs the STM-0/STM-1 data from an external device. The receive Telecom Bus data is byte-aligned and the entire payload, including SDH OH and POH, is passed in the device. The receive Telecom Bus C1J1 input (RxD_C1J1V1_FP) can be provisioned to provide two different types of indications, depending on the register setting. When CPOS is set to "1", the corresponding RxD_C1J1V1_FP signal provides two pulses.

For all sub-frames, the receive Telecom Bus PL input (RxD_PL) is "Low" during the SDH OH bytes in the RxD_D[7:0] stream and is "High" during the SPE bytes. This includes cases where pointer adjustments are performed and the SPE needs to be adjusted about the H3 bytes. For example, the H3 bytes are payload bytes during the frame in which a pointer decrement occurs, therefore the RxD_PL signal will be "High" coincident with the H3 bytes for that frame. Also in the frame where a pointer increment occurs, the three bytes after the H3 bytes become stuff, therefore the RxD_PL signal will be "Low" for those bytes. The parity checking can be configured through the use of the control bits in the interface control registers.

The receive Telecom Bus alarm output (RxD_ALARM) is generated by an external device in response to an alarm condition that will cause AIS-P to be generated. The RxD_ALARM input will remain active for the duration of the alarm condition that causes it to become set.

4.10 VT MAPPER

INTERFACES AND PROTOCOLS

This block has three interfaces to the outside world:

The Internal Bus interface through which the block communicates with the µP interface block which interfaces to the external processor that controls and monitors the VT Mapper.

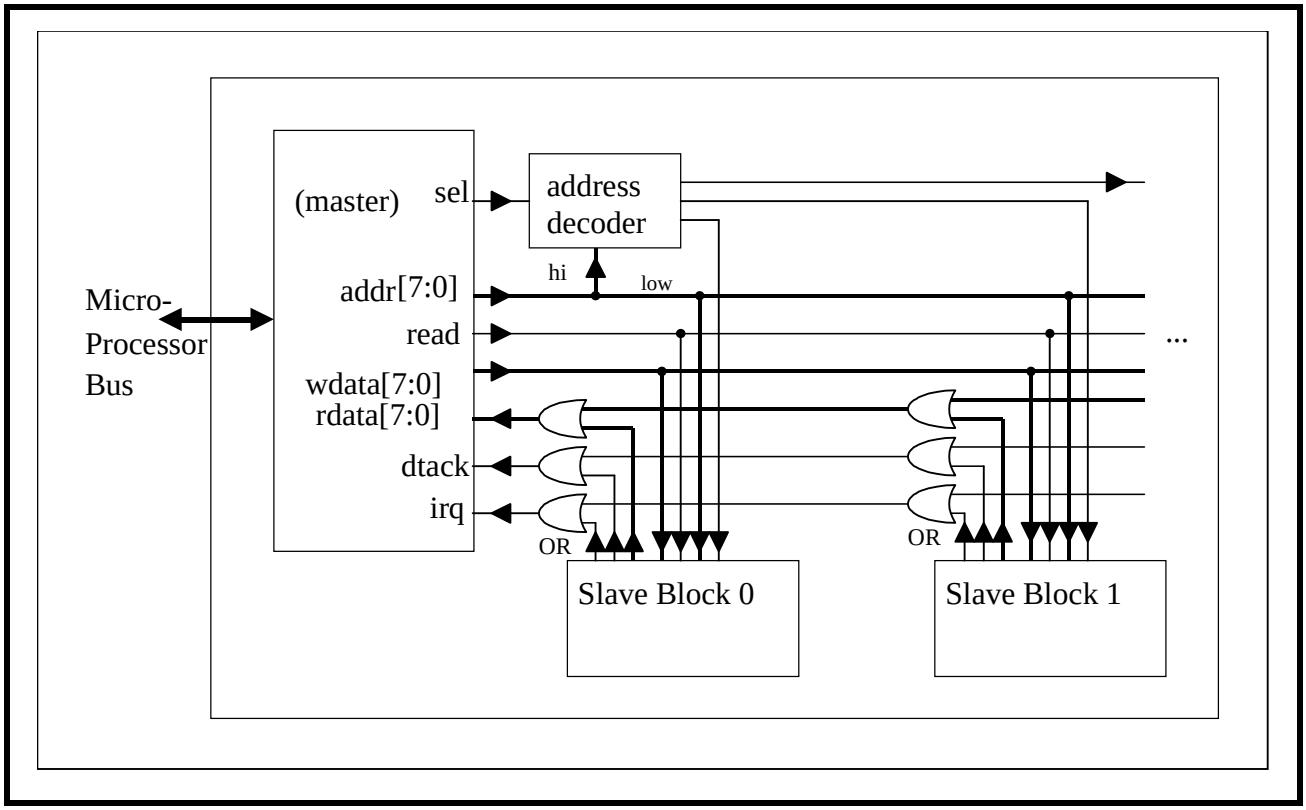
The Mid Bus interface through which the block communicates with the blocks processing the higher levels of SDH overhead.

The E1 I/O interface up to 21 digital signals.

INTERNAL BUS INTERFACE

Figure 27 shows the internal synchronous bus structure. It consists of two 8-bit data buses, an 8-bit address bus, and 5 control lines: clock (clk), select (sel), read (read), data transfer acknowledge (dtack), and interrupt request (irq). All of these lines are active High.

FIGURE 27. INTERNAL BUS STRUCTURE



Byte-oriented addressing is used for all of the address maps.

Internal Bus Signals

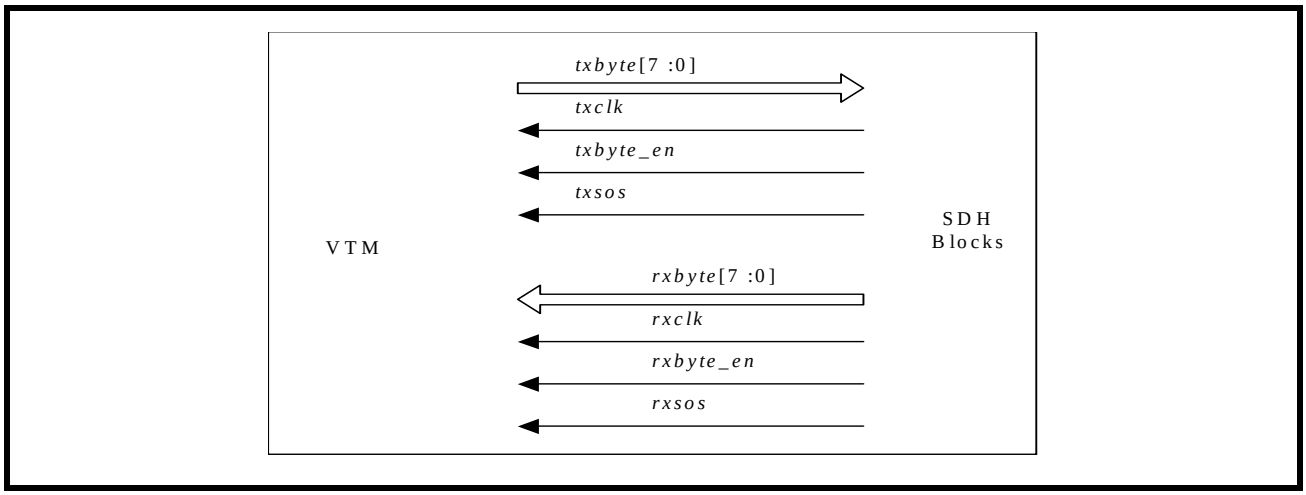
Signals and their usage are described. **Clk**, **Sel** and **Read** are driven high or low by the pif block, based on the **Clk**, **Chip Select**, and **WE** signals from the microprocessor. irq and dtack are low or high driven by internal registers. addr, rdata and wdata may be undefined as long as no read or write action is taken. All signals are Clk aligned and sensitive to the positive edge of Clk.

SIGNAL	DIRECTION	DESCRIPTION
Clk	input	System clock signal, input from external processor
Sel	input	Select signal, when it goes high, selects internal register
Read	input	Read/write control signalHIGH: read data from data bus.LOW: Write data to data bus.
Dtack	output	Data transfer acknowledge signal, comes from internal registers, indicate internal registers are ready to send or accept data.
addr[7:0]	input	Register address.
Irq	output	Interrupt request signal when it goes to 1 indicates an interrupt request.
rdata[7:0]	output	Reads data signals from internal register.
wdata[7:0]	input	Write Data signals to internal register.

MID BUS INTERFACE

The interface between the VTM and the other SDH blocks is a single edge synchronous interface. It consists of a clock, enable pair, and an 8-bit data bus in each direction. The enable signals are active High and data is transferred on the rising edge of the corresponding clock.

FIGURE 28. MID BUS INTERFACE

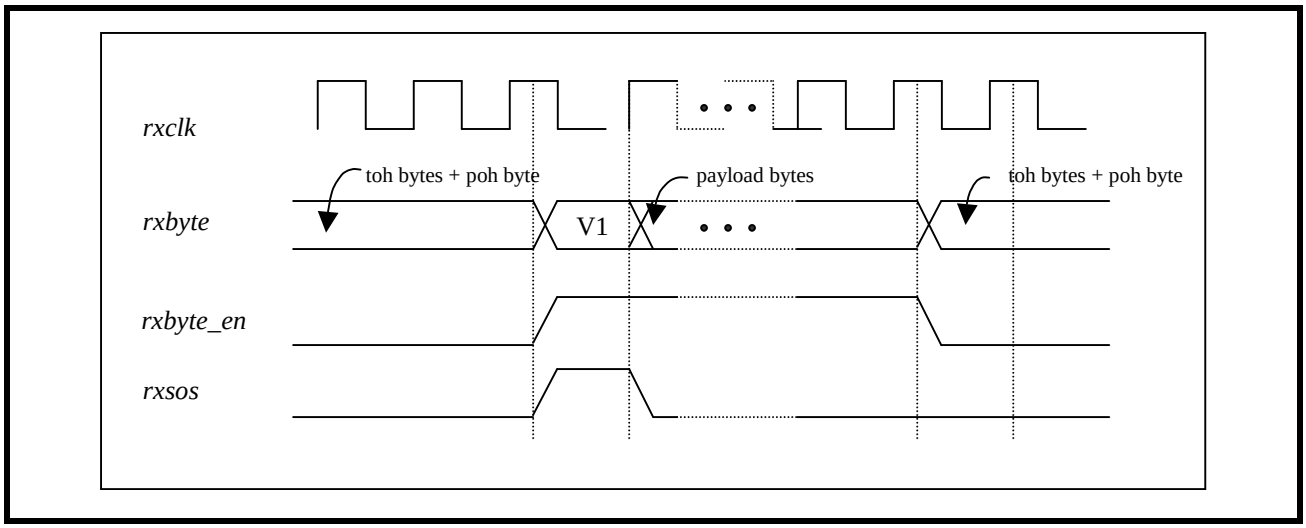


SDH to VTM Direction

In this direction, the higher level SDH block is sending data to the VT Mapper. Data presented on the rxbyte[7:0] data bus of the VTM by the SDH block must be valid to be sampled on the rising edge of rxclk when rxbyte_en is "High". The VTM block samples the rxbyte_en and rxbyte[7:0] lines on each rising edge of rxclk. If rxbyte_en is "High", the data on rxbyte[7:0] is processed as valid data. The transitions on the rxbyte[7:0] and rxbyte_en lines should be timed to satisfy the VTM's setup & hold requirements with respect to rxclk.

For all timing diagrams in this section, it is implied that the data lines can change at every clock cycle. Only when the nature of the data carried on the data lines changes is there a boundary shown on the data line.

FIGURE 29. SDH TO VTM DATA TRANSFER WITH ZERO POINTER OFFSET

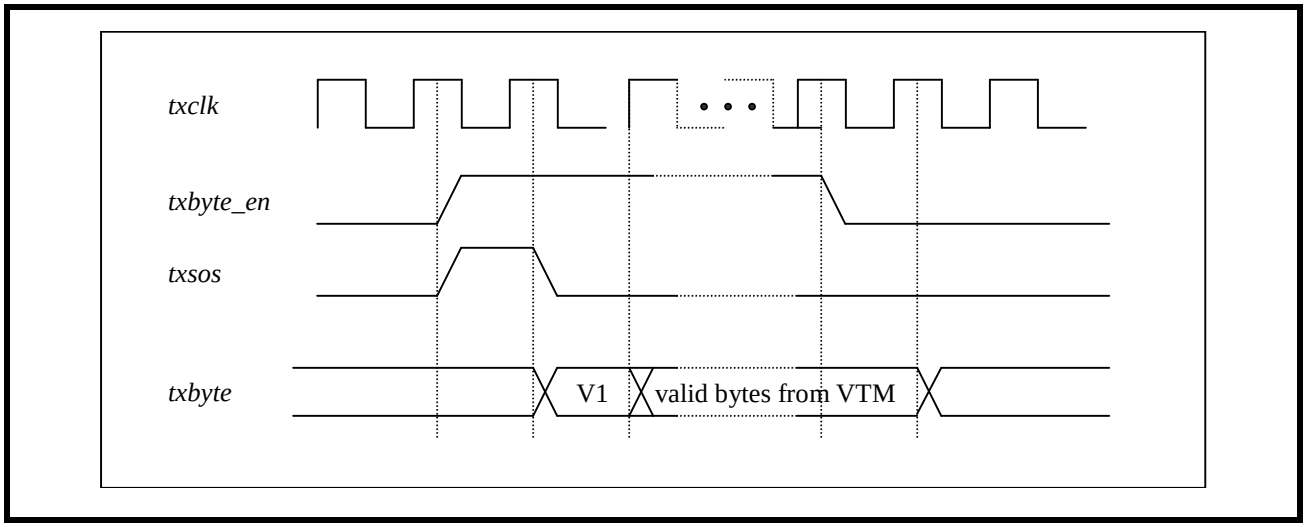


The Start of Superframe signal is asserted while the first V1 byte of the Superframe is present on rxbyte.

VTM to SDH Direction

When the SDH block is receiving data from the VTM, txbyte_en is used as a command signal. When the SDH block asserts txbyte_en "High", data from the VTM is produced on the next rising txclk edge. **Figure 30** gives an example of such a transaction. Transitions of lines txbyte[7:0] and txsos occur on the rising edge of txclk so setup time requirements of up to one txclk period can be satisfied. It is up to the interface designer to make sure that the other timing requirements of circuits connected to the VTM are satisfied.

FIGURE 30. VTM TO SDH DATA TRANSFER



Although a minimum of buffering is done at the VTM Mid Bus output to compensate for the jitter introduced by the transport and path overhead columns (SDH OH & POH), it is assumed and required that txbyte_en and txclk clock ticks will occur at an average frequency of 6.192MHz (i.e. 6.48MHz txclk with a 86:90 enable ratio) and will be approximately equally spaced (burst reads are not supported).

E1 I/O LINE INTERFACE

Each of the 21 E1 input channels has its own clock and data input signals (internally provided from the E1 line interface). In addition, each of the 21 E1 input channels has a Start of SuperFrame input that is used for synchronous mappings of E1 signals. Each of the 21 E1 output channels has it's own clock, data and Start of SuperFrame output signals (internally routed to the E1 line interface). Input data and Start of SuperFrame are sampled on the rising edge of the input clock. Output data and Start of SuperFrame are valid to be sampled on the rising edge of the output clock.

When doing synchronous mappings of E1 signals, the position of the first bit of an E1 SuperFrame is indicated by a high on the Start of Superframe line.

FIGURE 31. E1 INTERFACE TIMING (INTERNAL TO THE CHIP)

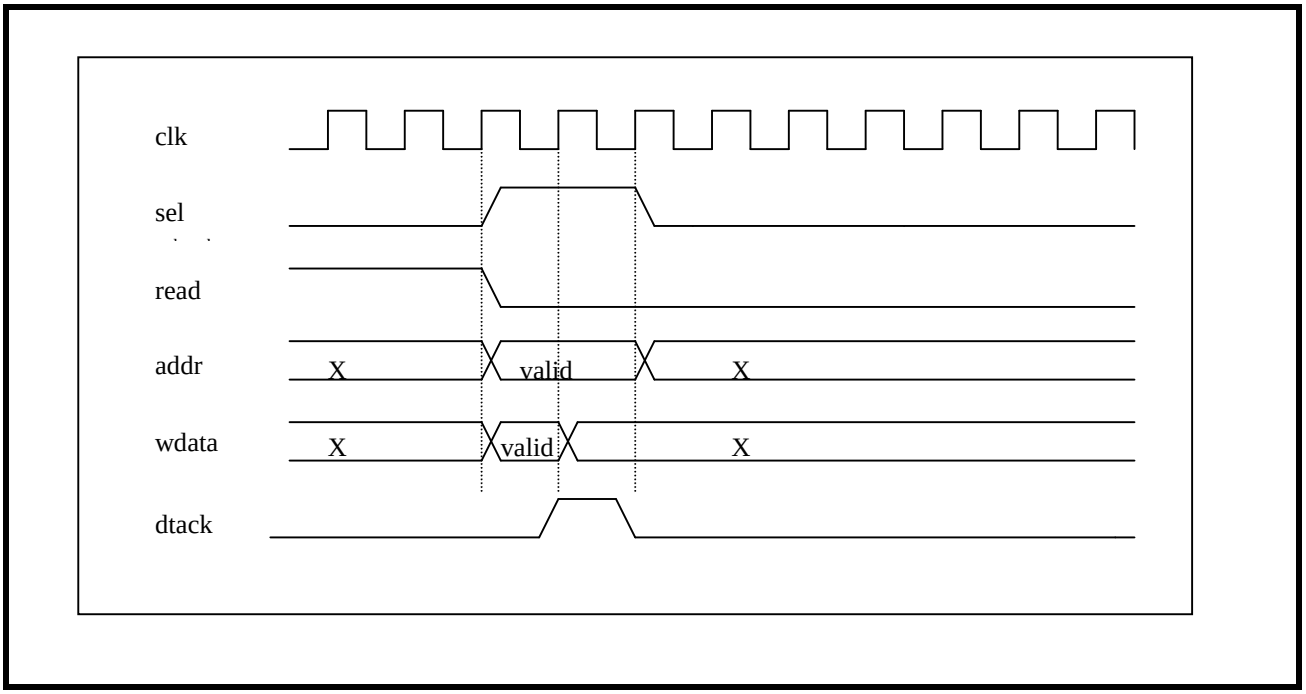
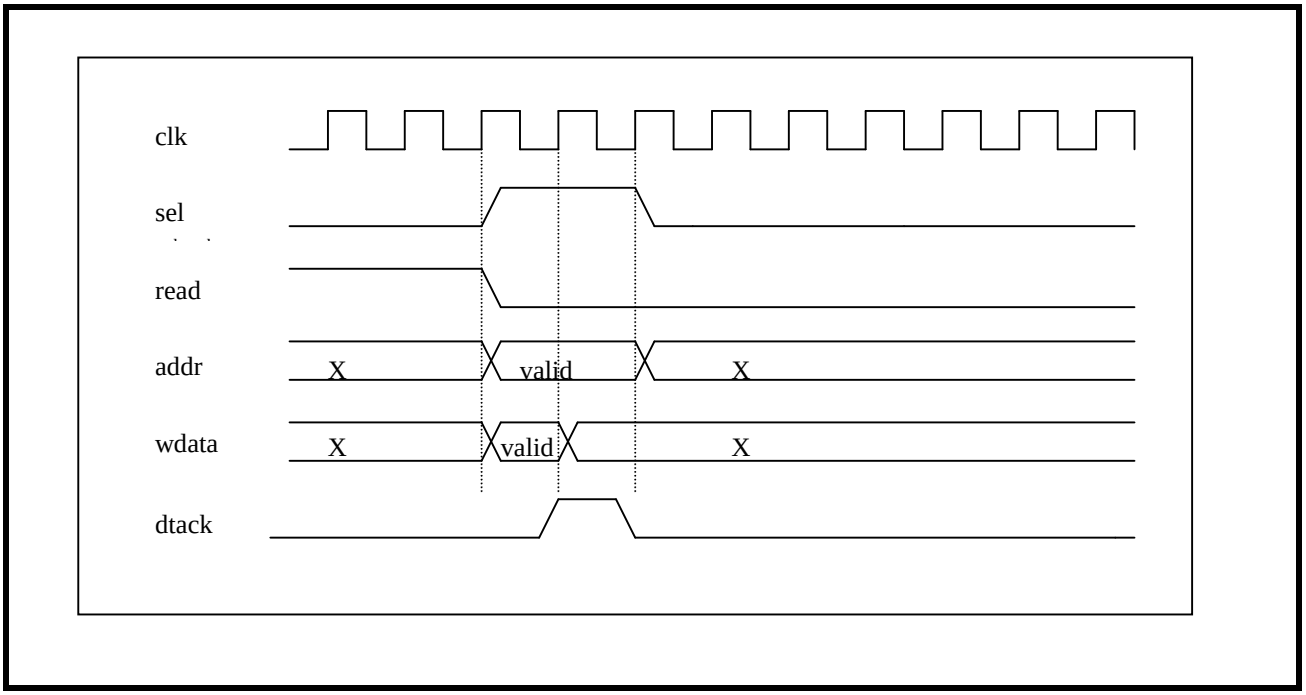


FIGURE 32. E1 INTERFACE TIMING (E1 SYNCHRONOUS MAPPING, INTERNAL TO THE CHIP)



DESIGN DESCRIPTION

The function of this reusable block is limited to the construction and extraction of the VT structured content of the SDH STM-0 Payload Capacity / SDH VC-3 as described by Telcordia's GR-253-CORE Generic Requirements and ITU-T's G.707 recommendations. The rest of the work for the higher levels of hierarchy including Transport and Path Overhead is handled by the STM-0 SDH blocks.

VT STRUCTURED STM-0 PAYLOAD CAPACITY

This section briefly describes the structure of the SDH data stream used to carry lower bit-rate channels. The STM-0 Payload Capacity is made up of 84 columns of 9 rows each. The Payload Capacity is divided equally amongst seven Groups. Each Group can contain three VT2/TU-12 tributaries. VT2/TU-12 tributaries are used to carry an E1 signal.

VT Superframe

Four consecutive STM-0 frames of Payload Capacity are used to make up a VT Superframe. The first byte of each Tributary in each frame has a special function. These special bytes are called V1 to V4.

V1 & V2 : VT Payload Pointer

The V1 and V2 bytes form the VT Payload Pointer. In asynchronous mappings or on transmission, the VT Payload Pointer is assigned a fixed value by this block such that the V5, J2, Z6/N2 and Z7/K4 bytes immediately follow the V1 to V4 bytes. In synchronous mappings or on reception, the VT Payload Pointer is processed as prescribed in Telcordia and ITU. Each time a received VT Payload Pointer is incremented or decremented, internal counters are available to be read by the processor in registers BIP2CNT1 to BIP2CNT21 and REICNT1 to REICNT21 are incremented.

V3 : VT Pointer Action Byte

This byte is used as a negative stuff byte when required by a pointer decrement. Otherwise, it is Undefined. It is never used by this block on transmission of asynchronously mapped signals. In synchronous mappings or on reception, this byte is processed along with the VT Payload Pointer bytes as prescribed in the Telcordia and ITU documents.

V4 : Undefined

This byte is reserved for future growth and is treated as Undefined. It is ignored on reception and is transmitted as all zeros.

VT Path Overhead

Each Virtual Tributary has it's own set of Path Overhead bytes which are processed as described in the following paragraphs.

V5 : VT Path Error Checking, Signal Label and Path Status

The bit assignments for the V5 byte are shown in **Table 7**.

TABLE 7: V5 - VT PATH ERROR CHECKING, SIGNAL LABEL AND PATH STATUS

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BIP-2		REI-V	RFI-V	Signal Label			RDI-V

Bits [7:6] of V5 are used for error performance monitoring. A BIP-2 scheme is defined as follows. When generating a tributary, bit 7 is set to the exclusive-or of all the odd numbered bits (bits 7,5,3 and 1) of the previous VT SPE (including the V5, J2, Z6/N2 or Z7/K4 byte but not the V1 to V4 bytes, except V3 when it is used as a negative stuff byte), bit 6 is set to the exclusive-or of all the even numbered bits (bits 6, 4, 2 and 0) of the previous VT SPE. When terminating a tributary, bit 7 is compared to the exclusive-or of all the odd numbered bits of the previous VT SPE, bit 6 is compared to the exclusive-or of all the even numbered bits of the previous VT SPE. If there is any difference, bit 5 of V5 (REI-V) of the peer tributary generator is set to "1",

otherwise it is set to "0". Detected errors are tallied in the BIP2CNTx counters that can be read by the processor in registers BIP2CNT1 to BIP2CNT21

Bit 4 of V5 is used for VT Path Remote Failure Indication (RFI-V). As described in GR-253-CORE, when automatic RFI-V insertion is enabled by writing "1" to bit VTRFIEN of registers INS1 to INS21, RFI-V will be signalled by inserting a "1" in the RFI-V bit of byte V5 when LOP-V, AIS-V, UNEQ-V or PLM-V is detected for more than 2½±½ seconds on the received tributary in the corresponding time slot. The RFI-V signalling is removed, and bit RFI-V of byte V5 is cleared if the condition that triggered it is absent for 10±½ seconds.

Bits [3:1] of V5 are used for VT Path Signal Label and indicate the contents of the tributary. Only the following codes are generated by the tributary generator or expected by the VT PTE:

000 : Unequipped or not provisioned

010 : Asynchronous Mapping of E1

100 : Byte Synchronous Mapping E1

Bit 0 of V5 is used for one-bit VT Path Remote Defect Indication (RDI-V) As described in GR-253-CORE. When automatic RDI-V insertion is enabled by writing "1" to bit VTRDIEN of registers INS1 to INS21, RDI-V will be signalled by inserting a "1" in the RDI-V bit of byte V5 when LOP-V, AIS-V, UNEQ-V or PLM-V is detected on the received tributary in the corresponding time slot.

VC-12 Path Remote Loopback Signaling

Voyager-lite supports in-band signaling within the low-order VC-12 path overhead to request VC-12 path remote loopback (E1 payloads) provisioning at down-stream equipment. Signaling will be sent on the STM-1 transmit output from the request originating system (sending system) and received on the STM-1 input of the far-end system (receiving system). Once the receiving system detects this in-band message, a status flag is set to indicate the remote loopback request detection. The system software will detect this flag through interrupts and subsequently provision the appropriate low-order path for remote loopback. The sending system shall continue sending the in-band message until such time that the remote loopback should be removed. At this time, the VC-12 Path Overhead/Payload content within the STM-1 transmit output of the sending system shall resume normal function. Upon detecting termination of the remote loopback request, the receiving equipment shall set a status flag to indicate the clearance of the remote loopback request. The system software can detect this flag and subsequently remove the remote loopback provisioning for the appropriate low-order path. This function is provided on a per VC-12 basis.

The LSB of the bit stuff byte immediately following V5 is used as the location for the remote loopback request messaging. During normal operation, this bit will contain the usual stuff bits. However, during remote loopback request transmission, this bit shall transmit a continuous, alternating pattern of 1's and 0's. The pattern shall always begin with a "1" and terminate immediately upon release of the software control bit for the remote loopback request enable. The receiving equipment shall monitor this bit location for the pattern of "1010101010", or exactly ten bits of alternating 1's and 0's with the first bit having a value of "1". Once the stated pattern is detected, the receiver sets a status flag indicating detection of the remote loopback request. This bit should be reset upon read and should not be set again until clearance of the remote loopback request is detected, and a new remote loopback request message is received.

Detection and cancellation examples:

J2 : VT Path Trace

Byte J2 is used to transmit repetitively a Low Order Path Access Point Identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. The Path Access Point Identifier supports both 16-byte and 64-byte frame as the J0 byte defined in the earlier section.

The 64 byte RAM is used on a shared basis with J2 and N2 bytes. When the 64 byte J2 message mode is configured, the N2 tandem connection feature is disabled. When the J2 message mode is configured as 16 byte, two 16 byte segments are used for TC (tandem connection) and J2.

Z6/N2 : VT PATH GROWTH (TANDEM CONNECTION, TC)

N2 is allocated for Tandem Connection Monitoring for the VC2, VC-12 and VC-11 level. The structure of the N2 byte is given in **Table 8**.

- Bits 1-2 are used as an even BIP-2 for the Tandem Connection.
- Bit 3 is fixed to "1". This guarantees that the contents of N2 are not all zeroes at the TC source. This enables the detection of an unequipped or supervisory unequipped signal at the Tandem Connection sink without the need for monitoring further OH-bytes.
- Bit 4 operates as an "incoming AIS" indicator.
- Bit 5 operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 operate in a 76 multiframe as:
  - the access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format of J0;
  - the TC-RDI, indicates to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink; An 8-bit ounter is provided for counting the number of REI bits received as 1 in bit 5 of N2. An REI indicates that the distant end has detected one or two errors between the BIP-2 calculation of the previous frame (all the bytes) and the BIP-2 value carried in the N2 byte in the current frame.
  - the ODI, indicates to the far end that TU-AIS has been inserted at the TC-sink into the egressing TU-n due to defects before or within the Tandem Connection; An 8-bit counter is provided for counting the number of OEI bits received as equal to 1 in bit 6 of N2. An OEI indication (a1) indicates that the distant end has detected one or two errors when, the BIP-2 calculated for the previous frame is compared against the BIP-2 value carried in the V5 byte in the current frame.
  - reserved capacity (for future standardization).
  - The structure of the multiframe is given in **Table 9** and **Table 10**.

TCM Functionality - Source

- If no valid TU-n is entering the Tandem Connection at the TC-source, a valid pointer is inserted. This results in a VC-AIS signal and bit 4 is set to "1". Even BIP-2 parity is calculated over the inserted VC-AIS signal and written into bits 1-2 of N2.
- If a valid TU-n is entering the Tandem Connection at the TC source, then even BIP-2 parity is calculated over the incoming valid VC-n or the inserted VC-AIS signal and written into bits 1-2 of N2.
  - The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
  - The original BIP-2 is compensated according to the algorithm described below.

NOTE: *In an unequipped or supervisory unequipped signal entering a Tandem Connection, the N2 and V5 bytes are overwritten with values not equal to all zeroes.*

TABLE 8: N2 BYTE STRUCTURE

B1	B2	B3	B4	B5	B6	B7	B8
BIP-2		"1"	"Incoming AIS"	TC-REI	OEI	TC-APId, TC-RDI ODI, reserved	

TABLE 9: B7-B8 MULTIFRAME STRUCTURE

FRAME #	B7-B8 DEFINITION
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 C1C2C3C4C5C6C7]
13-16	TC-APId byte #2 [0 X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X]
:	:
:	:
:	:
65-68	TC-APId byte #15 [0 X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X]
73-76	TC-RDI, ODI and Reserved

TABLE 10: STRUCTURE OF FRAMES # 73 - 76 OF THE B7-B8 MULTIFRAME

TC-RDI, ODI AND RESERVED CAPACITY		
FRAME #	B7 DEFINITION	B8 DEFINITION
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

TCM FUNCTIONALITY - SINK

If no valid TU-n is present at the TC-sink, a defect caused within the Tandem Connection is stated and the TC-RDI and ODI conditions apply.

If a valid TU-n is present at the TC-sink, the N2 byte is monitored:

- ·An "all-zeroes" N1-byte indicates a miss or disconnection within the Tandem Connection. In this case, the TC-RDI and ODI-bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.
- Bit 4 of the received N2 is set to "1" to indicate that a defect has already occurred before the Tandem Connection. In this case, the ODI bit is set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.
- The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found, the TC-RDI and ODI bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.
- The TC-APId is recovered and compared with the expected TC-APId. In the case of a mismatch, the TC-RDI and ODI bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.

The even BIP-2 is computed for each bit pair of every byte of the preceding VC-n including V5 and compared with the BIP-2 retrieved from the V5 byte. A difference not equal to zero indicates that the VC-n has been corrupted and, then the OEI bit is set to "1" in the reverse direction. Furthermore the actual BIP-2 is compared

with the BIP-2 retrieved from the N2-byte. A difference not equal to zero indicates that the VC-n has been corrupted within the Tandem Connection and, then the TC-REI is set to "1" in the reverse direction.

If TU-AIS is not inserted at the Tandem Connection sink, then the N2-Byte is set to all zeroes and the BIP is compensated according to the algorithm described below.

Multiframe Generation and Synchronization

Loss of multiframe occurs when two consecutive Frame Alignment Signals (1111 1111 1111 1110) are detected in error (i.e., one or more errors in each FAS). Multiframe alignment is recovered when one consecutive non-errored FAS are found. Two status bits are used to indicate the Loss Of MultiFrame (TXAnLOMF, RXDnLOMF).

The TC trace identifier message comparison is based on the same state machine as that used for the 16-byte J2 message. The TC lock is removed (instable, INV) when 3 messages are received in error and the TC_INV alarm is declared. The TC lock is established when 3 valid, identical messages are received. A comparison is performed between the microprocessor-written TC and the contents of the incoming message. The message consists of TC Trace ID bytes 0 to 15. A TC Trace Identifier Mismatch (TC_MIS) alarm is declared when any byte does not match. Recovery occurs when there is a match between the expected message and the accepted message.

Bit 8 in frame 73 is defined as a Tandem Connection Remote Defect Indication (TC RDI). A TC RDI alarm occurs when a "1" has been detected in bit 8 in frame 73 for five consecutive multiframes (where each multiframe is 38 ms). The TC RDI alarm state is exited when bit 8 is equal to 0 for five consecutive multiframes. An alarm indication is reported as TC_RDI.

Bit 7 in frame 74 is defined as a Tandem Connection Outgoing Defect Indication (TC ODI). A TC ODI alarm occurs when a "1" has been detected in bit 7 in frame 74 for five consecutive multiframes (where each multiframe is 38 ms). The TC ODI alarm state is exited when bit 7 is equal to 0 for five consecutive multiframes. An alarm indication is reported as TC_ODI.

Tandem Connection Unequipped Status

Unequipped Tandem Connection detection is provided. Five or more consecutive received tandem connection N2 bytes equal to XX00 0000 result in a TC unequipped indication (TC_UNEQ). The alarm state is exited when five or more consecutive received tandem connection N2 (Z6) bytes are not equal to XX00 0000. Note that bits 1 and 2 of the N2 (Z6) byte are masked (shown as X) and do not affect the detection. The XX represents a don't care value and may be equal to a BIP-2 value.

BIP-2 Compensation

Since the BIP-2 parity check is taken over the VC-n (including N2), writing into N2 at the TC-source or TC-sink will affect the VC-2/VC-12/VC-11 path parity calculation. Unless this is compensated, the error monitoring mechanism of BIP-2 is corrupted. Because the parity should always be consistent with the current state of the VC-n, the BIP has to be compensated each time the N2-byte is modified. Since the BIP-2 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-2 bits in the previous frame shall also be considered in the compensation of BIP-2 in the current frame.

Z7/K4 : VT PATH APS AND VT PATH REMOTE DEFECT INDICATION

Bits [7:4] are used for VT Path APS signalling (APS-V).

Bits [3:1] are for the optional Enhanced VT Path Remote Defect Indication (ERDI-V). Bits 5 to 7 of byte K4 may provide a remote defect indication with additional differentiation between the remote payload defect (LCD), server defects (AIS, LOP), and the remote connectivity defects (TIM, UNEQ). The optional codes from Table 11 will be used. Use of the "010" code to indicate payload defects does not imply a requirement to use the "101" and "110" codes to distinguish between server and connectivity defects.

TABLE 11: K4 (B5-B7) CODING AND INTERPRETATION

B5/B8 OF V5	B6	B7	MEANING	TRIGGERS
0	0	0	No remote defect	No remote defect
0	0	1	No remote defect	No remote defect
0	1	1	No remote defect	No remote defect
0	1	0	Remotepayload defect	LCD(Note 1)
1	0	0	Remote defect	AIS, LOPTIM, UNEQ(or PLM, LCD)(Note 2)
1	1	1	Remote defect	AIS, LOPTIM, UNEQ(or PLM, LCD)(Note 2)
1	0	1	Remoteserver defect	AIS, LOP(Note 3)
1	1	0	Remoteconnectivity defect	TIM,UNEQ

NOTES:

1. *LCD is the only currently defined payload defect and is applicable to ATM equipment only.*
2. *Old equipment may include LCD or PLM as a trigger condition. PLM and UNEQ have previously been covered by SLM.*
3. *Remote server defect and server signal failure are defined in Recommendation G.783.*

For these optional codes, bit 7 is always set to the inverse of bit 6 to allow equipment which supports this feature to identify that it is interworking with equipment that uses the single bit RDI. In such a case, equipment at both ends will interpret only V5.

Bit 0 is reserved for future growth and is treated as Undefined.

TABLE 12: Z7/K4 - VT PATH GROWTH AND VT PATH REMOTE DEFECT INDICATION

7 (MSB)	6	5	4	3	2	1	0 (LSB)
APS-V				ERDI-V			Undefined

MAKE PAYLOAD BLOCK (MKP)

Figure 33 and Figure 34 show the internal workings of the Make Payload block.

FIGURE 33. MKP (MAKE PAYLOAD), ONE OF SEVEN MKG : MAKE VT/TU GROUP

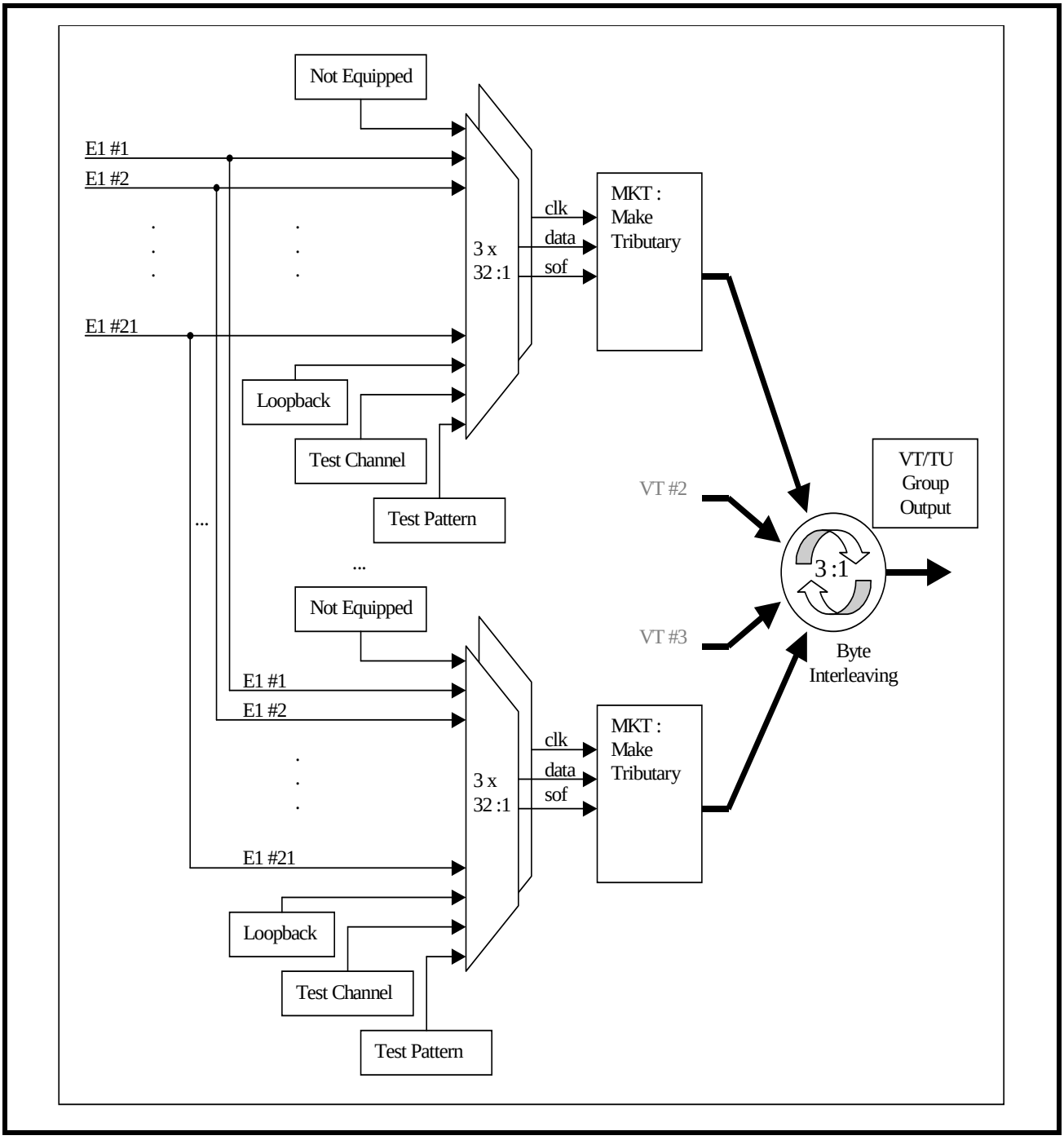
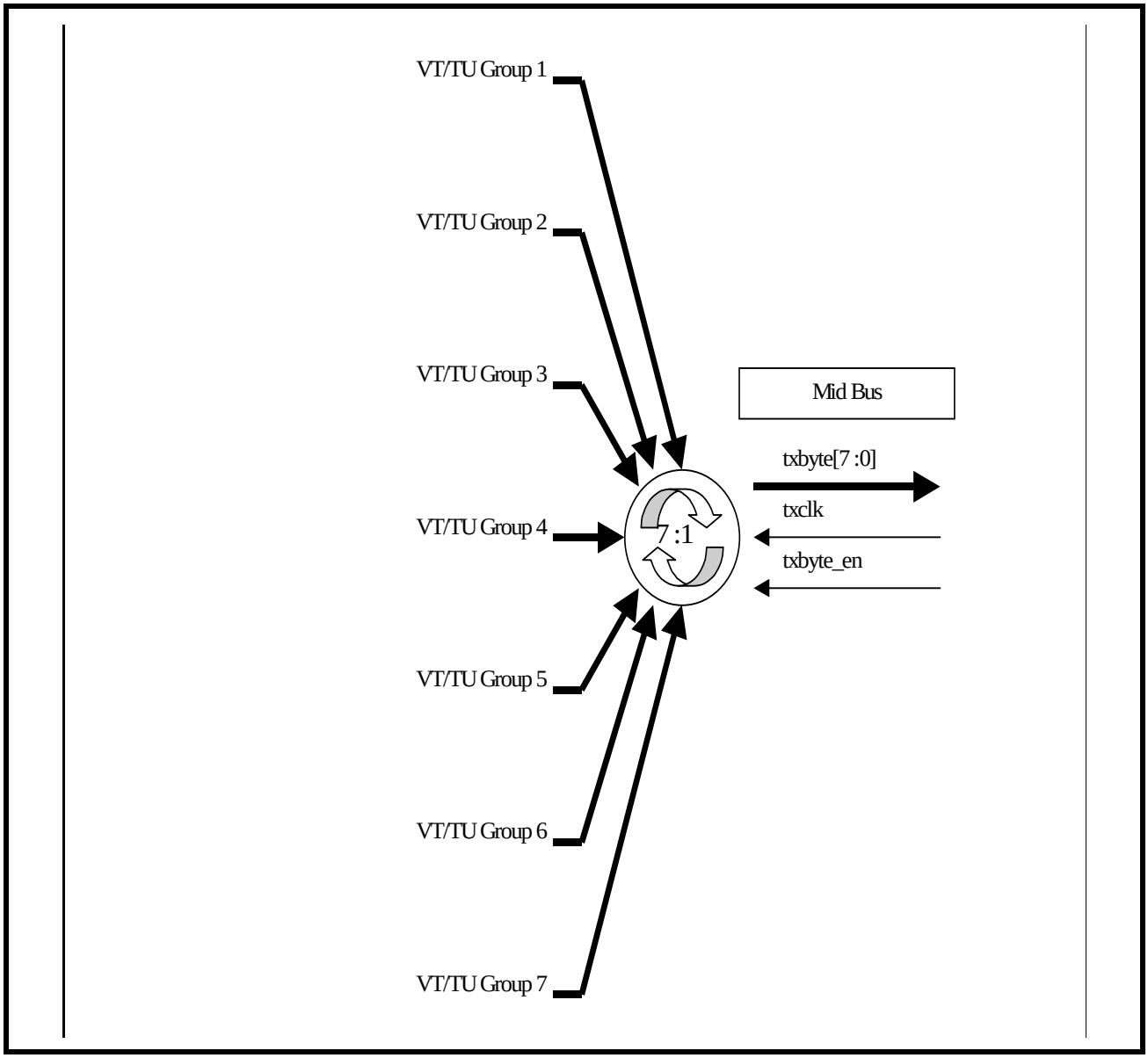


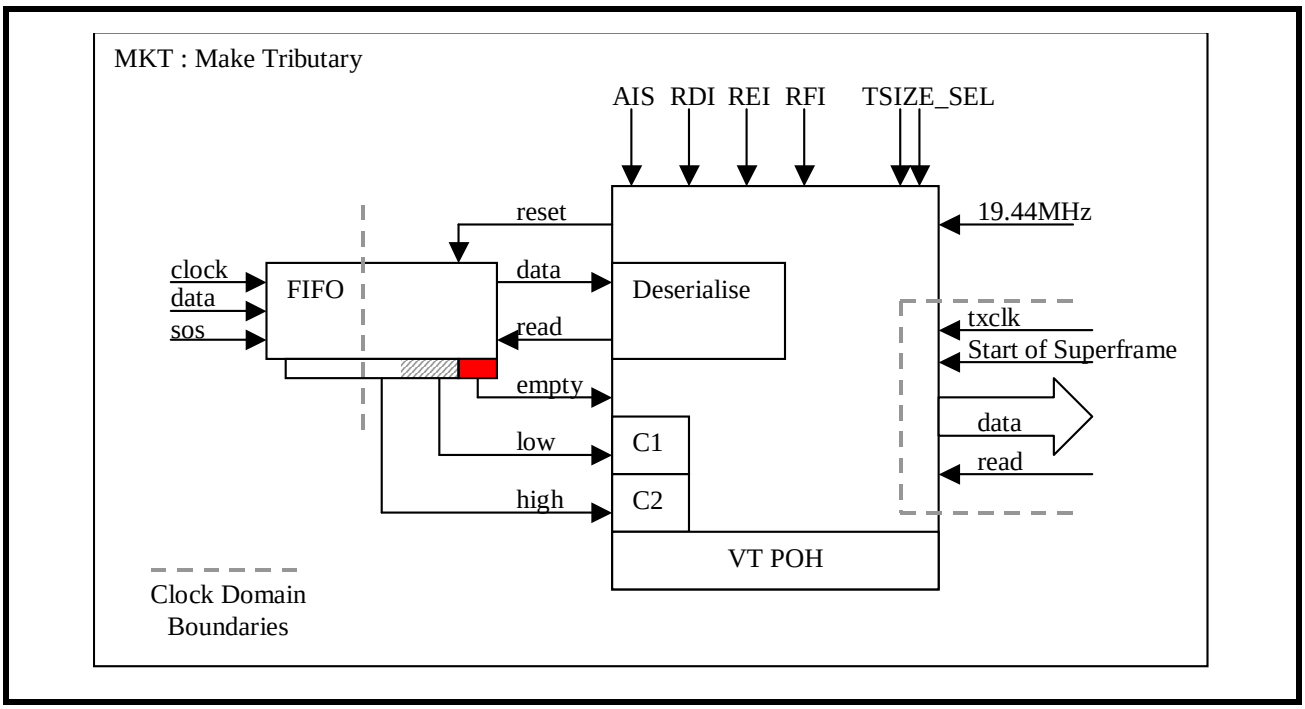
FIGURE 34. MKP (MAKE PAYLOAD), VT/TU GROUP INTERLEAVING.



Make Tributary block (MKT)

Each of the 21 Make Tributary blocks (MKT) illustrated in **Figure 35** takes the output of its channel multiplexer and builds a tributary suitable for byte interleaving into a tributary group. It takes care of deserialization, VT POH generation and stuff bit control. If the Alarm Indication Signal (AIS) is asserted, a tributary made up of all ones is generated.

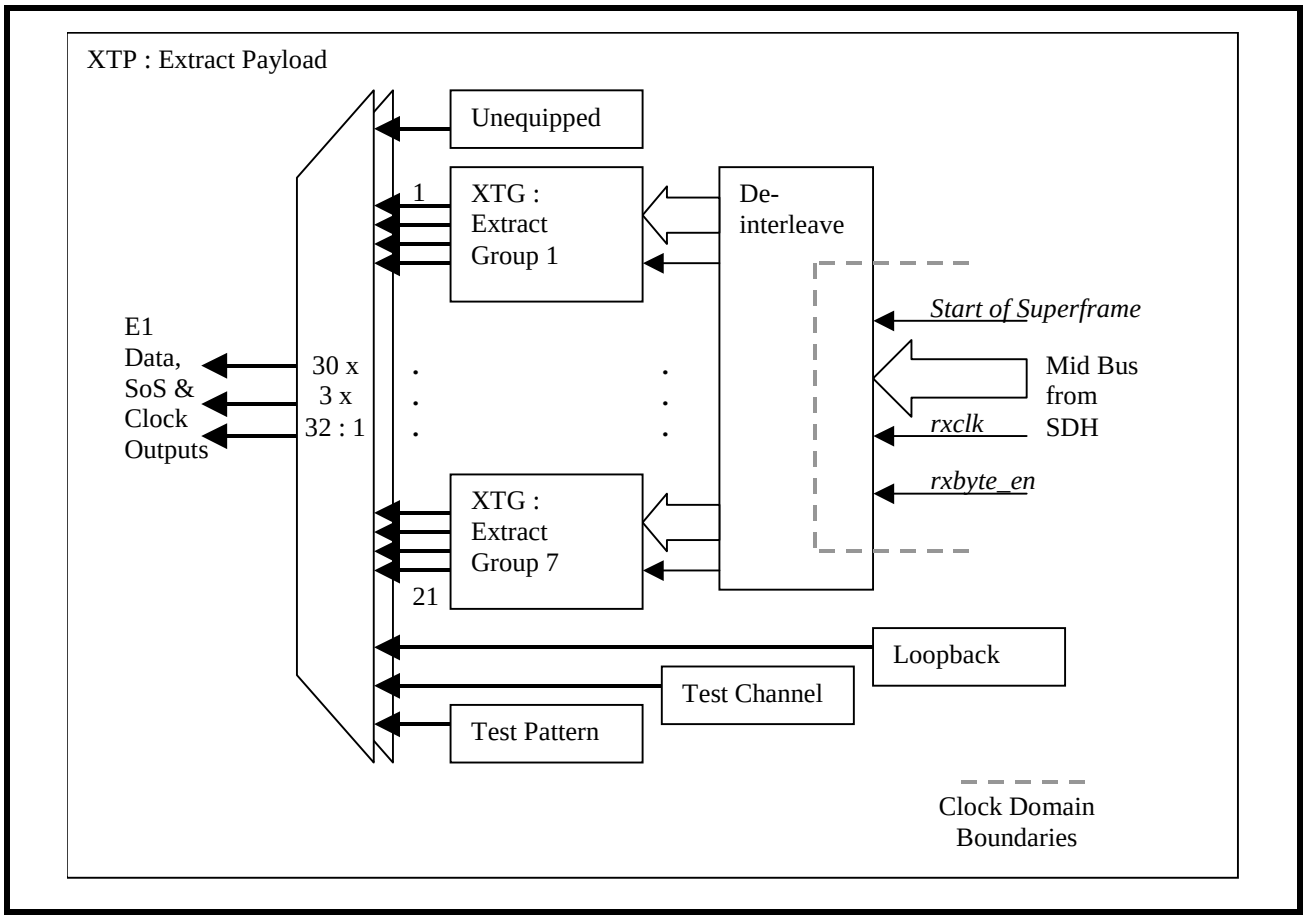
FIGURE 35. MAKE TRIBUTARY (MKT)



Extract Payload block (XTP)

This block, illustrated in Figure 36, extracts the individual E1 channels from the SDH data stream. The seven groups are first de-interleaved, Fixed Stuff columns are removed, and then one to four tributaries are extracted from each group. This block handles the V1-V2 VT Payload Pointer processing, VT POH, and stuff bits.

FIGURE 36. EXTRACT PAYLOAD (XTP)



Test Channel

Two extra E1 channels (one input, the other output) are available to be used as a test channel. The test channel's input and output can be used in the same way as any of the 21 E1 signals' inputs and outputs. They can be mapped into or extracted from the SDH stream, they can be looped back, or fed by or compared to the test pattern generator.

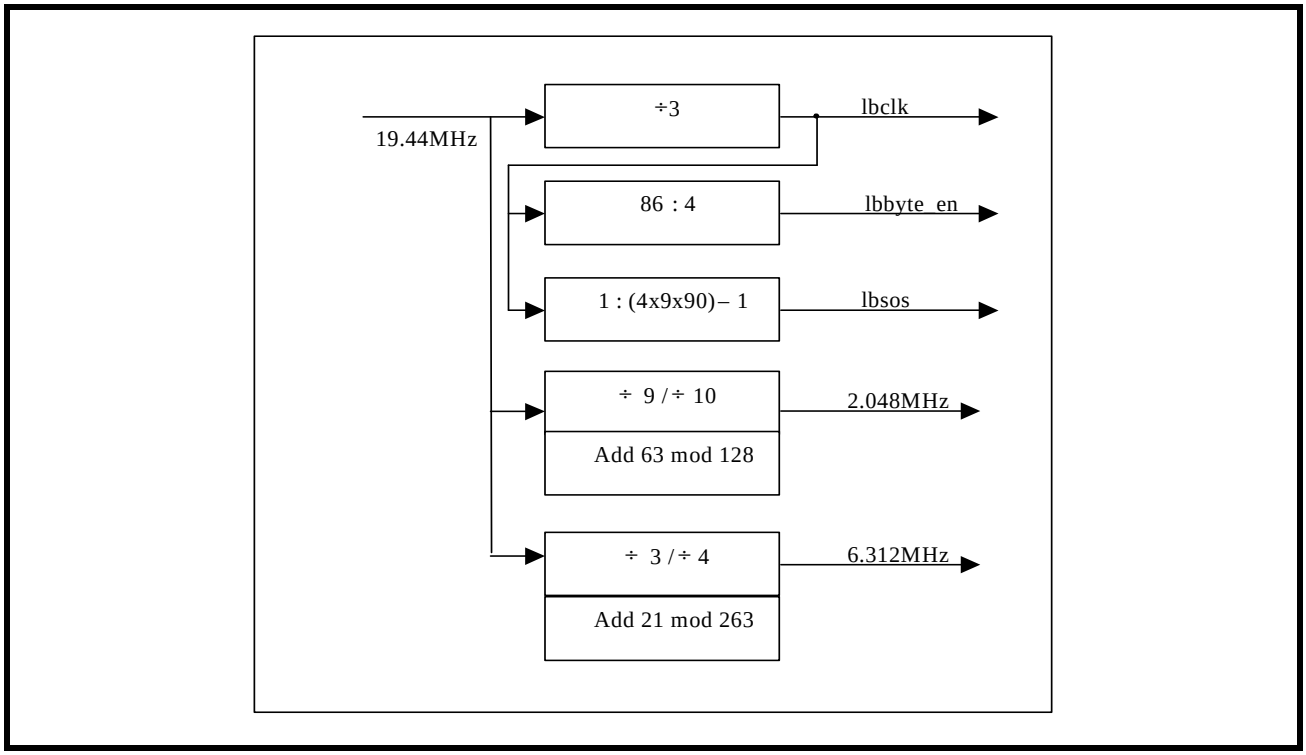
Test Pattern Generator (TPG)

The Test Pattern Generator can generate or compare to a pseudo random test pattern of length 2^{15}-1, a fixed pattern of all zeros, all ones, or alternating ones and zeros as recommended in ITU/CCITT Recommendation O.151. The pseudo random pattern is generated by a fifteen stage shift register whose 14th and 15th stage outputs are added in a modulo-two stage, and the result is fed back to the input of the first stage. The fed back bit is inverted before it is used as the next bit in the pseudo random sequence either for output or to be compared to. The test patterns of correct bit rate is made available to each of the seven groups according to the size of the tributaries assigned to each group. In addition to valid clock and data signals, the TPG generates a valid Start of Superframe Pulse one E1 clock tick wide at appropriate intervals, for synchronous E1 mappings. This will emulate four null signalling bits.

Reference Clocks Generation (RCG)

The Reference Clock Generator block (RCG) divides the 19.44MHz input clock to generate clock signals of precise frequencies and signals used in loopback modes. The SDH loopback clock lbclk is simply a 6.48MHz clock obtained by dividing the input frequency by three. The loopback byte enable signal lbbyte_en is asserted for 86 out of every 90 lbclk clock ticks. The loopback Start of Superframe signal lbsos is a single pulse, one lbclk tick wide that occurs once every 4x9x90 lbclk ticks.

FIGURE 37. REFERENCE CLOCKS GENERATOR (RCG)

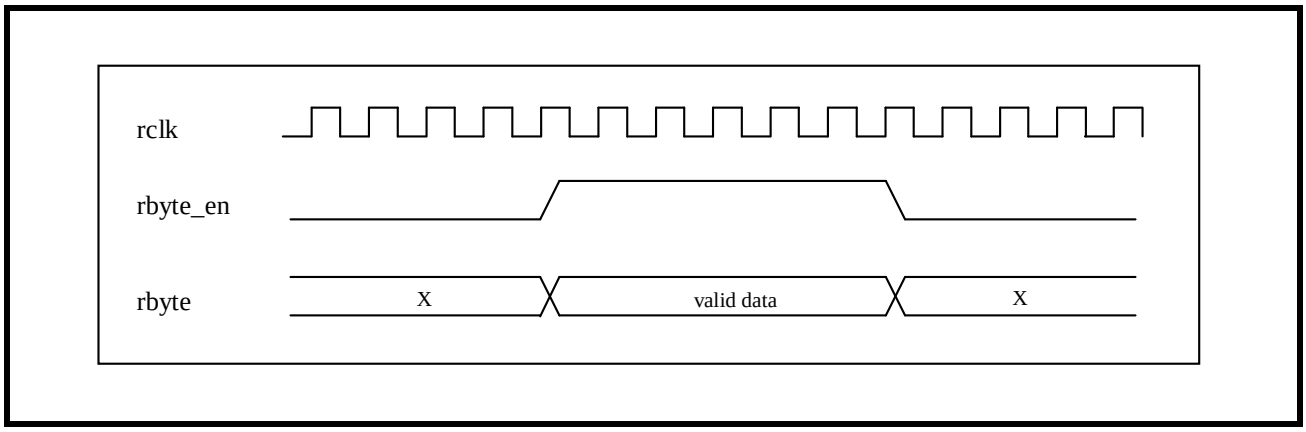


DATA INTERFACE BETWEEN SDH/FRAMER AND MAPPER

The data interface between the SDH and the Mapper blocks consist of three lines/buses in each direction: clk, byte lane, and byte enable. There are 1 byte lanes (8 bits) and 1 byte enable running at a data rate of 6.48MHz.

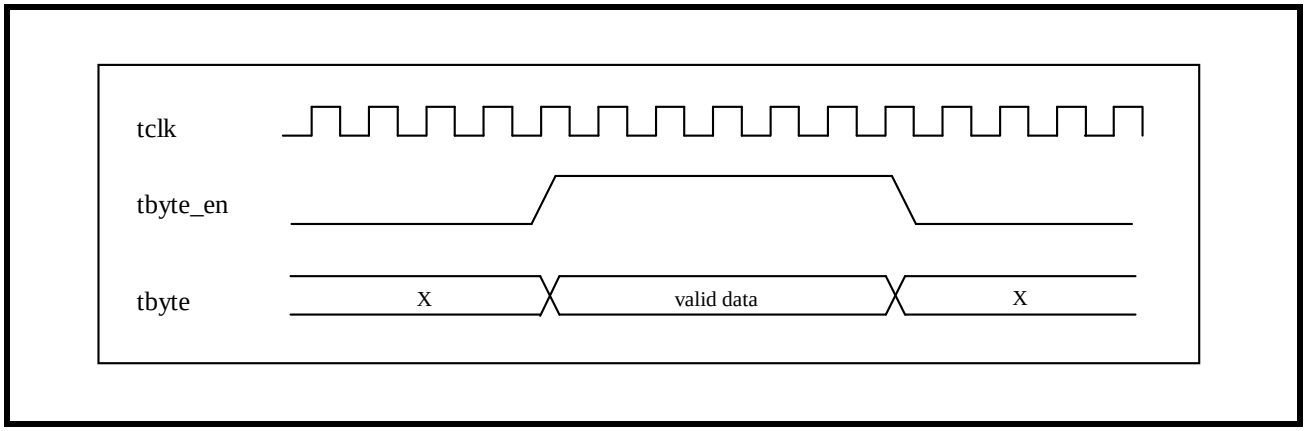
In the receive direction, the SDH payload data is sent to the receive mapper block. Data is presented on the byte lane on the rising edge of rclk with rbyte_en "High" representing the data is valid. The mapper block then fetches the data on the next rising edge of rclk.

FIGURE 38. RECEIVE SDH/FRAMER-ATM INTERFACE



In the transmit direction, the SDH payload data is pulled from the transmit Mapper block. tbyte_en is used as an acknowledge signal indicating that data is recognized. When tbyte_en is asserted "High", data from the Mapper is latched into the SDH block on the next rising tclk edge.

FIGURE 39. TRANSMIT SDH/FRAMERMAPPER INTERFACE

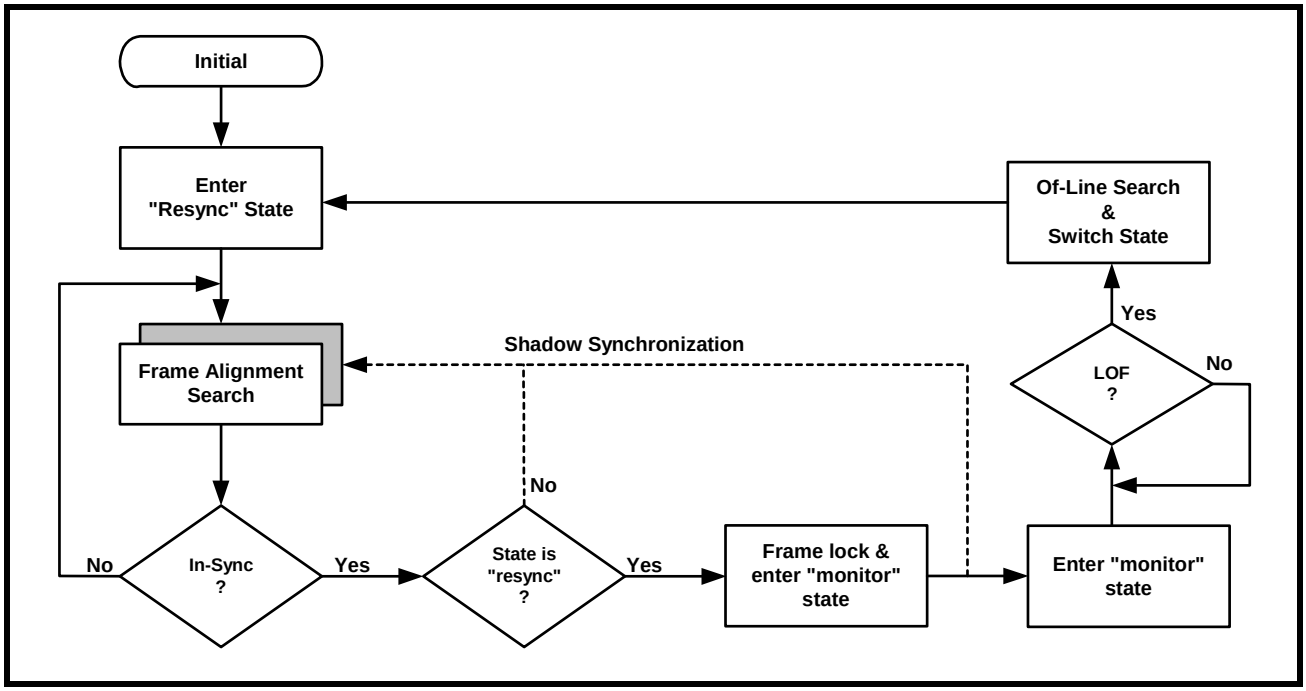


E1 FRAME SYNCHRONIZATION

The E1 framer establishes frame and multiframe boundaries by searching for frame alignment, CRC multiframe alignment, and channel associated signaling multiframe alignment in the incoming PCM data stream, and provides an output clock useful for data conditioning and decoding. User access to the E1 framer is via the microprocessor bus interface. The framer incorporates a robust framing algorithm which prevents false synchronization on patterns that mimic the framing bits.

The E1 framer monitors the incoming data stream from the LIU line interface module for loss of frame, loss of CRC multiframe and CAS multiframe alignment based on user-selectable criteria, and searches for new frame alignment pattern when sync loss is detected. When sync loss is detected, the framer begins an off-line search for the new alignment and shifts into resync mode; all output timing signals remain at the old alignment during this period. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next frame (or multiframe). One frame later, the framer resumes the normal sync monitoring mode and outputs the valid sync signal. The general synchronization flow diagram is illustrated in Figure 40.

FIGURE 40. E1 FRAMER SYNCHRONIZATION FLOW DIAGRAM



FAS Synchronization

Three steps are involved in the synchronization process. The first one is finding FAS frame alignment. The second one searches for FAS using one of two user selectable algorithms as defined in Recommendation G.706. In addition, a two frame check sequence can be added optionally to either one of these two algorithm to provide protection against false frame alignment in the presence of random mimic patterns.

Algorithm 1:

Step 1: Seach for the presence of the correct 7-bit FAS pattern. Go to step 2 if found;

Step 2: Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timslot 0 byte is a one. Go back to step 1 if verification failed; Otherwise, go to step 3;

Step 3: Check if the FAS is present in the assumed timeslot 0 byte of the third frame. Go back to step 1 if failed.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the errored timeslot 0 byte locaiton. If both conditions are met and frame check sequence is enabled, then an additional check sequence is initiated. The check sequence consists of verifying correct frame alignment for an additional two frames.

Step 4: Once the frame alignment is found, check if the FAS is absent in the following frame by verifying the bit 2 of timeslot 0 being a one. If verification failed, go back to step 1.

Step 5: Check that the FAS is present of the next frame. If not, go back to step 1.

The second algorithm is similar to the first one, but adds a one frame hold-off in the second step to begin a new search in the bit immediately following the second (third frame) assumed FAS. This extra frame hold-off is performed only after the condition in step 2 fails to provide a robust algorithm which allows the framer to operate correctly in the presence of fixed timeslot imitating the FAS pattern.

Algorithm 2:

Step 1: Seach for the presence of the correct 7-bit FAS pattern. Go to step 2 if found;

Step 2: Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timslot 0 byte is a one. Go to step 4 if varification failed; Otherwise, go to step 3;

Step 3: Check if the FAS is present in the assumed timeslot 0 byte of the third frame. Go back to step 1 if failed; Otherwise start check sequence if enabled.

Step 4: Wait for assumed FAS in next frame, then go back to step 1.

If both conditions are met and frame check sequence is enabled, then an additional check sequence is initiated. The check sequence consists of verifying correct frame alignment for an additional two frames.

Step 5: Once the frame alignment is found, check if the FAS is absent in the following frame by verifying the bit 2 of timeslot 0 being a one. If verification failed, go back to step 4.

Step 6: Check that the FAS is present of the next frame. If not, go back to step 1.

When synchronization is achieved, the framer monitors alignment signals for errors. A Red Alarm (FASRED) is generated if frame alignment is lost. The criteria for loss of frame alignment in FAS framing is dictated by an E1 Framing Control Register (FCR). The MSB of this register is an RSYNC bit which imposes the framer to restart the resync process even if the frame is currently in sync. This bit will be cleared after the framer resumes its normal sync monitoring mode. The FAS criteria bits specify the number of consecutive erred FAS patterns determining the loss of FAS alignment. Note: Loss of FAS alignment forces loss of CAS and loss of CRC alignment.

It is important to note that the off-line searching is conducted by a shadow synchronizer. The shadow synchronizer continuously searches for the frame alignment even if the framer is in the in-sync state. Once the loss of frame is declared and the resync mode is entered, the framer can shift back into monitor mode by moving to the new alignment at the beginning of the next frame as long as the shadow synchronizer is in-sync. This feature dramatically reduces the reframe time required.

CRC Synchronization

After the FAS frame alignment is declared, the second step is to find the CRC-4 multiframe alignment. This is done by observing whether the international bits (bit 1 of timeslot 0) of non-FAS frames match the CRC multiframe alignment pattern. Multiframe alignment is declared if at least the valid CRC multiframe alignment signals are observed within 8ms. The CRC synchronization logic will force a FAS frame search when CRC multiframe alignment has not been found for 8ms.

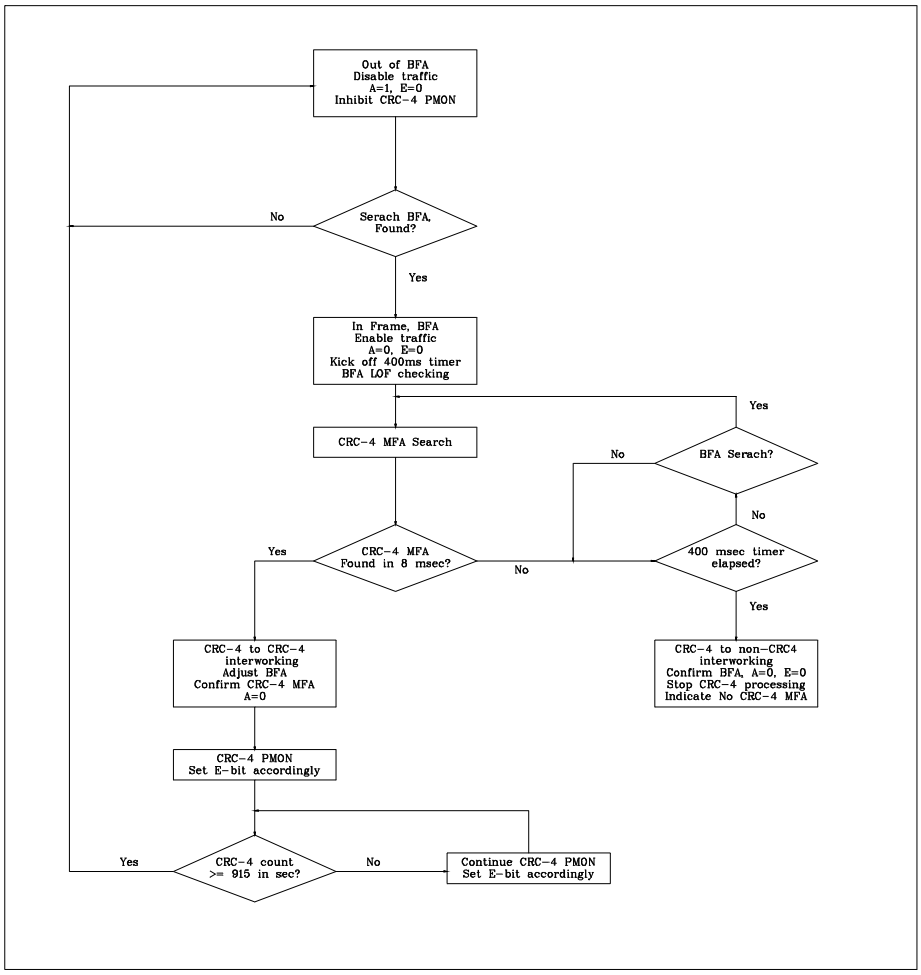
Once the CRC multiframe alignment is found, the Out Of CRC MultiFame alignment indication is cleared. The CRC synchronizer monitors the multiframe alignment signal, indicates errors occurring in the 6-bit CRC pattern, and indicates the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The loss of CRC multiframe alignment is declared if consecutive CRC multiframe alignment signals have been received in error.

When synchronization is achieved, the framer monitors the multiframe alignment signals for errors. A CRC LOF indication is set to "1" if frame alignment is lost. The criteria for loss of CRC multiframe alignment is dictated by CRCC bits in E1 Framing Control Register.

Annex B compliance

When ModEnb is "1", G.706 Annex B modified CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400ms while the basic frame alignment signal is present, it is assumed that the remote end is a non-CRC-4 equipment. The flow chart in **Figure 41** demonstrates this algorithm.

FIGURE 41. FLOW OF CRC-4 MULTIFRAME ALIGNMENT FOR INTERWORKING



A 400ms CRC-4 multiframe alignment search period is applied for interworking detection. The 400 msec timer is triggered on the initial recovery of basic frame alignment and is not reset until the loss of basic frame alignment occurs. A re-search for FAS will be initiated if CRC-4 multifame alignment can not be found in 8ms and will not reset the 400ms timer or invoke the consequent actions associated with loss of FAS. All subsequent searches for CRC-4 multiframe alignment are associated with each basic FAS found. In order to maintain no disturbance to traffic during the 400ms CRC-4 multiframe search, traffic should be allowed through with synchronization to the initially determined primary basic frame alignment sequence. If a CRC-4 multiframe alinment signal is found befoe the 400ms timer elapses, then the basic FAS associated with the CRC-4 multiframe alignment signal should be the one chosen, i.e. the primary basic FAS should be amended accordingly if the basic FAS alignment changed. If a CRC-4 multiframe alignment sequence can not be found in 400ms, it should be concluded that a condition of interworking between equipments with and without a CRC-4 capability exist, so the traffic should be maintained to the initially determined FAS alignment.

If the path is reconfigured at any time, then it is assumed that the new pair of path will need to re-establish the complete framing process, i.e. the algorithm is reset.

Consequent actions are taken while a non-CRC-4 remote side is detected:

- The Framer will provide an indication that there is no incoming CRC-4 multiframe alignment signal
- The Framer will inhibit further CRC-4 processing
- The Framer will continue to transmit CRC-4 data to the remote side with both E bits set to zero

In this modified framing mode, the framer always sets the return E bits to zero until the interworking relationship has been established. If CRC-4-to-CRC-4 interworking is established, then normal CRC-4 processing of erred CRC-4 block data should commence. If CRC-4-to-non-CRC-4 interworking is established, the E bits should remain at 0.

CAS Synchronization

After the FAS frame alignment is declared, the third step is to find CAS multiframe alignment. Two user-selectable algroithms are available.

Algorthm 1 monitors the sixteenth timeslot of each frame and declares CAS multiframe alignment when 15 consecutive frames with bits 1-4 of timeslot 16 not containing the alignment pattern are observed to precede a frame with timeslot 16 containing the correct alignment pattern.

Algorthm 2 monitors the sixteenth timeslot of each frame and declares CAS multiframe alignment when non-zero bits 1-4 of timeslot 16 are observed to precede a timeslot 16 containing the correct alignment pattern.

Once the CAS multiframe alignment is found, the Out Of CAS MultiFame alignment indication is cleared. The CAS synchronizer monitors the multiframe alignment signal, indicates errors occurring in the 4-bit alignment pattern, and indicates the debounced value of the remote signaling multiframe alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe).

When synchronization is achieved, the framer monitors multiframe alignment signals for errors. The CAS LOF indication turns on if frame alignment is lost. The criteria for loss of CRC multiframe alignment is dictated by the CASC bits in the E1 Framing Control Register.

FRAME COUNTERS AND TIMING GENERATION

Receive Frame and Multiframe counters and timing generators provide timing for frame and multiframe alignment, CRC-4 check, signaling extraction, facility data link extraction, yellow alarm, and all the timing for per-channel parameter fetch. The data extracted from this timing is placed into the appropriate internal storage elements for the microprocessor to access. The information extracted is not valid unless the receive module has achieved valid synchronization.

CRC-4 VERIFICATION

The CRC verification is performed by calculating the 4-bit CRC checksum for each incoming sub-multiframe and comparing this result to the received CRC remainder bits in the subsequent sub-multiframe. The CRC errors are accumulated over one second intervals. Optionally, a CRC frame resync can be initiated when 915 or more CRC errors occur in one second. The number of CRC errors accumulated during the previous second is available by reading the E1 Receive Synchronization Bit Error Counter.

ALARM AND ERROR INDICATION

The Alarm indication logic examines the incoming E1 data for alarm conditions. When the change of an alarm condition is detected, corresponding bits are set in the Alarm and Error Status Register. The Alarm and Error Interrupt Enable Register is used to select the events that generate interrupts on the microprocessor interrupt pin when their state changes.

LOF (Red Alarm) Defect/Alarm

When DEFDET=1, the Loss Of Frame defect is detected when "FASC" (in framing control register) consecutive incorrect frame alignment signals have been received (default is 3 to comply with G.706). It is cleared when 2 consecutive FAS's are detected.

When DEFDET = 0, The red alarm is detected by monitoring the occurrence of Loss Of Frame (LOF) over a 4 ms interval. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 25 valid intervals have been accumulated. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

TRANSMIT SLIP BUFFERING

The Voyager-Lite has two-frame (512 bits) elastic stores. This store can be enabled or disabled via programming bits SB_ENB in the Slip Buffer Control and Status Register (SBCSR). If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. If the slip buffer is bypassed (SB_ENB[1:0] = 00 or 11), the slip buffer is used as a regular JA buffer. If SB_ENB = 2, the slip buffer is put into a FIFO mode. In the FIFO mode, the slip buffer is acting like a standard first-in-first-out storage. A fixed read and write latency is maintained in a programmable fashion controlled by the FIFO Latency Register. However, the user should assume the responsibility to phase lock the input clock to the receive clock to avoid either overrun or under-run. A Slip Buffer Control & Status register is used to control the slip buffer operations and control interrupts and report its status.

4.11 E1 PHY LOOPBACK DIAGNOSTICS

This section provides some architectural views and implementation details regarding to the system level integration and performance.

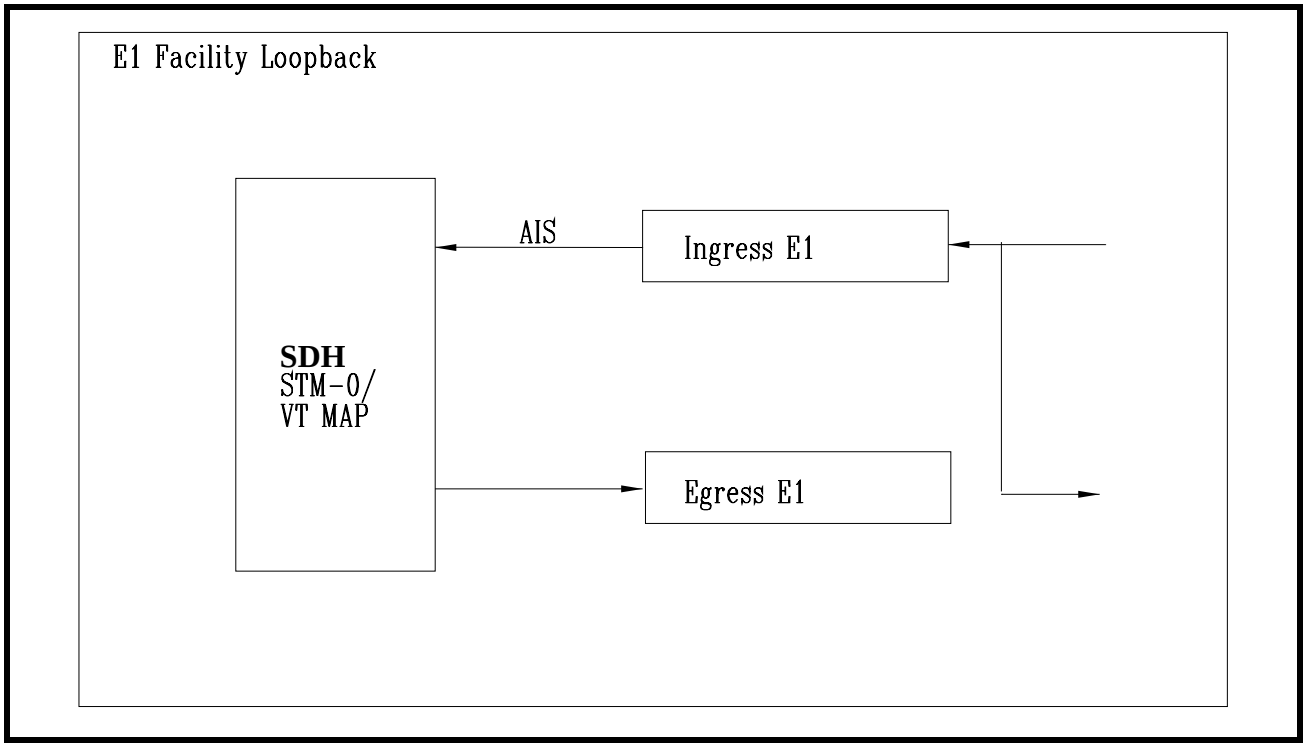
4.11.1 E1 LOOPBACKS

Various controls in the VT Mapper module and E1 framer module allow Voyager-Lite to conduct many types of loopbacks for supporting system diagnosis. Three of them are explained here: E1 facility loopback, E1 facility I/O loopback and E1 module loopback.

E1 facility loopback

Figure 42 shows this type of loopback by sending the ingress E1 inputs back to egress E1 outputs.

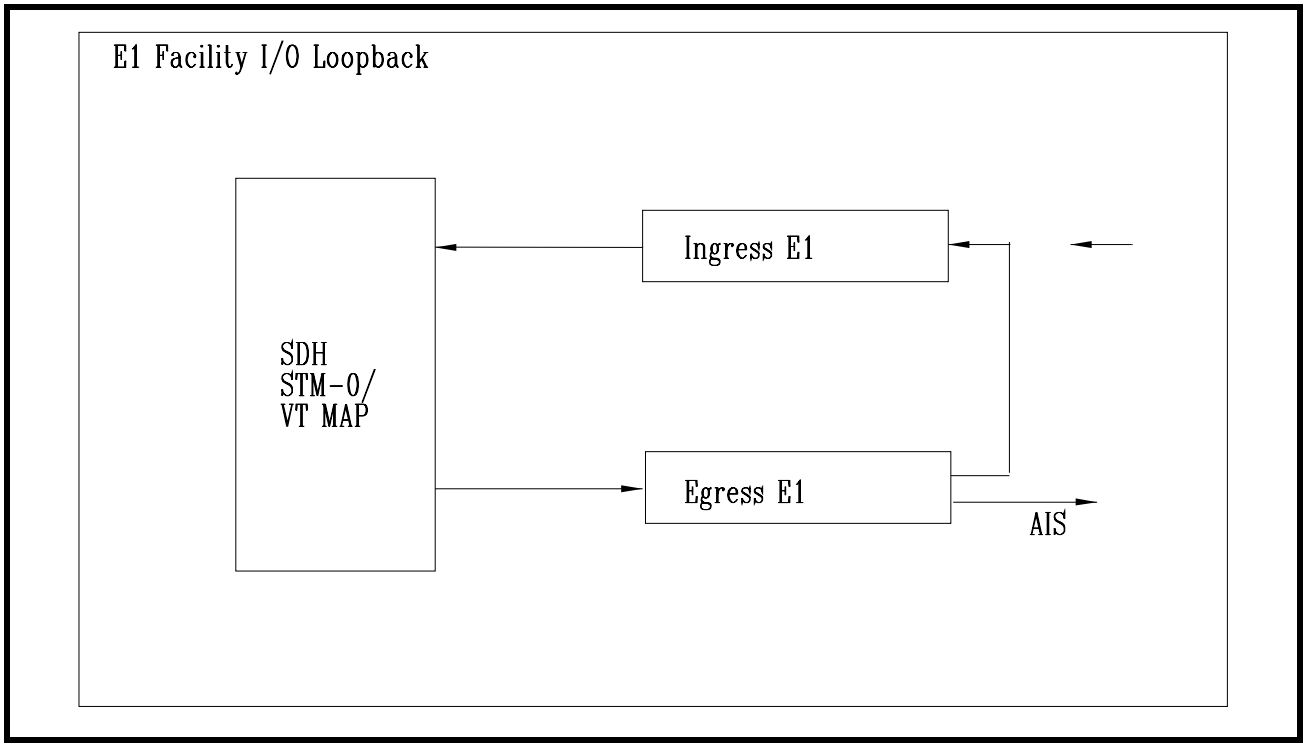
FIGURE 42. E1 FACILITY LOOPBACK



4.11.2 E1 facility I/O loopback

Figure 43 shows the this type of loopback by connecting the egress E1 outputs to the ingress E1 inputs.

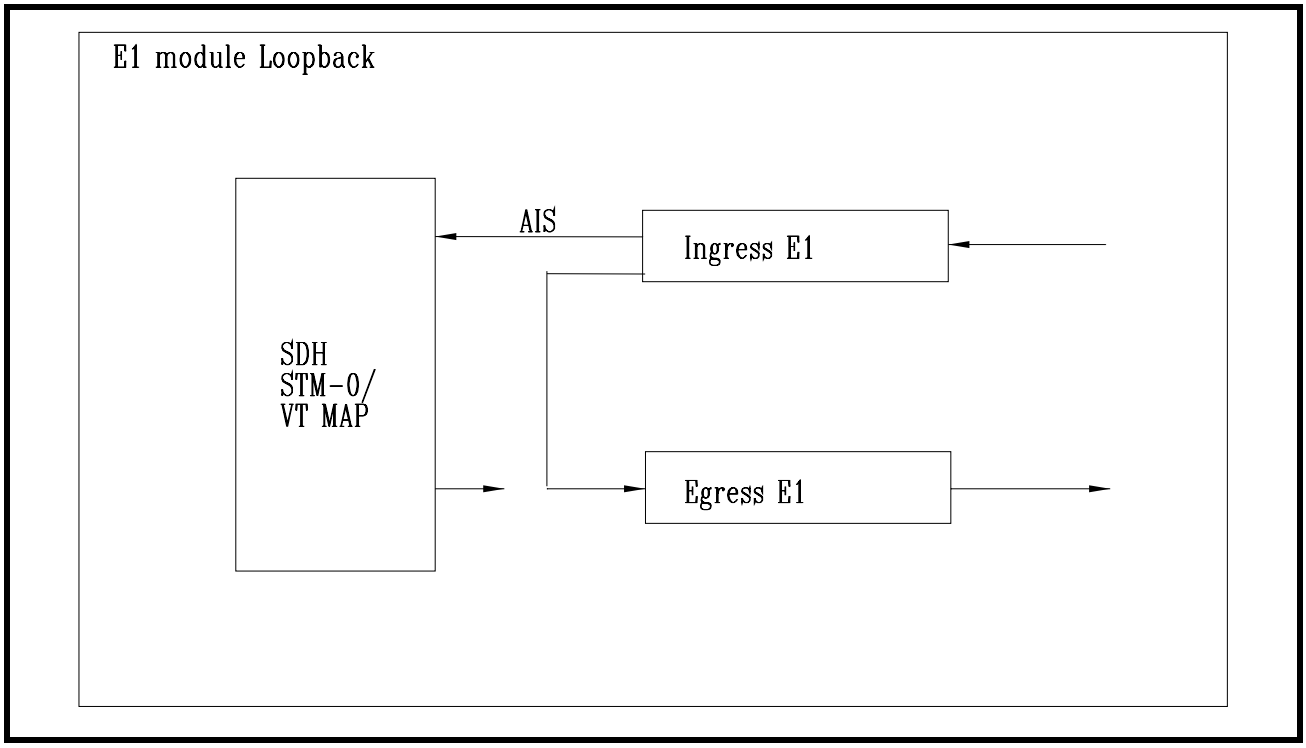
FIGURE 43. E1 FACILITY I/O LOOPBACK



4.11.3 E1 module loopback

Figure 44 shows the this type of loopback by sending the ingress E1 framer outputs back to egress E1 framer inputs.

FIGURE 44. E1 MODULE LOOPBACK



4.11.4 ALARM AND AUTO AIS

Voyager-Lite provides the capability to insert alarm, especially AIS, automatically into the data down stream while exceptional conditions occur. **Figure 45** shows the basic structure of the Auto AIS insertion. Note: Each condition is optional

FIGURE 45. E1 AUTO AIS INSERTION

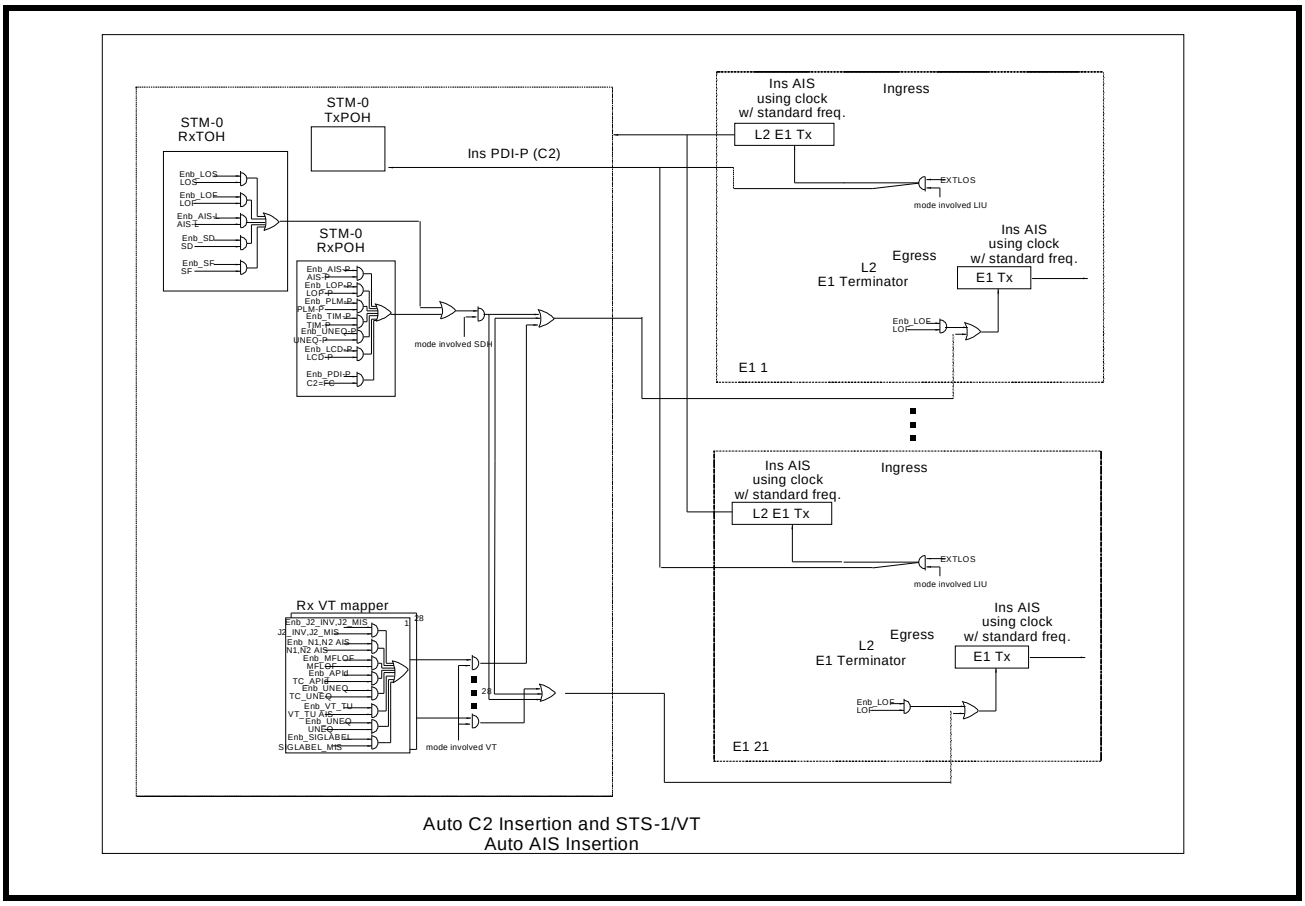


TABLE 13: E1 TO STM-0 - RESPONSE TIME < 125 US

E1 CONDITION	STM-0 RESPONSE
LOS	E1-AIS,PDI-P/AIS-P
LOF	PDI-P/AIS-P
AIS-L	PDI-P/AIS-P

TABLE 14: STM-0 TO E1 - RESPONSE TIME < 125 USEC

STM-0 CONDITION	E1 RESPONSE	STM-0 RETURN PATH
LOS	E1 AIS	RDI-L, RDI-P
LOF	E1 AIS	RDI-L, RDI-P
AIS-L	E1 AIS	RDI-L, RDI-P

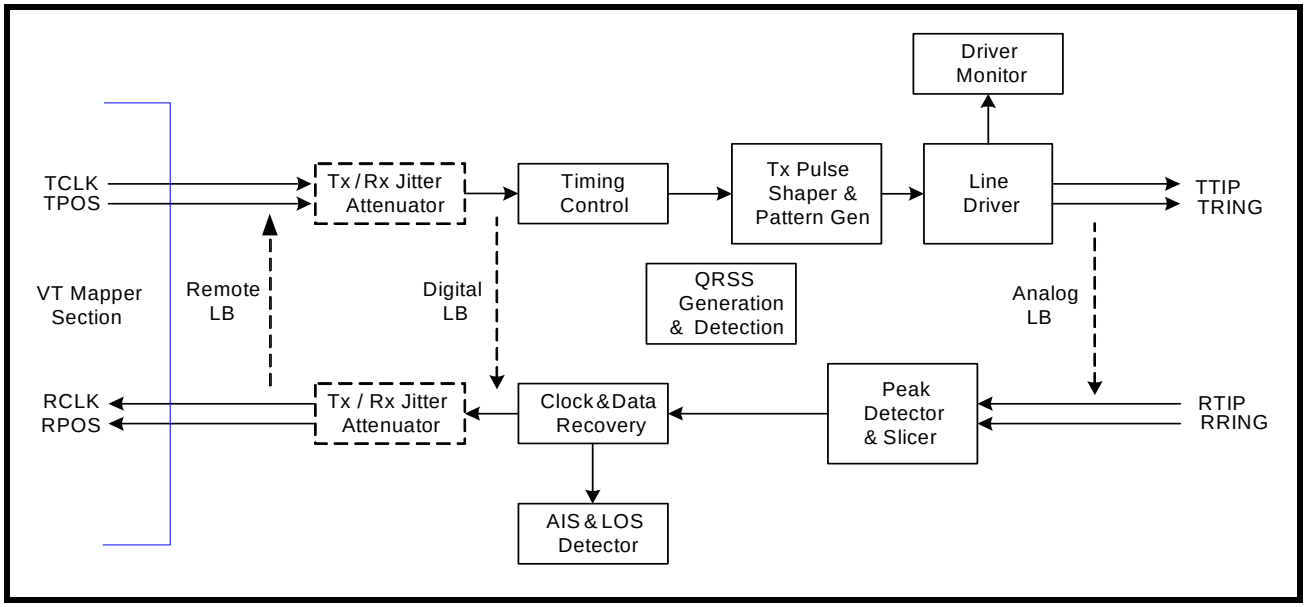
TABLE 14: STM-0 TO E1 - RESPONSE TIME < 125 USEC

STM-0 CONDITION	E1 RESPONSE	STM-0 RETURN PATH
LOP-P	E1 AIS	RDI-P
AIS-P	E1 AIS	RDI-P
UNEQ-P	E1 AIS	RDI-P
PLM-P	E1 AIS	RDI-P
TIM-P	E1 AIS	RDI-P

5.0 ANALOG FRONT END / LINE INTERFACE UNIT (LIU) SECTION

The analog front end section is a fully integrated, 21-channel E1 LIU for 75Ω or 120Ω applications. With internal termination and an option for high impedance, the LIU uses one bill of materials to support Coax or Twisted Pair medium and supports 1:1 or 1+1 redundancy. Each transmitter has an optional Jitter Attenuator and can provide basic diagnostic features that can be used to send data to the line interface. Each receiver accepts standard E1 pulses, provides clock and data recovery, basic diagnostic detection, and an optional Jitter Attenuator before presenting data to the VT Mapper section. A simplified block diagram of the LIU section can be seen below.

FIGURE 46. SIMPLIFIED BLOCK DIAGRAM OF THE LIU SECTION



5.1 TRANSMIT LINE INTERFACE UNIT

5.1.1 Jitter Attenuator

The LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The jitter attenuator can be selected in the transmit path with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady E1 output. The maximum gap width that the jitter attenuator can accept without a disruption in data flow is shown below.

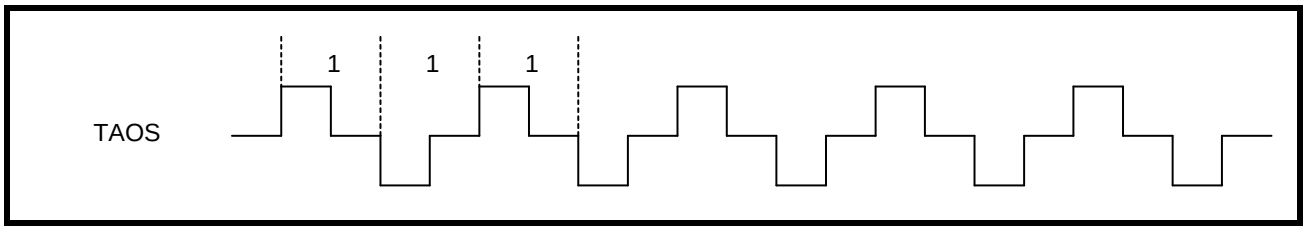
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator can be selected in the receive path. See the Receive LIU Section of this datasheet.*

5.1.2 TAOS (Transmit All Ones)

The LIU section has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data present on its digital inputs from the VT Mapper section. **Figure 47** is a diagram showing the all ones signal at TTIP and TRING.

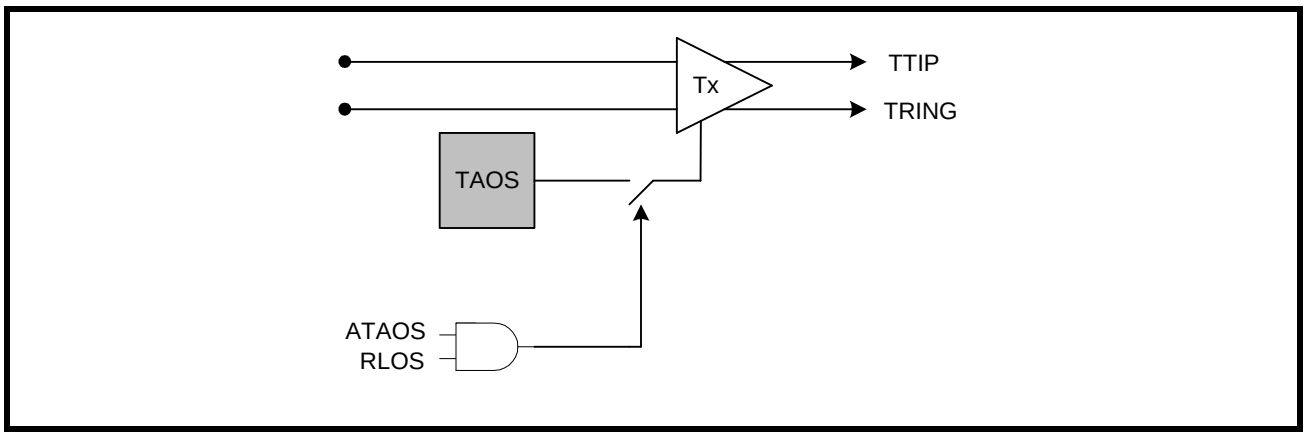
FIGURE 47. TAOS (TRANSMIT ALL ONES)



5.1.3 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in **Figure 48**.

FIGURE 48. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



5.1.4 QRSS/PRBS Generation

The LIU section can transmit a QRSS/PRBS random sequence to a remote location from TTIP/TRING. To select QRSS or PRBS, see the register map for programming details. The polynomial for each selection is shown below.

RANDOM PATTERN	E1
QRSS	$2^{20} - 1$
PRBS	$2^{15} - 1$

5.1.5 Transmit Pulse Shaper and Filter

If TCLK is not present from the VT Mapper section, pulled "Low", or pulled "High" the transmitter outputs at TTIP/TRING will automatically send an all ones or an all zero signal to the line by programming the appropriate global register. By default, the transmitters will send all zeros. To send all ones, the TCLKCNL bit must be set "High".

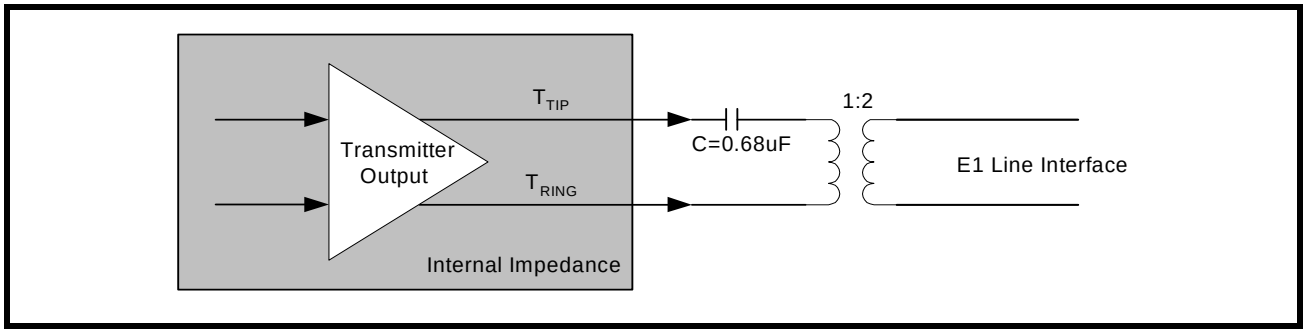
5.1.6 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at the TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

5.2 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for E1 twisted pair or E1 coaxial cables. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for 75Ω and 120Ω reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68µF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in Figure 49.

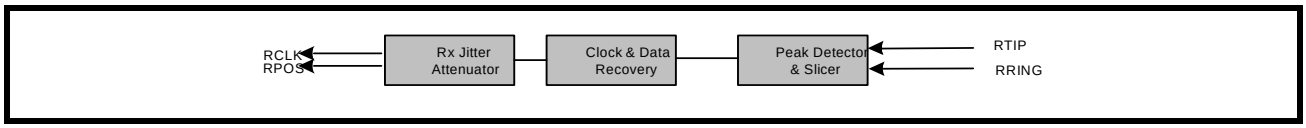
FIGURE 49. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



5.3 Receive path line interface

The receive path of the LIU section consists of 21 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS outputs which are then sent to the VT Mapper interface internal to the chip. A simplified block diagram of the receive path is shown in Figure 50.

FIGURE 50. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



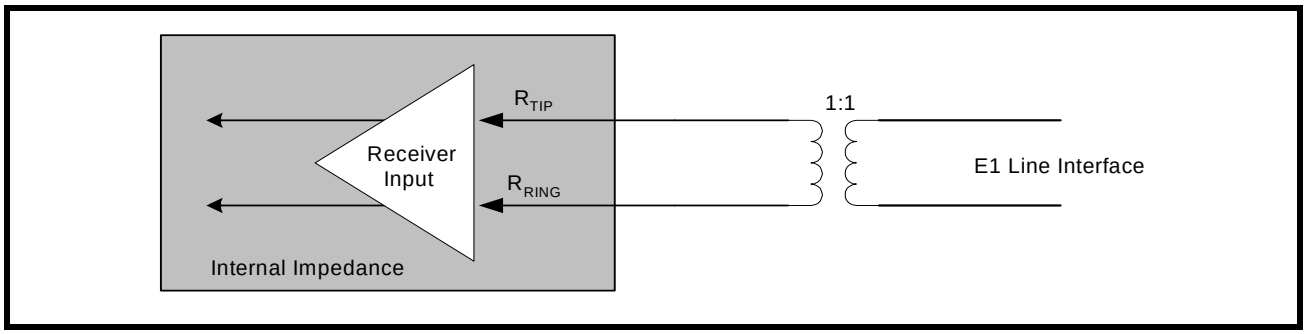
5.3.1 Line Termination (RTIP/RRING)

The input stage of the receive path accepts standard E1 twisted pair or coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for 75Ω and 120Ω operation reducing the number of external components necessary in system design. The receive termination impedance (along with the transmit impedance) is selected by programming TERSEL to match the line impedance. Selecting the internal impedance is shown below.

TERSEL	LINE TERMINATION
0	75Ω
1	120Ω

The LIU section has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). See Figure 51 for a typical connection diagram using the internal termination.

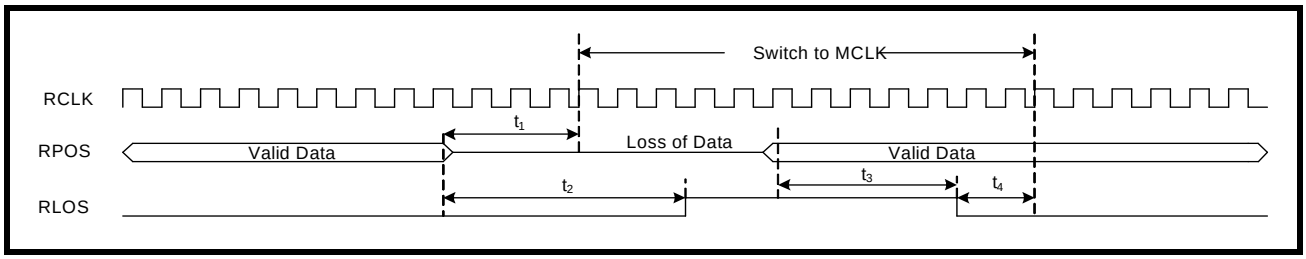
FIGURE 51. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



5.3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel E1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock (64 x E1) as its reference (MCLK). Once, RLOS is cleared, the recovered line clock switches back to RCLK. See **Figure 52** for the detailed timing specifications.

FIGURE 52. RECOVERED LINE CLOCK PLL TIMING



PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Switching time from RCLK to MCLK	t_1			14.6	µS
RLOS declares Loss of Signal	t_2		See Note 2.		
RLOS clears Loss of Signal	t_3		See Note 2		
Switching time from MCLK to RCLK	t_4			18.1	µS

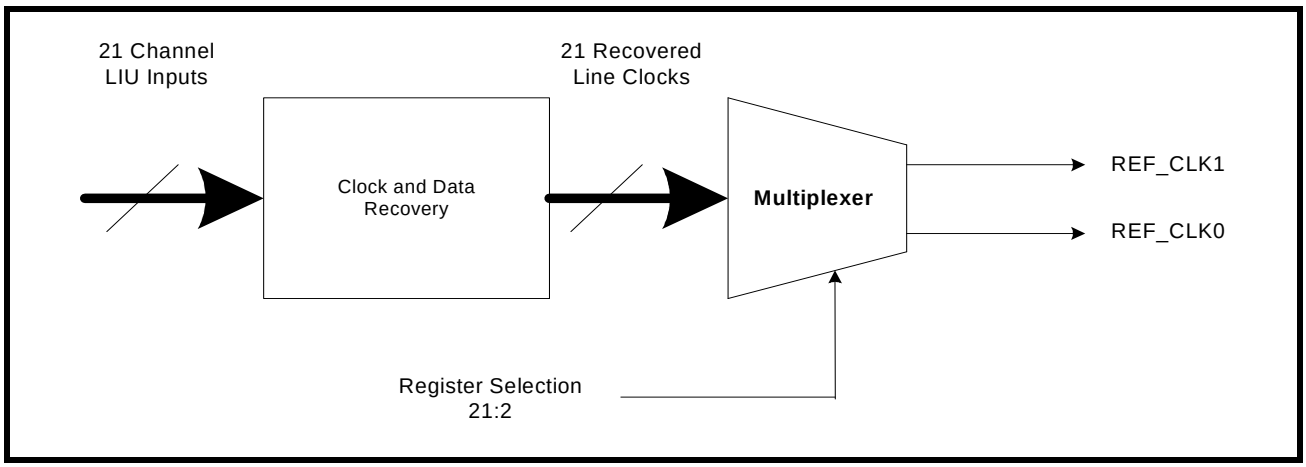
NOTE: *1. VDD=3.3V ±5%, T_A=25℃, Unless Otherwise Specified*

NOTE: *2. RLOS declaration and clearance depends on which mode is selected. The LIU supports both G.775 and ETSI-300-233. Refer to the register map for more details.*

5.3.3 Recovered Line Clock Outputs

There are two output pins that can be used to select among the 21 Recovered Line Clock signals. These signals can be used as a timing reference relative to the two channels chosen. The pins are REF_REC1 and REF_REC0.

FIGURE 53. REF_REC[1:0] RECOVERED LINE CLOCK SELECTION TO OUTPUT PINS



5.3.4 RLOS (Receiver Loss of Signal)

The LIU section supports both G.775 or ETSI-300-233 RLOS detection.

In G.775 mode, RLOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode, the device declares RLOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits RLOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window.

5.3.5 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS. By default, EXLOS is disabled and RLOS operates in normal mode.

5.3.6 Jitter Attenuator

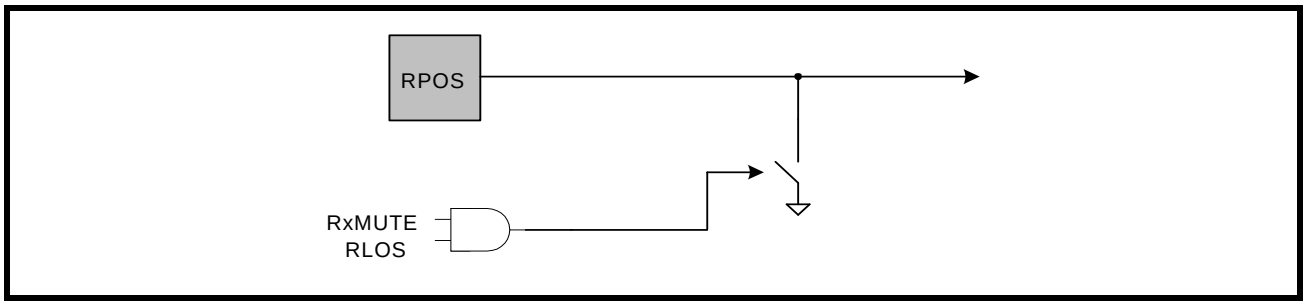
The jitter attenuator reduces phase and frequency jitter in the recovered clock if it is selected in the receive path. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled in the receive path. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: *If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the jitter attenuator can be selected in the transmit path to smooth out the gapped clock. See the Transmit LIU Section of this datasheet.*

5.3.7 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull RPOS "Low" to prevent data chattering to the internal connection to the VT Mapper section. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in **Figure 54**.

FIGURE 54. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION



6.0 MEMORY AND REGISTER MAP

This section provides a complete list of the Voyager-Lite register address map as an over view followed by a full description of each register.

6.1 MEMORY MAPPED I/O ADDRESSING

In order to support a multiple channel implementation, maintain rich user controlled features, and provide future scalability without sacrificing performance for microcontroller access, Voyager-Lite chooses an addressing scheme to channelize the access for the microcontroller interface. This mapping scheme was chosen such that Voyaer-Lite is compatible with its 28 Channel predecessor, Voyager XRT86SH328 which also supports DS1, DS-3, M13 Mux, STS-1/STS-3 SONET Framer/VT Mapper and many other features.

TABLE 15: CHANNEL MAPPING SCHEME

N	CHANNELS
1-3	Channel 1 through Channel 3
5-7	Channel 4 through Channel 6
9-11	Channel 7 through Channel 9
13-15	Channel 10 through Channel 12
17-19	Channel 13 through Channel 15
21-23	Channel 16 through Channel 18
25-27	Channel 19 through Channel 21

6.2 OVERVIEW OF CONTROL REGISTERS

TABLE 16: MEMORY MAP - E1 FRAMERS

ADDRESS	CONTENTS
0x0001 - 0x004F	SDH Operation Control
0x0202 - 0x027F	Receive TOH Block
0x0281 - 0x02F3	Receive POH Block AU-3 ***NOTE:*** *When 0x02 is replaced with 0x05, the part is processing AU-4. (0x0581 - 0x05F3)*
0x0700 - 0x0753	Transmit TOH Block
0x0781 - 0x07D3	Transmit POH Block AU-3 ***NOTE:*** *When 0x07 is replaced with 0x0A, the part is processing AU-4. (0x0A81 - 0x0AD3)*
0xN000 - 0xN011	E1 Line Interface Unit
0xN100 - 0xNB01	E1 Receive Synchronizer Framer
0xNC03 - 0xNF3F	VT Mapping Operation Control

6.3 SDH Operation Control Register Descriptions

TABLE 17: INTERRUPT TYPE SELECT (ITS 0X0001H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					INT_SEL	CLEAR_INT	INT_GEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Interrupt Type Select:

This bit is used to select between Reset-Upon-Read or Write-1-to-Clear

- 0 - RUR
- 1 - WC

BIT 1 - Clear Interrupt Enable After Read

This bit is used to select the Auto-Clear function that will reset all the interrupt enable bits back to their default values.

- 0 - Interrupt enable bit is not cleared after status reading.
- 1 - Interrupt enable bit is cleared after status reading.

BIT 0 - Interrupt Generation Enable

This bit is used to select between an interrupt generation or status polling (No INT) environment.

- 0 - Status Polling
- 1 - Interrupt Generation Enabled

TABLE 18: RECEIVE STM CLOCK DETECT (RSTMCD 0X0003H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	RxSCLKDET	Reserved					SDH_RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Receive STM-x Clock Detect

This bit allows the Transmit Clock Output to be looped back to the Receive Clock Input in the event that the receive clock is missing.

- 0 - Disabled
- 1 - Enabled

BIT [5:1] - Reserved

BIT 0 - SDH Block Software Reset

This bit is used to reset the internal circuitry of the entire SDH blocks to their default state. This bit does NOT reset any register bits.

- 0 - Normal Operation
- 1 - SDH Software Reset

TABLE 19: DEVICE ID REGISTER (DEVID 0X0004H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DEVID[7:0]							
RO	RO	RO	RO	RO	RO	RO	RO
0	1	0	1	0	0	0	1

BIT [7:0] - Device ID

The contents of this Read Only register should always be set to 0x51h. The purpose of this register is for identification only.

TABLE 20: REVISION ID REGISTER (REVID 0X0005H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
REVID[7:0]							
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	1

BIT [7:0] - Device ID

The contents of this Read Only register should be set to 0x01h for revision A silicon. The purpose of this register is for revision identification only.

TABLE 21: TELECOM BUS PARITY ENABLE (TBPE 0X000BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved							TBPINTEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Reserved

BIT 0 - Telecom Bus Parity Interrupt Enable

This bit is used to enable parity interrupt while configured to operate in the telecom bus mode.

- 0 - Disabled
- 1 - Parity Interrupt Enabled

TABLE 22: TELECOM BUS PARITY ERROR ENABLE (TBPEE 0X000FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved							TBPERR_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Reserved

BIT 0 - Telecom Bus Parity Error Interrupt Enable

This bit is used to enable parity interrupt while configured to operate in the telecom bus mode.

- 0 - Disabled
- 1 - Parity Error Interrupt Enabled

TABLE 23: OPERATION BLOCK INTERRUPT REGISTER 1 (OPIR1 0X0012H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OP_CNTL	Reserved	VTMAPPER	Reserved	E1	Reserved	RXLIU	TXLIU
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT 7 - Operation control interrupts including Telecom bus interrupts

Operation control block interrupt for all interrupts in operation control register address map including telecom bus and APS interrupts. When 1, an interrupt is pending.

BIT 6 - Reserved

BIT 5 - VT Mapper Block Interrupt.

When 1, an interrupt from the VT Mapper block is pending.

BIT 4 - Reserved

BIT 3 - E1 framing synchronizer block Interrupt.

When 1, an interrupt from the E1 Framing Synchronizer block is pending.

BIT 2 - Reserved

BIT 1 - Receive Line Interface Block Interrupt.

When 1, an interrupt from the Receive Line interface block is pending.

BIT - 0 Transmit Line Interface Block Interrupt.

When 1, an interrupt from the Transmit Line Interface block is pending.

TABLE 24: OPERATION BLOCK INTERRUPT REGISTER BYTE 0 (OPIR0 0X0013H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	RXSTOH	RXSPOH	Reserved		EXTINT1	EXTINT0	Reserved
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Receive SDH Transport Overhead Block Interrupt

When 1, an interrupt from the SDH TOH block is pending.

BIT 5 - Receive SDH Path Overhead Block Interrupt

When 1, an interrupt from the SDH POH block is pending.

BIT [4:3] - Reserved

BIT 2 - External interrupt input 1

When 1, an interrupt from the EXT_INT_1 pin is pending.

BIT 1 - External interrupt input 0

When 1, an interrupt from the EXT_INT_0 pin is pending.

BIT 0 - Reserved

TABLE 25: OPERATION BLOCK INTERRUPT ENABLE REGISTER BYTE 1 (OPIER1 0X0016H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OP_CNTL_E	Reserved	VTMAP_ENB	Reserved	E1_ENB	Reserved	RXLIU_ENB	TXLIU_ENB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Operation Control Block Interrupt Enable

When 0, interrupts are disabled.

When 1, interrupts are enabled.

BIT 6 - Reserved

BIT 5 - VT Mapper Block Interrupt Enable

When 0, interface interrupts are disabled.

When 1, interrupts are enabled.

BIT 4 - Reserved

BIT 3 - E1synchronizer block Interrupt Enable

When 0, interrupts are disabled.

When 1, interrupts are enabled.

BIT 2 - Reserved

BIT 1 - Receive Line Interface Block Interrupt Enable

When 0, receive Line Interface interrupts are disabled.

When 1, receive Line Interface interrupts are enabled.

BIT 0 - Transmit Line Interface Block Interrupt Enable

When 0, receive Line Interface interrupts are disabled.

When 1, receive Line Interface interrupts are enabled.

TABLE 26: OPERATION BLOCK INTERRUPT ENABLE REGISTER BYTE 0 (OPIER0 0X0017H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	RXTOH_ENB	RXPOH_ENB	Reserved		EXTINT1_EN	EXTINT0_EN	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Receive SDH Transport Overhead Block Interrupt Enable

When 0, receive transport overhead interrupts are disabled.

When 1, receive STOH interrupts are enabled.

BIT 5 - Receive SDH Path Overhead Block Interrupt Enable

When 0, receive path overhead interrupts are disabled.

When 1, receive SPOH interrupts are enabled.

BIT [4:3] - Reserved

BIT 2 - External interrupt input 1 Interrupt Enable

When 0, the interrupts is disabled.

When 1, the interrupt is enabled.

BIT 1 - External interrupt input 0 Interrupt Enable

When 0, the interrupts is disabled.

When 1, the interrupt is enabled.

BIT 0 - Reserved

TABLE 27: DE-SYNC AND AU3 MAPPING CONTROL (DSAU3MC 0X001BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DSYNC_DIS	Reserved						AU3_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - De-Sync Disable

This bit is used to disable the de-sync function for all egress E1 line outputs.

- 0 - Normal De-Sync Function
- 1 - Disabled

BIT [6:1] - Reserved

BIT 0 - AU3 Mapping Enable

This bit is used to select AU3 mapping instead of TUG3.

- 0 - TUG3 Mapping
- 1 - AU3 Mapping

TABLE 28: SDH LOOP BACK SELECT (SDHLBS 0X001FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved				SDHLOOP[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT [3:0] - SDH Loop Back Select

These bits are used to select the SDH loop back mode for diagnostic testing.

- 0000 - No Loop Back
- 0001 - Reserved
- 0010 - Local Transport LB (TOH, POH, and Payload)
- 0011 - Local Path LB (POH and Payload)
- 11xx - Reserved

TABLE 29: HIGH BYTE FRAME BOUNDARY LATENCY (HBFBL 0X0034H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
HB_FB_Latency[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - High Byte of the Frame Boundary Latency [15:8]

This bit is used to determine the latency between the Frame Sync input pulse to the first byte of the SDH Frame out of this device.

TABLE 30: LOW BYTE FRAME BOUNDARY LATENCY (LBFBL 0X0035H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
LB_FB_Latency[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Low Byte of the Frame Boundary Latency [7:0]

This bit is used to determine the latency between the Frame Sync input pulse to the first byte of the SDH Frame out of this device.

TABLE 31: TELECOM BUS CONTROL 1 (TBC1 0X0036H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TBRATE	EMPTY_TS	MST_FP	TS_SEL[1:0]		V5POHPE	FP_EN	V5POHE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Telecom Bus Rate Select

This bit is used to select between STM-0 or STM-1 while in the Telecom Bus mode.

- 0 - STM-1 19.44 MHz
- 1 - STM-0 6.48 MHz

BIT 6 - Empty Time Slot Select

If this chip is configured as the Master device in STM-1, this bit is used to determine the state of the parallel data within the two empty slots on the shared telecom bus.

- 0 - Two Empty Slots are Filled With All Zeros
- 1 - Two Empty Slots are Tri-Stated

BIT 5 - SLOT 0 Master Frame Pulse Select

The state of this bit determines if the chip is the Master device or Slave device.

- 0 - Frame Pulse is an Input (Slave Device)
- 1 - Frame Pulse is an Output (Master Device)

BIT [4:3] - Time Slot Select

These bits indicate the time slot number on the telecom bus where this chip resides if it's configured to tri-state the two empty slots. The master device "Must" occupy time slot 0.

- 00 - Time Slot 0
- 01 - Time Slot 1
- 10 - Time Slot 2
- 11 - Reserved

BIT 2 - V5Path Over Head Parity Enable

This bit is used to enable V5 in the parity generation and checking.

- 0 - Disabled
- 1 - V5POH Enabled

BIT 1 - FP_ENB

This bit is used to configure the Telecom Bus as a parallel port and only clock, data and frame pulse (c1j1 signal) are valid signals.

- 0 - Normal Operation
- 1 - FP Enabled

BIT 0 - V5 Path Over Head Enable

This bit is used to enable the V5 POH byte.

- 0 - Disabled
- 1 - V5 POH Enabled

TABLE 32: TELECOM BUS CONTROL 0 (TBC0 0X0037H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TB_EN	TB_High-Z	FP2kHz	TBP_SEL	J1_ONLY	TBPAR_SEL	TBPAR_EN	Re-Phase
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Telecom Bus Enable

This bit is used to enable the Telecom Bus. By default, this bit is set to 1 (enabled).

- 0 - Disabled
- 1 - Enabled

BIT 6 - Telecom Bus Tri-State

This bit is used to tri-state the Telecom Bus.

- 0 - Normal Operation
- 1 - Tri-Stated

Bit 5 - Frame Pulse Operates at 2kHz

This bit is used to enable V1 alignment which sets the frame pulse at a rate of 2kHz.

- 0 - Normal Rate
- 1 - Frame Pulse is 2kHz

BIT 4 - Telecom Bus Parity Select

This bit is used to select which data is used for parity generation and check.

- 0 - Data Bits Only
- 1 - Data Bits, C1J1, and PL

BIT 3 - Telecom Bus J1 ONLY

This bit determines the usage of the Telecom bus while the C1J1V1_FP signal generates C1J1 pulse or just J1 pulse.

- 0 - Both C1 and J1 pulses are generated
- 1 - Only J1 pulse is generated

BIT 2- Telecom Bus Parity Select

This bit determines whether the parity is odd or even for the Telecom Bus.

- 0 - Even Parity
- 1 - Odd Parity

BIT 1- Telecom Bus Parity Enable

This bit determines whether parity generation and checking are enabled on the Telecom Bbus.

- 0 - Parity Enabled
- 1 - Parity Disabled

BIT 0 - Re-Phase On

This bit determines the usage of the Telecom bus while it is selected as Rephase/Sync interface in Telecom bus mode. In Re-Phase Off mode, frame synchronization is gained from the data stream. In Re-Phase On mode, the SDH framer block uses the C1J1V1_FP for "Re-Phasing" frame alignment to the external frame pulse pin.

- 0 - Re-Phase Off
- 1 - Re-Phase On

TABLE 33: GENERAL PURPOSE INPUT/OUTPUT (GPIO 0X0047H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
GPIO[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - General Purpose Input/Output

These bits either generate or monitor the activity on the hardware pins according to the direction.

TABLE 34: GENERAL PURPOSE INPUT/OUTPUT DIRECTION (GPIOD 0X004BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
GPIO_DIR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0[] - General Purpose I/O Direction Select

These bits are used to set the direction of the GPIO Hardware Pins.

- 0 - Inputs
- 1 - Outputs

TABLE 35: RECOVERED LINE CLOCK REFERENCE 1 (RLCR1 0X004DH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved			RECCLK_SEL0[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Reserved

BIT [4:0] - Recovered Clock Select 0

These bits select one of the 21 recovered E1 clocks to output on RCLK_REC0 output pin. See **Table 37**.

TABLE 36: RECOVERED LINE CLOCK REFERENCE 0 (RLCR0 0X004EH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved			RECCLK_SEL1[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Reserved

BIT [4:0] - Recovered Clock Select 1

These bits select one of the 21 recovered E1 clocks to output on RCLK_REC1 output pin. See **Table 37**.

TABLE 37: RECOVERED LINE CLOCK SELECT FOR RCLK_REC1 AND RCLK_REC0 HARDWARE PINS

BIT[4:0]	RECOVERED LINE CLOCK CHANNEL
00000	Tri-State
00001	Channel 0
00010	Channel 1
00011	Channel 2
00100	Channel 3
00101	Channel 4
00110	Channel 5
00111	Channel 6
01000	Channel 7
01001	Channel 8
01010	Channel 9
01011	Channel 10
01100	Channel 11
01101	Channel 12
01110	Channel 13
01111	Channel 14
10000	Channel 15
10001	Channel 16
10010	Channel 17
10011	Channel 18
10100	Channel 19
10101	Channel 20
10110 - 11111	Tri-State

TABLE 38: CHANNEL INTERRUPT INDICATION REGISTER 11 (CHIIR11 0X0054H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					E1_SLOT[20:18]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

TABLE 39: CHANNEL INTERRUPT INDICATION REGISTER 10 (CHIIR10 0X0055H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_SLOT[17:15]			Reserved	E1_SLOT[14:12]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

TABLE 40: CHANNEL INTERRUPT INDICATION REGISTER 9 (CHIIR9 0X0056H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_SLOT[11:9]			Reserved	E1_SLOT[8:6]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

TABLE 41: CHANNEL INTERRUPT INDICATION REGISTER 8 (CHIIR8 0X0057H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_SLOT[5:3]			Reserved	E1_SLOT[2:0]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 slot

TABLE 42: CHANNEL INTERRUPT INDICATION REGISTER 7 (CHIIR7 0X0058H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					E1_LIU_SLOT[20:18]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

TABLE 43: CHANNEL INTERRUPT INDICATION REGISTER 6 (CHIIR6 0X0059H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_LIU_SLOT[17:15]			Reserved	E1_LIU_SLOT[14:12]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1LIU Channel slot

TABLE 44: CHANNEL INTERRUPT INDICATION REGISTER 5 (CHIIR5 0X005AH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_LIU_SLOT[11:9]			Reserved	E1_LIU_SLOT[8:6]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

TABLE 45: CHANNEL INTERRUPT INDICATION REGISTER 4 (CHIIR4 0X005BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	E1_LIU_SLOT[5:3]			Reserved	E1_LIU_SLOT[2:0]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding E1 LIU Channel slot

TABLE 46: CHANNEL INTERRUPT INDICATION REGISTER 3 (CHIIR3 0X005CH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					VT_SLOT[20:18]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

TABLE 47: CHANNEL INTERRUPT INDICATION REGISTER 2 (CHIIR2 0X005DH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	VT_SLOT[17:15]			Reserved	VT_SLOT[14:12]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

TABLE 48: CHANNEL INTERRUPT INDICATION REGISTER 1 (CHIIR1 0X005EH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	VT_SLOT[11:9]			Reserved	VT_SLOT[8:6]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

TABLE 49: CHANNEL INTERRUPT INDICATION REGISTER 0 (CHIIR0 0X005FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	VT_SLOT[5:3]			Reserved	VT_SLOT[2:0]		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [6:4] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

BIT [2:0] - Each bit indicates an interrupt has been generated by the corresponding VT channel slot.

6.4 Receive Transport Overhead Operation Control Register Descriptions

TABLE 50: RECEIVE STM-0/STM-1 TRANSPORT CONTROL REGISTER 1 (RTCR1 = 0X0202)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Sync on B1	Unused	No OH Extract
R/O	R/O	R/O	R/O	R/O	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

BIT 2 - Sync on B1

This bit is used to enable B1 verification as part of the synchronization process. SYNC_ON_B1 can only be declared after 2 consecutive correct B1 bytes after A1 and A2 have been identified.

- 0 - Disabled
- 1 - Enabled

BIT 1 - Unused

BIT 0 - No Overhead Data Extract

This bit is used to disable TOH extraction. By default, TOH extraction is enabled.

- 0 - TOH Extraction Occurs
- 1 - TOH Extraction Disabled

TABLE 51: RECEIVE STM-0/STM-1 TRANSPORT CONTROL REGISTER 0 (RTCR0 = 0X0203)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble-Disable	SONET/SDH	REI-LError Type	B2 ErrorType	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Signal Failure (SF) Defect Condition Detect Enable

This READ/WRITE bit-field is used to enable or disable SF Defect Detection and Declaration by the Receive STM-0/STM-1 TOH Processor block.

- 0 - Configures the Receive STM-0/STM-1 TOH Processor block to NOT declare nor clear the SF defect condition per the user-specified SF defect declaration and clearance criteria.
- 1 - Configures the Receive STM-0/STM-1 TOH Processor block to declare and clear the SF defect condition per the user-specified SF defect declaration and clearance criteria.

BIT 5 - Signal Degrade (SD) Defect Condition Detect Enable

This READ/WRITE bit-field is used to enable or disable SD Detection and Declaration by the Receive STM-0/STM-1 TOH Processor block.

- 0 - Configures the Receive STM-0/STM-1 TOH Processor block to NOT declare nor clear the SD defect condition per the user-specified SD defect declaration and clearance criteria.
- 1 - Configures the Receive STM-0/STM-1 TOH Processor block to declare and clear the SD defect condition per the user-specified SD defect declaration and clearance criteria.

BIT 4 - De-Scramble Disable

This READ/WRITE bit-field is used to either enable or disable de-scrambling by the Receive STM-0/STM-1 TOH Processor block, associated with channel N.

- 0 - De-Scrambling is enabled.
- 1 - De-Scrambling is disabled.

BIT 3 - SONET/SDH Select

This bit is used to select between SONET processing or SDH processing.

- 0 - SONET Processing
- 1 - SDH Processing

BIT 2 - REI-L Error Type

This READ/WRITE bit-field is used to specify how the Receive STM-0/STM-1 TOH Processor block will count (or tally) REI-L events, for Performance Monitoring purposes. The user can configure the Receive STM-0/STM-1 TOH Processor block to increment REI-L events on either a per-bit or per-frame basis.

If the user configures the Receive STM-0/STM-1 TOH Processor block to increment REI-L events on a per-bit basis, then it will incrememt the Receive STM-0/STM-1 Transport REI-L Error Count register by the value of the lower nibble within the M0/M1 byte of the incoming STM-0 data-stream.

If the user configures the Receive STM-0/STM-1 TOH Processor block to increment REI-L events on a per-frame basis, then it will increment the Receive STM-0/STM-1 Transport REI-L Error Count register each time it receives an STM-0 or STM-1 frame, in which the lower nibble of the M0/M1 byte is set to a non-zero value.

- 0 - Configures the Receive STM-0/STM-1 TOH Processor block to count or tally REI-L events on a per-bit basis.
- 1 - Configures the Receive STM-0/STM-1 TOH Processor block to count or tally REI-L events on a per-frame basis.

BIT 1 - B2 Error Type

This READ/WRITE bit-field is used to specify how the Receive STM-0 TOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 TOH Processor block to increment B2 byte errors on either a per-bit or a per-frame basis.

If the user configures the Receive STM-0 TOH Processor block to increment B2 byte errors on a per-bit basis, then it will increment the Receive Transport B2 Byte Error Count register by the number of bits (within the B2 byte value) that is in error.

If the user configures the Receive STM-0 TOH Processor block to increment B2 byte errors on a per-frame basis, then it will increment the Receive Transport B2 Byte Error Count register each time it receives an STM-0 frame that contains an erred B2 byte.

- 0 - Configures the Receive STM-0 TOH Processor block to count B2 byte errors on a per-bit basis.
- 1 - Configures the Receive STM-0 TOH Processor block to count B2 byte errors on a per-frame basis.

BIT 0 - B1 Error Type

This READ/WRITE bit-field is used to specify how the Receive STM-0 TOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 TOH Processor block to increment B1 byte errors on either a per-bit or per-frame basis.

If the user configures the Receive STM-0 TOH Processor block to increment B1 byte errors on a per-bit basis, then it will increment the Receive Transport B1 Byte Error Count register by the number of bits (within the B1 byte value) that is in error.

If the user configures the Receive STM-0 TOH Processor block to increment B1 byte errors on a per-frame basis, then it will increment the Receive Transport B1 Byte Error Count Register each time it receives an STM-0 frame that contains an erred B1 byte.

- 0 - Configures the Receive STM-0 TOH Processor block to count B1 byte errors on a per-bit basis.
- 1 - Configures the Receive STM-0 TOH Processor block to count B1 byte errors on a per-frame basis.

TABLE 52: RECEIVE STM-0/STM-1 TRANSPORT STATUS REGISTER 1 (RTSR1 = 0X0206)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Section Trace Message (J0) Mismatch Defect Declared	Section Trace Message (J0) Unstable Defect Declared	AIS-L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

BIT 2 - Section Trace Message Mismatch Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the Section Trace Mismatch defect condition. The Receive STM-0 TOH Processor block will declare the Section Trace Message Mismatch defect condition, whenever it accepts a Section Trace Message (via the J0 byte, within the incoming STM-0 data-stream) that differs from the Expected Section Trace Message.

- 0 - Indicates that the Section Trace Message Mismatch Defect Condition is NOT currently being declared.
- 1 - Indicates that the Section Trace Message Mismatch Defect Condition is currently being declared.

BIT 1 - Section Trace Message Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STM-0 TOH Processor block will declare the Section Trace Message Unstable defect condition, whenever the Section Trace Message Unstable counter reaches the value 8.

The Section Trace Message Unstable counter will be incremented for each time that it receives a Section Trace message that differs from the Expected Section Trace Message.

The Section Trace Message Unstable counter is cleared to 0 whenever the Receive STM-1 TOH Processor block has received a given Section Trace Message 3 (or 5) consecutive times.

NOTE: *Receiving a given Section Trace Message 3 (or 5) consecutive times also sets this bit-field to 0.*

- 0 - Section Trace Message Unstable defect condition is NOT currently being declared.
- 1 - Section Trace Message Unstable defect condition is currently being declared.

BIT 0 - AIS-L Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the AIS-L (Line AIS) defect condition. The Receive STM-0 TOH Processor block will declare the AIS-L defect condition within the incoming STM-0 data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value [1, 1, 1] for five consecutive STM-0 frames.

- 0 - Indicates that the AIS-L defect condition is NOT currently being declared.
- 1 - Indicates that the AIS-L defect condition is currently being declared.

TABLE 53: RECEIVE STM-0/STM-1 TRANSPORT STATUS REGISTER 0 (RTSR0 = 0X0207)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOFDefect Detected	SEFDefect Declared	LOSDefect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - RDI-L Defect Declared Indicator

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is detecting the RDI-L (Line-Remote Defect Indicator) defect condition, within the incoming STM-0 signal. The Receive STM-0 TOH Processor block will declare the RDI-L defect condition whenever bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the 1, 1, 0 pattern in 5 consecutive incoming STM-0 frames.

- 0 - Indicates that the RDI-L defect condition is NOT currently being declared.
- 1 - Indicates that the RDI-L defect condition is currently being declared.

BIT 6 - S1 Byte Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the S1 Byte Unstable defect condition. The Receive STM-0 TOH Processor block will declare the S1 Byte Unstable defect condition whenever the S1 Byte Unstable Counter reaches the value 32. The S1 Byte Unstable Counter is incremented for each time that the Receive STM-0 TOH Processor block receives an STM-0 frame that contains an S1 byte that differs from the previously received S1 byte. The S1 Byte Unstable Counter is cleared to 0 when the same S1 byte is received for 8 consecutive STM-0 frames.

NOTE: *Receiving a given S1 byte, in 8 consecutive STM-0 frames also sets this bit-field to 0.*

- 0 - Indicates that the S1 Byte Unstable Defect Condition is NOT currently being declared.
- 1 - Indicates that the S1 Byte Unstable Defect Condition is currently being declared.

BIT 5 - K1, K2 Byte Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the K1, K2 Byte Unstable defect condition. The Receive STM-0 TOH Processor block will declare the K1, K2 Byte Unstable defect condition whenever the Receive STM-0 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive incoming STM-0 frames. The K1, K2 Byte Unstable defect condition is cleared whenever the Receive STM-0 TOH Processor block has received a given set of K1, K2 byte values within three consecutive incoming STM-0 frames.

- 0 - Indicates that the K1, K2 Byte Unstable Defect Condition is NOT currently being declared.
- 1 - Indicates that the K1, K2 Byte Unstabel Defect Condition is currently being declared.

BIT 4 - SF (Signal Failure) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the SF defect condition. The Receive STM-0 TOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain user-specified B2 Byte Error threshold.

- 0 - Indicates that the SF Defect condition is NOT currently being declared.

This bit is set to 0 when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the SF Defect Declaration threshold.

- 1 - Indicates that the SF Defect condition is currently being declared.

This bit is set to 1 when the number of B2 errors (accumulated over a given interval of time) does exceed the SF Defect Declaration threshold.

BIT 3 - SD (Signal Degrade) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the SD defect condition. The Receive STM-0 TOH Processor block will declare the SD defect condition anytime it has

determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain user-specified B2 Byte Error threshold.

- 0 - Indicates that the SD Defect condition is NOT currently being declared.

This bit is set to 0 when the number of B2 errors (accumulated over a given interval of time) does not exceed the SD Declaration threshold.

- 1 - Indicates that the SD Defect condition is currently being declared.This bit is set to 1 when the number of B2 errors (accumulated over a given interval of time) does exceed the SD Defect Declaration threshold.

BIT 2 - LOF (Loss of Frame) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the LOF defect condition. The Receive STM-0 TOH Processor block will declare the LOF defect condition if it has been declaring the SEF condition for 24 consecutive STM-0 frame periods. Once the LOF defect is declared, then the Receive STM-0 TOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STM-0 frame periods).

- 0 - Indicates that the Receive STM-0 TOH Processor block is NOT currently declaring the LOF defect condition.
- 1 - Indicates that the Receive STM-0 TOH Processor block is currently declaring the LOF defect condition.

BIT 1 - SEF (Severely Errored Frame) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the SEF defect condition. The Receive STM-0 TOH Processor block will declare the SEF defect condition if it detects Framing Alignment byte errors in four consecutive STM-0 frames. Once the Receive TOH Processor block declares the SEF defect condition, the Receive STM-0 TOH Processor block will then clear the SEF defect condition if it detects two consecutive STM-0 frames with un-erred framing alignment bytes. If the Receive TOH Processor block declares the SEF defect condition for 24 consecutive STM-0 frame periods, then it will declare the LOF defect condition.

- 0 - Indicates that the Receive STM-0 TOH Processor block is NOT currently declaring the SEF defect condition.
- 1 - Indicates that the Receive STM-0 TOH Processor block is currently declaring the SEF defect condition.

BIT 0 - LOS (Loss of Signal) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 TOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Receive STM-0 TOH Processor block will declare the LOS defect condition if it detects LOS_THRESHOLD[15:0] consecutive All Zero bytes in the incoming STM-0 data stream.

NOTE: *The user can set the LOS_THRESHOLD[15:0] value by writing the appropriate data into the Receive STM-0 Transport - LOS Threshold Value Register (Address Location= 0x022E and 0x022F).*

- 0 - Indicates that the Receive STM-0 TOH Processor block is NOT currently declaring the LOS defect condition.
- 1 - Indicates that the Receive STM-0 TOH Processor block is currently declaring the LOS defect condition.

TABLE 54: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT STATUS REGISTER 2 (RTISR2 = 0X0209)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-LDefect Condition Interrupt Status	Change of RDI-L Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7: 2] - Unused

BIT 1 - Change of AIS-L (Line AIS) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of AIS-L Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following occurrences.· Whenever the Receive STM-0 TOH Processor block declares the AIS-L defect condition.· Whenever the Receive STM-0 TOH Processor block clears the AIS-L defect condition.

- 0 - Indicates that the Change of AIS-L Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change of AIS-L Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the current state of the AIS-L defect condition by reading the contents of BIT 0 (AIS-L Defect Declared) within the Receive STM-0 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 0 - Change of RDI-L (Line - Remote Defect Indicator) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of RDI-L Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following occurrences.

- Whenever the Receive STM-0 TOH Processor block declares the RDI-L defect condition.·
- Whenever the Receive STM-0 TOH Processor block clears the RDI-L defect condition.

- 0 - Indicates that the Change of RDI-L Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change of RDI-L Defect Condition interrupt has occurred since the last read of this register.Note:

NOTE: *The user can obtain the current state of the RDI-L defect condition by reading out the state of BIT7 (RDI-L Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

TABLE 55: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT STATUS REGISTER 1 (RTISR1 = 0X020A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 ByteInter-rupt Status	Change in S1 Byte UnstableDe-fect Condi-tionInterrupt Status	Change in Section Trace Mes-sage Unsta-ble Defect Condition Interrupt Sta-tus	New Section Trace Mes-sage Inter-rupt Status	Change in Section Trace Mes-sage Mis-matchDefect Declared Interrupt Sta-tus	Unused	Change in K1, K2 Byte Unstable Defect Cond-tion Interrupt Status	NEW K1K2 Byte Value Interrupt Sta-tus
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - New S1 Byte Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New S1 Byte Value Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate the New S1 Byte Value Interrupt, anytime it has accepted a new S1 byte, from the incoming STM-0 data-stream.

- 0 - Indicates that the New S1 Byte Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New S1 Byte Value interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the value for this most recently accepted value of the S1 byte by reading the Receive STM-0 Transport S1 Byte Value register (Address Location= 0x0227).*

BIT 6 - Change in S1 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in S1 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the S1 Byte Unstable defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the S1 Byte Unstable defect condition.

- 0 - Indicates that the Change in S1 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.
- 1 - Indicates that the Change in S1 Byte Unstable Defect Condition Interrupt has not occurred since the last read of this register.

NOTE: *The user can obtain the current S1 Byte Unstable Defect condition by reading the contents of BIT6 (S1 Byte Unstable Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 5 - Change in Section Trace Message Unstable Defect condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Section Trace Message Unstable defect condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the Section Trace Message Unstable defect condition.
- Whenever the Receive STM-0 TOH Processor block clear the Section Trace Message Unstable defect condition.

- Indicates that the Change in Section Trace Message Unstable defect condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in Section Trace Message Unstable defect condition interrupt has occurred since the last read of this register.

BIT 4 - New Section Trace Message Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New Section Trace Message interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt anytime it has accepted a new Section Trace Message within the incoming STM-0 data-stream.

- 0 - Indicates that the New Section Trace Message Interrupt has not occurred since the last read of this register.
- 1 - Indicates that the New Section Trace Message Interrupt has occurred since the last read of this register.

NOTE: *The user can read out the contents of the Receive Section Trace Message Buffer, which is located at Address Locations 0x0400 through 0x04FF).*

BIT 3 - Change in Section Trace Message Mismatch Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Section Trace Mismatch Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.· Whenever the Receive STM-0 TOH Processor block declares the Section Trace Message Mismatch defect condition· Whenever the Receive STM-0 TOH Processor block clears the Section Trace Mismatch defect condition.

- 0 - Indicates that the Change in Section Trace Message Mismatch Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in Section Trace Message Mismatch Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether the Section Trace Message Mismatch condition is currently cleared or declared by reading the state of BIT 2 (Section Trace Message Mismatch Defect Declared) within the Receive STM-0 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 2 - Unused

BIT 1 - Change in K1, K2 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in K1, K2 Byte Unstable Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the K1, K2 Byte Unstable Defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the K1, K2 Byte Unstable Defect condition.

- 0 - Indicates that the Change of K1, K2 Byte Unstable Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of K1, K2 Byte Unstable Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether the K1, K2 Byte Unstable Defect Condition is currently being declared or cleared by reading out the contents of BIT 5 (K1, K2 Byte Unstable Defect Declared), within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 0 - New K1, K2 Byte Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New K1, K2 Byte Value Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt whenever its has accepted a new set of K1, K2 byte values from the incoming STM-0 data-stream

- 0 - Indicates that the New K1, K2 Byte Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New K1, K2 Byte Value Interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the contents of the new K1 byte by reading out the contents of the Receive STM-0 Transport K1 Byte Value Register (Address Location= 0xN11F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the Receive STM-0 Transport K2 Byte Value Register (Address Location= 0x0223).*

TABLE 56: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT STATUS REGISTER 0 (RTISR0 = 0X020B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect ConditionIn-terrupt Sta-tus	Change of SD Defect Condition Interrupt Sta-tus	Detection of REI-L Event Error Inter-rupt Status	Detection of B2 Byte Error Inter-rupt Status	Detection of B1 Byte Error Inter-rupt Status	Change of LOF Defect Condition Interrupt Sta-tus	Change of SEF Defect Interrupt Sta-tus	Change of LOS Defect Condition Interrupt Sta-tus
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Change of Signal Failure (SF) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SF Defect Condition Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the SF Defect Condition.
- Whenever the Receive STM-0 TOH Processor block clears the SF Defect Condition.

- 0 - Indicates that the Change of SF Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SF Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the SF defect condition is currently being declared by reading out the state of BIT 4(SF Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 6 - Change of Signal Degrade (SD) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SD Defect Condition Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenver the Receive STM-0 TOH Processor block declares the SD Defect Condition.
- Whenever the Receive STM-0 TOH Processor block clears the SD Defect Condition.

- 0 - Indicates that the Change of SD Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SD Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the SD Defect condition is currently being declareds by reading out the state of BIT 3 (SD Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 5 - Detection of REI-L (Line - Remote Error Indicator) Event Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of REI-L Event Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt anytime it detects an REI-L event within the incoming STM-0 data-stream.

- 0 - Indicates that the Detection of REI-L Event Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of REI-L Event Interrupt has occurred since the last read of this register.

BIT 4 - Detection of B2 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B2 Byte Error Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STM-0 data-stream.

- 0 - Indicates that the Detection of B2 Byte Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of B2 Byte Error Interrupt has occurred since the last read of this register.

BIT 3 = Detection of B1 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B1 Byte Error Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt anytime it detects a B1 byte error within the incoming STM-0 data-stream.

- 0 - Indicates that the Detection of B1 Byte Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of B1 Byte Error Interrupt has occurred since the last read of this register

BIT 2 - Change of Loss of Frame (LOF) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of LOF Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the LOF Defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the LOF Defect condition.

- 0 - Indicates that the Change of LOF Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of LOF Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STM-0 TOH Processor block is currently declaring the LOF defect condition by reading out the state of BIT 2 (LOF Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 1 - Change of SEF Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SEF Defect Condition Interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the SEF defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the SEF defect condition.

- 0 - Indicates that the Change of SEF Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SEF Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STM-0 TOH Processor block is currently declaring the SEF defect condition by reading out the state of BIT 1 (SEF Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 0 - Change of Loss of Signal (LOS) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of LOS Defect Condition interrupt has occurred since the last read of this register. The Receive STM-0 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the LOS defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the LOS defect condition.

- 0 - Indicates that the Change of LOS Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of LOS Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STM-0 TOH Processor block is currently declaring the LOS defect condition by reading out the contents of BIT 0 (LOS Defect Declared) within the Receive STM-0 Transport Status Register - Byte 0 (Address Location= 0x0207).*

TABLE 57: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT ENABLE REGISTER 2 (RTIER2 = 0X020D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-LDefect Condition Interrupt Enable	Change of RDI-LDefect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT 1- Change of AIS-L (Line AIS) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of AIS-L Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 TOH Processor block declares the AIS-L defect condition.·
- When the Receive STM-0 TOH Processor block clears the AIS-L defect condition.

- 0 - Disables the Change of AIS-L Defect Condition Interrupt.
- 1 - Enables the Change of AIS-L Defect Condition Interrupt.

BIT 0 - Change of RDI-L (Line Remote Defect Indicator) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of RDI-L Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.· When the Receive STM-0 TOH Processor block declares the RDI-L defect condition.· When the Receive STM-0 TOH Processor block clears the RDI-L defect condition.

- 0 - Disables the Change of RDI-L Defect Condition Interrupt.
- 1 - Enables the Change of RDI-L Defect Condition Interrupt.

TABLE 58: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT ENABLE REGISTER 1 (RTIER1 = 0X020E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect ConditionInterrupt Enable	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	New Section Trace Message Interrupt Enable	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	Unused	Change in K1, K2 Byte Unstable Defect ConditionInterrupt Enable	New K1K2 Byte Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - New S1 Byte Value Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the New S1 Byte Value Interrupt.

If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STM-0 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STM-0 frames.

- 0 - Disables the New S1 Byte Value Interrupt.
- 1 - Enables the New S1 Byte Value Interrupt.

BIT 6 - Change in S1 Byte Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in S1 Byte Unstable Defect Condition Interrupt..

If the user enables this bit-field, then the Receive STM-0 TOH Processor block will generate an interrupt in response to either of the following conditions

- When the Receive STM-0 TOH Processor block declares the S1 Byte Unstable defect condition
- When the Receive STM-0 TOH Processor block clears the S1 Byte Unstable defect condition.

- 0 - Disables the Change in S1 Byte Unstable Defect Condition Interrupt.
- 1 - Enables the Change in S1 Byte Unstable Defect Condition Interrupt.

BIT 5 - Change in Section Trace Message Unstable defect condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in Section Trace Message Unstable Defect Condition Interrupt.

If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STM-0 TOH Processor block declares the Section Trace Message Unstable defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the Section Trace Message Unstable defect condition.

- 0 - Disable the Change of Section Trace Message Unstable defect condition Interrupt.
- 1 - Enables the Change of Section Trace Message Unstable defect condition Interrupt.

BIT 4 - New Section Trace Message Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the New Section Trace Message interrupt.

If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message within the incoming STM-0 data-stream. The Receive STM-0 TOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times.

- 0 - Disables the New Section Trace Message Interrupt.
- 1 - Enables the New Section Trace Message Interrupt.

BIT 3 - Change in Section Trace Mismatch Defect Condition interrupt enable:

This READ/WRITE bit-field is used to either enable or disable the Change in Section Trace Mismatch defect condition interrupt.

If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the Section Trace Message Mismatch Defect condition.
- whenever the Receive STM-0 TOH Processor block clears the Section Trace Message Mismatch defect condition.

NOTE: *The user can determine whether or not the Receive STM-0 TOH Processor block is currently declaring the Section Trace Message Mismatch defect condition by reading the state of BIT 2 (Section Trace Message Mismatch Defect Condition Declared) within the Receive STM-0 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 2 - Unused

BIT 1 - Change of K1, K2 Byte Unstable Defect Condition - Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of K1, K2 Byte Unstable defect condition interrupt. If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate an Interrupt in response to either of the following events.a.Whenever the Receive STM-0 TOH Processor block declares the K1, K2 Byte Unstable defect condition. b.Whenever the Receive STM-0 TOH Processor block clears the K1, K2 Byte Unstable defect condition.

- 0 - Disables the Change of K1, K2 Byte Unstable Defect Condition Interrupt.
- 1 - Enables the Change of K1, K2 Byte Unstable Defect Condition Interrupt.

BIT 0 - New K1, K2 Byte Value Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New K1, K2 Byte Value Interrupt. If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STM-0 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STM-0 frames.

- 0 - Disables the New K1, K2 Byte Value Interrupt.
- 1 - Enables the New K1, K2 Byte Value Interrupt.

TABLE 59: RECEIVE STM-0/STM-1 TRANSPORT INTERRUPT STATUS REGISTER 0 (RTIER0 = 0X020F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect-Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of REI-L Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Change of Signal Failure (SF) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of Signal Failure (SF) Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to any of the following events.

- Whenever the Receive STM-0 TOH Processor block declares the SF defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the SF defect condition.

▶ 0 - Disables the Change of SF Defect Condition Interrupt.

▶ 1 - Enables the Change of SF Defect Condition Interrupt.

BIT 6 - Change of Signal Degrade (SD) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of Signal Degrade (SD) Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following events.

- Whenever the Receive STM-0 TOH Processor blolck declares the SD defect condition.
- Whenever the Receive STM-0 TOH Processor block clears the SD defect condition.

▶ 0 - Disables the Change of SD Defect Condition Interrupt.

▶ 1 - Enables the Change of SD Defect Condition Interrupt.

BIT 5 - Detection of REI-L (Line - Remote Error Indicator) Event Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of REI-L Event interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STM-0 TOH Processor block detects an REI-L condition within the incoming STM-0 data-stream.

▶ 0 - Disables the Detection of REI-L Event Interrupt.

▶ 1 - Enables the Detection of REI-L Event Interrupt.

BIT 4 - Detection of B2 Byte Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of B2 Byte Error Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STM-0 TOH Processor block detects a B2 byte error within the incoming STM-0 data-stream.

▶ 0 - Disables the Detection of B2 Byte Error Interrupt.

▶ 1 - Enables the Detection of B2 Byte Error Interrupt.

BIT 3 - Detection of B1 Byte Error Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Detection of B1 Byte Error Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STM-0 TOH Processor block detects a B1 byte error within the incoming STM-0 data-stream.

▶ 0 - Disables the Detection of B1 Byte Error Interrupt.

▶ 1 - Enables the Detection of B1 Byte Error Interrupt.

BIT 2 - Change of Loss of Frame (LOF) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of LOF Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions

- When the Receive STM-0 TOH Processor block declares the LOF defect condition
- When the Receive STM-0 TOH Processor block clears the LOF defect condition.

▶ 0 - Disables the Change of LOF Defect Condition Interrupt.

▶ 1 - Enables the Change of LOF Defect Condition Interrupt.

BIT 1 - Change of SEF Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of SEF Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 TOH Processor block declares the SEF defect condition.
- When the Receive STM-0 TOH Processor block clears the SEF defect condition.

▶ 0 - Disables the Change of SEF Defect Condition Interrupt.

▶ 1 - Enables the Change of SEF Defect Condition Interrupt.

BIT 0 - Change of Loss of Signal (LOS) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of LOF Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 TOH Processor block declares the LOF defect condition.
- When the Receive STM-0 TOH Processor block clears the LOF defect condition.

▶ 0 - Disables the Change of LOF Defect Condition Interrupt.

▶ 1 - Enables the Change of LOF Defect Condition Interrupt.

TABLE 60: RECEIVE STM-0/STM-1 TRANSPORT - B1 BYTE ERROR COUNT REGISTER 3 (B1BECR3 = 0X0210)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STM-0 Transport - B1 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor Block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error

2. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.

TABLE 61: RECEIVE STM-0/STM-1 TRANSPORT - B1 BYTE ERROR COUNT REGISTER 2 (B1BECR2 = 0X0211)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STM-0 Transport - B1 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.

TABLE 62: RECEIVE STM-0/STM-1 TRANSPORT - B1 BYTE ERROR COUNT REGISTER 1 (B1BECR1 = 0X0212)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STM-0 Transport - B1 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error

2. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.

TABLE 63: RECEIVE STM-0/STM-1 TRANSPORT - B1 BYTE ERROR COUNT REGISTER 0 (B1BECR0 = 0X0213)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive STM-0 Transport - B1 Byte Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor Block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.

TABLE 64: RECEIVE STM-0/STM-1 TRANSPORT - B2 BYTE ERROR COUNT REGISTER 3 (B2BECR3= 0X0214)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STM-0 Transport - B2 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B2 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.

TABLE 65: RECEIVE STM-0/STM-1 TRANSPORT - B2 BYTE ERROR COUNT REGISTER 2 (B2BECR2 = 0X0215)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B2 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.

TABLE 66: RECEIVE STM-0/STM-1 TRANSPORT - B2 BYTE ERROR COUNT REGISTER 1 (B2BECR1 = 0X0216)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B2 byte error.

NOTES:

1. If the Receive STM-0 TOH Processror block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.

TABLE 67: RECEIVE STM-0/STM-1 TRANSPORT - B2 BYTE ERROR COUNT REGISTER 0 (B2BECR0 = 0X0217)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a B2 byte error.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.

2. If the Receive STM-0 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.

TABLE 68: RECEIVE STM-0/STM-1 TRANSPORT - REI-L EVENT COUNT REGISTER 3 (REILECR3 = 0X0218)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - MSB

This RESET-upon-READ register, along with Receive STM-0 Transport - REI-L Event Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-0 data-stream.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STM-0 frame.

2. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a non-zero REI-L value.

TABLE 69: RECEIVE STM-0/STM-1 TRANSPORT - REI-L EVENT COUNT REGISTER 2 (REILECR2 = 0X0219)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STM-0 Transport - REI-L Event Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-0 data-stream.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STM-0 frame.

2. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a non-zero REI-L value.

TABLE 70: RECEIVE STM-0/STM-1 TRANSPORT - REI-L EVENT COUNT REGISTER 1 (REILECR1 = 0X021A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STM-0 Transport - REI-L Event Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a Line -Remote Error Indicator event within the incoming STM-0 data-stream.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STM-0 frame.

2. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a non-zero REI-L value.

TABLE 71: RECEIVE STM-0/STM-1 TRANSPORT - REI-L EVENT COUNT REGISTER 0 (REILECR0 = 0X021B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - LSB

This RESET-upon-READ register, along with Receive STM-0 Transport - REI-L Event Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STM-0 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-0 data-stream.

NOTES:

1. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.

2. If the Receive STM-0 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a non-zero REI-L value.

TABLE 72: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVED K1 BYTE VALUE REGISTER (RK1BVR = 0X021F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0]Filtered/Accepted K1 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered K1 byte value that the Receive STM-0 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STM-0 frames.

This register should be polled by Software in order to determine various APS codes.

TABLE 73: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVED K2 BYTE VALUE REGISTER (RK2BVR = 0X0223)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0]Filtered/Accepted K2 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered K2 Byte value that the Receive STM-0 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STM-0 frames.

This register should be polled by Software in order to determine various APS codes.

TABLE 74: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVED S1 BYTE VALUE REGISTER (RS1BVR = 0X0227)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_S1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Filtered/Accepted S1 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered S1 byte value that the Receive STM-0 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STM-0 frames.

TABLE 75: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE IN-SYNC THRESHOLD REGISTER (RISTR = 0X022B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FRPATOUT[1:0]		FRPATIN[1:0]		Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT [4:3] - FRPATOUT[1:0]

These bits allow software to select from 3 different framing algorithms when the framer is trying to detect SEF (OOF).

- 00, 01 - 16-Bits (Last A1 byte + First A2 byte)
- 10 - 32-Bits (Last two A1 bytes + First two A2 bytes)
- 11 - 48-Bits (Last three A1 bytes + First three A2 bytes)

BIT [2:1] - FRPATIN[1:0]

These bits allow software to specify the algorithm used to check for frame alignment patterns (A1/A2).

- 00, 01 - 16-Bits (Last A1 byte + First A2 byte)
- 10 - 32-Bits (Last two A1 bytes + First two A2 bytes)
- 11 - 48-Bits (Last three A1 bytes + First three A2 bytes)

BIT 0 - Unused

TABLE 76: RECEIVE STM-0/STM-1 TRANSPORT - LOS THRESHOLD VALUE 1 (LOSTV1 = 0X022E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - LOS Threshold Value - MSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - LOS Threshold Value - LSB register is used specify the number of consecutive (All Zero) bytes that the Receive STM-0/STM-1 TOH Processor block must detect (within the incoming STM-0/STM-1 data-stream) before it can declare the LOS defect condition.

NOTE: *This register contains the MSB (Most Significant Byte) of this 16-bit expression.*

TABLE 77: RECEIVE STM-0/STM-1 TRANSPORT - LOS THRESHOLD VALUE 0 (LOSTV0 = 0X022F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - LOS Threshold Value - LSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - LOS Threshold Value - MSB register is used to specify the number of consecutive (All Zero) bytes that the Receive STM-0/STM-1 TOH Processor block must detect (within the incoming STM-0/STM-1 data-stream) before it can declare the LOS defect condition.

NOTE: *This register contains the LSB (Least Significant Byte) of this 16-bit expression.*

TABLE 78: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL 2 (RSFSMI2= 0X0231)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - SF SET Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STM-0/STM-1 TOH Processor block is checking the incoming STM-0/STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Declaration monitoring period. If, during this SF Defect Declaration Monitoring Period, the Receive STM-0/STM-1 TOH Processor block accumulates more B2 byte errors than that specified within the Receive Transport SF SET Threshold register, then the Receive STM-0/STM-1 TOH Processor block will declare the SF defect condition.

NOTES:

1. *The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.*
2. *This particular register byte contains the MSB (most significant byte) value of the three registers that specify the SF Defect Declaration Monitoring Period.*

TABLE 79: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL 1 (RSFSMI1 = 0X0232)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL (Bits 15 through 8)

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - SF SET Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STM-0/STM-1 TOH Processor block is checking the incoming STM-0/STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Declaration Monitoring Period. If, during this SF Defect Declaration Monitoring Period the Receive STM-0/STM-1 TOH Processor block accumulate more B2 byte errors than that specified within the Receive STM-0/STM-1 Transport

SF SET Threshold register, then the Receive STM-0/STM-1 TOH Processor block will declare the SF defect condition.

NOTE: *The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.*

TABLE 80: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL 0 (RSFSMI0 = 0X0233)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - SF SET Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STM-0/STM-1 TOH Processor block is checking the incoming STM-0/STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Declaration Monitoring Period. If, during this SF Defect Declaration Monitoring Period, the Receive STM-0/STM-1 TOH Processor block accumulates more B2 byte errors than that specified within the Receive STM-0/STM-1 Transport SF SET Threshold register, then the Receive STM-0/STM-1 TOH Processor block will declare the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SF Defect Declaration Monitoring period.

TABLE 81: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE SF SET THRESHOLD 1 (RSFST1= 0X0236)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - SF SET Threshold - Byte 0 registers are used to specify the number of B2 byte errors that will cause the Receive STM-0/STM-1 TOH Processor block to declare the SF (Signal Failure) Defect condition.

When the Receive STM-0/STM-1 TOH Processor block is checking for declaring the SF defect condition, it will accumulate B2 byte errors throughout the SF Defect Declaration Monitoring Period. If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the Receive STM-0 Transport SF SET Threshold - Byte 0 register, then the Receive STM-0/STM-1 TOH Processor block will declare the SF defect condition.

NOTE: *This particular register byte contains the MSB (most significant byte) value of this 16-bit expression.*

TABLE 82: RECEIVE STM-0/STM-1 TRANSPORT - RECEIVE SF SET THRESHOLD 0 (RSFST0 = 0X0237)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STM-0/STM-1 Transport - SF SET Threshold - Byte 1 registers are used to specify the number of B2 byte errors that will cause the Receive STM-0/STM-1 TOH Processor block to declare the SF (Signal Failure) Defect condition.

When the Receive STM-0/STM-1 TOH Processor block is checking for declaring the SF defect condition, it will accumulate B2 byte errors throughout the SF Defect Monitoring Period. If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the Receive STM-0 Transport SF SET Threshold - Byte 1 register, then the Receive STM-0/STM-1 TOH Processor block will declare the SF defect condition.

TABLE 83: RECEIVE STM-0 TRANSPORT - RECEIVE SF CLEAR THRESHOLD 2 (RSFCT2= 0X023A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SF CLEAR Threshold - Byte 0 registers are used to specify the upper limit for the number of B2 bit errors that will cause the Receive STM-0 TOH Processor block to clear the SF (Signal Failure) defect condition.

When the Receive STM-0 TOH Processor block is checking for clearing the SF defect condition, it will accumulate B2 byte errors throughout the SF Defect Clearance Monitoring Period. If the number of accumulated B2 byte errors is less than that programmed into this and the Receive STM-0 Transport SF CLEAR Threshold - Byte 0 register, then the Receive STM-0 TOH Processor block clear the SF defect condition.

TABLE 84: RECEIVE STM-0 TRANSPORT - RECEIVE SF CLEAR THRESHOLD 1 (RSFCT1 = 0X023B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SF CLEAR Threshold - Byte 1 registers are used to specify the upper limit for the number of B2 bit errors that will cause the Receive STM-0 TOH Processor block to clear the SF (Signal Failure) defect condition.

When the Receive STM-0 TOH Processor block is checking for clearing the SF defect condition, it will accumulate B2 byte errors throughout the SF Defect Clearance Monitoring Period. If the number of accumulated B2 byte errors is less than that programmed into this and the Receive STM-0 Transport SF CLEAR Threshold - Byte 1 register, then the Receive STM-0 TOH Processor block will clear the SF defect condition.

TABLE 85: RECEIVE STM-0 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL 0 (RSFCT0 = 0X023D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD SET Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Declaration monitoring period. If, during this SD Defect Declaration Monitoring period, the Receive STM-0 TOH Processor block accumulates more B2 byte errors than that specified within the Receive STM-0 Transport SD SET Threshold register, then the Receive STM-0 TOH Processor block will declare the SD defect condition.

NOTES:

1. The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (Most significant byte) value of the three registers that specify the SD Defect Declaration Monitoring Period.

TABLE 86: RECEIVE STM-0 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL 1 (RSDSMI1 = 0X023E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD SET Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Declaration Monitoring Period. If, during this SD Defect Declaration Monitoring Period the Receive STM-0 TOH Processor block accumulates more B2 byte errors than that specified within the Receive STM-0 Transport SD SET Threshold register, then the Receive STM-0 TOH Processor block will declare the SD defect condition.

NOTE: *The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.*

TABLE 87: RECEIVE STM-0 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL 0 (RSDSMI0 = 0X023F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD SET Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-speciifed SD Defect Declaration Monitoring Period. If, during this SD Defect Declaration Monitoring Period, the Receive STM-0 TOH Processor block accmulattes more B2 byte errors than that specified within the Receive STM-0 Transport SD SET Threshold register, then the Receive STM-0 TOH Processor block will declare the SD defect condition.

NOTES:

1. The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SD Defect Declaration Monitoring period.

TABLE 88: RECEIVE STM-0 TRANSPORT - RECEIVE SD SET THRESHOLD 1 (RSDST1= 0X0242)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_SET_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD SET Threshold - Byte 0 registers are used to specify the number of B2 bit errors that will cause the Receive STM-0 TOH Processor block to declare the SD (Signal Degrade) defect condition.

When the Receive STM-0 TOH Processor block is checking for declaring the SD defect condition, it will accumulate B2 byte errors throughout the SD Defect Declaration Monitoring Period. If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the Receive STM-0 Transport SD SET Threshold - Byte 0 register, then the Receive STM-0 TOH Processor block will declare the SD defect condition.

TABLE 89: RECEIVE STM-0 TRANSPORT - RECEIVE SD SET THRESHOLD 0 (RSDST0 = 0X0243)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_SET_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD SET Threshold - Byte 1 registers are used to specify the number of B2 bit errors that will cause the Receive STM-0 TOH Processor block to declare an SD (Signal Degrade) defect condition.

When the Receive STM-0 TOH Processor block is checking for declaring the SD defect condition, it will accumulate B2 byte errors throughout the SD Defect Monitoring Period. If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the Receive STM-0 Transport SD SET Threshold - Byte 1 register, then the Receive STM-0 TOH Processor block will declare the SD defect condition.

TABLE 90: RECEIVE STM-0 TRANSPORT - RECEIVE SD CLEAR THRESHOLD 1 (RSDCT1= 0X0246)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD CLEAR Threshold - Byte 0 registers are used to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-0 TOH Processor block to clear the SD (Signal Degrade) defect condition.

When the Receive STM-0 TOH Processor block is checking for clearing the SD defect condition, it will accumulate B2 byte errors throughout the SD Defect Clearance Monitoring Period. If the number of accumulated B2 byte errors is less than that programmed into this and the Receive STM-0 Transport SD CLEAR Threshold - Byte 0 register, then the Receive STM-0 TOH Processor block will clear the SD defect condition.

TABLE 91: RECEIVE STM-0 TRANSPORT - RECEIVE SD CLEAR THRESHOLD 0 (RSDCT0 = 0X0247)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD CLEAR Threshold - Byte 1 registers are used to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-0 TOH Processor block to clear the SD (Signal Degrade) defect condition.

When the Receive STM-0 TOH Processor block is checking for clearing the SD defect condition, it will accumulate B2 byte errors throughout the SD Defect Clearance Monitoring Period. If the number of accumulated B2 byte errors is less than that programmed into this and the Receive STM-0 Transport SD CLEAR Threshold - Byte 1 register, then the Receive STM-0 TOH Processor block will clear the SD defect condition.

TABLE 92: RECEIVE STM-0 TRANSPORT - FORCE SEF DEFECT CONDITION REGISTER (FSDCR = 0X024B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - SEF Defect Condition FORCE

This READ/WRITE bit-field is used to force the Receive STM-0 TOH Processor block (within the corresponding Channel) to declare the SEF defect condition. The Receive STM-0 TOH Processor block will then attempt to reacquire framing.

Writing a 1 into this bit-field configures the Receive STM-0 TOH Processor block to declare the SEF defect. The Receive STM-0 TOH Processor block will automatically set this bit-field to 0 once it has reacquired framing (e.g., has detected two consecutive STM-0 frames with the correct A1 and A2 bytes).

TABLE 93: RECEIVE STM-0 TRANSPORT - RECEIVE SECTION TRACE MESSAGE BUFFER CONTROL REGISTER (RSTMBCR = 0X024F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4 - Receive Section Trace Message Buffer Read Selection

This READ/WRITE bit-field is used to specify which of the following Receive Section Trace Message buffer segments to read.

- The Actual Receive Section Trace Message Buffer which contains the contents of the most recently received (and accepted) Section Trace Message via the incoming STM-0 data-stream.
- The Expected Receive Section Trace Message Buffer which contains the contents of the Section Trace Message that the user expects to receive. The contents of this particular buffer are usually specified by the user.

▶ 0 - Executing a READ to the Receive Section Trace Message Buffer address space, will return contents within the Actual Receive Section Trace Message buffer.

▶ 1 - Executing a READ to the Receive Section Trace Message Buffer address space will return contents within the Expected Receive Section Trace Message Buffer.

NOTE: *In the case of the Receive STM-1 TOH Processor block, the Receive Section Trace Message Buffer is located at Address Location 0x0400 through 0x043F.*

BIT 3 - Receive Section Trace Message Accept Threshold

This READ/WRITE bit-field is used to select the number of consecutive times that the Receive STM-0 TOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given Section Trace Message has been accepted then it can be read out of the Actual Receive Section Trace Message Buffer.

▶ 0 - The Receive STM-0 TOH Processor block accepts the Section Trace Message after it has received it the third time in succession.

▶ 1 - The Receive STM-0 TOH Processor block accepts the Section Trace Message after it has received in the fifth time in succession.

BIT 2 - Section Trace Message Alignment Type

This READ/WRITE bit-field is used to specify how the Receive STM-0 TOH Processor block will locate the boundary of the Section Trace Message within the incoming STM-0 data-stream, as indicated below.

▶ 0 - Message boundary is indicated by Line Feed.

▶ 1 - Message boundary is indicated by the presence of a 1 in the MSB of the first byte (within the Section Trace Message).

BIT [1:0] - Receive Section Trace Message Length[1:0]

These READ/WRITE bit-fields are used to specify the length of the Section Trace Message that the Receive STM-0 TOH Processor block will receive. The relationship between the content of these bit-fields and the corresponding Receive Section Trace Message Length is presented below

Trace Message Length

RECEIVE SECTION TRACE MESSAGE LENGTH[1:0]	RESULTING RECEIVE SECTION TRACE MESSAGE LENGTH (IN TERMS OF BYTES)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

TABLE 94: RECEIVE STM-0 TRANSPORT - RECEIVE SD BURST ERROR TOLERANCE 1 (RSDBET1 = 0X0252)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_BURST_TOLERANCE - MSB

These READ/WRITE bits, along with the contents of the Receive STM-0 Transport - SD BURST Tolerance - Byte 0 registers are used to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STM-0 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-0 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SD defect condition.*

TABLE 95: RECEIVE STM-0 TRANSPORT - RECEIVE SD BURST ERROR TOLERANCE 0 (RSDBET0 = 0X0253)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_BURST_TOLERANCE - LSB

These READ/WRITE bits, along with the contents of the Receive STM-0 Transport - SD BURST Tolerance - Byte 1 registers are used to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STM-0 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-0 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SD defect condition.*

TABLE 96: RECEIVE STM-0 TRANSPORT - RECEIVE SF BURST ERROR TOLERANCE 1 (RSFBET1 = 0X0256)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_BURST_TOLERANCE - MSB

These READ/WRITE bits, along with the contents of the Receive STM-0 Transport - SF BURST Tolerance - Byte 0 registers are used to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STM-0 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM-0 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SF defect condition.*

TABLE 97: RECEIVE STM-0 TRANSPORT - RECEIVE SF BURST ERROR TOLERANCE 0 (RSFBET0 = 0X0257)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_BURST_TOLERANCE - LSB

These READ/WRITE bits, along with the contents of the Receive STM-0 Transport - SF BURST Tolerance - Byte 1 registers are used to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STM-0 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM-0 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SF defect condition.*

TABLE 98: RECEIVE STM-0 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL 2 (RSDCMI2= 0X0259)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD Clear Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defect Clearance Monitoring period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SD Clear Threshold register, then the Receive STM-0 TOH Processor block will clear the SD defect condition.

NOTES:

1. The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (Most significant byte) value of the three registers that specifiy the SD Defect Clearance Monitoring period.

TABLE 99: RECEIVE STM-0 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL 1 (RSDCMI1 = 0X025A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD Clear Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defecf Clearance Monitoring Period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SD Clear Threshold register, then the Receive STM-0 TOH Processor block will clear the SD defect condition.

NOTE: *The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.*

TABLE 100: RECEIVE STM-0 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL 0 (RSDCMI0 = 0X025B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WIN-DOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SD Clear Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance

.When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defect Clearance Monitoring period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SD Clear Threshold register, then the Receive STM-0 TOH Processor block will clear the SD defect condition

NOTES:

1. The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.

2. This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SD Defect Clearance Monitoring period.

TABLE 101: RECEIVE STM-0 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL 2 (RSFCMI2= 0X025D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SF Clear Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SF Clear Threshold register, then the Receive STM-0 TOH Processor blolck will clear the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (Most significant byte) value of the three registers that specify the SF Defect Clearance Monitoring period.

TABLE 102: RECEIVE STM-0 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL 1 (RSFCMI1 = 0X025E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SF Clear Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance.

When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SF Clear Threshold register, then the Receive STM-0 TOH Processor block will clear the SF defect condition.

NOTE: *The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.*

TABLE 103: RECEIVE STM-0 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL 0 (RSFCMI0 = 0X025F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STM-0 Transport - SF Clear Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance.When the Receive STM-0 TOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STM-0 TOH Processor block accumulates less B2 byte errors than that programmed into the Receive STM-0 Transport SF Clear Threshold register, then the Receive STM-0 TOH Processor block will clear the SF defect condition.

NOTES:

1. *The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.*
2. *This particular register byte contains the LSB (Least Significant byte) value of the three registers that specify the SF Defect Clearance Monitoring period.*

TABLE 104: RECEIVE STM-0 TRANSPORT - AUTO AIS CONTROL REGISTER (AAISCR = 0X0263)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P (Down-stream) upon Section Trace Mes-sage Unsta-ble	Transmit AIS-P (Down-stream) Upon Sec-tion Trace Message Mismatch	Transmit AIS-P (Down-stream) upon SF	Transmit AIS-P (Down-stream) upon SD	Unused	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Transmit Path AIS upon Declaration of the Section Trace Message Unstable Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block), anytime it declares the Section Trace Message Unstable defect condition within the incoming STM-0 data-stream.

- 0 - Does not configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Unstable defect condition.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Unstable defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 6 - Transmit Path AIS (AIS-P) upon Declaration of the Section Trace Message Mismatch Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Mismatch defect condition within the incoming STM-0 data stream.

- 0 - Does not configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Section Trace Mismatch defect condition.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Mismatch defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 5 - Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the SF defect condition.

- 0 - Does not configure the Receive STM-0 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the SF defect.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the SF defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 4 - Transmit Path AIS upon declaration of the Signal Degrade (SD) defect

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block) anytime (and for the duration that) it declares the SD defect condition.

- 0 - Does not configure the Receive STM-0 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the SD defect.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the SD defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 3 - Unused

BIT 2 - Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the LOF defect condition.

- 0 - Does not configure the Receive STM-0 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the LOF defect.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the LOF defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 1 - Transmit Path AIS upon declaration of the Loss of Signal (LOS) defect

This READ/WRITE bit-field is used to configure the Receive STM-0 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the LOS defect condition.

- 0 - Does not configure the Receive STM-0 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) anytime it declares the LOS defect condition.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the LOS defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 0 - Automatic Transmission of AIS-P Enable

This READ/WRITE bit-field serves two purposes.

It is used to configure the Receive STM-0 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STM-0 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF or LOS defect conditions.

It also is used to configure the Receive STM-0 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STM-0 POH Processor block) anytime it declares the AIS-L defect condition within the incoming STM-0 datastream.

- 0 - Configures the Receive STM-0 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the downstream traffic) upon declaration of the AIS-L defect condition or any of the above-mentioned defect conditions.
- 1 - Configures the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) upon declaration of the AIS-L defect or any of the above-mentioned defect conditions.

NOTE: *The user must also set the corresponding bit-fields (within this register) to 1 in order to configure the Receive STM-0 TOH Processor block to automatically transmit the AIS-P indicator upon declaration of a given alarm/ defect condition.*

RECEIVE STM-0 TRANSPORT - AUTO AIS (IN DOWNSTREAM E1S) CONTROL REGISTER (AAISDSCR= 0X026B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit AIS (via Down-stream T1/ E1s) upon LOS	Transmit AIS (via Down-stream T1/ E1s) upon LOF	Transmit AIS (via Down-stream T1/ E1s) upon SD	Transmit AIS (via Down-stream T1/ E1s) upon SF	Unused	Transmit AIS (via Down-stream T1/ E1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BIT 5 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the LOS (Loss of Signal) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the LOS defect condition.3

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime the Receive STM-0 TOH Processor block declares the LOS defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the LOS defect condition.

BIT 4 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the LOF (Loss of Frame) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the LOF defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime the Receive STM-0 TOH Processor block declares the LOF defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the LOF defect condition.

BIT 3 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the SD (Signal Degrade) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the SD defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime the Receive STM-0 TOH Processor block declares the SD defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the SD defect condition.

BIT 2 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the Signal Failure (SF) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the SF defect condition.

- 0 - Does not configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime the Receive STM-0 TOH Processor block declares the SF defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 TOH Processor block declares the SF defect condition.

BIT 1 - Unused

BIT 0 - Automatic Transmission of E1 AIS (via the downstream E1s) Enable

This READ/WRITE bit-field serves two purposes.It is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, upon declaration of either the SF, SD, LOS or LOF defect conditions via the Receive STM-0 TOH Processor block.

It also is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS indicator, via its outbound E1 signals, upon declaration of the AIS-L defect condition, via the Receive STM-0 TOH Processor block.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS indicator, whenever the Receive STM-0 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS indicator, whenever (and for the duration that) the Receive STM-0 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

TABLE 105: RECEIVE STM-0/STM-1 TRANSPORT - A1, A2 BYTE ERROR COUNT REGISTER 1 (A1A2BE1 = 0X026E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive A1, A2 Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive A1, A2 Byte Error Count Register - MSB Register

This RESET-upon-READ register, along with the Receive STM-0/STM-1 Transport - A1, A2 Byte Error Count Register - Byte

0 presents a 16-bit representation of the total number of A1 and A2 byte errors that the Receive STM-0/STM-1 TOH Processor block has detected (within the incoming STM-0/STM-1 data-stream) since the last read of this register.

NOTE: *This register contains the MSB (Most Significant Byte) of this 16-bit expression.*

TABLE 106: RECEIVE STM-0/STM-1 TRANSPORT - A1, A2 BYTE ERROR COUNT REGISTER 0 (A1A2BE0 = 0X026F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive A1, A2 Byte Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive A1, A2 Byte Error Count Register - LSB Register

This RESET-upon-READ register, along with the Receive STM-0/STM-1 Transport - A1, A2 Byte Error Count Register - Byte 1 presents a 16-bit representation of the total number of A1 and A2 byte errors that the Receive STM-0/STM-1 TOH Processor block has detected (within the incoming STM-0/STM-1 data-stream) since the last read of this register.

NOTE: *This register contains the LSB (Least Significant Byte) of this 16-bit expression.*

6.5 Receive Path Overhead Operation Control Register Descriptions

TABLE 107: RECEIVE STM-0 PATH - RECEIVE CONTROL REGISTER 0 (RCR0 = 0X0283)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				CheckStuff	RDI-PType	REI-PError Type	B3 Error Type
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - Check (Pointer Adjustment) Stuff Select

This READ/WRITE bit-field is used to enable/disable the SDH standard recommendation that a pointer increment or decrement operation, detected within 3 SDH frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.

- 0 - Disables this SDH standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.
- 1 - Enables this SDH standard implementation. In this mode, all pointer-adjustment operations that are detected within 3 SDH frame periods of a previous pointer-adjustment operation will be ignored.

BIT 2 - Path - Remote Defect Indicator Type Select

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to support either the Single-Bit or the Enhanced RDI-P form of signaling, as described below.

- 0 - Configures the Receive STM-0 POH Processor block to support Single-Bit RDI-P.

In this mode, the Receive STM-0 POH Processor block will only monitor BIT 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the RDI-P defect condition.

- 1 - Configures the Receive STM-0 POH Processor block to support Enhanced RDI-P (ERDI-P).

In this mode, the Receive STM-0 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.

BIT 1 - REI-P Error Type

This READ/WRITE bit-field is used to specify how the Receive STM-0 POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive STM-0 POH Processor block to increment REI-P events on either a per-bit or per-frame basis.

If the user configures the Receive STM-0 POH Processor block to increment REI-P events on a per-bit basis, then it will increment the Receive Path REI-P Error Count register by the value of the lower nibble within the G1 byte of the incoming STM-0 data-stream.

If the user configures the Receive STM-0 POH Processor block to increment REI-P events on a per-frame basis, then it will increment the Receive Path REI-P Error Count register each time it receives an STM-0 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a non-zero value.

- 0 - Configures the Receive STM-0 POH Processor block to count or tally REI-P events on a per-bit basis.
- 1 - Configures the Receive STM-0 POH Processor block to count or tally REI-P events on a per-frame basis.

BIT 0 - B3 Error Type

This READ/WRITE bit-field is used to specify how the Receive STM-0 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 POH Processor block to increment B3 byte errors on either a per-bit or per-frame basis.

If the user configures the Receive STM-0 POH Processor block to increment B3 byte errors on a per-bit basis, then it will increment the Receive Path B3 Byte Error Count register by the number of bits (within the B3 byte value) that is in error.

If the user configures the Receive STM-0 POH Processor block to increment B3 byte errors on a per-frame basis, then it will increment the Receive Path B3 Byte Error Count register each time it receives an STM-0 frame that contains an erred B3 byte.

- 0 - Configures the Receive STM-0 POH Processor block to count B3 byte errors on a per-bit basis
- 1 - Configures the Receive STM-0 POH Processor block to count B3 byte errors on a per-frame basis.

TABLE 108: RECEIVE STM-0 PATH - CONTROL REGISTER (PCR = 0X0286)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - Path Trace Message Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive STM-0 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the Path Trace Message Unstable counter reaches the value 8. The Path Trace Message Unstable counter will be incremented for each time that it receives a Path Trace message that differs from the previously received message. The Path Trace Unstable counter is cleared to 0 whenever the Receive STM-0 POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times.

NOTE: *Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to 0*

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the Path Trace Message Unstable defect.
- 1 - Indicates that the Receive STM-0 POH Processor blolck is currently declaring the Path Trace Message Unstable defect condition.

TABLE 109: RECEIVE STM-0 PATH - SDH RECEIVE POH STATUS (RPOHS = 0X0287)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P Defect Declared	C2 Byte UnstableDe-fect Declared	UNEQ-PDe-fectDeclared	PLM-PDe-fectDeclared	RDI-PDe-fectDeclared	RDI-P Unstable-Condition	LOP-PDe-fectDeclared	AIS-PDefect-Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Trace Identification Mismatch (TIM-P) Defect Indicator

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the Path Trace Identification Mismatch (TIM-P) defect condition. The Receive STM-0 POH Processor block will declare the TIM-P defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STM-0 data-stream) matches the expected 64 byte message.The Receive STM-0 POH Processor block will clear the TIM-P defect condition, when 80% of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the TIM-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the TIM-P defect condition.

BIT 6 - C2 Byte (Path Signal Label Byte) Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the Path Signal Label Byte Unstable defect condition. The Receive STM-0 POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the C2 Byte Unstable counter reaches the value 5. The C2 Byte Unstable counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The C2 Byte Unstable counter is cleared to 0 whenever the Receive STM-0 POH

Processor block has received 3 (or 5) consecutive SPEs that each contains the same C2 byte value.Note:Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to 0.

- 0 - Indicates that the Receive STM-0 POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.

BIT 5 - Path - Unequipped (UNEQ-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the UNEQ-P defect condition. The Receive STM-0 POH Processor block will declare the UNEQ-P defect condition, anytime that it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to the value 0x00 (which indicates that the SPE is Unequipped).

The Receive STM-0 POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to a value other than 0x00.

- 0 - Indicates that the Receive STM-0 POH Processor block is currently NOT declaring the UNEQ-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the UNEQ-P defect condition.

NOTE: *:The Receive STM-0 POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive STM-0 frames with C2 bytes being set to 0x00 (e.g., if the Receive STM-0 Path - Expected Path Label Value Register -Address Location= 0x0297) is set to 0x00.*

BIT 4 - Path Payload Mismatch (PLM-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the PLM-P defect condition.The Receive STM-0 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to a value other than that which it is expecting to receive. Whenever the Receive STM-0 POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers.

- The Receive STM-0 Path - Received Path Label Value Register (Address Location= 0xN196).
- The Receive STM-0 Path - Expected Path Label Value Register (Address Location= 0xN197).

The Receive STM-0 Path - Expected Path Label Value Register contains the value of the C2 bytes, that the Receive STM-0 POH Processor blocks expects to receive.The Receive STM-0 Path - Received Path Label Value Register contains the value of the C2 byte, that the Receive STM-0 POH Processor block has most received validated (by receiving this same C2 byte in five consecutive STM-0 frames). The Receive STM-0 POH Processor block will declare the PLM-P defect condition if the contents of these two register do not match. The Receive STM-0 POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match.

- 0 - Indicates that the Receive STM-0 POH Processor block is currently NOT declaring the PLM-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the PLM-P defect condition

NOTE: *The Receive STM-0 POH Processor block will clear the PLM-P defect, upon declaring the UNEQ-P defect condition.*

BIT 3 - Path Remote Defect Indicator (RDI-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the RDI-P defect condition.

If the Receive STM-0 POH Processor block is configured to support the Single-bit RDI-P function, then it will declare the RDI-P defect condition if BIT 5 (within the G1 byte of the incoming STM-0 frame) is set to 1 for RDI-P_THRD number of incoming consecutive STM-0 frames.

If the Receive STM-0 POH Processor block is configured to support the Enhanced RDI-P (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STM-0 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for RDI-P_THRD number of consecutive STM-0 frames.

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the RDI-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the RDI-P defect condition.

NOTE: *The user can specify the value for RDI-P_THRD by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the Receive STM-0 Path - SDH Receive RDI-P Register (Address Location= 0x0293).*

BIT 2 - RDI-P (Path - Remote Defect Indicator) Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the

RDI-P Unstable defect condition. The Receive STM-0 POH Processor block will declare a RDI-P I Unstable defect condition whenever the RDI-P Unstable Counter reaches the value RDI-P THRD. The RDI-P Unstable counter is incremented for each time that the Receive STM-0 POH Processor block receives an RDI-P value that differs from that of the previous STM-0 frame. The RDI-P Unstable counter is cleared to 0 whenever the same RDI-P value is received in RDI-P_THRD consecutive STM-0 frames.

NOTE: *Receiving a given RDI-P value, in RDI-P_THRD consecutive STM-0 frames also clears this bit-field to 0.*

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the RDI-P Unstable defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the RDI-P Unstable defect condition.

NOTE: *The user can specify the value for RDI-P_THRD by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the Receive STM-0 Path - SDH Receive RDI-P Register (Address Location= 0x0293).*

BIT 1 - Loss of Pointer Indicator (LOP-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition.

The Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SDH frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STM-0 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive incoming STM-0 frames.

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT declaring the LOP-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition.

BIT 0 - Path AIS (AIS-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.·

- The H1, H2 and H3 bytes are set to an All Ones pattern.·
- The entire SPE is set to an All Ones pattern.

The Receive STM-0 POH Processor block will clear the AIS-P defect condition when it detects a valid STM-0 pointer (H1 and H2 bytes) and a set or normal NDF for three consecutive STM-0 frames.

- 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the AIS-P defect condition.
- 1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition

NOTE: *The Receive STM-0 POH Processor block will NOT declare the LOP-P defect condition if it detects an All Ones pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.*

TABLE 110: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT STATUS 2 (RPIS2 = 0X0289)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4 - Detection of AIS Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of AIS Pointer interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it detects an AIS Pointer in the incoming STM-0 data stream.

NOTE: *An AIS Pointer is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an All Ones pattern.*

- 0 - Indicates that the Detection of AIS Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of AIS Pointer interrupt has occurred since the last read of this register.

BIT 3 - Detection of Pointer Change Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Change Interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes).

- 0 - Indicates that the Detection of Pointer Change Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Change Interrupt has occurred since the last read of this register.

BIT 2 - Unused

BIT 1 - Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt

This RESET-upon-READ bit-field indicates whether or not the Change in TIM-P Defect Condition interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STM-0 POH Processor block declares the TIM-P defect condition.
- Whenever the Receive STM-0 POH Processor block clears the TIM-P defect condition.

- 0 - Indicates that the Change in TIM-P Defect Condition Interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in TIM-P Defect Condition Interrupt has occurred since the last read of this register.

BIT 0 - Change in Path Trace Identification Message Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Path Trace Message Unstable Defect Condition Interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STM-0 POH Processor block declare the Path Trace Message Unstable Defect Condition.
- Whenever the Receive STM-0 POH Processor block clears the Path Trace Message Unstable defect condition.

- 0 - Indicates that the Change in Path Trace Message Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in Path Trace Message Unstable Defect Condition Interrupt has occurred since the last read of this register.

TABLE 111: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT STATUS 1 (RPIS1 = 0X028A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - New Path Trace Message Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New Path Trace Message Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted (or validated) a new Path Trace Message.

- 0 - Indicates that the New Path Trace Message Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New Path Trace Message Interrupt has occurred since the last read of this register.

BIT 6 - Detection of REI-P Event Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of REI-P Event Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming STM-0 data-stream.

- 0 - Indicates that the Detection of REI-P Event Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of REI-P Event Interrupt has occurred since the last read of this register.

BIT 5 - Change in UNEQ-P (Path - Unequipped) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in UNEQ-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 POH Processor block declares the UNEQ-P Defect Condition.
- When the Receive STM-0 POH Processor block clears the UNEQ-P Defect Condition.

- 0 - Indicates that the Change in UNEQ-P Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in UNEQ-P Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STM-0 POH Processor block is currently declaring the UNEQ-P defect condition by reading out the state of BIT 5 (UNEQ-P Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 Register (Address Location= 0xN187).*

BIT 4 - Change in PLM-P (Path - Payload Mismatch) Defect Condition Interrupt Status

This RESET-upon-READ bit indicates whether or not the Change in PLM-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 POH Processor block declares the PLM-P Defect Condition.
- When the Receive STM-0 POH Processor block clears the PLM-P Defect Condition.

- 0 - Indicates that the Change in PLM-P Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in PLM-P Defect Condition Interrupt has occurred since the last read of this register.

BIT 3 - New C2 Byte Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New C2 Byte Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.

- 0 - Indicates that the New C2 Byte Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New C2 Byte Interrupt has occurred since the last read of this register.

BIT 2 - Change in C2 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in C2 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STM-0 POH Processor block declares the C2 Byte Unstable defect condition.
- When the Receive STM-0 POH Processor block clears the C2 Byte Unstable defect condition.

- 0 - Indicates that the Change in C2 Byte Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.

- 1 - Indicates that the Change in C2 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.

NOTE: The user can determine whether or not the Receive STM-0 POH Processor block is currently declaring the C2 Byte Unstable Defect Condition by reading out the state of BIT6 (C2 Byte Unstable Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 Register (Address Location= 0x0287).

BIT 1 - Change in RDI-P Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in RDI-P Unstable Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STM-0 POH Processor block declares an RDI-P Unstable defect condition.
- When the Receive STM-0 POH Processor block clears the RDI-P Unstable defect condition.

- 0 - Indicates that the Change in RDI-P Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in RDI-P Unstable Defect Condition Interrupt has occurred since the last read of this register.

NOTE: The user can determine the current state of RDI-P Unstable Defect condition by reading out the state of BIT 2 (RDI-P Unstable Defect Condition) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 Register (Address Location= 0x0287).

BIT 0 - New RDI-P Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New RDI-P Value interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it receives and validates a new RDI-P value.

- 0 - Indicates that the New RDI-P Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New RDI-P Value Interrupt has occurred since the last read of this register.

NOTE: The user can obtain the New RDI-P Value by reading out the contents of the RDI-P ACCEPT[2:0] bit-fields. These bit-fields are located in Bits 6 through 4, within the Receive STM-0 Path - SDH Receive RDI-P Register (Address Location= 0x0293).

TABLE 112: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT STATUS 0 (RPIS0 = 0X028B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Detection of B3 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B3 Byte Error Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STM-0 data stream.

- 0 - Indicates that the Detection of B3 Byte Error Interrupt has NOT occurred since the last read of this interrupt.
- 1 - Indicates that the Detection of B3 Byte Error Interrupt has occurred since the last read of this interrupt.

BIT 6 - Detection of New Pointer Interrupt Status

This RESET-upon-READ indicates whether the Detection of New Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STM-0 frame.

NOTE: *Pointer Adjustments with NDF will not generate this interrupt.*

- 0 - Indicates that the Detection of New Pointer Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of New Pointer Interrupt has occurred since the last read of this register.

BIT 5 - Detection of Unknown Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Unknown Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime that it detects a pointer that does not fit into any of the following categories.

- An Increment Pointer
- A Decrement Pointer
- An NDF Pointer
- An AIS (e.g., All Ones) Pointer
- New Pointer

- 0 - Indicates that the Detection of Unknown Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Unknown Pointer interrupt has occurred since the last read of this register.

BIT 4 - Detection of Pointer Decrement Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Decrement Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a Pointer Decrement event.

- 0 - Indicates that the Detection of Pointer Decrement interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Decrement interrupt has occurred since the last read of this register.

BIT 3 - Detection of Pointer Increment Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Increment Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a Pointer Increment event.

- 0 - Indicates that the Detection of Pointer Increment interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Increment interrupt has occurred since the last read of this register.

BIT 2 - Detection of NDF Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of NDF Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.

- 0 - Indicates that the Detection of NDF Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of NDF Pointer interrupt has occurred since the last read of this register.

BIT 1 - Change of LOP-P Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in LOP-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STM-0 POH Processor block declares the LOP-P defect condition.
- ·When the Receive STM-0 POH Processor block clears the LOP-P defect condition.

- 0 - Indicates that the Change in LOP-P Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in LOP-P Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition by reading out the state of BIT 1 (LOP-P Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 Register (Address Location=0x0287).*

BIT 0 - Change of AIS-P Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of AIS-P Defect Condition Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STM-0 POH Processor block declares the AIS-P defect condition.
- Whenever the Receive STM-0 POH Processor block clears the AIS-P defect condition.

- 0 - Indicates that the Change of AIS-P Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of AIS-P Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition by reading out the state of BIT 0 (AIS-P Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 Register (Address Location= 0x0287).*

TABLE 113: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT ENABLE 2 (RPIE2 = 0X028D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4 - Detection of AIS Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of AIS Pointer interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an AIS Pointer, in the incoming STM-0 data stream.

NOTE: *An AIS Pointer is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an All Ones Pattern.*

- 0 - Disables the Detection of AIS Pointer Interrupt.
- 1 - Enables the Detection of AIS Pointer Interrupt.

BIT 3 - Detection of Pointer Change Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Pointer Change Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.

- 0 - Disables the Detection of Pointer Change Interrupt.
- 1 - Enables the Detection of Pointer Change Interrupt.

BIT 2 - Unused

BIT 1 - Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt

This READ/WRITE bit-field is used to either enable or disable the Change in TIM-P Condition interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- If the TIM-P defect condition is declared.
- If the TIM-P defect condition is cleared.

- 0 - Disables the Change in TIM-P Defect Condition Interrupt.
- 1 - Enables the Change in TIM-P Defect Condition Interrupt.

BIT 0 - Change in Path Trace Message Unstable Defect Condition Interrupt Status

This READ/WRITE bit-field is used to either enable or disable the Change in Path Trace Message Unstable Defect Condition Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STM-0 POH Processor block declares the Path Trace Message Unstable Defect Condition.· Whenever the Receive STM-0 POH Processor block clears the Path Trace Message Unstable Defect Condition.

- 0 - Disables the Change in Path Trace Message Unstable Defect Condition interrupt.
- 1 - Enables the Change in Path Trace Message Unstable Defect Condition interrupt.

TABLE 114: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT ENABLE 1 (RPIE1 = 0X028E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-PValue Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - New Path Trace Message Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New Path Trace Message Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.

- 0 - Disables the New Path Trace Message Interrupt.
- 1 - Enables the New Path Trace Message Interrupt.

BIT 6 - Detection of REI-P Event Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of REI-P Event Interrupt.

If this interrupt is enabled, then he Receive STM-0 POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STM-0 data-stream.

- 0 - Disables the Detection of REI-P Event Interrupt.
- 1 - Enables the Detection of REI-P Event Interrupt.

BIT 5 - Change in UNEQ-P (Path - Unequipped) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in UNEQ-P Defect Condition interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions

- When the Receive STM-0 POH Processor block declares the UNEQ-P Defect Condition.
- When the Receive STM-0 POH Processor block clears the UNEQ-P Defect Condition.

- 0 - Disables the Change in UNEQ-P Defect Condition Interrupt.
- 1 - Enables the Change in UNEQ-P Defect Condition Interrupt.

BIT 4 - Change in PLM-P (Path - Payload Label Mismatch) Defect Condition Interrupt Enable

This READ/WRITE bit is used to either enable or disable the Change in PLM-P Defect Condition interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STM-0 POH Processor block declares the PLM-P defect Condition.
- Whenever the Receive STM-0 POH Processor block clears the PLM-P defect Condition.

- 0 - Disables the Change in PLM-P Defect Condition Interrupt.
- 1 - Enables the Change in PLM-P Defect Condition Interrupt.

BIT 3 - New C2 Byte Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New C2 Byte Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.

- 0 - Disables the New C2 Byte Interrupt.
- 1 - Enables the New C2 Byte Interrupt.

NOTE: *The user can obtain the value of this New C2 byte by reading the contents of the Receive STM-0 Path - Received Path Label Value Register (Address Location= 0x0296).*

BIT 2 - Change in C2 Byte Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in C2 Byte Unstable Condition Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STM-0 POH Processor block declares the C2 Byte Unstable defect condition.
- When the Receive STM-0 POH Processor block clears the C2 Byte Unstable defect condition.

- 0 - Disables the Change in C2 Byte Unstable Defect Condition Interrupt.
- 1 - Enables the Change in C2 Byte Unstable Defect Condition Interrupt.

BIT 1 - Change in RDI-P Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in RDI-P Unstable Defect Condition interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STM-0 POH Processor block declares the RDI-P Unstable defect condition.
- Whenever the Receive STM-0 POH Processor block clears the RDI-P Unstable defect condition.

- 0 - Disables the Change in RDI-P Unstable Defect Condition Interrupt.
- 1 - Enables the Change in RDI-P Unstable Defect Condition Interrupt.

BIT 0 - New RDI-P Value Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New RDI-P Value interrupt.If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it receives and validates a new RDI-P value.

- 0 - Disables the New RDI-P Value Interrupt.
- 1 - Enable the New RDI-P Value Interrupt.

TABLE 115: RECEIVE STM-0 PATH - SDH RECEIVE PATH INTERRUPT ENABLE 0 (RPIE0 = 0X028F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte ErrorInter-ruptEnable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Inter-rupt Enable	Detection of Pointer Dec-rement Inter-rupt Enable	Detection of Pointer IncrementIn-terrupt Enable	Detection of NDF Pointer-Interrupt Enable	Change of LOP-P DefectCondi-tion Interrupt Enable	Change of AIS-P DefectCondi-tionInterrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Detection of B3 Byte Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of B3 Byte Error Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STM-0 data-stream.

- 0 - Disables the Detection of B3 Byte Error interrupt.
- 1 - Enables the Detection of B3 Byte Error interrupt.

BIT 6 - Detection of New Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of New Pointer interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STM-0 frame.

NOTE: *:Pointer Adjustments with NDF will not generate this interrupt.*

- 0 - Disables the Detection of New Pointer Interrupt.
- 1 - Enables the Detection of New Pointer Interrupt.

BIT 5 - Detection of Unknown Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Unknown Pointer interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a Pointer Adjustment that does not fit into any of the following categories.· An Increment Pointer.· A Decrement Pointer· An NDF Pointer· AIS Pointer· New Pointer.

- 0 - Disables the Detection of Unknown Pointer Interrupt.
- 1 - Enables the Detection of Unknown Pointer Interrupt.

BIT 4 - Detection of Pointer Decrement Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the Detection of Pointer Decrement Interrupt.

If this interrupt is enabled, then the Receive STM-0 TOH Processor block will generate an interrupt anytime it detects a Pointer-Decrement event.

- 0 - Disables the Detection of Pointer Decrement Interrupt.
- 1 - Enables the Detection of Pointer Decrement Interrupt.

BIT 3 - Detection of Pointer Increment Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Pointer Increment Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a Pointer Increment event.

- 0 - Disables the Detection of Pointer Increment Interrupt.
- 1 - Enables the Detection of Pointer Increment Interrupt.

BIT 2 - Detection of NDF Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of NDF Pointer Interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.

- 0 - Disables the Detection of NDF Pointer interrupt.
- 1 - Enables the Detection of NDF Pointer interrupt.

BIT 1 - Change of LOP-P Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in LOP (Loss of Pointer) Condition interrupt. If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STM-0 POH Processor block declares the LOP-P defect condition condition.
- When the Receive STM-0 POH Processor block clears the LOP-P defect condition.

- 0 - Disable the Change of LOP-P Defect Condition Interrupt.
- 1 - Enables the Change of LOP-P Defect Condition Interrupt.

NOTE: *The user can determine the current state of the LOP-P Defect condition by reading out the contents of BIT 1 (LOP-P Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 (Address Location= 0x0287).*

BIT 0 - Change of AIS-P Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of AIS-P (Path AIS) Defect Condition interrupt.

If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STM-0 POH Processor block declares the AIS-P Defect condition.
- When the Receive STM-0 POH Processor block clears the AIS-P Defect condition.

- 0 - Disables the Change of AIS-P Defect Condition Interrupt.
- 1 - Enables the Change of AIS-P Defect Condition Interrupt.

NOTE: *The user can determine the current state of the AIS-P Defect Condition by reading out the contents of BIT 0 (AIS-P Defect Declared) within the Receive STM-0 Path - SDH Receive POH Status - Byte 0 (Address Location= 0x0287).*

TABLE 116: RECEIVE STM-0 PATH - SDH RECEIVE RDI-P REGISTER (RRDIPR = 0X0293)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT [6:4] - Accepted RDI-P Value

These READ-ONLY bit-fields contain the value of the most recently accepted RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive STM-0 POH Processor block.

NOTE: *A given RDI-P value will be accepted by the Receive STM-0 POH Processor block, if this RDI-P value has been consistently received in RDI-P THRESHOLD[3:0] number of STM-0 frames.*

BIT [3:0] - RDI-P Threshold[3:0]

These READ/WRITE bit-fields are used to defined the RDI-P Acceptance Threshold for the Receive STM-0 POH Processor Block.

The RDI-P Acceptance Threshold is the number of consecutive STM-0 frames, in which the Receive STM-0 POH Processor block must receive a given RDI-P value, before it accepts or validates it.

The most recently accepted RDI-P value is written into the RDI-P ACCEPT[2:0] bit-fields, within this register.

TABLE 117: RECEIVE STM-0 PATH - RECEIVED PATH LABEL VALUE (RPLV = 0X0296)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT [7:0] - Received Filtered C2 Byte Value

These READ-ONLY bit-fields contain the value of the most recently accepted C2 byte, via the Receive STM-0 POH Processor block.

The Receive STM-0 POH Processor block will accept a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive STM-0 frames.

NOTE: *The Receive STM-0 POH Processor block uses this register, along the Receive STM-0 Path - Expected Path Label Value Register (Address Location = 0x0297), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

TABLE 118: RECEIVE STM-0 PATH - EXPECTED PATH LABEL VALUE (EPLV = 0X0297)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - Expected C2 Byte Value

These READ/WRITE bit-fields are used to specify the C2 (Path Label Byte) value, that the Receive STM-0 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions.

If the contents of the Received C2 Byte Value[7:0] (see Receive STM-0 Path - Received Path Label Value register) matches the contents in these register, then the Receive STM-0 POH will not declare any defect conditions.

NOTE: *The Receive STM-0 POH Processor block uses this register, along with the Receive STM-0 Path - Receive Path Label Value Register (Address Location = 0x0296), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

TABLE 119: RECEIVE STM-0 PATH - B3 BYTE ERROR COUNT REGISTER 3 (B3BECR3 = 0X0298)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STM-0 Path - B3 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.

NOTES:

1. *If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.*
2. *If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.*

TABLE 120: RECEIVE STM-0 PATH - B3 BYTE ERROR COUNT REGISTER 2 (B3BECR2 = 0X0299)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STM-0 Path - B3 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.

NOTES:

1. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.

2. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.

TABLE 121: RECEIVE STM-0 PATH - B3 BYTE ERROR COUNT REGISTER 1 (B3BECR1 = 0X029A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STM-0 Path - B3 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.

NOTES:

1. *If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.*
2. *If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.*

TABLE 122: RECEIVE STM-0 PATH - B3 BYTE ERROR COUNT REGISTER 0 (B3BECR0 = 0X029B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive STM-0 Path - B3 Byte Error Count Register - Bytes 3 through 1 function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.

NOTES:

1. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.

2. f the Receive STM-0 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.

TABLE 123: RECEIVE STM-0 PATH - REI-P EVENT COUNT REGISTER 3 (REIPECR3 = 0X029C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - MSB

This RESET-upon-READ register, along with Receive STM-0 Path - REI-P Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path - Remote Error Indicator event within the incoming STM-0 SPE data-stream.

NOTES:

1. *If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STM-0 SPE.*
2. *If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains a non-zero REI-P value.*

TABLE 124: RECEIVE STM-0 PATH - REI-P EVENT COUNT REGISTER 2 (REIPECR2 = 0X029D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STM-0 Path - REI-P Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path - Remote Error Indicator event within the inconing STM-0 SPE data-stream.

NOTES:

1. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STM-0 frame.

2. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains a non-zero REI-P value.

TABLE 125: RECEIVE STM-0 PATH - REI-P EVENT COUNT REGISTER 1 (REIPECR1 = 0X029E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STM-0 Path - REI-P Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path - Remote Error Indicator event within the incoming STM-0 SPE data-stream.

NOTES:

1. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STM-0 SPE.

2. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains a non-zero REI-P value

TABLE 126: RECEIVE STM-0 PATH - REI-P EVENT COUNT REGISTER 0 (REIPECR0 = 0X029F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - LSB

This RESET-upon-READ register, along with Receive STM-0 Path - REI-P Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path - Remote Error Indicator event within the incoming STM-0 SPE data-stream.

NOTES:

1. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.

2. If the Receive STM-0 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains a non-zero REI-P value.

TABLE 127: RECEIVE STM-0 PATH - RECEIVE PATH TRACE MESSAGE BUFFER CONTROL REGISTER (RPTMBCR = 0X02A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		New Message Ready	Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Type	Receive Path Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BIT 5 - New Message Ready

This READ/WRITE bit-field indicates whether or not the Receive Path Trace Message buffer has received a new expected value.

- 0 - Indicates NO new expected value has been downloaded into the receive J1 trace buffer.
- 1 - Indicates a new expected value has been downloaded into the receive J1 trace buffer and can be used to make comparisons with the accepted J1 message.

BIT 4 - Receive Section Trace Message Buffer Read Selection

This READ/WRITE bit-field is used to specify which of the following Receive Path Trace Message buffer segments to read.

a. The Actual Receive Path Trace Message Buffer. The Actual Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STM-0 data-stream.

b. The Expected Receive Path Trace Message Buffer. The Expected Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user expects to receive. The contents of this particular buffer are usually specified by the user.

- 0 - Executing a READ to the Receive J1 Trace Buffer, will return contents within the Valid Message buffer.
- 1 - Executing a READ to the Receive J1 Trace Buffer, will return contents within the Expected Message Buffer.

NOTE: *In the case of the Receive STM-0 POH Processor block, the Receive J1 Trace Buffer is located at Address Location 0x0500 through 0x053F.*

BIT 3 - Path Trace Message Accept Threshold

This READ/WRITE bit-field is used to select the number of consecutive times that the Receive STM-0 POH Processor block must receive a given Receive Trace Message, before it is accepted and loaded into the Receive Path Trace Message.

- 0 - The Receive STM-0 POH Processor block accepts the Path Trace Message after it has received it the third time in succession.
- 1 - The Receive SDH POH Processor block accepts the incoming Path Trace Message after it has received in the fifth time in succession.

BIT 2 - Path Trace Message Alignment Type

This READ/WRITE bit-field is used to specify have the Receive STM-0 POH Processor block will locate the boundary of the J1 Trace Message.

- 0 - Message boundary is indicated by Line Feed.
- 1 - Message boundary is indicated by the presence of a 1 in the MSB of a the first byte (within the J1 Trace Message).

BIT [1:0] - Path Trace Message Length[1:0]

These READ/WRITE bit-fields are used to specify the length of the Receive Path Trace Message that the Receive STM-0 POH Processor block will receive. The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.

Receive Trace Path Message Length

MSG LENGTH[1:0]	RESULTING PATH TRACE MESSAGE LENGTH
00	1 Byte
01	16 Bytes
10/11	64 Bytes

TABLE 128: RECEIVE STM-0 PATH - POINTER VALUE 1 (PV1 = 0X02A6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Current_Pointer Val-ueMSB[9:8]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - Current Pointer Value - MSB

These READ-ONLY bit-fields, along with that from the Receive STM-0 Path - Pointer Value - Byte 0 Register combine to reflect the current value of the pointer that the Receive STM-0 POH Processor block is using to locate the SPE within the incoming STM-0 data stream.Note

These register bits comprise the Upper Byte value of the Pointer Value.

TABLE 129: RECEIVE STM-0 PATH - POINTER VALUE 0 (PV0 = 0X02A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Current Pointer Value - LSB

These READ-ONLY bit-fields, along with that from the Receive STM-0 Path - Pointer Value - Byte 1 Register combine to reflect the current value of the pointer that the Receive STM-0 POH Processor block is using to locate the SPE within the incoming STM-0 data stream.Note

These register bits comprise the Lower Byte value of the Pointer Value.

TABLE 130: RECEIVE STM-0 PATH - RECEIVE AUTO AIS - C2 BYTE VALUE REGISTER (AISC2VR = 0X02B9)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Defect_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Defect_C2_Byte_Value[7:0]

These READ/WRITE bit-fields are used to configure the Receive STM-0 POH Processor block to automatically force the transmission of the E1 AIS pattern (in the Egress Direction of all 28 channels) anytime it accepts a C2 byte value matching that written into this register.

NOTE: *The chip will only automatically transmit the E1 AIS Pattern if BIT 1 (Defect C2 Byte Downstream AIS Enable), within the Receive STM-0 Path - Receive Auto AIS - C2 Byte Control Register is set to 1.*

TABLE 131: RECEIVE STM-0 PATH - RECEIVE AUTO AIS - C2 BYTE CONTROL REGISTER (AISC2CR = 0X02BA)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Defect C2 Byte Down-stream AIS Enable	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT 1] - Defect C2 Byte Downstream AIS Enable

This bit enables downstream AIS insertion when the received C2 matches the C2 defect value specified in the Defect_C2_Value.

- 0 - Disable
- 1 - Enable

BIT 0 - Unused

TABLE 132: RECEIVE STM-0 PATH - AUTO AIS CONTROL REGISTER (AUTOACR = 0X02BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (Down-stream) Upon C2 Byte Unstable	Transmit AIS-P (Down-stream) Upon UNEQ-P	Transmit AIS-P (Down-stream) Upon PLM-P	Transmit AIS-P (Down-stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down-stream) upon TIM-P	Transmit AIS-P (Down-stream) upon LOP-P	Transmit AIS-P (Down-stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Transmit Path AIS (Downstream) upon Declaration of the Unstable C2 Byte Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the Unstable C2 Byte Defect condition within the incoming STM-0 data-stream.

- 0 - Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Unstable C2 Byte defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Unstable C2 Byte defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 5 - Transmit Path AIS (Downstream) upon Declaration of the UNEQ-P (Path - Unequipped) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the UNEQ-P defect condition.

- 0 - Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the UNEQ-P defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the UNEQ-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 4 - Transmit Path AIS (Downstream) upon Declaration of the PLM-P (Path - Payload Label Mismatch) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the PLM-P defect condition.

- 0 - Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the PLM-P defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the PLM-P defect condition.Note

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 3 - Transmit Path AIS (Downstream) upon declaration of the Path Trace Message Unstable Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the

incoming STM-0 data-stream.

- 0 - Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Path Trace Message Unstable defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Path Trace Message Unstable defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 2 - Transmit Path AIS (Downstream) upon declaration of the TIM-P (Path Trace Message Identification Mismatch) defect condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the TIM-P defect condition within the incoming STM-0 data-stream.

- 0 - Does not configure the Receive STM-0 POH Processor block to transmit the AIS-P indicator (via the downstream traffic) whenever it declares the TIM-P defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to transmit the AIS-P indicator (via the downstream traffic) whenever it declares the TIM-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 1 - Transmit Path AIS (Downstream) upon Detection of Loss of Pointer (LOP-P) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STM-0 data-stream.

- 0 - Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards the corresponding Transmit SDH POH Processor block) whenever it declares the LOP-P defect condition.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards the corresponding Transmit SDH POH Processor block) whenever it declares the LOP-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 0 - Automatic Transmission of AIS-P Enable

This READ/WRITE bit-field serves two purposes.

- It is used to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS indicator, via the down-stream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks), upon detection of an UNEQ-P, PLM-P, LOP-P or LOS conditions.
- It also is used to configure the Receive STM-0 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit E1 Framer blocks) anytime it detects an AIS-P condition in the incoming STM-0 data-stream.

- 0 - Configures the Receive STM-0 POH Processor block to NOT automatically transmit the AIS-P indicator (via the downstream traffic, towards each of the 28 Egress Direction Transmit E1 Framer blocks) whenever it declares any of the above-mentioned defect conditions.
- 1 - Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards each of the 28 Egress Direction Transmit E1 Framer blocks) whenever it declares any of the above-mentioned defect condition.

NOTE: *The user must also set the corresponding bit-fields (within this register) to 1 in order to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/ defect condition.*

TABLE 133: RECEIVE STM-0 PATH - SDH RECEIVE AUTO ALARM REGISTER (RAAR = 0X02C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS (via Downstream T1/E1s) upon LOP-P	Transmit AIS (via Down-stream T1/ E1s) upon-PLM-P	Unused	Transmit AIS (via Down-stream T1/ E1s) upon UNEQ-P	Transmit AIS (via Down-stream T1/ E1s) upon TIM-P	Transmit AIS (via Down-stream T1/ E1s) upon AIS-P	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the LOP-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the LOP-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime the Receive STM-0 POH Processor block declares the LOP-P defect.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the LOP-P defect.

BIT 5 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the PLM-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the PLM-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime the Receive STM-0 POH Processor block declares the PLM-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the PLM-P defect condition.

BIT 4 - Unused

BIT 3 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the UNEQ-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the UNEQ-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime the Receive STM-0 POH Processor block declares the UNEQ-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the UNEQ-P defect condition.

BIT 2 - Transmit E1 AIS (via Downstream T1/E1s) upon declaration of the TIM-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the TIM-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime the Receive STM-0 POH Processor block declares the TIM-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares

the TIM-P defect condition.

BIT 1 - Transmit E1 AIS (via Downstream T1/E1s) upon AIS-P

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the AIS-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the E1 AIS Indicator via the downstream E1 signal, anytime the Receive STM-0 POH Processor block declares the AIS-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit E1 Framer blocks to automatically transmit the AIS-P Indicator via the downstream E1 signals, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the AIS-P defect condition.

BIT 0 - Unused

TABLE 134: RECEIVE STM-0 PATH - RECEIVE NEGATIVE POINTER ADJUSTMENT COUNT REGISTER 1 (RNPACR1 = 0X02C4)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Negative Pointer Adjustment Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Negative Pointer Adjustment Count - MSB

These RESET-upon-READ bits, along with that in Receive STM-0 Path - Receive Negative Pointer Adjustment Count Register - Byte 0 present a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that the Receive STM-0 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 135: RECEIVE STM-0 PATH - RECEIVE NEGATIVE POINTER ADJUSTMENT COUNT REGISTER 0 (RNPACR0 = 0X02C5)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Negative Pointer Adjustment Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Negative Pointer Adjustment Count - LSB

These RESET-upon-READ bits, along with that in Receive STM-0 Path - Receive Negative Pointer Adjustment Count Register - Byte 1 present a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that the Receive STM-0 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

TABLE 136: RECEIVE STM-0 PATH - RECEIVE POSITIVE POINTER ADJUSTMENT COUNT REGISTER 1 (RPPACR1 = 0X02C6)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Positive Pointer Adjustment Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Positive Pointer Adjustment Count - MSB

These RESET-upon-READ bits, along with that in Receive STM-0 Path - Receive Positive Pointer Adjustment Count Register - Byte 0 present a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that the Receive STM-0 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 137: RECEIVE STM-0 PATH - RECEIVE POSITIVE POINTER ADJUSTMENT COUNT REGISTER 0 (RPPACR0 = 0X02C7)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Positive Pointer Adjustment Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Positive Pointer Adjustment Count - LSB

These RESET-upon-READ bits, along with that in Receive STM-0 Path - Receive Positive Pointer Adjustment Count Register - Byte 1 present a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that the Receive STM-0 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

TABLE 138: RECEIVE STM-0 PATH - RECEIVE J1 BYTE CAPTURE REGISTER (RJ1BCR = 0X02D3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - J1 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new J1 byte value.

TABLE 139: RECEIVE STM-0 PATH - RECEIVE B3 BYTE CAPTURE REGISTER (RB3BCR = 0X02D7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new B3 byte value.

TABLE 140: RECEIVE STM-0 PATH - RECEIVE C2 BYTE CAPTURE REGISTER (RC2BCR = 0X02DB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - C2 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new C2 byte value.

TABLE 141: RECEIVE STM-0 PATH - RECEIVE G1 BYTE CAPTURE REGISTER (RG1BCR = 0X02DF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - G1 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new G1 byte value.

TABLE 142: RECEIVE STM-0 PATH - RECEIVE F2 BYTE CAPTURE REGISTER (RF2BCR = 0X02E3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - F2 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new F2 byte value.

TABLE 143: RECEIVE STM-0 PATH - RECEIVE H4 BYTE CAPTURE REGISTER (RH4BCR = 0X02E7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - H4 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new H4 byte value.

TABLE 144: RECEIVE STM-0 PATH - RECEIVE Z3 BYTE CAPTURE REGISTER (RZ3BCR = 0X02EB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z3 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new Z3 byte value.

TABLE 145: RECEIVE STM-0 PATH - RECEIVE Z4 (K3) BYTE CAPTURE REGISTER (RZ4BCR = 0X02EF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z4 (K3) Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new Z4 (K3) byte value.

TABLE 146: RECEIVE STM-0 PATH - RECEIVE Z5 BYTE CAPTURE REGISTER (RZ5BCR = 0X02F3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z5 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STM-0 frame.

This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new Z5 byte value.

6.6 Transmit Transport Overhead Port Control Register Descriptions

TABLE 147: TRANSMIT STM-0 SECTION CONTROL REGISTER 3 (TSCR3 0X0700H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved				CNTL_PTR[3:0]			
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT [3:0] - Control Pointer [3:0]

This pointer value is used to select the slot in current TxSOH group (up to 3) to be programmed.

- 0000 - Slot 0
- 0001 - Slot 1
- 0010 - Slot 2
- 0011 - 1111 - Not Used

TABLE 148: TRANSMIT STM-0 SECTION CONTROL REGISTER 2 (TSCR2 0X0701H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					AUTO MS-AIS_En	RSDCC Relocate	MSDCC Relocate
RO	RO	RO	RO	RO	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Multiplex Section AUTO AIS Alarm Enable

When enabled, the MS-AIS will be automatically inserted upon receiving MS-AIS alarm from upstream.

- 0 - Disabled
- 1 - AUTO MS-AIS Enabled

BIT 1 - Regenerator Section Data Communication Channel Relocate

SOH passthrough must be enabled for this bit to have function. The first channel upstream RSDCC (D1,D2,D3) will be mapped to RSDCC location of the second slot of this channel. For example, the RSDCC of a STM1 AU4 input stream for slot 0 will be inserted into slot 4 which is the second slot of this STM1. The RSDCC for slot 0 will be inserted internally either through external interface or internal register.

- 0 - Disabled
- 1 - Relocate RSDCC (D1,D2,D3)

BIT 0 - Multiplex Section Data Communication Channel Relocate

SOH passthrough must be enabled for this bit to have function. The first channel upstream MSDCC (D4-D12) will be mapped to MSDCC location of the second slot of this channel. For example, the MSDCC of a STM1 AU4 input stream for slot 0 will be inserted into slot 4 which is the second slot of this STM1. The MSDCC for slot 0 will be inserted internally either through external interface or internal register.

- 0 - Disabled
- 1 - Relocate MSDCC (D4-D12)

TABLE 149: TRANSMIT STM-0 SECTION CONTROL REGISTER 1 (TSCR1 0X0702H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	STM-N Overhead Insert	E2 Insert Method	E1 Insert Method	F1 Insert Method	S1 Insert Method	K1K2 Insert Method	M0M1 Insert Method [1]
RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - STM-N Overhead Insert

This READ/WRITE bit-field permits the user to configure the TxSOH input port to insert the SOH for the outbound STM-0 or STM-1 signal.

- 0 - Disabled
- 1 - Enabled

BIT 5 - E2 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the E2 byte, within the transmit output STM-0 or STM-1 data stream.

- 0 - E2 Byte is obtained from TxSOH Serial Input Port.
- 1 - E2 Byte is obtained from the contents within the Transmit Section - E2 Byte Value register (Address Location = 0x0747). This selection provides the user with software control over the value of the outbound E2 byte.

BIT 4 - E1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the E1 byte, within the transmit output STM-0 or STM-1 data stream.

- 0 - E1 Byte is obtained from TxSOH Serial Input Port.
- 1 - E1 Byte is obtained from the contents within the Transmit Section - E1 Byte Value register (Address Location= 0x0743). This selection provides the user with software control over the value of the outbound E1 byte.

BIT 3 - F1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the F1 byte, within the transmit output STM-0 data stream.

- 0 - F1 Byte is obtained from TxSOH Serial Input Port.
- 1 - F1 Byte is obtained from the contents within the Transmit Section - F1 Byte Value register (Address Location= 0x073F). This selection provides the user with software control over the value of the outbound F1 byte.

BIT 2 - S1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the S1 byte, within the transmit output STM-0 data stream.

- 0 - S1 Byte is obtained from TxSOH Serial Input Port.
- 1 - S1 Byte is obtained from the contents within the Transmit Section - S1 Byte Value register (Address Location= 0x073B). This selection provides the user with software control over the value of the outbound S1 byte.

BIT 1 - K1K2 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the K1 and K2 bytes, within the transmit output STM-0 data stream.

- 0 - K1 and K2 Bytes are obtained from TxSOH Serial Input Port.
- 1 - K1 and K2 Bytes are obtained from the contents within the Transmit Section - K2 Byte Value register - Byte 1 (Address Location= 0x072E) and the Transmit Section - K1 Byte Value register - Byte 0 (Address Location= 0x072F). This selection provides the user with software control over the value of the outbound K1 and K2 bytes.

BIT 0 - M0M1 Byte Insert Method [1]

This READ/WRITE bit-field, along with M0M1 Insert Method[0] (located in the next Register 0x0703h) are used to specify the source of the contents of the M0/M1 byte, within the transmit output STM-0 data stream. The relationship between these two bit-fields and the corresponding source of the M0/M1 byte is presented below.

TABLE 150: SOURCE OF M0/M1 BYTE

M0M1 INSERT METHOD [1:0]		SOURCE OF M0/M1 BYTE
0	0	From the Receive STM-0 SOH Processor Block (B2 Byte Error Count).
0	1	Obtained from the contents of the Transmit STM-0 Section - M0/M1 Byte Value register (Address Location = 0x0737).
1	0	M0/M1 Byte is obtained from the TxSOH Serial Input Port.
1	1	From the Receive STM-0 SOH Processor Block (B2 Byte Error Count).

TABLE 151: TRANSMIT STM-0 SECTION CONTROL REGISTER 0 (TSCR0 0X0703H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
M0M1 Insert Method [0]	UDFN SOH Value	Force MS-RDI	Force MS-AIS	Force LOS Pattern	Scramble Enable	B2 Byte Error Insert	A1A2 Byte Error Insert
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - M0M1 Byte Insert Method [0]

This READ/WRITE bit-field, along with M0M1 Insert Method[1] (located in the Transmit Section - SDH Control Register - Byte 1) are used to specify the source of the contents of the M0/M1 byte, within the transmit output STM-0 data stream. The relationship between these two bit-fields and the corresponding source of the M0/M1 byte is presented below.

Source of M0/M1 Byte

M0M1 INSERT METHOD [1:0]		SOURCE OF M0/M1 BYTE
0	0	From the Receive STM-0 SOH Processor Block (B2 Byte Error Count).
0	1	Obtained from the contents of the Transmit STM-0 Section - M0/M1 Byte Value register (Address Location = 0x0737).
1	0	M0/M1 Byte is obtained from the TxSOH Serial Input Port.
1	1	From the Receive STM-0 SOH Processor Block (B2 Byte Error Count).

BIT 6 - Undefined Section Overhead Byte Value Assignment

This READ/WRITE bit-field specifies the value assigned to the undefined Section Overhead Bytes.

- 0 - Undefined Section Overhead Bytes will be assigned the value 0x00.
- 1 - Undefined Section Overhead Bytes will be assigned the value 0xFF.

BIT 5 - Force Multiplex Section - Remote Defect Indicator

This READ/WRITE bit-field is used to (by software control) force the Transmit STM-0 SOH Processor Block to generate and transmit the MS-RDI indicator to the remote terminal equipment by forcing bits-2, 1, and 0 of the K2 byte to the value 3'b110.

- 0 - Normal Operation.
- 1 - Force MS-RDI.

NOTE: *This bit-field is ignored if the Transmit STM-0 SOH Processor Block is currently transmitting the Mutiplex Section AIS (MS-AIS) indicator or LOS pattern.*

BIT 4 - Force Multiplex Section - Alarm Indication Signal

This READ/WRITE bit-field is used to (by software control) force the Transmit STM-0 SOH Processor Block to generate and transmit the MS-AIS indicator to the remote terminal equipment.

- 0 - Normal Operation.
- 1 - Force MS-AIS.

NOTE: *This bit-field is ignored if the Transmit STM-0 SOH Processor Block is transmitting the LOS pattern.*

BIT 3 - Force LOS Pattern

This READ/WRITE bit-field is used to (by software control) force the Transmit STM-0 SOH Processor Block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment.

- 0 - Normal Operation.
- 1 - Configures the Transmit STM-0 SOH Processor Block to transmit the LOS pattern. In this case, the Transmit STM-0 SOH Processor Block will force all bytes (within the outbound SDH frame) to an All Zeros pattern.

BIT 2 - Scramble Enable

This READ/WRITE bit-field is used to either enable or disable the Scrambler, within the Transmit STM-0 SOH Processor Block circuitry.

- 0 - Disables the Scrambler.
- 1 - Enables the Scrambler.

BIT 1 - B2 Byte Error Insert Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to insert errors into the outbound B2 bytes, per the contents within the Transmit STM-0 Section - Transmit B2 Byte Error Mask Register.

- 0 - Normal Operation.
- 1 - Configures the Transmit STM-0 SOH Processor Block to insert into the B2 bytes (per the contents within the Transmit B2 Byte Error Mask Register).

BIT 0 - A1A2 Byte Error Insert Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to insert errors into the outbound A1 and A2 bytes, within the outbound STM-0 or STM-1 data-stream.

- 0 - Normal Operation.
- 1 - Configures the Transmit STM-0 SOH Processor Block to insert errors into the A1 and A2 bytes (per the contents within the “Transmit A1 Byte Error Mask” and “Transmit A2 Byte Error Mask” Registers.

TABLE 152: TRANSMIT STM-0 SECTION A1 BYTE ERROR MASK (TSA1EM 0X0717H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved							STM-0 Channel 0 A1 Byte Error Enable
RO	RO	RO	RO	RO	RO	RO	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Reserved

BIT 0 - STM-0 Channel 0 - A1 Byte Error Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to transmit a continuous stream of STM-0 frames, in which the A1 byte is erred by inverting the A1 byte to the value 0x09.

- 0 - Normal Operation
- 1 - Configures the Transmit STM-0 SOH Processor Block to transmit STM-0 frames with erred A1 bytes.

NOTE: *This bit-field is only valid if Bit-0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SDH Transmit Control Register – Byte 0 (Address Location= 0x0703) is set to "1".*

TABLE 153: TRANSMIT STM-0 SECTION A2 BYTE ERROR MASK (TSA2EM 0X071FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved							STM-0 Channel 0 A2 Byte Error Enable
RO	RO	RO	RO	RO	RO	RO	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Reserved

BIT 0 - STM-0 Channel 0 - A2 Byte Error Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to transmit a continuous stream of STM-0 frames, in which the A2 byte is erred by inverting the A2 byte to the value 0xD7.

- 0 - Normal Operation
- 1 - Configures the Transmit STM-0 SOH Processor Block to transmit STM-0 frames with erred A2 bytes.

NOTE: *This bit-field is only valid if Bit-0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SDH Transmit Control Register – Byte 0 (Address Location= 0x0703) is set to "1".*

TABLE 154: TRANSMIT STM-0 SECTION B1 BYTE ERROR MASK (TSB1EM 0X0723H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Transmit B1 Byte Error Mask [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Mask [7:0]

These READ/WRITE bit-fields are used to insert bit errors into the B1 bytes, within the outbound STM-0 data stream. The Transmit STM-0 SOH Processor Block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the outbound STM-0 data stream. For each bit-field (within this register) that is set to 1, the corresponding bit, within the B1 byte will be in error.

NOTE: *For normal operation, the user should set this register to 0x00.*

TABLE 155: TRANSMIT STM-0 SECTION B2 BYTE SELECT ERROR ENABLE (TSB2SEE 0X0727H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
							STM-0 Channel 0 B2 Byte Error Enable
RO	RO	RO	RO	RO	RO	RO	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Reserved

BIT 0 - STM-0 Channel 0 - B2 Byte Error Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to perform the XOR operation with the contents of the Transmit STM-0 Section -Transmit B2 Bit Error Mask Register (Address Location = 0x072B)

- 0 - Normal Operation
- 1 - Enables the XOR operation. In this setting, the Transmit STM-0 SOH Processor will perform the XOR operation of the value of the B2 byte (within the outbound STM-0 frame) with the contents within the Transmit STM-0 Section - Transmit B2 Bit Error Mask register.

NOTE: *This bit-field is only valid if BIT 1 (B2 Byte Error Insert), within the "Transmit STM-0 Section – SDH Transmit Control Register – Byte 0 (Address = 0x0703) set to "1".*

TABLE 156: TRANSMIT STM-0 SECTION B2 BYTE ERROR MASK (TSB2EM 0X072BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Transmit B2 Byte Error Mask [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit B2 Byte Error Mask [7:0]

These READ/WRITE bit-fields are used to insert B2 byte errors into the outbound STM-0 data-stream, for diagnostic purposes.

For the selected STM-0 channel (Transmit B2 Byte Select Error Enable) within the Transmit STM-0 Section - Transmit B2 Byte Error Register (Address Location = 0x0727) that is set to 1, then Transmit STM-0 SOH Processor Block will be configured to perform an XOR operation between the contents of this register, with the contents of the selected STM-0 channel outbound B2 byte. The results of this calculation is written back into the B2 byte position, within the outbound STM-0 frame. Hence, for every bit (within this register) that is set to 1, the corresponding bit (within the outbound B2 byte) will be erred.

NOTES:

1. *For normal (e.g., un-erred) operation, the user should ensure that this register is set to the value 0x00.*
2. *These register bits are ignored unless an STM-0 channel is selected (Transmit B2 Byte Select Error Enable), within the Transmit STM-0 Section - Transmit B2 Byte Error Register has been set to "1".*
3. *This bit-field is only valid if BIT 1 (B2 Byte Error Insert), within the "Transmit STM-0 Section – SDH Transmit Control Register – Byte 0 (Address = 0x0703) set to "1".*

TABLE 157: TRANSMIT STM-0 SECTION K2 BYTE VALUE REGISTER (TSK2VR 0X072EH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Transmit K2 Byte Value [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit K2 Byte Value

If the appropriate K1K2 Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the K2 byte, within the outbound STM-0 signal.

NOTE: *If BIT 1 (K1K2 Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STM-0 SOH Processor Block will load the contents of this register into the K2 byte-field, within each outbound STM-0 frame. These register bits are ignored if BIT 1 (K1K2 Insert Method) is set to 0.*

TABLE 158: TRANSMIT STM-0 SECTION K1 BYTE VALUE REGISTER (TSK1VR 0X072FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Transmit K1 Byte Value [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit K1 Byte Value

If the appropriate K1K2 Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the K1 byte, within the outbound STM-0 signal.

If BIT 1 (K1K2 Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STM-0 SOH Processor Block will load the contents of this register into the K1 byte-field, within each outbound STM-0 frame. These register bits are ignored if BIT 1 (K1K2 Insert Method) is set to 0.

TABLE 159: TRANSMIT STM-0 SECTION MS-RDI CONTROL REGISTER (TSMSRDICR 0X0733H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved				External MS-RDI Enable	Transmit MS-RDI upon MS-AIS	Transmit MS-RDI upon LOF	Transmit MS-RDI upon LOS
RO	RO	RO	RO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT 3 - External Multiplex Section Remote Defect Indicator Enable

This READ/WRITE bit-field is used to externally insert the value for bits 6, 7 and 8 (of the K2 byte) into the outbound STM-0 data stream. If the user enables this feature, then the user can enable or disable the insertion of the MS-RDI indicator, via the TxSOH_n input pin.

- 0 - Disables this feature.
- 1 - Enables this feature.

BIT 2 - Transmit Multiplex Section Remote Defect Indicator (MS-RDI) upon Detection of MS-AIS

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to automatically transmit an MS-RDI indicator to the remote terminal anytime (and for the duration) that the Receive STM-0 SOH Processor Block is detecting an Multiplex Section AIS (MS-AIS) indicator.

- 0 - Disables this feature.
- 1 - Configures the Transmit STM-0 SOH Processor Block to automatically transmit the MS-RDI indicator, upon the Receive STM-0 SOH Processor Block detecting the MS-AIS indicator.

BIT 1 - Transmit Multiplex Section Remote Defect Indicator (MS-RDI) upon Detection of LOF

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to automatically transmit an MS-RDI indicator to the remote terminal anytime (and for the duration) that the Receive STM-0 SOH Processor Block is declaring the LOF defect.

- 0 - Disables this feature.
- 1 -Configures the Transmit STM-0 SOH Processor Block to automatically transmit the MS-RDI indicator, whenever the Receive STM-0 SOH Processor Block declares the LOF defect.

BIT 0 - Transmit Multiplex Section Remote Defect Indicator (MS-RDI) upon Detection of LOS

This READ/WRITE bit-field is used to configure the Transmit STM-0 SOH Processor Block to automatically transmit an MS-RDI indicator to the remote terminal anytime (and for the duration) that the Receive STM-0 SOH Processor Block is declaring the LOS defect.

- 0 - Disables this feature.
- 1 -Configures the Transmit STM-0 SOH Processor Block to automatically transmit the MS-RDI indicator, whenever the Receive STM-0 SOH Processor Block declares the LOS defect.

TABLE 160: TRANSMIT STM-0 SECTION M0M1 BYTE VALUE REGISTER (TSM0M1VR 0X0737H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
M0M1 Byte Value [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit M0M1 Byte Value

If the appropriate M0M1 Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the M0M1 byte, within the outbound STM-0 signal.

NOTE: *If Bit-0 (M0M1 Insert Method - BIT 1) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) and Bit-7 (M0M1 Byte Insert Method - BIT 0) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 0 (Address Location= 0x0703) are set to 0, 1, then the STM-0 Transmit Block will load the contents of this register into the M0M1 byte-field, within each outbound STM-0 frame. These register bits are ignored if the M0M1 Insert Method[1:0] bits are set to any value other than 0, 1.*

TABLE 161: TRANSMIT STM-0 SECTION - S1 BYTE VALUE REGISTER (TSS1VR 0X073B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit S1 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit S1 Byte Value

If the appropriate S1 Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the S1 byte, within the outbound STM-0 signal. If BIT 2 (S1 Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the STM-0 Transmit Block will load the contents of this register into the S1 byte-field, within each outbound STM-0 frame.

NOTE: *These register bits are ignored if BIT 2 (S1 Insert Method) is set to 0.*

TABLE 162: TRANSMIT STM-0 SECTION - F1 BYTE VALUE REGISTER (TSF1VR 0X073F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit F1 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit F1 Byte Value

If the appropriate F1 Byte Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the F1 byte, within the outbound STM-0 signal.

NOTE: *If BIT 3 (F1 Byte Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STM-0 SOH Processor Block will load the contents of this register into the F1 byte-field, within each outbound STM-0 frame. These register bits are ignored if BIT 3 (F1 Insert Method) is set to 0.*

TABLE 163: TRANSMIT STM-0 SECTION - E1 BYTE VALUE REGISTER (TSE1VR 0X0743)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit E1 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit E1 Byte Value

If the appropriate E1 Byte Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the E1 byte, within the outbound STM-0 signal. Note

NOTE: *If BIT 4 (E1 Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STM-0 SOH Processor Block will load the contents of this register into the E1 byte-field, within each outbound STM-0 frame. These register bits are ignored if BIT 4 (E1 Insert Method) is set to 0.*

TABLE 164: TRANSMIT STM-0 SECTION - E2 BYTE VALUE REGISTER (TSE2VR 0X0747)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit E2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit E2 Byte Value

If the appropriate E2 Byte Insert Method is selected, then these READ/WRITE bit-fields are used to specify the contents of the E2 byte, within the outbound STM-0 signal.

NOTE: *If BIT 5 (E2 Insert Method) within the Transmit STM-0 Section - SDH Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STM-0 SOH Processor Block will load the contents of this register into the E2 byte-field, within each outbound STM-0 frame. These register bits are ignored if BIT 5 (E2 Insert Method) is set to 0.*

TABLE 165: TRANSMIT STM-0 SECTION - J0 BYTE VALUE REGISTER (TSJ0VR 0X074B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit J0 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit J0 Byte Value

These READ/WRITE bits are used to specify the value of the J0 byte, that will be transmitted via the Transport Overhead, within the very next STM-0 Frame. This register is only valid if the Transmit STM-0 SOH Processor Block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STM-0 frame. The user accomplishes this by setting Bits 1 and 0 (J0_TYPE), within the Transmit STM-0 Section - J0 Byte Control Register (Address Location= 0x074F) to 1, 0.

TABLE 166: TRANSMIT STM-0 SECTION - TRANSMITTER J0 BYTE CONTROL REGISTER (TSJ0CR 0X074F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Message Length[1:0]		J0 Type[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:2] - Message Length[1:0]

These two READ/WRITE bit-fields are used to specify the length of the message that is to be repetitively transmitted via the J0 byte as shown in the table below.

Message Length

MSG_LENGTH[1:0]	CORRESPONDING MESSAGE LENGTH(BYTES)
00	1 Byte
01	16 Bytes
10 or 11	64 Bytes

BIT [1:0] - Transmit J0 Source[1:0]

These two READ/WRITE bit-fields are used to specify the source of the message that will be transported via the J0 byte/message, within the outbound STM-0 data-stream, as shown in the table below

Source of J0 Byte Message

J0_TYPE [1:0]	CORRESPONDING SOURCE OF J0 BYTE/MESSAGE.
00	Automatically set the J0 Byte, in each outbound STM-0 frame to 0x01.
01	The Transmit Section TraceMessage BufferThe Transmit STM-0 Section Trace Buffer Memory is located at Address locations 0x0900 through 0x093F.
10	From the Transmit J0 Byte Value[7:0] Register. In this setting, the Transmit STM-0 SOH Processor Block will read out the contents of the Transmit J0 Value[7:0] Register (Address Location= 0x074B), and will insert this value into the J0 byte of each outbound STM-0 frame.
11	From the TxSOH_n Input pin.

6.7 TRANSMIT PATH OVERHEAD PROCESSOR BLOCK REGISTERS

The register map for the Transmit STM-0 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the Transmit STM-0 POH Processor Block registers is presented below.

TABLE 167: TRANSMIT STM-0 PATH CONTROL REGISTER - BYTE 2 (TPCR2 0X0781)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Payload Type[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - Payload Type[1:0]

This READ/WRITE bit-field is used to configure the device for the type of VC-3 payload the device will be carrying.

- 00 - LTE (input POH and fixed stuffing).
- 01 - Asynchronous E1 mapping.
- 10 - Reserved
- 11 - Reserved

TABLE 168: TRANSMIT STM-0 PATH CONTROL REGISTER - BYTE 1 (TPCR1 0X0782)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Z5 Insertion Type	Z4 Insertion Type	Z3 Insertion Type	H4 Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - Z5 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit Z5 Value Register or the TPOH input pin as the source for the Z5 byte, in the outbound VC-3.

- 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit Z5 Value Register (Address Location= 0x07B3).
- 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the Z5 byte, in the outbound VC-3.

BIT 2 - Z4 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit Z4 Value Register or the TPOH input pin as the source for the Z4 byte, in the outbound VC-3.

- 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit Z4 Value Register (Address Location= 0x07AF).
- 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the Z4 byte, in the outbound VC-3.

BIT 1 - Z3 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit Z3 Value Register or the TPOH input pin as the source for the Z3 byte, in the outbound VC-3.

- 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit Z3 Value Register (Address Location = 0x07AB).
- 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the Z3 byte, in the outbound VC-3.

BIT 0 - H4 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit H4 Value Register or the TPOH input pin as the source for the H4 byte, in the outbound VC-3.

- 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit H4 Value Register (Address Location= 0x07A7).
- 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the H4 byte, in the outbound VC-3.

TABLE 169: TRANSMIT STM-0 PATH CONTROL REGISTER - BYTE 0 (TPCR0 0X0783)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2 Insertion Type	HP-REI Insertion Type[1:0]		HP-RDI Insertion Type[1:0]		C2 Byte Insertion Type	C2 Byte Auto Insert Mode Enable	Transmit AU-AIS Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - F2 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit F2 Value Register or the TPOH input pin as the source for the F2 byte, in the outbound VC-3.

▶ 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit F2 Value Register (Address Location= 0x07A3).

▶ 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the F2 byte, in the outbound VC-3.

BIT [6:5] - High Order Path Remote Error Indication (HP-REI) Insertion Type[1:0]

These two READ/WRITE bit-fields are used to configure the Transmit STM-0 POH Processor Block to use one of the three following sources for the HP-REI bit-fields (e.g., Bit-7 through -4, within the G1 byte of the outbound VC-3).

- From the corresponding Receive STM-0 POH Processor Block (e g., when it detects B3 bytes in its incoming VC-3 data).
- From the Transmit G1 Byte Value Register (Address Location= 0x079F).
- From the TPOH input pin.

▶ 00/11 - Configures the Transmit STM-0 POH Processor Block to set Bits-7 through -4 (in the G1 byte of the outbound VC-3) based upon receive conditions as detected by the corresponding Receive STM-0 POH Processor Block.

▶ 01 - Configures the Transmit STM-0 POH Processor Block to set Bits-7 through -4 (in the G1 byte of the outbound VC-3) based upon the contents within the Transmit G1 Byte Value register (Address Location= 0x079F).

▶ 10 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input pin as the source of Bits 1 through 4 (in the G1 byte of the outbound VC-3).

BIT [4:3] - High Order Path Remote Defect Indicator (HP-RDI) Insertion Type[1:0]

These two READ/WRITE bit-fields are used to configure the Transmit STM-0 POH Processor Block to use one of the three following sources for the HP-RDI bit-fields (e.g., Bits-3 through -1, within the G1 byte of the outbound VC-3).

- From the Receive STM-0 POH Processor Block (e g., when it detects various alarm conditions within its incoming VC-3 data).
- From the Transmit G1 Byte Value Register (Address Location = 0x079F).
- From the TPOH input pin.

▶ 00/11 - Configures the Transmit STM-0 POH Processor Block to set Bits-3 through -1 (in the G1 byte of the outbound VC-3) based upon receive conditions as detected by the Receive STM-0 POH Processor Block.

▶ 01 - Configures the Transmit STM-0 POH Processor Block to set Bits-3 through -1 (in the G1 byte of the outbound VC-3) based upon the contents within the Transmit G1 Byte Value register.

▶ 10 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input pin as the source of Bits 5 through 7 (in the G1 byte of the outbound VC-3).

BIT 2 - C2 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to use either the Transmit STM-0 Path - Transmit C2 Byte Value Register or the TPOH input pin as the source for the C2 byte, in the outbound VC-3.

▶ 0 - Configures the Transmit STM-0 POH Processor Block to use the Transmit STM-0 Path - Transmit C2 Value Register (Address Location= 0x079B).

▶ 1 - Configures the Transmit STM-0 POH Processor Block to use the TPOH input as the source for the C2 byte, in the

outbound VC-3.

BIT 1 - Auto-Insert HP-PDI Indicator Enable

This READ/WRITE bit-field are used to configure the Transmit STM-0 POH Processor Block to automatically insert the HP-PDI (Path - Payload Defect Indicator) whenever the AU-AIS indicator is received from the Receive SONET POH Processor Block.

If this feature is enabled, then the Transmit STM-0 POH Processor Block will automatically set the C2 byte (within the outbound VC-3) to 0xFC (to indicate a HP-PDI condition) whenever it receives the AU-AIS indicator, from the Receive SONET POH Processor Block.

BIT 0 - Transmit AU-AIS Enable

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to (via software control) transmit an AU-AIS indicator to the remote PTE. If this feature is enabled, then the Transmit STM-0 POH Processor Block will automatically set the H1, H2, H3 and all the VC-3 bytes to an All Ones pattern, prior to routing this data to the Transmit STM-0 TOH Processor Block.

- 0 - Configures the Transmit STM-0 POH Processor Block to NOT transmit the AU-AIS indicator to the remote PTE.
- 1 - Configures the Transmit STM-0 POH Processor Block to transmit the AU-AIS indicator to the remote PTE.

TABLE 170: TRANSMIT STM-0 PATH J1 BYTE VALUE REGISTER (TPJ1VR 0X0793)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit J1 Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit J1 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the J1 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 2 (C2 Insertion Type) within the Transmit STM-0 Path - J1 Control Register register (Address Location= 0x0783).

TABLE 171: TRANSMIT STM-0 PATH B3 BYTE ERROR MASK REGISTER (TPB3EM 0X0797)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit B3 Byte Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit B3 Byte Mask[7:0]

This READ/WRITE bit-field is used to insert errors into the B3 byte, within the outbound VC-3, prior to transmission to the Transmit STM-0 TOH Processor Block.

The Transmit STM-0 POH Processor Block will perform an XOR operation with the contents of this register, and the B3 byte value. The results of this operation will be written back into the B3 byte of the outbound VC-3.

NOTE: *If the user sets a particular bit-field, within this register, to 1, then that corresponding bit, within the outbound B3 byte will be in error. For normal operation, the user should set this register to 0x00.*

TABLE 172: TRANSMIT STM-0 PATH C2 BYTE VALUE REGISTER (TPC2VR 0X079B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit C2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit C2 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the C2 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 2 (C2 Byte Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 0 register (Address Location= 0x0783).

TABLE 173: TRANSMIT STM-0 PATH G1 BYTE VALUE REGISTER (TPG1VR 0X079F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit G1 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit G1 Byte Value:

These READ/WRITE bit-fields are used to have software control over the contents of the HP-RDI and HP-REI bit-fields, within each G1 byte in the outbound VC-3.

NOTE: *If the users sets HP-REI Insertion Type[1:0] and HP-RDI Insertion Type[1:0] bits to the value [0, 1], then contents of the HP-REI and the HP-RDI bit-fields (within each G1 byte of the outbound VC-3) will be dictated by the contents of this register. The HP-REI Insertion Type[1:0] and HP-RDI Insertion Type[1:0] bit-fields are located in the Transmit STM-0 Path - SONET Control Register - Byte 0 Register (Address Location= 0x0783)*

TABLE 174: TRANSMIT STM-0 PATH F2 BYTE VALUE REGISTER (TPF2VR 0X07A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit F2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit F2 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the F2 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT7 (F2 Byte Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 0 register (Address Location= 0x0783).

TABLE 175: TRANSMIT STM-0 PATH H4 BYTE VALUE REGISTER (TPH4VR 0X07A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit H4 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit H4 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the H4 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 0 (H4 Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 1 register (Address Location= 0x07A7).

TABLE 176: TRANSMIT STM-0 PATH Z3 BYTE VALUE REGISTER (TPZ3VR 0X07AB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Z3 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z3 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z3 byte, within each outbound VC-3. If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 1 (Z3 Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 177: TRANSMIT STM-0 PATH Z4 BYTE VALUE REGISTER (TPZ4VR 0XN9AF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Z4 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z4 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z4 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 2 (Z4 Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 178: TRANSMIT STM-0 PATH Z5 BYTE VALUE REGISTER (TPZ5VR 0X07B3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Z5 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z5 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z5 byte, within each outbound VC-3.

If the user configures the Transmit STM-0 POH Processor Block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each outbound VC-3.

This feature is enabled whenever the user writes a 0 into BIT 3 (Z5 Insertion Type) within the Transmit STM-0 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 179: TRANSMIT STM-0 PATH POINTER CONTROL REGISTER (TPPCR 0X07B7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BITt 5 - Pointer Force

This READ/WRITE bit-field is used to load the values contained within the Transmit STM-0 POH Arbitrary H1 Pointer and Transmit STM-0 POH Arbitrary H2 Pointer registers (Address Location= 0x07BF and 0x07C3) into the H1 and H2 bytes (within the outbound STM-0 data stream).

The actual location of the VC-3 will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an Invalid Pointer condition.

- 0 - Configures the Transmit STM-0 POH and TOH Processors to Transmit STM-0 data will normal and correct H1 and H2 bytes.
- 1 - Configures the Transmit STM-0 POH and TOH Processor Blocks to overwrite the values of the H1 and H2 bytes (in the outbound STM-0 data-stream) with the values in the Transmit STM-0 POH Arbitrary H1 and H2 Pointer registers.

BITt 4 - Check Stuff Monitoring

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH and TOH Processor Blocks to only execute a Positive, Negative or NDF event (via the Insert Positive Stuff, Insert Negative Stuff, Insert Continuous or Single NDF options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 STM-0 frame periods.

- 0 - Disables this feature.In this mode, the Transmit STM-0 POH and TOH Processor Block will execute a software-commanded pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 STM-0 frame periods.
- 1 - Enables this feature.In this mode, the Transmit STM-0 POH and TOH Processor Block will ONLY execute a software-commanded pointer adjustment event, if no pointer adjustment event has occurred during the last 3 STM-0 frame periods.

BITt 3 - Insert Negative Stuf

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH and TOH Processor Blocks to insert a negative-stuff into the outbound STM-0 data stream. This command, in-turn will cause a Pointer Decrementing event at the remote terminal.

- Writing a 0 to 1 transition into this bit-field causes the following to happen.
  - A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STM-0 data stream).
  - The D bits, within the H1 and H2 bytes will be inverted (to denote a Decrementing Pointer Adjustment event).
  - The contents of the H1 and H2 bytes will be decremented by 1, and will be used as the new pointer from this point on.

NOTE: *Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

BITt 2 - Insert Positive Stuff

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH and TOH Processor Blocks to insert a positive-stuff into the outbound STM-0 data stream. This command, in-turn will cause a Pointer Incrementing event at the remote terminal.

- Writing a 0 to 1 transition into this bit-field causes the following to happen.

- A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STM-0 data-stream, immediately after the H3 byte position within the outbound STM-0 data stream).
- The I bits, within the H1 and H2 bytes will be inverted (to denote a Incrementing Pointer Adjustment event).
- The contents of the H1 and H2 bytes will be incremented by 1, and will be used as the new pointer from this point on.Note

NOTE: *Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

BITt 1 - Insert Continuous NDF Events

This READ/WRITE bit-field is used configure the Transmit STM-0 POH and TOH Processor Blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STM-0 data stream.

As the Transmit STM-0 POH and TOH Processor Blocks insert the NDF event into the STM-0 data stream, it will proceed to load in the contents of the Transmit STM-0 POH Arbitrary H1 Pointer and Transmit STM-0 POH Arbitrary H2 Pointer registers into the H1 and H2 bytes (within the outbound STM-0 data stream).

▶ 0 - Configures the Transmit STM-0 TOH and POH Processor Blocks to not continuously insert NDF events into the outbound STM-0 data stream.

▶ 1- Configures the Transmit STM-0 TOH and POH Processor Blocks to continuously insert NDF events into the outbound STM-0 data stream.

BITt 0 - Insert Single NDF Event

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH and TOH Processor Blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STM-0 data stream.

▶ Writing a 0 to 1 transition into this bit-field causes the following to happen

- The N bits, within the H1 byte will set to the value 1001
- The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the Transmit STM-0 POH - Arbitrary H1 Pointer and Transmit STM-0 POH Arbitrary H2 Pointer registers (Address Location= 0x07BF and 0xN9C3).

NOTE: *Afterwards, the N bits will resume their normal value of 0110 and this new pointer value will be used as the new pointer from this point on. Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

TABLE 180: TRANSMIT STM-0 PATH J1 CONTROL REGISTER (TPJ1CR 0X07BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Insertion Method[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - J1 Byte Insertion_Method[1:0]

These READ/WRITE bit-fields are used to specify the method that the user will use to insert the J1 byte into the outbound VC-3. The relationship between the contents of these bit-fields and the corresponding J1 Byte Insertion Method is presented below.

Insertion Method

J1 BYTE INSERTION METHOD[1:0]	RESULTING INSERTION METHOD
00	Insert the value 0x00
01	Not Valid
10	Insert from the Transmit SONET Path - Transmit J1 Byte Value Register (Address Location= 0x0793)
11	Insert via the TxPOH_n input port

TABLE 181: TRANSMIT STM-0 PATH ARBITRARY H1 POINTER REGISTER (TPH1PR 0X07BF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NDF Bits				SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - NDF (New Data Flag) Bits

These READ/WRITE bit-fields are used provide the value that will be loaded into the NDF bit-field (of the H1 byte), whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STM-0 Path - Transmit Path Control Register (Address Location= 0x07B7).

BIT [3:2] - SS Bits

These READ/WRITE bit-fields is used to provide the value that will be loaded into the SS bit-fields (of the H1 byte) whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STM-0 Path - Transmit Path Control Register (Address Location= 0x07B7).

The SS bits have no functional value, within the H1 byte.

BIT [1:0] - H1 Pointer Value[1:0]

These two READ/WRITE bit-fields, along with the constants of the Transmit STM-0 Path - Transmit Arbitrary H2 Pointer Register (Address Location= 0x07C3) are used to provide the contents of the Pointer Word.

These two READ/WRITE bit-fields are used to define the value of the two most significant bits within the Pointer word. Whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STM-0 Path - Transmit Path Control Register (Address Location= 0x07B7), the values of these two bits will be loaded into the two most significant bits within the Pointer Word.

TABLE 182: TRANSMIT STM-0 PATH ARBITRARY H2 POINTER REGISTER (TPH2PR 0X07C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - H2 Pointer Value[1:0]

These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the Transmit STM-0 Path - Transmit Arbitrary H1 Pointer Register (Address Location= 0x07C3) are used to provide the contents of the Pointer Word. These two READ/WRITE bit-fields are used to define the value of the eight least significant bits within the Pointer word.

- Whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STM-0 Path - Transmit Path Control Register (Address Location= 0x07B7), the values of these eight bits will be loaded into the H2 byte, within the outbound STM-0 data stream.

TABLE 183: TRANSMIT STM-0 PATH CURRENT POINTER BYTE REGISTER - BYTE 1 (TPCPR1 0X07C6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Tx Pointer High[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	0

BIT [7:2] - Unused

BIT [1:0] - Transmit Pointer Word - High[1:0]

These two READ-ONLY bits, along with the contents of the Transmit STM-0 Path - Transmit Current Pointer Byte Register - Byte 0 (Address Location= 0x07C7) reflect the current value of the pointer (or offset of VC-3 within the STM-0 frame). These two bits contain the two most significant bits within the 10-bit pointer word.

TABLE 184: TRANSMIT STM-0 PATH CURRENT POINTER BYTE REGISTER - BYTE 0 (TPCPR0 0X07C7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx Pointer Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	1	0

BIT [7:0] - Transmit Pointer Word - Low[7:0]

These two READ-ONLY bits, along with the contents of the Transmit STM-0 Path - Transmit Current Pointer Byte Register - Byte 1 (Address Location= 0x07C6) reflect the current value of the pointer (or offset of VC-3 within the STM-0 frame). These two bits contain the eight least significant bits within the 10-bit pointer word.

TABLE 185: TRANSMIT STM-0 PATH HP-RDI CONTROL REGISTER - BYTE 2 (TPHP-RDICR2 0X07C9)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				HP-PLM HP-RDI Code[2:0]			Transmit HP-RDI upon HP-PLM
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:1] - HP-PLM (High Order Path - Payload Mismatch) - HP-RDI Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STM-0 POH Processor Block will transmit, within the HP-RDI bit-fields of the G1 byte (within the outbound VC-3), whenever the corresponding Receive STM-0 POH Processor Block detects and declares a HP-PLM condition. In order to enable this feature, the user must set BIT 0 (HP-RDI upon HP-PLM) within this register to 1.

BIT 0 - Transmit HP-RDI upon HP-PLM

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to automatically transmit the HP-RDI Code (as configured in Bits 3 through 1 - within this register) whenever the corresponding Receive STM-0 POH Processor Block declares a HP-PLM condition.

- 0 - Disables the automatic transmission of HP-RDI upon detection of HP-PLM.
- 1 - Enables the automatic transmission of HP-RDI upon detection of HP-PLM.

TABLE 186: TRANSMIT STM-0 PATH HP-RDI CONTROL REGISTER - BYTE 1 (TPHP-RDICR1 0X07CA)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HP-TIM HP-RDI Code[2:0]			Transmit HP-RDI upon HP-TIM	HP-UNEQ HP-RDI Code[2:0]			Transmit HP-RDI upon HP-UNEQ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - HP-TIM (High Order Path - Trace Identification Message Mismatch) - HP-RDI Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STM-0 POH Processor Block will transmit within the HP-RDI bit-fields of the G1 byte (within the outbound VC-3), whenever the Receive STM-0 POH Processor Block detects and declares the HP-TIM defect condition.

To enable this feature, the user must set BIT 4 (Transmit HP-RDI upon HP-TIM) within this register to 1.

BIT 4 - Transmit HP-RDI upon HP-TIM

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STM-0 POH Processor Block declares the HP-TIM defect condition.

- 0 - Disables the automatic transmission of HP-RDI upon detection of HP-TIM.
- 1 - Enables the automatic transmission of HP-RDI upon detection of HP-TIM.

BIT [3:1] - HP-UNEQ (High Order Path - Unequipped) - HP-RDI Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STM-0 POH Processor Block will transmit, within the HP-RDI bit-fields of the G1 byte (within the outbound VC-3), whenever the Receive STM-0 POH Processor Block detects and declares the HP-UNEQ defect condition.

To enable this feature, the user must set BIT 0 (Transmit HP-RDI upon HP-UNEQ) within this register to 1.

BIT 0 - Transmit HP-RDI upon HP-UNEQ

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to automatically transmit the HP-RDI Code (as configured in Bits 3 through 1 - within this register) whenever the corresponding Receive STM-0 POH Processor Block declares the HP-UNEQ defect condition.

- 0 - Disables the automatic transmission of HP-RDI upon detection of HP-UNEQ.
- 1 - Enables the automatic transmission of HP-RDI upon detection of HP-UNEQ.

TABLE 187: TRANSMIT STM-0 PATH HP-RDI CONTROL REGISTER - BYTE 0 (TPHP-RDICR0 0X07CB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AU-LOP HP-RDI Code[2:0]			Transmit HP-RDI upon AU-LOP	AU-AIS HP-RDI Code[2:0]			Transmit HP-RDI upon AU-AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - AU-LOP (Administrative Unit - Loss of Pointer) - HP-RDI Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STM-0 POH Processor Block will transmit, within the HP-RDI bit-fields of the G1 byte (within the outbound VC-3), whenever the corresponding Receive STM-0 POH Processor Block detects and declares a AU-LOP condition.

To enable this feature, the user must set BIT 4 (HP-RDI upon AU-LOP) within this register to 1.

BIT 4 - Transmit HP-RDI upon AU-LOP

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STM-0 POH Processor Block declares a AU-LOP condition

- 0 - Disables the automatic transmission of HP-RDI upon detection of AU-LOP.
- 1 - Enables the automatic transmission of HP-RDI upon detection of AU-LOP.

BIT[3:1]AU-AIS (Administrative Unit - Alarm Indication Signal) - HP-RDI Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STM-0 POH Processor Block will transmit, within the HP-RDI bit-fields of the G1 byte (within the outbound VC-3), whenever the corresponding Receive STM-0 POH Processor Block detects and declares an AU-AIS condition.

To enable this feature, the user must set BIT 4 (HP-RDI upon AU-AIS) within this register to 1.

BIT 0 - Transmit HP-RDI upon AU-AIS

This READ/WRITE bit-field is used to configure the Transmit STM-0 POH Processor Block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STM-0 POH Processor Block declares a AU-AIS condition.

- 0 - Disables the automatic transmission of HP-RDI upon detection of AU-AIS.
- 1 - Enables the automatic transmission of HP-RDI upon detection of AU-AIS.

TABLE 188: TRANSMIT STM-0 PATH SERIAL PORT CONTROL REGISTER (TPSPCR 0X07CF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxPOH Clock Speed[4:0]			
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3:0] - TxPOHClk Output Clock Signal Speed

These READ/WRITE bit-fields are used to specify the frequency of the TxPOHClk output clock signal. The formula that relates the contents of these register bits to the TxPOHClk frequency is presented below.

FREQ = 51.84 /[2 * (TxPOH_CLOCK_SPEED + 1)

For STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 2.36MHz to 25.92MHz

6.8 Global E1 Line Interface Unit Register Descriptions (LIU)

TABLE 189: GLOBAL LINE INTERFACE CONTROL REGISTER 5 (GLICR5 0X0100H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	ATAOS	Reserved				TCLKCNTL	LIUSRST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Automatic All Ones Generation Upon RLOS Condition

This bit will force an Unframed All Ones signal to the Egress Tx LIU Line Interface whenever its corresponding Ingress Rx LIU input experiences an RLOS condition.

- 0 - Disabled
- 1 - Enable ATAOS

BIT [5:2] - Reserved

BIT 1 - Transmit Clock Control

This bit is used to set the transmitter activity in the event that the transmit clock is missing.

- 0 - Send All Zeros to the Line
- 1 - Send All Ones to the Line

BIT 0 - Software Reset of LIU Blocks Only

This bit grants permission to reset all internal circuits to their default state. This bit does NOT reset the register values.

- 0 - Normal Operation
- 1 - LIU Software Reset

TABLE 190: GLOBAL LINE INTERFACE CONTROL REGISTER 4 (GLICR4 0X0101H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
LCV_OFSEL	Reserved				RXMUTE	EXLOS	ICT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Line Code Violation / Over Flow Monitoring Select

This bit is used to select the monitoring function of the LCV_OF alarm in the LIU interrupt block.

- 0 - Monitors LCV errors
- 1 - Monitors the over flow status of the LCV Counter

BIT [6:3] - Reserved

BIT 2 - Receive Mute Upon RLOS

This bit forces All Zeros on the Ingress Path to prevent data chattering whenever the Rx LIU Line Interface experiences an RLOS condition.

- 0 - Disabled
- 1 - RXMUTE enabled

BIT 1 - Extended Loss of Signal

This bit is used to extend the time period to 4,096 recovered line clocks before declaring/clearing RLOS on the Ingress path.

- 0 - Normal RLOS declaration/clearance
- 1 - EXLOS Enabled

BIT 0 - In Circuit Testing

This bit forces all Ingress and Egress signals to be High-Z.

- 0 - Disabled
- 1 - Enabled

TABLE 191: GLOBAL LINE INTERFACE CONTROL REGISTER 3 (GLICR3 0X0102H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved						MCLKSEL[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved

BIT [1:0] - Master Clock Select

These bits configure the input reference clock to the Low speed interface blocks.

- 00 - 2.048Mhz Input Clock Reference
- 01 = 4.096MHz Input Clock Reference
- 10 - 8.192 MHz Input Clock Reference
- 11 = 16.384MHz Input Clock Reference

TABLE 192: GLOBAL LINE INTERFACE CONTROL REGISTER 2 (GLICR2 0X0103H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	GCHIS[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [6:0] - Global Channel Interrupt Status for the LIU Blocks

TABLE 193: GLOBAL LINE INTERFACE CONTROL REGISTER 1 (GLICR1 0X0104H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	GCHIS[13:7]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [6:0] - Global Channel Interrupt Status for the LIU Blocks

TABLE 194: GLOBAL LINE INTERFACE CONTROL REGISTER 0 (GLICR0 0X0105H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	GCHIS[20:14]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [6:0] - Global Channel Interrupt Status for the LIU Blocks

6.9 Individual Channel E1 Line Interface Unit Register Descriptions (LIU)

TABLE 195: CHANNEL LINE INTERFACE CONTROL REGISTER 9 (CLICR9 0XN000H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PRBS_QRSS	PRBS_Tx_Rx	RxON	Reserved				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - PRBS/QRSS Select

This bit is used to select the type of diagnostic pattern.

- 0 - PRBS
- 1 - QRSS

BIT 6 - Random Bit Sequence Direction Select

This bit selects which direction the diagnostic pattern will be sent.

- 0 - Egress (TTIP/TRING)
- 1 - Ingress (Toward the VT Mapper Block)

BIT 5 - Receiver On Select

This bit is used to turn the receiver On of Off.

- 0 - Off
- 1 - On

BIT [4:0] - Reserved

TABLE 196: CHANNEL LINE INTERFACE CONTROL REGISTER 8 (CLICR8 0XN001H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RxTSEL	TxTSEL	Force to 0	TERSEL	JASEL[1:0]		JBWSEL	FIFOSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Receive Termination Select

This bit is used to select between the internal receive termination (line impedance) and High-Z.

- 0 - High-Z
- 1 - Internal Termination

BIT 6 - Transmit Termination Select

This bit is used to select between the internal transmit termination (line impedance) and High-Z.

- 0 - High-Z
- 1 - Internal Impedance

BIT 5 - This bit must be set to 0 at all times

BIT 4 - Transmit and Receive Termination Select

This bit sets the termination impedance for both the LIU Receiver and Transmitter.

- 0 - 75 Ω
- 1 - 120 Ω

BIT [3:2] - Jitter Attenuator Select

This bit is used to enable the receive jitter attenuator.

- 00 - Disabled
- 01 - Transmit Path
- 10 - Receive Path
- 11 - Receive Path

BIT 1 - Jitter Bandwidth Select

This bit is used to select the band width of the Receive and Transmit Jitter Attenuators.

- 0 - 10 Hz
- 1 - 1.5 Hz

BIT 0 - FIFO Depth Select

This bit is used to select the depth of the FIFO within both the Receive and Transmit Jitter Attenuators.

- 0 - 32-Bit FIFO
- 1 - 64-Bit FIFO

TABLE 197: CHANNEL LINE INTERFACE CONTROL REGISTER 7 (CLICR7 0XN002H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INVPRBS	TxTEST[2:0]			TxON	LOOP[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Invert PRBS/QRSS Pattern

This bit is used to invert the pattern chosen in register CLICR0 and if enabled in TxTEST[2:0] bits below.

- 0 - Normal Pattern
- 1 - Pattern Inversion Enabled

BIT [6:4] - Transmit Test Pattern Select

These bits are used to select diagnostic test pattern to be enabled to the egress LIU block.

- 0xx - Reserved
- 100 - PRBS/QRSS Pattern
- 101 - TAOS
- 11x - Reserved

BIT 3 - Transmitter Enable

This bit is used to enable the transmitter output.

- 0 - Disabled
- 1 - Enabled

BIT [2:0] - Diagnostic Loop Back Test Enable

These bits are used to enable the various loop back modes supported in the LIU block.

- 0xx - No Loop Back
- 100 - Dual Loop Back Enabled
- 101 - Analog Loop Back Enabled
- 110 - Remote Loop Back Enabled
- 111 - Digital Loop Back Enabled

TABLE 198: CHANNEL LINE INTERFACE CONTROL REGISTER 6 (CLICR6 0XN003H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					INSBPV	INSBER	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Insert Bipolar Violation

This bit is used to force one bipolar violation error in the egress transmit direction. This feature is enabled by the transition of a 0 to 1.

- 0 - Disabled (Idle State)
- 1 - Force One Bipolar Violation

BIT 1 - Insert Bit Error

This bit is used to force one bit error in the egress transmit direction. This feature is enabled by the transition of a 0 to 1.

- 0 - Disabled (Idle State)
- 1 - Force One Bit Error

BIT 0 - Reserved

TABLE 199: CHANNEL LINE INTERFACE CONTROL REGISTER 5 (CLICR5 0XN004H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	DMOIE	FLSIE	LCV_OFIE	Reserved	AISIE	RLOSIE	QRPIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Digital Monitor Output Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

BIT 5 - FIFO Limit Status Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

BIT 4 - Line Code Violation / Over Flow Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

BIT 3 - Reserved

BIT 2 - Alarm Indication Signal Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

BIT 1 - Receive Loss of Signal Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

BIT 0 - PRBS / QRSS Random Pattern Interrupt Enable

- 0 - Disabled
- 1 - Interrupt Enabled

TABLE 200: CHANNEL LINE INTERFACE CONTROL REGISTER 4 (CLICR4 0XN005H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	DMOD	FLSD	LCV_OFD	Reserved	AISD	RLOSD	QRPD
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Digital Monitor Output Detection

This bit field monitors the DMO function and will be set to 1 if there is no activity present on the transmitter outputs for 128 consecutive clock cycles. At all other times, this bit will be set to 0.

- 0 - No Alarm
- 1 - Alarm Detected

BIT 5 - FIFO Limit Status Detection

This bit field monitors the FIFO and will be set to 1 if the Read and Write pointers are with +/- 3bits. At all other times, this bit will be set to 0.

- 0 - No Alarm
- 1 - Alarm Detected

BIT 4 - Line Code Violation / Over Flow Detection

This bit field monitors the LCV function on the receiver inputs and will be set to 1 if either (a) a line code violation occurs, or (b) the LCV counter is full. This is dependent on bit 7 in GLICR1.

- 0 - No Alarm
- 1 - Alarm Detected

BIT 3 - Reserved

BIT 2 - Alarm Indication Signal Detection

This bit field monitors the AIS function on the receiver inputs and will be set to 1 if an alarm indication signal is detected according to ITU-T G.775 Specifications.

- 0 - No Alarm
- 1 - Alarm Detected

BIT 1 - Receive Loss of Signal Detection

This bit field monitors the RLOS function on the receiver inputs and will be set to 1 if a Receiver Loss of Signal occurs according to either ITU-T G.775 or ETSI-300-233.

- 0 - No Alarm
- 1 - Alarm Detected

BIT 0 - PRBS / QRSS Random Pattern Detection

This bit field monitors the PRBS/QRSS function on the receiver inputs and will be set to 1 if the chosen pattern in register CLICR0 is detected.

- 0 -No Alarm
- 1 - Alarm Detected

TABLE 201: CHANNEL LINE INTERFACE CONTROL REGISTER 3 (CLICR3 0XN006H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved	DMOIS	FLSIS	LCV_OFIS	Reserved	AISIS	RLOSIS	QRPIS
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT 6 - Digital Monitor Output Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

BIT 5 - FIFO Limit Status Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

BIT 4 - Line Code Violation / Over Flow Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

BIT 3 - Reserved

BIT 2 - Alarm Indication Signal Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

BIT 1 - Receive Loss of Signal Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

BIT 0 - PRBS / QRSS Random Pattern Interrupt Status

- 0 - Disabled
- 1 - Change of Status Occurred

TABLE 202: CHANNEL LINE INTERFACE CONTROL REGISTER 2 (CLICR2 0XN007H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
LCNTR_ENB	Reserved		RSTALL	UPDATEALL	BYTESEL	UPDATE	RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Line Code Violation Counter Enable

This bit enables a 16-Bit LCV counter for this particular channel.

- 0 - Disabled
- 1 - Enabled

BIT [6:5] - Reserved

BIT 4 - Reset All LCV Counters

Although each channel has independent control over its LCV counter, this bit grants access to reset all 21 LCV counters with one write. This bit must be set to 1 for at least 1mS.

- 0 - Normal Operation
- 1 - Reset All 21 LCV Counters

BIT 3 - Update All LCV Counters

Although each channel has indepedent control over its LCV counter, this bit grants access to Update all 21 LCV counters with one write dependent on the BYTESEL bit in this register. Once initiated, if the BYTESEL bit is set to 0, the Low byte of all 21 LCV Counter values will be updated to register CLICR17 for each channel. Conversely, if the BYTESEL bit is set to 1, the High byte of all 21 LCV Counter values will be updated to register CLCR16 for each channel.

- 0 - Normal Operation
- 1 - Update All 21 LCV Counters

BIT 2 - LCV Counter Byte Select

This bit is used select which between the lower and upper bytes while updating the holding registers.

- 0 - Lower Byte is Selected
- 1 - Upper Byte is Selected

BIT 1 - Update Channel LCV Counter

This bit Update this channel's LCV counter dependent on the BYTESEL bit in this register. Once initiated, if the BYTESEL bit is set to 0, the Low byte of the LCV Counter values will be updated to register CLICR17. Conversely, if the BYTESEL bit is set to 1, the High byte of the LCV Counter values will be updated to register CLCR16.

- 0 - Normal Operation
- 1 - Update This Channel's LCV Counter

BIT 0 - Reset Channel LCV Counters

Although each channel has independent control over its LCV counter, this bit grants access to reset all 21 LCV counters with one write. This bit must be set to 1 for at least 1mS.

- 0 - Normal Operation
- 1 - Reset This Channel's LCV Counter

TABLE 203: CHANNEL LINE INTERFACE CONTROL REGISTER 1 (CLICR1 0XN010H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
HIBYTE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - High Byte of the Line Code Violation Counter [15:8]

These bits reflect the MSB of the current value in the LCV Counter once it's updated in register CLICR7.

TABLE 204: CHANNEL LINE INTERFACE CONTROL REGISTER 0 (CLICR0 0XN011H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
LOBYTE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Low Byte of the Line Code Violation Counter [7:0]

These bits reflect the LSB of the current value in the LCV Counter once it's updated in register CLICR7.

6.10 E1 Synchronization Framer Register Descriptions (Egress Direction Only)

TABLE 205: CLOCK SELECT REGISTER (CSR 0XN100H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved						CSS[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved

BIT [1:0] - Clock Source Select

The CSS bits are used to select the source of the Egress transmit clock for the Line Interface.

- 00 - The recovered received channel input clock is chosen as the transmit clock
- 01 - The de-mapped channel input clock is chosen as the transmit clock.
- 10 - The internal master clock derived from the PLL is chosen as the transmit clock
- 11 - Same as setting 00

TABLE 206: SLIP BUFFER CONTROL REGISTER (SBCR 0XN116H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved						SB_ENB[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved

BIT [1:0] - Slip Buffer ENaBle Bits

This bit is used to enable slip buffer.

00, 11 = Buffer is bypassed.

01 = Elastic store (slip buffer) is enabled.

10 = Buffer acts as a FIFO. The data latency is dictated by FIFO Latency Register.

TABLE 207: FIFO LATENCY REGISTER (FIFOLR 0XN117H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved			LATENCY[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

BIT [7:5] - Reserved

BIT [4:0] - Programmable FIFO Latency Delay

These bits fix the distance of slip buffer read and write pointers in FIFO mode.

TABLE 208: FRAMING SELECT REGISTER RE-SYNC (FSRRS 0XN10BH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RSYNC	CASC[1:0]		CRCC[1:0]		FASC[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	1	1

BIT 7 - Force Re-Sync Process, Auto Clear After Synchronization

This bit forces frame to restart synchronization process. This bit is cleared automatically after synchronization has been reached.

- 0 - No Re-Sync
- 1 - Force Re-Sync

BIT [6:5] - CAS Re-Synchronization Criteria

These bits determine the criteria of loss of CAS multiframe alignment.

- 00 - Two consecutive Multiframe Alignment Signal (MAS) errors.
- 01 - Three consecutive Multiframe Alignment Signal (MAS) errors.
- 10 - Four consecutive Multiframe Alignment Signal (MAS) errors.
- 11 - Eight consecutive Multiframe Alignment Signal (MAS) errors10 - CAS multiframe alignment algorithm 2 (G.732) is enabled.

BIT [4:3] - CRC Re-Synchronization Criteria

These bits determine the criteria of loss of CRC-4 multiframe alignment.

- 00 - Declare loss of CRC multiframe alignment if four consecutive CRC multiframe alignment signals have been received in error.
- 01 - Declare loss of CRC multiframe alignment if two consecutive CRC multiframe alignment signals have been received in error.
- 10 - Declare loss of CRC multiframe alignment if eight consecutive CRC multiframe alignment signals have been received in error.
- 11 - Declare loss of CRC multiframe alignment if 915 or more CRC-4 errors have been detecteded in one second.

Bit [2:0] - FAS Re-Synchronization Criteria

These bits represent the number of consecutive errored FAS patterns to cause the declaration of loss of FAS alignment.

Zero is illegal. The default is set to 011b.

TABLE 209: BLOCK INTERRUPT STATUS REGISTER (BISR 0XNB00H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					SLIP	Reserved	E1FRAME
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Slip Buffer Interrupt

BIT 1 - Reserved

BIT 0 - E1 Framer Interrupt

TABLE 210: BLOCK INTERRUPT ENABLE REGISTER (BIER 0XNB01H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					SLIP_ENB	Reserved	E1FRM_ENB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Slip Buffer Interrupt Enable

BIT 1 - Reserved

BIT 0 - E1 Framer Interrupt Enable

TABLE 211: ALARM AND ERROR STATUS REGISTER (AESR 0XNB02H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RxLOF_state	Reserved				RxLOF	Reserved	
RO	RO	RO	RO	RO	RUR/WC	RUR/WC	RUR/WC
0	0	0	0	0	0	0	0

BIT 7 - LOF Alarm State

This bit is used to indicate that a loss of frame alignment has occurred.

- 0 - No red alarm occurs.
- 1 - Red alarm occurs.

BIT [6:3] - Reserved

BIT 2 - LOF State Change

This bits indicates the change of LOF defect (DEFDET=1) or Red alarm (DEFDET=0) state.

- 0 - No state change of Red alarm is recorded.
- 1 - The state of Red alarm has changed.

BIT [1:0] - Reserved

TABLE 212: ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER 0XNB03H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					RxRED_ENB	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Red Alarm State Change Interrupt Enable

Setting this bit will enable the interrupt generation when the change state of red alarm has been detected.

- 0 = Disables the interrupt generation of loss of frame detection.
- 1 = Enables the interrupt generation of loss of frame detection.

BIT [1:0] - Reserved

TABLE 213: FRAMER INTERRUPT STATUS REGISTER (FISR 0XNB04H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
COMFA	Reserved		COFA	IF	FMD	SE	FE
RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC
0	0	0	0	0	0	0	0

BIT 7 - Change of CAS Multiframe Alignment

This bit is used to indicate that the receive synchronization signal has changed CAS multiframe alignment with respect to its last multiframe position.

- 0 - No COMFA occurs.
- 1 - COMFA occurs.

BITS [6:5] - Reserved

BIT 4 - Change of Frame Alignment

This bit is used to indicate that the receive synchronization signal has changed alignment with respect to its last multiframe position.

- 0 - No COFA occurs.
- 1 - COFA occurs.

BIT 3 - In-Frame State

This bit indicates the occurrence of state change of in-frame indication.

- 0 - No state change occurs of in-frame indication.
- 1 - In-frame indication has changed state.

BIT 2 - Frame Mimic State Change

This bit indicates the occurrence of state change of framing mimic detection.

- 0 - No state change occurs of framing mimic detection.
- 1 - Framing mimic detection has changed state.

BIT 1 - Synchronization Bit Error

This bit indicates the occurrence of synchronization bit error event.

- 0 - No synchronization bit error occurs.
- 1 - Synchronization bit error occurs.

BIT 0 - Framing Error

- This bit is used to indicate that one or more frame alignment bit error have occurred. This bit doesn't not necessarily indicate that synchronization has been lost.
  - 0 - No framing bit error occurs.
  - 1 - Framing bit error occurs.

TABLE 214: FRAMER INTERRUPT ENABLE REGISTER (FIER 0XNB05H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
COMFA_ENB	Reserved		COFA_ENB	IF_ENB	FMD_ENB	SE_ENB	FE_ENB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Change of CAS Frame Alignment Interrupt Enable

Setting this bit will enable the interrupt generation when the frame search logic determines that CAS multiframe alignment has been reached and that the new alignment differs from the previous alignment.

- 0 - Disables the interrupt generation of COMFA detection.
- 1 - Enables the interrupt generation of COMFA detection.

BITS [6:5] - Reserved

BIT 4 - Change of Frame Alignment Interrupt Enable

Setting this bit will enable the interrupt generation when the frame search logic determines that frame alignment has been reached and that the new alignment differs from the previous alignment.

- 0 - Disables the interrupt generation of COFA detection.
- 1 - Enables the interrupt generation of COFA detection.

BIT 3 - In-Frame Interrupt Enable

Setting this bit will enable the interrupt generation of an in-frame recognition.

- 0 - Disables the interrupt generation of an in-frame detection.
- 1 - Enables the interrupt generation of an in-frame detection.

BIT 2 - Frame Mimic Detection Interrupt Enable

Setting this bit will enable the interrupt generation when the frame search logic detects the presence of framing bit mimics.

- 0 - Disables the interrupt generation of framing mimic detection.
- 1 - Enables the interrupt generation of framing mimic detection.

BIT 1 - Synchronization Bit Error Interrupt Enable

SE_ENB : Setting this bit will enable the generation of an interrupt when a synchronization bit error event has been detected. A synchronization bit error event is defined as CRC-4 error.

- 0 - The detection of synchronization bit errors does not generate an interrupt.
- 1 - The detection of synchronization bit errors does generate an interrupt

BIT 0 - Framing Error Interrupt Enable

This bits enables the generation of an interrupt when a framing bit error has been detected.

- 0 - Any error in the framing bits does not generate an interrupt.
- 1 - A error in the framing bits does generate an interrupt.

TABLE 215: SLIP BUFFER STATUS REGISTER (SBSR 0XNB08H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					SB_FULL	SB_EMPTY	SB_SLIP
RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC	RUR/WC
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Slip Buffer Fills & a Frame is Deleted

This bit is set when the elastic store fills and a frame is deleted.

BIT 1 - Slip Buffer Empties and a Frame is Repeated

This bit is set when the elastic store empties and a frame is repeated.

BIT 0 - Receive Slips

This bit is set when the slip buffer slips.

TABLE 216: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER 0XNB09H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reserved					SB_FULL	SB_EMPTY	SB_SLIP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved

BIT 2 - Interrupt Enable Bit for Slip Buffer Full

Setting this bit enables interrupt when the elastic store fills and a frame is deleted.

BIT 1 - Interrupt Enable Bit for Slip Buffer Empty

Setting this bit enables interrupt when the elastic store empties and a frame is repeated.

BIT 0 - Interrupt Enable Bit for Slip Buffer Slip

Setting this bit enables interrupt when the slip buffer slips.

6.11 VT Mapping Operation Control Register Descriptions

TABLE 217: GLOBAL VT-MAPPER BLOCK - VT MAPPER BLOCK CONTROL REGISTER (VTMCR = 0X0C03)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Latch Count	REI-V Enable	VT-Mapper Local Loopback [1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT 3 - Latch Count

A "0 to 1" transition within this bit-field commands each of the VT-De-Mapper blocks to update the contents within the following Bit-Fields/PMON registers.

BIT FIELDS	REGISTER NAME	ADDRESS LOCATION
VT-Payload Pointer Increment Count[3:0]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1"	0xND4A
BIP-2 Error Count[11:8]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1"	0xND4A
BIP-2 Error Count[7:0]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 0	0xND4B
VT-Payload Pointer Decrement Count[3:0]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1	0xND4E
REI-V Event Count[11:8]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1	0xND4E
REI-V Event Count[7:0]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 0	0xND4F

BIT 2 - REI-V Enable

This READ/WRITE bit-field is used to configure a given Transmit VT-Mapper block to automatically insert the appropriate REI-V value (based upon the number of BIP-8 bit errors that are detected by the corresponding Receive VT-Mapper block) into the V5 byte, within its outbound VC-12 data-stream.

- 0 - Configures the Transmit VT-Mapper block to NOT automatically insert the REI-V value into each V5 byte, within the outbound VC-12 data-stream.
- 1 - Configures the Transmit VT-Mapper block to automatically insert the REI-V value into each V5 byte, within the outbound VC-12 data-stream.

BIT [1:0] - VT Mapper Local Loopback:

This READ/WRITE bit-field permits the user to configure the XRT86SH221 device to operate in the "VT Mapper Local Loopback" Mode. If the user configures the XRT86SH221 device to operate in this mode, then the output from the VT-Mapper block will be internally looped back into the input of the VT-De-Mapper block.

VT MAPPER LOCAL LOOPBACK [1:0]	VT MAPPER LOCAL LOOPBACK TYPE
00	**No Loopback**
01	**Local Timing VT Mapper Local Loopback Mode:** The VT Mapper Block output data stream along with the external source signals TXCLK, TXBYTE_EN, and TXSOS are internally looped-back into the input of the VT DeMapper Block.
10	**Undefined**
11	**Looptiming VT Mapper Local Loopback Mode:** The VT Mapper Block output data stream along with the internally generated signals LBCLK, LBBYTE_EN, and LBSOS are internally looped-back into the input of the VT DeMapper Block.

TABLE 218: GLOBAL VT MAPPER BLOCK - TEST PATTERN CONTROL REGISTER 1 (VTMTPCR1 = 0X0C0E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Latch Error Count	Insert Pattern Error	Reserved					
R/W	R/W	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Latch Error Count

A 0 to 1 transition within this bit-field commands the Test Pattern Receiver to latch its current Bit Error Count into Bits 6 - 0 (Test Pattern Error Count[14:8]) and BIT [7:0] (Test Pattern Error Count[7:0]) within the VT Mapper - Test Pattern Detector Error Count Register (Address Locations = 0x0C16 and 0x0C17).

BIT 6 - Insert Pattern Error

This bit-field is used to configure the VT-Mapper Test Pattern Generator block to insert a single bit-error into the outbound VT data-stream. A 0 to 1 transition within this bit-field will command the VT-Mapper Test Pattern Generator block to insert a single bit-error into the outbound VT data-stream.

Bits [5:0] - Reserved

TABLE 219: GLOBAL VT-MAPPER BLOCK - TEST PATTERN CONTROL REGISTER 0 (VTMTPCR0 = 0X0C0F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		VC-12 Transmit Test Pattern[1:0]		Reserved			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved

BIT [5:4] - VT2 Transmit Test Pattern[1:0]

This READ/WRITE bit-field is used to specify the test pattern that the VT2 Test Pattern Generator will generate and transmit.

Transmitted Test Pattern

VC-12 TRANSMIT TEST PATTERN[1:0]	TEST PATTERN TRANSMITTED
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

BIT [3:0] - Reserved

TABLE 220: GLOBAL VT-DEMAPPER BLOCK - TEST PATTERN DROP REGISTER 1 (VTDTPDR1 = 0X0C12)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Channel Size[1:0]		Test Channel Drop Side SDH	Test Channel Drop Side[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Test Channel Size[1:0]:

These two READ/WRITE bit-fields are used to specify the Size of the Test Channel (e.g., the Channel that will be used to transport the user-specified Test Pattern.

Test Channel Size

TEST CHANNEL SIZE[1:0]	TEST CHANNEL SIZE
00	Reserved
01	Reserved
10	VC-12
11	Reserved

BIT 5 - Test Channel Drop Side SDH

This READ/WRITE bit-field is used to select the source of the Test Channel. In this case, the user can either select either a E1 Channel originating from the Receive SDH Block or a E1 Channel originating from the Ingress Direction E1 Blocks.

- 0 - Configures the Test Channel Source to be one of the E1 Channels, originating from the Ingress Direction E1 Blocks.
- 1 - Configures the Test Channel Source to be the E1 Channels, originating from the Receive SDH Blocks

BIT [4:0] - Test Channel Drop Side[4:0]

These READ/WRITE bit-fields are used to select which data-stream will be output via the Test Channel.

Output Data Stream via Test Channel

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
00000	Unequipped
00001	E1 Channel 1
00010	E1 Channel 2
00011	E1 Channel 3
00100	Reserved
00101	E1 Channel 4
00110	E1 Channel 5
00111	E1 Channel 6
01000	Reserved
01001	E1 Channel 7
01010	E1 Channel 8

Output Data Stream via Test Channel

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
01011	E1 Channel 9
01100	Reserved
01101	E1 Channel 10
01110	E1 Channel 11
01111	E1 Channel 12
10000	Reserved
10001	E1 Channel 13
10010	E1 Channel 14
10011	E1 Channel 15
10100	Reserved
10101	E1 Channel 16
10110	E1 Channel 17
10111	E1 Channel 18
11000	Reserved
11001	E1 Channel 19
11010	E1 Channel 20
11011	E1 Channel 21
11100	Reserved
11101	AIS will be Generated
11110	Test Channel Input
11111	User Selected Test Pattern

TABLE 221: GLOBAL VT-DEMAPPER BLOCK - TEST PATTERN DROP REGISTER 0 (VTDTPDR0 = 0X0C13)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive (Expected) Pattern[1:0]		Test Channel Drop Side - SDH	Test Channel Drop Side[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Receive (Expected) Pattern:

This READ/WRITE bit-field is used to specify the Test Pattern, that the VT-Mapper Pattern Receiver should be expecting, as shown in the table below.

Expected Test Pattern

RECEIVE (EXPECTED) PATTERN[1:0]	EXPECTED TEST PATTERN
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^{15}-1 PRBS Pattern

BIT 5 - Test Channel Drop-Side SDH

This READ/WRITE bit-field is used to select which set of E1 traffic should be used, as a basis of comparison against the Test Signal. In this case, the user can either select the either the E1 traffic originating from the Ingress Direction E1 Blocks or the E1 traffic originating from the Receive SDH Blocks.

- 0 - Configures the Pattern Receiver to compare the Test Signal with one of the E1 Channels, originating from the Ingress Direction E1 Blocks.
- 1 - Configures the Pattern Receiver to compare the Test Signal with one of the E1 Channels, originating from the Receive SDH Blocks.

BIT [4:0] - Test Channel Drop Side[4:0]:

These READ/WRITE bit-fields are used to select which data-stream will be compared with the Test Signal.

Test Channel Selection

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
00000	Unequipped
00001	E1 Channel 1
00010	E1 Channel 2
00011	E1 Channel 3
00100	Reserved
00101	E1 Channel 4
00110	E1 Channel 5
00111	E1 Channel 6
01000	Reserved

Test Channel Selection

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
01001	E1 Channel 7
01010	E1 Channel 8
01011	E1 Channel 9
01100	Reserved
01101	E1 Channel 10
01110	E1 Channel 11
01111	E1 Channel 12
10000	Reserved
10001	E1 Channel 13
10010	E1 Channel 14
10011	E1 Channel 15
10100	Reserved
10101	E1 Channel 16
10110	E1 Channel 17
10111	E1 Channel 18
11000	Reserved
11001	E1 Channel 19
11010	E1 Channel 20
11011	E1 Channel 21
11100	Reserved
11101	AIS will be Generated
11110	Test Channel Input
11111	Disable Pattern Receiver

TABLE 222: GLOBAL VT-DEMAPPER - TEST PATTERN DETECTOR ERROR COUNT REGISTER 1 (VTDTPDECR1 = 0X0C16)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Mapper Test Pattern Sync	Test Pattern Error Count[14:8]						
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - VT-Mapper Test Pattern Sync:

This READ-ONLY bit-field indicates whether or not the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the incoming Test Signal.

- 0 - VT-Mapper Pattern Receiver is NOT currently declaring Pattern Sync with the incoming Test Signal.
- 1 - VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the incoming Test Signal.

BIT [6:0] - Test Pattern Error Count[14:8]:

These seven (7) RESET-upon-READ bit-fields, along with the Test Pattern Error Count[7:0] bit-fields function as a 15-bit Pattern Bit Error Count Register. If the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the designated Test Signal, then it will increment this register (by the value of 1) each time that it detects Pattern Bit Error.

These seven (7) bit-fields function as the seven most-significant bits of this 15-bit counter.

TABLE 223: GLOBAL VT-DEMAPPER - TEST PATTERN DETECTOR ERROR COUNT REGISTER 0 (VTDTPDECR0 = 0X0C17)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Pattern Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Test Pattern Error Count[7:0]:

These eight (8) RESET-upon-READ bit-fields, along with the Test Pattern Error Count[14:8] bit-fields function as a 15-bit Pattern Bit Error Count Register. If the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the designated Test Signal, then it will increment this register (by the value of 1) each time that it detects Pattern Bit Error.

These eight (8) bit-fields function as the eight least-significant bits of this 15-bit counter.

TABLE 224: GLOBAL VT-MAPPER - TRANSMIT TRIBUTARY SIZE SELECT REGISTER 1 (VTMTTSSR1 = 0X0C1A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		TxTributary Size Select - VT#6[1:0]		TxTributary Size Select - VT#5[1:0]		TxTributary Size Select - VT#4[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1

BIT [7:6] - Reserved:

BIT [5:4] - Transmit Tributary Size Select for VT# 6[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 6) will support.

Size of VT #6

TXTRIBUTARY SIZE SELECT - VT#6[1:0]	RESULTING SIZE OF VT # 6
00	Reerved
01	Reserved
10	VC-12
11	Reserved

NOTE: *This configuration setting only applies to the Transmit VT-Mapper block. This configuration setting does not configure the Receive VT-De-Mapper block to expect any particular VT-type within VT Group # 6. The user must separately configure the Receive VT-De-Mapper block's handling of VT-Group # 6 by setting Bits 4 and 5 (RxTributary Size Select - VT# 6[1:0]) within the VT-Mapper - Receive Tributary Size Select Register (Address = 0x0C1E).*

BIT [3:2] - Transmit Tributary Size Select for VT# 5[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 5) will support.

Size of VT #5

TXTRIBUTARY SIZE SELECT - VT#5[1:0]	RESULTING SIZE OF VT # 5
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [1:0] - Transmit Tributary Size Select for VT# 4[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 4), will support.

Size of VT #4

TXTRIBUTARY SIZE SELECT - VT#4[1:0]	RESULTING SIZE OF VT # 4
00	Reerved
01	Reserved
10	VC-12
11	Reserved

TABLE 225: GLOBAL VT-MAPPER - TRANSMIT TRIBUTARY SIZE SELECT REGISTER 0 (VTMTTSSR0 = 0X0C1B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTributary Size Select - VT#3[1:0]		TxTributary Size Select - VT#2[1:0]		TxTributary Size Select - VT#1[1:0]		TxTributary Size Select - VT#0[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:6] - Transmit Tributary Size Select for VT# 3[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 3), will support.

TxTributary Size Select of VT#3

TXTRIBUTARY SIZE SELECT - VT#3[1:0]	RESULTING SIZE OF VT # 3
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [5:4] - Transmit Tributary Size Select for VT# 2[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 2) will support.

TxTributary Size Select of VT#2

TXTRIBUTARY SIZE SELECT - VT#2[1:0]	RESULTING SIZE OF VT # 2
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [3:2] - Transmit Tributary Size Select for VT# 1[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 1) will support.

TxTributary Size Select of VT#1

TXTRIBUTARY SIZE SELECT - VT#1[1:0]	RESULTING SIZE OF VT # 1
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [1:0] - Transmit Tributary Size Select for VT# 0[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper Block (associated with Virtual Tributary Group # 0) will support.

TxTributary Size Select of VT#0

TXTRIBUTARY SIZE SELECT - VT#0[1:0]	RESULTING SIZE OF VT # 0
00	Reerved
01	Reserved
10	VC-12
11	Reserved

TABLE 226: GLOBAL VT-DEMAPPER - RECEIVE TRIBUTARY SIZE SELECT REGISTER 1 (VTDRTSSR1 = 0X0C1E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		RxTributary Size Select - VT#6[1:0]		RxTributary Size Select - VT#5[1:0]		RxTributary Size Select - VT#4[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1

BIT [7:6] - Reserved:

BIT [5:4] - Receive Tributary Size Select for VT# 6[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper Block (associated with Virtual Tributary Group # 6) will support.

Resulting Size of VT#6

RXTRIBUTARY SIZE SELECT - VT#6[1:0]	RESULTING SIZE OF VT # 6
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [3:2] - Receive Tributary Size Select for VT# 5[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 5) will support.

Resulting Size of VT#5

RXTRIBUTARY SIZE SELECT - VT#5[1:0]	RESULTING SIZE OF VT # 5
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [1:0] - Receive Tributary Size Select for VT# 4[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 4) will support.

Resulting Size of VT#4

RXTRIBUTARY SIZE SELECT - VT#4[1:0]	RESULTING SIZE OF VT # 4
00	Reerved
01	Reserved
10	VC-12
11	Reserved

TABLE 227: GLOBAL VT-DEMAPPER - RECEIVE TRIBUTARY SIZE SELECT REGISTER 0 (VTDRTSSR0 = 0X0C1F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTributary Size Select - VT#3[1:0]		RxTributary Size Select - VT#2[1:0]		RxTributary Size Select - VT#1[1:0]		RxTributary Size Select - VT#0[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:6] - Receive Tributary Size Select for VT# 3[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 3) will support.

Resulting Size of VT#3

RXTRIBUTARY SIZE SELECT - VT#3[1:0]	RESULTING SIZE OF VT # 3
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [5:4] - Receive Tributary Size Select for VT# 2[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 2) will support.

Resulting Size of VT#2

RXTRIBUTARY SIZE SELECT - VT#2[1:0]	RESULTING SIZE OF VT # 2
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [3:2] - Receive Tributary Size Select for VT# 1[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 1) will support.

Resulting Size of VT#1

RXTRIBUTARY SIZE SELECT - VT#1[1:0]	RESULTING SIZE OF VT # 1
00	Reerved
01	Reserved
10	VC-12
11	Reserved

BIT [1:0] - Receive Tributary Size Select for VT# 0[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 0) will support.

Resulting Size of VT#0

RXTRIBUTARY SIZE SELECT - VT#0[1:0]	RESULTING SIZE OF VT # 0
00	Reerved
01	Reserved
10	VC-12
11	Reserved

TABLE 228: CHANNEL CONTROL - VT-MAPPER E1 INSERTION CONTROL REGISTER 1 (VTME1ICR1 = 0XND42)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Ingress Direction E1 AIS Defect Declared	Ingress E1 Loss of Clock Defect Declared	BIP-2 Error Insert	VT Signal Label[2:0]			Auto Transmit RFI-V Indicator	Auto Transmit RDI-V Indicator
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Receive (Ingress Direction) E1 AIS Defect Declared:

This READ/WRITE bit-field indicates whether or not the corresponding E1 signal (that is being handled by this Transmit VT-Mapper block) is transporting the AIS indicator.

- 0 - Indicates that the Ingress Direction E1 signal is NOT currently transporting the AIS indicator.
- 1 - Indicates that the Ingress Direction E1 signal is currently transporting the AIS indicator.

BIT 6 - Receive E1 Loss of Clock Defect Declared:

This READ/WRITE bit-field indicates whether the Transmit VT-Mapper block is currently declaring the Loss of Clock defect condition within the corresponding Ingress Direction E1 signal.

- 0 - Indicates that the Transmit VT-Mapper block is NOT currently declaring the Loss of Clock Defect condition with the corresponding E1 signal.
- 1 - Indicates that the Transmit VT-Mapper block is currently declaring the Loss of Clock Defect condition with the corresponding E1 signal.

BIT 5 - BIP-2 Error Insert into V5

This READ/WRITE bit-field is used to configure the corresponding Transmit VT-Mapper block to transmit erred BIP-2 bits to the remote terminal equipment. If the user invokes this feature, then the Transmit VT-Mapper block will automatically invert the value of the locally-computed BIP-2 bits, prior to transmitting this data to the remote terminal equipment.

- 0 - Configures the Transmit VT-Mapper block to NOT transmit erred BIP-2 bits to the remote terminal equipment.
- 1 - Configures the Transmit VT-Mapper block to transmit erred BIP-2 bits to the remote terminal equipment.

NOTE: *For normal operation, the user should set this bit-field to 0.*

BIT [4:2] - VT Label[2:0]:

These two READ/WRITE bit-fields are used to set the VT Label bit-fields (within each outbound V5 byte) the value of the users choice.

BIT 1 - Auto Transmit RFI-V Indicator

This READ/WRITE bit-field is used to select the source of the RFI-V bit-field, within the V5 byte of each outbound VC-12 traffic.

- 0 - Configures the Transmit VT-Mapper Block to use the on-chip register as the source of the RFI-V bit-field.
- 1 - Configures the Transmit VT-Mapper block to set the RFI-V bit-fields to the appropriate value, based upon any defects that the corresponding Receive VT-Mapper block is currently declaring.

BIT 0 - Auto Transmit RDI-V Indicator

This READ/WRITE bit-field is used to select the source of the RDI-V bit-field, within the V5 byte of each outbound VT2 traffic. The Transmit VT-Mapper block will set the RDI-V bit-fields to the appropriate value, based upon any defect conditions that are currently being declared by the corresponding Receive VT-Mapper block.

- 0 - Configures the Transmit VT-Mapper Block to use the on-chip register as the source of the RDI-V bit-field.
- 1 - Configures the Transmit VT-Mapper block to set the RDI-V bit-fields to the appropriate value, based upon any defects that the corresponding Receive VT-Mapper block is currently declaring.

TABLE 229: CHANNEL CONTROL - VT-MAPPER E1 INSERTION CONTROL REGISTER 0 (VTME1ICR0 = 0XND43)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit RFI-V Value	Transmit RDI-V Value	Transmit AIS-V Indicator	E1 Cross Connect Channel Select_Ingress Direction[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Transmit RFI-V Value:

This READ/WRITE bit-field is used to exercise Software Control over the state of the RFI-V bit-field (within each V5 byte) of the outbound VT data-stream. If the user sets BIT 1 (Auto Transmit RFI-V Indicator), within the VT-Mapper Block - Ingress Direction - E1 Insertion Control Register - 2 to 0, then the Transmit VT-Mapper block will read out the contents within this bit-field, and it will load this value into the RFI-V bit-field within each V5 byte of the outbound VT-data-stream.

NOTE: *This bit-field is ignored if the user sets Bit 1 (Auto Transmit RFI-V Indicator), within the VT Mapper Block - Ingress Direction - E1 Insertion Control Register - 1 to 1.*

BIT 6 - Transmit RDI-V Value:

This READ/WRITE bit-field is used to exercise Software Control over the state of the RDI-V bit-field (within each V5 byte) of the outbound VT data-stream. If the user sets BIT 0 (Auto Transmit RDI-V Indicator), within the VT-Mapper Block - Ingress Direction - E1 Insertion Control Register - 2 to 0, then the Transmit VT-Mapper block will read out the contents within this bit-field, and it will load this value into the RDI-V bit-field within each V5 byte of the outbound VT-data-stream.

NOTE: *This bit-field is ignored if the user sets Bit 0 (Auto Transmit RDI-V Indicator), within the VT Mapper Block - Ingress Direction - E1 Insertion Control Register - 1 to 1.*

BIT 5 - Transmit AIS-V Indicator

This READ/WRITE bit-field is used to command the Transmit VT-Mappper block to transmit the AIS-V indicator (within the corresponding VT2) within the outbound VT-data-stream.

0 - Configures the Transmit VT-Mapper block to NOT transmit the AIS-V indicator within the outbound VT-data-stream.

1 - Configures the Transmit VT-Mapper block to transmit the AIS-V indicator within the outbound VT-data-stream.

BIT [4:0] - E1 (Cross-Connect) Channel Select[4:0]:

These READ/WRITE bit-fields is used to configure the Internal VT-Cross Connect. More specifically, these READ/WRITE bit-fields are used to select which (of the 21 Ingress Direction) E1 signals to be mapped into either a VT2 by this particular Transmit VT-Mapper block. The following table presents the relationship between the settings of these bit-fields and the resulting Cross Connect Configuration.

Cross Connect Configuration

E1 (CROSS-CONNECT) CHANNEL SELECT[4:0]	RESULTING INGRESS DIRECTION E1 CHANNEL BEING HANDLED BY THIS PARTICULAR TRANSMIT VT-MAPPER BLOCK	COMMENTS
00000	Unequipped	This particular VT will be transmitted as an Un-equipped signal
00001	Ingress Direction E1 Channel 1	
00010	Ingress Direction E1 Channel 2	
00011	Ingress Direction E1 Channel 3	
00100	Reserved	
00101	Ingress Direction E1 Channel 4	
00110	Ingress Direction E1 Channel 5	

Cross Connect Configuration

E1 (CROSS-CONNECT) CHANNEL SELECT[4:0]	RESULTING INGRESS DIRECTION E1 CHANNEL BEING HANDLED BY THIS PARTICULAR TRANSMIT VT-MAPPER BLOCK	COMMENTS
00111	Ingress Direction E1 Channel 6	
01000	Reserved	
01001	Ingress Direction E1 Channel 7	
01010	Ingress Direction E1 Channel 8	
01011	Ingress Direction E1 Channel 9	
01100	Reserved	
01101	Ingress Direction E1 Channel 10	
01110	Ingress Direction E1 Channel 11	
01111	Ingress Direction E1 Channel 12	
10000	Reserved	
10001	Ingress Direction E1 Channel 13	
10010	Ingress Direction E1 Channel 14	
10011	Ingress Direction E1 Channel 15	
10100	Reserved	
10101	Ingress Direction E1 Channel 16	
10110	Ingress Direction E1 Channel 17	
10111	Ingress Direction E1 Channel 18	
11000	Reserved	
11001	Ingress Direction E1 Channel 19	
11010	Ingress Direction E1 Channel 20	
11011	Ingress Direction E1 Channel 21	
11100	Reserved	
11101	NONE	
11110	The Test Channel	
11111	Test Pattern - From VT Pattern Generator	

TABLE 230: CHANNEL CONTROL - VT-DEMAPPER E1 DROP CONTROL REGISTER 3 (VTDE1DCR3 = 0XND44)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-V Accepted Value[3:0]				RDI-V Accept Threshold[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - RDI-V Accepted Value[3:0]:

These READ-ONLY bit-fields reflect the most recently value for RDI-V that has been accepted (or validated) by the Receive VT-Mapper Block. The Receive VT-Mapper block will accept (or validate) a given RDI-V value, once it has received this same RDI-V value, within RDI-V_Accept_Threshold[3:0] number of consecutive, incoming VT Multi-frames.

NOTES:

1. These bit-fields are only active if the user has configured the Receive VT-De-Mapper block to support ERDI-V (Enhanced RDI-V).

2. These bit-fields reflect the four-bit RDI-V value that the VT De-Mapper block has accepted via the K4 bytes within the incoming VT/TU data-stream.

BIT [3:0] - RDI-V Accept Threshold[3:0]:

These READ/WRITE bit-fields are used to define the RDI-V Validation criteria for the Receive VT-Mapper block. More specifically, these bit-fields are used to specify the number of consecutive, incoming VT Multi-frame, in which the Receive VT-Mapper block MUST receive a given RDI-V value BEFORE it validates it and loads it into BIT[7:4] (RDI-V Accepted Value[3:0]).

TABLE 231: CHANNEL CONTROL - VT-DEMAPPER E1 DROP CONTROL REGISTER 2 (VTDE1DCR2 = 0XND45)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Reserved						RDI-V Type
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT [6:1] - Unused:

BIT 0 - RDI-V Type:

This READ/WRITE bit-field is used to configure the VT-De-Mapper blocks (associated with a given channel) to support either the SRDI-V (Single Bit - RDI-V) or ERDI-V (Extended - RDI-V) form of signaling. If the user uses only Single-Bit RDI-V, then the RDI-V indicator will only be transported via Bit 0 (RDI-V) within the V5 byte in a VT-data-stream. Conversely, if a user uses Extended RDI-V, then the RDI-V indicator will be transported via both Bits 0 (RDI-V) within the V5 byte, and Bits 3, 2 and 1 within the Z7/K4 byte.

- 0 - Configures the VT-De-Mapper blocks to use the SRDI-V form of Signaling.
- 1 - Configures the VT-De-Mapper blocks to use the ERDI-V form of signaling.

NOTE: *This configuration setting only applies to the VT-De-Mapper block. If the user wishes to configure the VT-Mapper block to support either the "SRDI-V" or the "ERDI-V" form of signaling, then he/she must set Bit 1 (RDI-V Type) within the "Channel Control - VT-Mapper Block - Ingress Direction - Transmit RDI-V Control Register - Byte 0" to the appropriate state.*

TABLE 232: CHANNEL CONTROL - VT-DEMAPPER E1 DROP CONTROL REGISTER 1 (VTDE1DCR1 = 0XND46)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Error Event Declared	VT Size Error Defect Declared	LOP-V Defect Declared	Change in VT Label Value[2:0] Indicator	VT Label Value[2:0]			AIS-V Defect Declared
R/O	R/O	R/O	R/W1C	R/O	R/O	R/O	R/O
0	0	1	0	0	0	0	0

BIT 7 - VT Error Event Declared:

This READ-ONLY bit-field indicates that at least one of the following defects, errors or note-worthy conditions are currently being declared.

- VT Size Error
- LOP-V Defect Declared
- Change in VT Label Event
- AIS-V Defect Declared
- AIS-V Failure Declared
- RFI-V Defect Declared
- RDI-V Defect Declared

▶ 0 - Indicates that none of these above-mentioned defects, errors or note-worthy conditions are currently being declared.

▶ 1 - Indicates that at least one of the above-mentioned events are currently being declared.

BIT 6 - VT Size ErroDefect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-De-Mapper block is currently declaring the VT Size Error defect condition. The Receive VT-De-Mapper block will declare the VT Size Error defect condition anytime it receives a VT data-stream with V1 bytes that contains the incorrect VT-Size bit values, as depicted below.

▶ 0 - Indicates that the Receive VT-De-Mapper block is NOT currently declaring the VT Size Error Defect condition.

▶ 1 - Indicates that the Receive VT-De-Mapper block is currently declaring the VT Size Error Defect condition.

BIT 5 - LOP-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-Mapper block is currently declaring the LOP-V Defect condition.

▶ 0 - Indicates that the Receive VT-De-Mapper Block is currently NOT declaring the LOP-V Defect Condition.

▶ 1 - Indicates that the Receive VT-De-Mapper block is currently declaring the LOP-V Defect Condition

BIT 4 - Change in VT Label[2:0] Indicator:

This READ/WRITE 1 to CLEAR bit-field indicates whether or not the Receive VT-De-Mapper block has detected a Change in VT Signal Label, since the last time the user read and cleared this register bit

0 - Indicates that the Receive VT-De-Mapper block has NOT detected a Change in VT Signal Label since the last time the user read and cleared this register bit.

BIT [3:1] - VT Label Value[2:0]:

This READ-ONLY bit-field reflects the value of the most recently accepted (or validated) VT Signal Label value.

BIT 0 - AIS-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-De- Mapper block is currently declaring the AIS-V defect condition, or not.

▶ 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the AIS-V defect condition.

▶ 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the AIS-V defect condition.

TABLE 233: CHANNEL CONTROL - VT-DEMAPPER E1 DROP CONTROL REGISTER 0 (VTDE1DCR0 = 0XND47)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFI-V Defect Declared	RDI-V Defect Declared	Force E1 AIS In Egress Direction	E1 Cross Connect Channel Select_Egress Direction[4:0]				
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - RFI-V Defect Declared:

This READ/WRITE bit-field indicates whether or not the Receive VT-De-Mapper Block is currently declaring the RFI-V defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the RFI-V defect condition.
- 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the RFI-V defect condition.

BIT 6 - RDI-V Defect Declared:

This READ/WRITE bit-field indicates whether or not the Receive VT-De-Mapper Block is currently declaring the RDI-V defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the RDI-V defect condition.
- 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the RDI-V defect condition.

BIT 5 - Force E1 AIS In Egress Direction

This READ/WRITE bit-field is used to configure this particular Receive VT-De-Mapper block to transmit the E1 AIS indicator within the Egress Direction of this particular E1 Channel.

- 0 - Configures the Receive VT-De-Mapper Block to NOT transmit the E1 AIS Pattern within the Egress Direction corresponding to this particular channel.
- 1 - Configures the Receive VT-De-Mapper block to transmit the E1 AIS Pattern within the Egress Direction corresponding to this particular channel.

BIT [4:0] - E1 Cross Connect Channel Select_Egress Direction[4:0]:

These READ/WRITE bit-fields are used to configure the Internal VT-Cross Connect.

More specifically, these READ/WRITE bit-fields are used to select which (of the 21 Egress Direction) E1 Ports, that this particular Receive VT-Mapper block will route (or direct) its Egress Direction E1 Signal to.

The following table presents the relationship between the settings of these bit-fields and the resulting Cross-Connect Configuration.

Cross Connect Configuration

E1 (CROSS CONNECT) CHANNEL SELECT[4:0]	RESULTING PORT THAT THIS RECEIVE VT-MAPPER BLOCK WILL DIRECT ITS E1 TRAFFIC TO	COMMENTS
00000	Unequipped	
00001	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 1	
00010	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 2	
00011	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 3	
00100	Reserved	

Cross Connect Configuration

E1 (Cross Connect) Channel Select[4:0]	Resulting Port that this Receive VT-Mapper block will direct its E1 Traffic to	Comments
00101	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 4	
00110	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 5	
00111	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 6	
01000	Reserved	
01001	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 7	
01010	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 8	
01011	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 9	
01100	Reserved	
01101	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 10	
01110	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 11	
01111	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 12	
10000	Reserved	
10001	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 13	
10010	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 14	
10011	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 15	
10100	Reserved	
10101	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 16	
10110	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 17	
10111	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 18	
11000	Reserved	
11001	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 19	
11010	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 20	

Cross Connect Configuration

E1 (Cross Connect) Channel Select[4:0]	Resulting Port that this Receive VT-Mapper block will direct its E1 Traffic to	Comments
11011	Egress Direction E1 Signal is routed to the Egress Direction Output of E1 Channel 21	
11100	Reserved	
11101	Reserved	
11110	Reserved	
11111	Reserved	

TABLE 234: CHANNEL CONTROL - VT-DEMAPPER BIP-2 ERROR COUNT REGISTER 1 (VTDBIP2ECR1 = 0XND4A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Payload Pointer Increment Count[3:0]				BIP-2 Error Count[11:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:4] - VT Payload Pointer Increment Count[3:0]:

These RESET-upon-READ bit-fields reflect the number of VT Payload Pointer Increment events that the Receive VT-Mapper block has detected since the last read of this register. The Receive VT-Mapper block will increment the contents within these bit-fields each time that it detects a VT Payload Pointer Increment event within the incoming VT data-stream.

BIT [3:0] - BIP-2 Error Count[11:8]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 0, presents a 12-bit expression that reflects the number of BIP-2 Errors that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the four most significant bit-fields within this 12-bit expression.

TABLE 235: CHANNEL CONTROL - VT-DEMAPPER BIP-2 ERROR COUNT REGISTER 0 (VTDBIP2ECR0 = 0XND4B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIP-2 Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - BIP-2 Error Count[7:0]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1, presents a 12-bit expression that reflects the number of BIP-2 Errors that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the eight least significant bit-fields within this 12-bit expression.

TABLE 236: CHANNEL CONTROL - VT-DEMAPPER REI-V EVENT COUNT REGISTER 1 (VTDREIECR1 = 0XND4E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Payload Pointer Decrement Count[3:0]				REI-V Event Count[11:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:4] - VT Payload Pointer Decrement Count[3:0]:

These RESET-upon-READ bit-fields reflect the number of VT Payload Pointer Decrement events that the Receive VT-Mapper block has detected since the last read of this register. The Receive VT-Mapper block will increment the contents within these bit-fields each time that it detects a VT Payload Pointer Decrement event within the incoming VT data-stream.

BIT [3:0] - REI-V Event Count[11:8]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 0, presents a 12-bit expression that reflects the number of REI-V Events that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the four most significant bit-fields within this 12-bit expression.

TABLE 237: CHANNEL CONTROL - VT-DEMAPPER REI-V EVENT COUNT REGISTER 0 (VTDREIECR0 = 0XND4F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-V Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-V Event Count[7:0]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1, presents a 12-bit expression that reflects the number of REI-V Events that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the eight least significant bit-fields within this 12-bit expression.

TABLE 238: CHANNEL CONTROL - VT-DEMAPPER RECEIVE APS REGISTER 1 (VTDRAPSR1 = 0XND52)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Event Mask - VT Channel	VT Size Error - Event Mask	LOP-V Defect - Event Mask	Change of VT Label - Event Mask	Receive Elastic Store Overflow Event	AIS-V Failure - Event Mask	AIS-V Failure Declared	AIS-V Defect - Event Mask
R/W	R/W	R/W	R/W	R/W1C	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT 7 - Event Mask - VT Channel:

This READ/WRITE bit-field is used to either enable or disable the Channel Control - VT Error Event Declared bit-field (within the VT-Mapper Block - Ingress Direction - E1 Drop Control Register).

If the user disables the VT Error Event Declared register bit, then that particular bit-field will never be asserted in response to any of the following defects, errors or note-worthy conditions.

- VT Size Error
- LOP-V Defect Declared
- Change in VT Label Event
- AIS-V Defect Declared
- AIS-V Failure Declared
- RFI-V Defect Declared
- RDI-V Defect Declared
- Receive Elastic Store Overflow Event
- Change of Receive APS Value Event

▶ 0 - Disables the VT Error Event Declared bit-field, entirely

▶ 1 - Enables the VT Error Event Declared bit-field.

BIT 6 - VT Size Error - Event Mask

This READ/WRITE bit-field is used to either enable or disable the VT Size Error defect to/from causing both the VT Error Event Declared and the VT Size Error Event - Composite bit-fields to be asserted. If the user enables this feature, then the Receive VT-De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the VT Size Error Defect condition. Conversely, if the user disables this feature, then the Receive VT De-Mapper Block will NOT assert the VT Error Event Declared bit-field whenever it declares the VT Size Error Defect condition.

▶ 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the VT Size Error Defect condition.

▶ 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the VT Size Error Defect condition.

BIT 5 - LOP-V Defect - Event Mask

This READ/WRITE bit-field permits the user to either enable or disable the LOP-V Defect defect to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the LOP-V defect condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper Block will NOT assert the VT Error Event Declared bit-field whenever it declares the LOP-V defect condition.

▶ 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the LOP-V defect condition.

▶ 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the LOP-V defect condition

BIT 4 - Change of VT Label - Event Mask

This READ/WRITE bit-field permits the user to either enable or disable the Change of VT Label condition to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT-De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the Change of VT Label condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper block will NOT assert the VT Error Event Declared bit-field whenever it declares the Change of VT Label condition.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the Change of VT Label condition.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the Change of VT Label condition.

BIT 3 - Receive Elastic Store Overflow Event

This READ/W1C bit-field indicates whether or not the Receive Elastic Store Overflow event has occurred (within this Tributary) since the last time that the user has written a 1 to clear this bit-field.

- 0 - Indicates that the Receive Elastic Store Overflow Event has NOT occurred since the last time the user has written a 1 to clear this bit-field.
- 1 - Indicates that the Receive Elastic Store Overflow Event has occurred since the last time the user has written a 1 to clear this bit-field.

BIT 2 - AIS-V Failure - Event Mask

This READ/WRITE bit-field permits the user to either enable or disable the AIS-V Failure condition to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT-De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the AIS-V Failure condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper block will NOT assert the VT Error Event Declared bit-field whenever it declares the AIS-V Failure condition.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the AIS-V Failure condition.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the AIS-V Failure condition.

BIT 1 - AIS-V Failure Declared

This READ-ONLY bit-field indicates whether or not the Receive VT-De-Mapper block is currently declaring the AIS-V Failure condition.

The Receive VT-De-Mapper block will declare the AIS-V Failure condition if it continuously declares the AIS-V Defect condition for 2.5 ± 0.5 seconds. The Receive VT De-Mapper block will clear the AIS-V Failure condition, whenever it has cleared the AIS-V Defect condition for 10 ± 0.5 seconds.

- 0 - Indicates that the Receive VT-De-Mapper block is NOT currently declaring the AIS-V Failure condition.
- 1 - Indicates that the Receive VT-De-Mapper block is currently declaring the AIS-V Failure condition.

BIT 0 - AIS-V Defect - Event Mask

This READ/WRITE bit-field permits the user to either enable or disable the AIS-V Defect condition to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT-De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the AIS-V Defect condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper block will NOT assert the VT Error Event Declared bit-field whenever it declares the AIS-V Defect condition.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the AIS-V Defect condition.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the AIS-V Defect condition.

TABLE 239: CHANNEL CONTROL - VT-DEMAPPER RECEIVE APS REGISTER 0 (VTDRAPSR0 = 0XND53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFI-V Defect Event - Mask	RDI-V Defect Event - Mask	Change of Receive APS Value - Event Mask	Change of Receive APS Value	Receive APS Value[3:0]			
R/W	R/W	R/W	R/W1C	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - RFI-V Defect - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the RFI-V Defect defect to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the RFI-V defect condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper Block will NOT assert the VT Error Event Declared bit-field whenever it declares the RFI-V defect condition.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the RFI-V defect condition.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the RFI-V defect condition.

BIT 6 - RDI-V Defect - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the RDI-V Defect defect to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control - VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the RDI-V defect condition. Conversely, if the user disables this feature, then the Receive VT-De-Mapper Block will NOT assert the VT Error Event Declared bit-field whenever it declares the RDI-V defect condition.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the RDI-V defect condition.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the RDI-V defect condition.

BIT 5 - Change of Receive APS Value - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the Change of APS Value event to/from causing the VT Error Event Declared bit-field to be asserted. If the user enables this feature, then the Receive VT-De-Mapper block will assert Bit 7 (VT Error Event Declared) within the Channel Control VT Mapper Block - Egress Direction - E1 Drop Control Register - Byte 1 to 1 anytime it declares the Change of Receive APS Value event. Conversely, if the user disables this feature, then the Receive VT-De-Mapper Block will NOT assert the VT Error Event Declared bit-field whenever it declares the Change of Receive APS Value event.

- 0 - Configures the Receive VT-De-Mapper block to NOT assert the VT Error Event Declared bit-field whenever it declares the Change of Receive APS Value event.
- 1 - Configures the Receive VT-De-Mapper block to assert the VT Error Event Declared bit-field whenever it declares the Change of Receive APS Value event.

BIT 4 - Change of Receive APS Value:

This READ/W1C bit-field indicates whether or not the Change of Receive APS Value event has occurred (within this Tributary) since the last time that the user has written a 1 to clear this bit-field. The Receive VT-De-Mapper block will declare the Change of Receive APS Value whenever it has accepted a new value from the K4 bytes within the incoming VT data-stream.

- 0 - Indicates that the Change of Receive APS Value event has NOT occurred since the last time the user has written a 1 to clear this bit-field.
- 1 - Indicates that the Change of Receive APS Value event has occurred since the last time the user has written a 1 to clear this bit-field.

BIT [3:0] - Receive APS Value[3:0]:

These four (4) READ-ONLY bit-field reflects the APS value that the VT-De-Mapper block has received (via Bits 1 through 4, within the K4 byte) and has validated.

TABLE 240: CHANNEL CONTROL - VT-MAPPER TRANSMIT APS REGISTER 1 (VTMTAPSR1 = 0XND56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
E1 AIS - Event Mask	E1 LOC - Event Mask	Reserved		Transmit Elastic Store Overflow	Reserved		
R/W	R/W	R/W	R/W	W1C	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - E1 AIS - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of E1 AIS Defect Condition" event to/from causing the "Change of E1 AIS Defect Condition" interrupt to be generated. If the user enables this feature, then the VT-Mapper block will assert the "Change of E1 AIS Defect Condition" interrupt in response to either of the following conditions.

- Whenever the VT-Mapper block declares the "E1 AIS" defect condition within the Ingress Direction E1 Data-stream.
- Whenever the VT-Mapper block clears the "E1 AIS" defect condition within the Ingress Direction E1 Data Stream.

▶ 0 - Configures the VT-Mapper Block to NOT generate the "Change of E1 AIS Defect Condition" interrupt, whenever it declares or clears the E1 AIS defect condition.

▶ 1 - Configures the VT-Mapper Block to generate the "Change of E1 AIS Defect Condition" interrupt, whenever it declares or clears the "E1 AIS defect condition.

BIT 6 - E1 Loss of Clock Event - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of E1 LOC Defect Condition" event to/from causing the "Change of E1 LOC Defect Condition" interrupt to be generated. If the user enables this feature, then the VT-Mapper block will assert the "Change of E1 LOC Defect Condition" interrupt in response to either of the following conditions.

- Whenever the VT-Mapper block declares the "E1 LOC" defect condition within the Ingress Direction E1 Data-stream.
- Whenever the VT-Mapper block clears the "E1 LOC" defect condition within the Ingress Direction E1 Data Stream.

▶ 0 - Configures the VT-Mapper Block to NOT generate the "Change of E1 LOC Defect Condition" interrupt, whenever it declares or clears the E1 LOC defect condition.

▶ 1 - Configures the VT-Mapper Block to generate the "Change of E1 LOC Defect Condition" interrupt, whenever it declares or clears the "E1 LOC defect condition.

BIT [5:4] - Reserved:

BIT 3 - Transmit Elastic Store Overflow:

This READ/W1C bit-field indicates whether or not the VT Mapper block has declared a "Transmit Elastic Store Overflow" event since the last read of this register. The VT-Mapper Block will declare a "Transmit Elastic Store Overflow" event anytime that the "Transmit FIFO" (within the VT-Mapper block) has experience an "overflow" event.

▶ 0 - Indicates that the "Transmit Elastic Store Overflow" event has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Transmit Elastic Store Overflow" event has occurred since the last read of this register.

NOTE: *The VT-Mapper block will typically handle "small timing offsets" (between the Ingress Direction E1 signal and the "Transmit Direction" 19.44MHz or 51.84MHz clock signal via bit-stuffing (as it maps this E1 data into VTs. However, if this bit-field is set to "1", this is typically a indication of a significant clock frequency accuracy problem within the system.*

BIT [2:0] - Reserved:

TABLE 241: CHANNEL CONTROL - VT-MAPPER TRANSMIT APS/K4 REGISTER 0 (VTMTAPSR0 = 0XND57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	TxERDI[2:0]			TxAPS[3:0]			
R/O	R/W	R/W	R/W	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT [6:4] - Transmit ERDI-V[2:0]

These three (3) READ/WRITE bit-fields permit the user to exercise software control over the value of the "ERDI-V" bits that are transported via "Bits 5 through 7" (within the K4 byte) within the outbound VT data-stream.

NOTE: *This bit-field is only active if both of the following is true.*

- The user has configured VT-Mapper/De-Mapper blocks to support the ERDI-V (Extended - RDI-V) form of signaling and,
- The user has set Bit 6 (Transmit RDI-V Value) within the "Channel Control - VT Mapper Block - Ingress Direction - E1 Insertion Control Register - 0" to "1".

BIT [3:0] - Transmit APS Value[3:0]

These four (4) READ/WRITE bit-fields permit the user to exercise software control over the value of the "APS" bits that are transported via Bits 1 through 4 (within the K4 byte) within the outbound VT data-stream.

TABLE 242: CHANNEL CONTROL - VT-DEMAPPER TANDEM CONNECTION - RECEIVE BIP-2 ERROR COUNT REGISTER 2 (VTDTCBIP2ECR = 0XND59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TC_BIP_2 Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Tandem Connection Receive BIP-2 Error Count:

This RESET-upon-READ bit-fields present an 8-bit expression that reflects the number of BIP-2 Errors that the Receive VT-Mapper Block has detected (within Bit-7 and Bit-6 of the N2 Byte of the incoming VT-data-stream) since the last read of this register.

TABLE 243: CHANNEL CONTROL - VT-DEMAPPER TANDEM CONNECTION - RECEIVE REI-V EVENT COUNT REGISTER 1 (VTDTCREIECR = 0XND5B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TC_REI-V Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Tandem Connection Receive REI-V Event Count:

This RESET-upon-READ bit-fields present an 8-bit expression that reflects the number of REI-V Events that the Receive VT-Mapper Block has detected (within Bit-3 of the N2 Byte of the incoming VT-data-stream) since the last read of this register.

TABLE 244: CHANNEL CONTROL - VT-DEMAPPER TANDEM CONNECTION - RECEIVE OEI EVENT COUNT REGISTER 0 (VTDTCOEIECR = 0XND5F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TC_OEI Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Tandem Connection Receive OEI Event Count:

This RESET-upon-READ bit-fields present an 8-bit expression that reflects the number of OEI Events that the Receive VT-Mapper Block has detected (within Bit-2 of the N2 Byte of the incoming VT-data-stream) since the last read of this register.

TABLE 245: CHANNEL CONTROL - VT-DEMAPPER COMPOSITE STATUS REGISTER 1 (VTDCSR1 = 0XND60)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Change of Receive APS Value - Composite	Transmit or Receive Elastic Store Over-flow Event - Composite
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved:

BIT 1 - Change of Receive APS Value Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block has detected a change of state of the received VT path APS signalling. Three consecutive consistent new values for the received VT Path APS signal must be detected for this bit to be set.

- 0 - Indicates that the VT-De-Mapper block is NOT currently detecting a change of state of the VT Path APS signalling.
- 1 - Indicates that the VT-De-Mapper block is currently detecting a change of state of the VT Path APS signalling.

BIT 0 - Transmit or Receive Elastic Store Overflow Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block has experienced either a receive or a transmit elastic store overflow.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring a receive or a transmit elastic store overflow.
- 1 - Indicates that the VT-De-Mapper block is currently declaring a receive or a transmit elastic store overflow.

TABLE 246: CHANNEL CONTROL - VT-DEMAPPER COMPOSITE STATUS REGISTER 0 (VTDCSR0 = 0XND61)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Size Error Event - Composite	LOP-V Defect Event - Composite	RFI-V Defect Event - Composite	RDI-V Defect Event - Composite	AIS-V Defect Event - Composite	AIS Pointer Event - Composite	Change in VT Label Event - Composite	E1 AIS or LOC Event - Composite
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - VT Size Error Event - Composite:

This READ-ONLY bit-field reports whether or not an incorrect virtual container size bits were received. The valid virtual container size bits are "10" for VT2/TU-12.

- 0 - Indicates that the VT-De-Mapper block is NOT currently receiving an incorrect VT Size bits error.
- 1 - Indicates that the VT-De-Mapper block is currently receiving an incorrect VT Size bits error.

BIT 6 - LOP-V Defect Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "VT Path Loss of Pointer" (LOP-V) defect condition.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the LOP-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the LOP-V defect condition.

BIT 5 - RFI-V Defect Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Remote Failure Indicator" (RFI-V) defect condition. Three consecutive VT Frames with consistent RFI defect indicator value must be detected for this bit to be set.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the RFI-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the RFI-V defect condition.

BIT 4 - RDI-V Defect Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Remote Defect Indicator" (RDI-V) defect condition. Three consecutive VT Frames with consistent RDI defect indicator value must be detected for this bit to be set.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the RDI-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the RDI-V defect condition.

BIT 3 - AIS-V Defect Event - Composite:

This READ-ONLY bit-field indicates whether or not one or more of the VT-De-Mapper block is currently declaring the "Alarm Indication Signal" (AIS-V) defect condition due to one of the VT AIS-F fields in the RAPSxx registers being active and not masked. This bit will be set if AIS-V defect condition has been declared in any of the 21 VT-De-mapper block.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the AIS-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the AIS-V defect condition.

BIT 2 - AIS Pointer Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Alarm Indication Signal Pointer" (AISP-V) defect condition. Three consecutive VT Frames with all ones value for V1 and V2 pointer bytes must be detected for this bit to be set.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the AISP-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the AISP-V defect condition.

BIT 1 - Change in VT Label Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently detecting a VT Label change of state event. Three consecutive VT Frames with a consistently different VT Label value must be detected for this bit to be set.

- 0 - Indicates that the VT-De-Mapper block is NOT currently detecting a VT Label change condition.
- 1 - Indicates that the VT-De-Mapper block is currently detecting a VT Label change condition.

BIT 0 - E1 AIS or LOC Event - Composite:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Alarm Indication Signal Defect" (AIS-V) or "Loss of Clock" (LOC-V) defect condition.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the AIS-V or LOC-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the AIS-V or LOC-V defect condition.

TABLE 247: CHANNEL CONTROL - VT-DEMAPPER TANDEM CONNECTION STATUS REGISTER (VTDTCSR = 0XND62)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	TC RDI Defect Declared	TC ODI Defect Declared	TC API Message Mismatch Defect Declared	Unstable TC API Message Defect Declared	TC LOMF Defect Declared	TC UNEQ Defect Declared	TC AIS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - TC RDI-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently detecting a Remote Defect Indicator in Bit-0 of the Tandem Connection Frame 73 for 5 consecutive frames. This alarm is cleared when no RDI defect indicator is detected in Bit-0 of the Tandem Connection Frame 73 for 5 consecutive frames.

- 0 - Indicates that the VT-De-Mapper block is NOT currently detecting a TC RDI-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently detecting a TC RDI-V defect condition.

BIT 5 - TC ODI-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently detecting an Outgoing Defect Indicator in Bit-1 of the Tandem Connection Frame 74 for 5 consecutive frames. This alarm is cleared when no ODI-V defect indicator is detected in Bit-1 of the Tandem Connection Frame 74 for 5 consecutive frames.

- 0 - Indicates that the VT-De-Mapper block is NOT currently detecting a TC ODI-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently detecting a TC ODI-V defect condition.

BIT 4 - TC API-V Message Mismatch Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Tandem Connection Access Point Identifier Message Mismatch" defect condition. This defect is declared when a Tandem Connection API message is accepted that is different from the expected Tandem Connection API message. This defect is cleared when the expected API message is received on the J2 byte for N consecutive messages, where N is either 3 or 5 depending on the message acceptance threshold set for API messages on Bit-3 of the Channel Control - VT-De-Mapper Path Trace Buffer Control Register (VTDPTBCR) on address 0xND71.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring a TC API message mismatch.
- 1 - Indicates that the VT-De-Mapper block is currently declaring a TC API message mismatch.

BIT 3 - Unstable TC API-V Message Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "Tandem Connection Unstable Access Point Identifier Message" defect condition. This defect is declared when the internal TC API unstable message counter has detected 8 or more consecutively different API message. The VT-De-Mapper block will increment the internal TC API unstable message counter for each time that it receives a Tandem Connection API Message that differs from the previously received message. This defect is cleared when the same API message is received on the J2 byte for N consecutive messages, where N is either 3 or 5 depending on the message acceptance threshold set for API messages on Bit-3 of the Channel Control - VT-De-Mapper Path Trace Buffer Control Register (VTDPTBCR) on address 0xND71.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring a TC Unstable API message mismatch.
- 1 - Indicates that the VT-De-Mapper block is currently declaring a TC Unstable API message mismatch.

BIT 2 - TC LOMF-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring a "Tandem Connection Loss of Multiframe" defect condition.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the TC LOMF-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the TC LOMF-V defect condition.

BIT 1 - TC UNEQ-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently detecting a "Tandem Connection Unequipped Indication Signal" defect condition.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the TC UNEQ-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the TC UNEQ-V defect condition.

BIT 0 - TC AIS-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently detecting a "Tandem Connection Alarm Indication Signal" defect condition in the received N2 byte.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the TC AIS-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the TC AIS-V defect condition.

TABLE 248: CHANNEL CONTROL - VT-DEMAPPER J2 BYTE STATUS REGISTER (VTDJ2BSR = 0XND63)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					TIM-V Defect Declared	VT Path Trace Message Unstable Defect Declared	Reserved
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved:

BIT 2 - TIM-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "VT Trace Identification Mismatch" (TIM-V) defect condition.

The VT-De-Mapper block will declare the TIM-V defect condition, when none of the received 1, 16 or 64-byte string (received via the J2 byte, within the incoming VT-data-stream) matches the expected 1, 16 or 64 byte message.

The VT-De-Mapper block will clear the "TIM-V" defect condition, when 80% of the received 1, 16 or 64 byte string (received via the J2 byte) matches the 1, 16 or 64 byte message.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the TIM-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the TIM-V defect condition.

BIT 1 - VT Path Trace Message Unstable Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "VT Path Trace Message Unstable" defect condition. The VT-De-Mapper block will declare the "VT Path Trace Message Unstable" defect condition, whenever the "VT Path Trace Message Unstable" counter reaches the value "8". The VT-De-Mapper block will increment the "VT Path Trace Message Unstable" counter for each time that it receives a "VT Path Trace Message" that differs from the previously received message. The "VT Path Trace Message Unstable" counter is cleared to "0" whenever the VT-De-Mapper block has received a given "VT Path Trace Message" 3 (or 5) consecutive times.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the "VT:Path Trace Message Unstable" defect condition.
- 1 - Indicates that the VT De-Mapper block is currently declaring the "VT Path Trace Message Unstable" defect condition.

NOTE: *The VT-De-Mapper block will also set this bit-field "0" anytime it receives a given "VT Path Trace Message" 3 (or 5) consecutive times.*

BIT 0 - Reserved:

TABLE 249: CHANNEL CONTROL - VT-DEMAPPER COMPOSITE STATUS REGISTER 1 (VTDCSR1 = 0XND64)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Change of Receive APS Value- Composite	Elastic Store Overflow Event Composite
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved:

BIT 1 - Change of Receive APS Value Interrupt:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Receive APS Value" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "APS" value (from the K4 bytes within the incoming VT-data-stream).

- 0 - Indicates that the "Change of Receive APS Value" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of Receive APS Value" Interrupt has occurred since the last read of this register.

BIT 0 - Transmit or Receive Elastic Store Overflow Event Interrupt:

This RESET-upon-READ bit-field indicates whether or not the "VT Mapper/VT-De-Mapper" block has generated the "Elastic Store Overflow Event" Interrupt since the last read of this register. The VT-Mapper/De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the "Transmit FIFO" within the VT-Mapper Block, experiences an overflow event.
- Whenever the "Receive FIFO" within the VT-De-Mapper Block, experiences an overflow event.

- 0 - Indicates that the channel has NOT generated an "Elastic Store Overflow" Interrupt since the last read of this register.
- 1 - Indicates that the channel has generated an "Elastic Store Overflow" interrupt since the last read of this register.

TABLE 250: CHANNEL CONTROL - VT-DEMAPPER COMPOSITE STATUS REGISTER 0 (VTDCSR0 = 0XND65)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Size Error Interrupt Status	Change of LOP-V Defect Condition Interrupt Status	Change of RFI-V Defect Condition Interrupt Status	Change of RDI-V Defect Condition Interrupt Status	Change of AIS-V Failure Condition Interrupt Status	Change of AIS-V Defect Condition Interrupt Status	Change of VT Label Interrupt Status	Change of E1 AIS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - VT Size Error Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "VT Size Error" Interrupt since the last read of this register. The VT-De-Mapper block will generate the "VT Size Error" Interrupt anytime it declares the "VT Size Error" defect condition.

- 0 - Indicates that the VT Size Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the VT Size Error Interrupt has occurred since the last read of this register.

BIT 6 - Change of LOP-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of LOP-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the LOP-V defect condition.
- Whenever the VT-De-Mapper block clears the LOP-V defect condition.

- 0 - Indicates that the "Change of LOP-V Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of LOP-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 5 - Change of RFI-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of RFI-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the RFI-V defect condition
- Whenever the VT-De-Mapper block clears the RFI-V defect condition.

- 0 - Indicates that the "Change of RFI-V Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of RFI-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 4 - Change of RDI-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of RDI-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the RDI-V defect condition.
- Whenever the VT-De-Mapper block clears the RDI-V defect condition.

- 0 - Indicates that the "Change of RDI-V Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of RDI-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 3 - Change of AIS-V Failure Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of AIS-V Failure Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the AIS-V failure condition.
- Whenever the VT-De-Mapper block clears the AIS-V failure condition.

▶ 0 - Indicates that the "Change of AIS-V Failure Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of AIS-V Failure Condition" Interrupt has occurred since the last read of this register.

BIT 2 - Change of AIS-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of AIS-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the AIS-V defect condition.
- Whenever the VT-De-Mapper block clears the AIS-V defect condition.

▶ 0 - Indicates that the "Change of AIS-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of AIS-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 1 - Change of VT Label Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "Change of VT Label Value" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt anytime it has "accepted" a new VT Label value (that it has received via the V5 byte within the incoming VT data-stream).

▶ 0 - Indicates that the "Change of VT Label Value" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of VT Label Value" Interrupt has occurred since the last read of this register.

BIT 0 - Change of E1 AIS Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "Change of E1 AIS Defect Condition" Interrupt has occurred since the last read of this register. The VT-Mapper block will generate this interrupt in response to any one of the following conditions.

- Whenever the VT-Mapper block declares the E1 AIS Defect (with the Ingress Direction E1 traffic).
- Whenever the VT-Mapper block clears the E1 AIS Defect (within the Ingress Direction E1 traffic).

▶ 0 - Indicates that the "Change of E1 AIS Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of E1 AIS Defect Condition" Interrupt has occurred since the last read of this register.

TABLE 251: CHANNEL CONTROL - VT-DEMAPPER TANDEM CONNECTION INTERRUPT STATUS REGISTER (VTDTCISR = 0XND66)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	TC RDI Defect Interrupt Status	TC ODI Defect Interrupt Status	TC API Message Mismatch Defect Interrupt Status	Unstable TC API Message Defect Interrupt Status	TC LOMF Interrupt Status	TC UNEQ Defect Interrupt Status	TC AIS Defect Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - Change of TC RDI-V Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Remote Defect Indicator Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC RDI-V defect condition.
- Whenever the VT-De-Mapper block clears the TC RDI-V defect condition.

▶ 0 - Indicates that the "Change of TC RDI-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC RDI-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 5 - Change of TC ODI-V Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Outgoing Defect Indicator Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC ODI-V defect condition.
- Whenever the VT-De-Mapper block clears the TC ODI-V defect condition.

▶ 0 - Indicates that the "Change of TC ODI-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC ODI-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 4 - Change of TC API-V Message Mismatch Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Access Point Identifier Message Mismatch Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.
- Whenever the VT-De-Mapper block clears the TC API-V Message Mismatch defect condition.

▶ 0 - Indicates that the "Change of TC API-V Message Mismatch Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC API-V Message Mismatch Defect Condition" Interrupt has occurred since the last read of this register.

BIT 3 - Change of Unstable TC API-V Message Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Unstable Tandem Connection Access Point Identifier Message Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the Unstable TC API-V Message defect condition.
- Whenever the VT-De-Mapper block clears the Unstable TC API-V Message defect condition.

▶ 0 - Indicates that the "Change of Unstable TC API-V Message Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of Unstable TC API-V Message Defect Condition" Interrupt has occurred since the last read of this register.

BIT 2 - Change of TC LOMF-V Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Loss of Multiframe Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC LOMF-V defect condition.
- Whenever the VT-De-Mapper block clears the TC LOMF-V defect condition.

▶ 0 - Indicates that the "Change of TC LOMF-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC LOMF-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 1 - Change of TC UNEQ-V Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Unequipped Indication Signal Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC UNEQ-V defect condition.
- Whenever the VT-De-Mapper block clears the TC UNEQ-V defect condition.

▶ 0 - Indicates that the "Change of TC UNEQ-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC UNEQ-V Defect Condition" Interrupt has occurred since the last read of this register.

BIT 0 - Change of TC AIS-V Defect Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of Tandem Connection Alarm Indication Signal Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the TC AIS-V defect condition.
- Whenever the VT-De-Mapper block clears the TC AIS-V defect condition.

▶ 0 - Indicates that the "Change of TC AIS-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TC AIS-V Defect Condition" Interrupt has occurred since the last read of this register.

TABLE 252: CHANNEL CONTROL - VT-DEMAPPER INTERRUPT STATUS REGISTER 0 (VTDISR0 = 0XND67)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Change of VT Path Trace Message Unstable Defect Condition Interrupt Status	New VT Path Trace Message Interrupt Status	Change of TIM-V Defect Condition Interrupt Status	Reserved		
R/O	R/O	RUR	RUR	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved:

BIT 5 - Change of VT Path Trace Message Unstable Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the "VT Path Trace Message Unstable" Defect condition.
- Whenever the VT De-Mapper block clears the "VT Path Trace Message Unstable" Defect condition.

▶ 0 - Indicates that the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.

BIT 4 - New VT Path Trace Message Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "New VT Path Trace Message" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "VT Path Trace Message" via the incoming VT-data-stream.

▶ 0 - Indicates that the "New VT Path Trace Message" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "New VT Path Trace Message" Interrupt has occurred since the last read of this register.

BIT 3 - Change of TIM-V Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of TIM-V Defect Condition" interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TIM-V Defect condition.
- Whenever it clears the TIM-V Defect condition.

▶ 0 - Indicates that the "Change of TIM-V Defect Condition" interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TIM-V Defect Condition" interrupt has occurred since the last read of this register.

BIT [2:0] - Reserved:

TABLE 253: CHANNEL CONTROL - VT-DEMAPPER INTERRUPT ENABLE REGISTER 2 (VTDIER2 = 0XND68)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Change of Receive APS Value Interrupt Enable	Elastic Store Overflow Event Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved:

BIT 1 - Change of Receive APS Value Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive APS Value" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt anytime it has "accepted" a new APS value (via the K4 byte within the incoming VT-data-stream).

- 0 - Disables the "Change of Receive APS Value" Interrupt.
- 1 - Enables the "Change of Receive APS Value" Interrupt.

BIT 0 - Transmit or Receive Elastic Store Overflow Event Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Elastic Store Overflow Event" interrupt. If the user enables this interrupt, then the channel will generate this interrupt in response to either of the following conditions.

- Whenever the "Transmit FIFO" within the VT-Mapper Block, experiences an overflow event.
- Whenever the "Receive FIFO" within the VT-De-Mapper block, experiences an overflow event.

- 0 - Disables the "Elastic Store Overflow Event" Interrupt.
- 1 - Enables the "Elastic Store Overflow Event" Interrupt.

TABLE 254: CHANNEL CONTROL - VT-DE-MAPPER INTERRUPT ENABLE REGISTER 1 (VTDIER1 = 0XND69)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Size Error Interrupt Enable	Change of LOP-V Defect Condition Interrupt Enable	Change of RFI-V Defect Condition Interrupt Enable	Change of RDI-V Defect Condition Interrupt Enable	Change of AIS-V Failure Condition Interrupt Enable	Change of AIS-V Defect Condition Interrupt Enable	Change of VT Label Interrupt Enable	Change of E1 AIS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - VT Size Error Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "VT Size Error" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt anytime it declares the "VT Size Error" defect condition.

- 0 - Disables the "VT Size Error" Interrupt.
- 1 - Enables the "VT Size Error" Interrupt.

BIT 6 - Change of LOP-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOP-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the LOP-V Defect Condition.
- Whenever it clears the LOP-V Defect condition.

- 0 - Disables the "Change of LOP-V Defect Condition" Interrupt.
- 1 - Enables the "Change of LOP-V Defect Condition" Interrupt.

BIT 5 - Change of RFI-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of RFI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the RFI-V Defect Condition.
- Whenever it clears the RFI-V Defect condition.

- 0 - Disables the "Change of RFI-V Defect Condition" Interrupt.
- 1 - Enables the "Change of RFI-V Defect Condition" Interrupt.

BIT 4 - Change of RDI-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the RDI-V Defect Condition.
- Whenever it clears the RDI-V Defect condition.

- 0 - Disables the "Change of RDI-V Defect Condition" Interrupt.
- 1 - Enables the "Change of RDI-V Defect Condition" Interrupt.

BIT 3 - Change of AIS-V Failure Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-V Failure Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the AIS-V Failure Condition.
- Whenever it clears the AIS-V Failure condition.

▶ 0 - Disables the "Change of AIS-V Failure Condition" Interrupt.

▶ 1 - Enables the "Change of AIS-V Failure Condition" Interrupt.

BIT 2 - Change of AIS-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the AIS-V Defect Condition.
- Whenever it clears the AIS-V Defect condition.

▶ 0 - Disables the "Change of AIS-V Defect Condition" Interrupt.

▶ 1 - Enables the "Change of AIS-V Defect Condition" Interrupt.

BIT 1 - Change of VT Label Value Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of VT Label Value" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt anytime it has "accepted" a new "VT Label Value" via the V5 bytes within the incoming VT-data-stream.

▶ 0 - Disables the "Change of VT Label Value" Interrupt.

▶ 1 - Enables the "Change of VT Label Value" Interrupt.

BIT 0 - Change of E1 AIS Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of E1 AIS Defect Condition" interrupt. If the user enables this interrupt, then the "VT-Mapper" block will generate this interrupt in response to either of the following events.

- Whenever it declares the E1 AIS defect condition.
- Whenever it clears the E1 AIS defect condition.

▶ 0 - Disables the "Change of E1 AIS Defect Condition" interrupt.

▶ 1 - Enables the "Change of E1 AIS Defect Condition" interrupt.

TABLE 255: CHANNEL CONTROL - VT-DE-MAPPER TANDEM CONNECTION INTERRUPT ENABLE REGISTER (VTDTCIER = 0XND6A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	TC RDI Defect Interrupt Enable	TC ODI Defect Interrupt Enable	TC API Message Mismatch Defect Interrupt Enable	Unstable TC API Message Defect Interrupt Enable	TC LOMF Interrupt Enable	TC UNEQ Defect Interrupt Enable	TC AIS Defect Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - Change of TC RDI-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC RDI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TC RDI-V Defect Condition.
- Whenever it clears the TC RDI-V Defect condition.

▶ 0 - Disables the "Change of TC RDI-V Defect Condition" Interrupt.

▶ 1 - Enables the "Change of TC RDI-V Defect Condition" Interrupt.

BIT 5 - Change of TC ODI-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC ODI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TC ODI-V Defect Condition.
- Whenever it clears the TC ODI-V Defect condition.

▶ 0 - Disables the "Change of TC ODI-V Defect Condition" Interrupt.

▶ 1 - Enables the "Change of TC ODI-V Defect Condition" Interrupt.

BIT 4 - Change of TC API-V Message Mismatch Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC API-V Message Mismatch Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TC API-V Message Mismatch Condition.
- Whenever it clears the TC API-V Message Mismatch condition.

▶ 0 - Disables the "Change of TC API-V Message Mismatch Condition" Interrupt.

▶ 1 - Enables the "Change of TC API-V Message Mismatch Condition" Interrupt.

BIT 3 - Change of Unstable TC API-V Message Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Unstable TC API-V Message Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the Unstable TC API-V Message defect condition.
- Whenever it clears the Unstable TC API-V Message defect condition.

▶ 0 - Disables the "Change of Unstable API-V Message Defect Condition" Interrupt.

▶ 1 - Enables the "Change of Unstable API-V Message Defect Condition" Interrupt.

BIT 2 - Change of TC LOMF-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC LOMF-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TC LOMF-V Defect Condition.
- Whenever it clears the TC LOMF-V Defect condition.

▶ 0 - Disables the "Change of TC LOMF-V Defect Condition" Interrupt.

▶ 1 - Enables the "Change of TC LOMF-V Defect Condition" Interrupt.

BIT 1 - Change of TC UNEQ-V Indication Signal Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC UNEQ-V Indication Signal Condition" Interrupt. If the user enables this interrupt, then the "VT-Mapper" block will generate this interrupt in response to either of the following events.

- Whenever it declares the TC UNEQ-V Indication Signal condition.
- Whenever it clears the TC UNEQ-V Indication Signal condition.

▶ 0 - Disables the "Change of TC UNEQ-V Indication Signal" Interrupt.

▶ 1 - Enables the "Change of TC UNEQ-V Indication Signal" Interrupt.

BIT 0 - Change of TC AIS-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TC AIS-V Defect Condition" interrupt. If the user enables this interrupt, then the "VT-Mapper" block will generate this interrupt in response to either of the following events.

- Whenever it declares the TC AIS-V defect condition.
- Whenever it clears the TC AIS-V defect condition.

▶ 0 - Disables the "Change of TC AIS-V Defect Condition" interrupt.

▶ 1 - Enables the "Change of TC AIS-V Defect Condition" interrupt.

TABLE 256: CHANNEL CONTROL - VT-DE-MAPPER INTERRUPT ENABLE REGISTER 0 (VTDIER0 = 0XND6B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Change of VT Path Trace Message Unstable Defect Condition Interrupt Enable	New VT Path Trace Message Interrupt Enable	Change of TIM-V Defect Condition Interrupt Enable	Reserved		
R/O	R/O	R/W	R/W	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved:

BIT 5 - Change of VT Path Trace Message Unstable Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of VT Path Trace Message Unstable Defect Condition" interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt in response to either of the following events.

- Whenever the VT-De-Mapper block declares the "VT-Path Trace Message Unstable" defect condition.
- Whenever the VT-De-Mapper block clears the "VT-Path Trace Message Unstable" defect condition.

▶ 0 - Disables the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt.

▶ 1 - Enables the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt.

BIT 4 - New VT Path Trace Message Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "New VT Path Trace Message" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "VT Path Trace Message" via the incoming VT-data-stream.

▶ 0 - Disables the "New VT Path Trace Message" Interrupt.

▶ 1 - Enables the "New VT Path Trace Message" Interrupt.

BIT 3 - Change of TIM-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TIM-V Defect Condition" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt in response to either of the following events.

- Whenever it declares the TIM-V Defect Condition.
- Whenever it clears the TIM-V Defect Condition.

▶ 0 - Disables the "Change of TIM-V Defect Condition" Interrupt.

▶ 1 - Enables the "Change of TIM-V Defect Condition" Interrupt.

BIT [2:0] - Reserved:

TABLE 257: CHANNEL CONTROL - VT-DE-MAPPER PATH TRACE BUFFER CONTROL REGISTER (VTDPTBCR = 0XND71)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive TC Enable [1:0]		Reserved	Receive VT Path Trace Message Buffer Select	VT Path Trace Mes-sage Accept Threshold	VT Path Trace Message Type	VT Path Trace Message Length[1:0]	
R/W	R/W	RUR	RUR	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:6] - Received TC Enable[1:0]:

These two READ/WRITE bit-fields are used to enable the Tandem Connection feature in the VT DeMapper. The VT Path Trace Message Length [1:0] on Bit-1 and Bit-0 must be set to the value "0x01" or "0x00" depending on the expected 16 bytes or 1 byte message length.

The relationship between the contents of these bit-fields and the corresponding Receive Tandem Connection Messaging Type is presented below.

RECEIVE TC ENABLE[1:0]	RECEIVE TANDEM CONNECTION OPERATION
00	Tandem Connection feature is disabled.
01	Tandem Connection Enabled for 16-Byte Messaging Operation. The N2 Byte Messaging memory buffer segment is shared with the J2 64-Byte memory buffer. 16-Bytes message length must be selected using the appropriate values written on VT Path Trace Message Length[1:0] Bit-1 and Bit-0.
10	Reserved.
11	Tandem Connection Enabled for 1-Byte Messaging Operation. 1-Byte message length must be selected using the appropriate values written on VT Path Trace Message Length[1:0] Bit-1 and Bit-0.

BIT 5 - Reserved:

BIT 4 - Received VT Path Trace Message Buffer Select:

This READ/WRITE bit-field permits a user to specify which of the following "Receive VT Path Trace Message" buffer segments that the Microprocessor will read out whenever it reads out the contents of the Receive Path Trace Message buffer.

- a.The "Actual" Receive VT Path Trace Message Buffer. The "Actual" Receive VT Path Trace Message Buffer contains the contents of the most recently received (and accepted) VT Path Trace Messages via the incoming VT-data-stream.
- b.The "Expected" Receive VT Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the "VT Path Trace Message" that the user "expects" to receive. The contents of this particular buffer are usually specified by the user.

▶ 0 - Configures the chip to return the contents of the "Actual" Receive VT Path Trace Message" Buffer, whenever the user executes a READ to the "Receive VT Path Trace Message" Buffer.

▶ 1 - Configures the chip to return the contents of the "Expected" Receive VT Path Trace Message" Buffer, whenever the user executes a READ to the "Receive VT Path Trace Message" Buffer.

BIT 3 - Receive VT Path Trace Message Accept Threshold:

This READ/WRITE bit-field permits a user to select the number of consecutive times that the "VT-De-Mapper" block must receive a given "VT Path Trace Message" before it is "validated" and loaded into the "Actual" Receive VT Path Trace Message Buffer, as described below.

▶ 0 - Configures the VT-De-Mapper block to "validate" the incoming VT Path Trace Message after it has received it the

third time in succession.

- 1 - Configures the VT-De-Mapper block to "validate" the incoming VT Path Trace Message after it has received it the fifth time in succession.

BIT 2 - Receive VT Path Trace Message Type:

This READ/WRITE bit-field permits the user to specify how the "VT-De-Mapper" block will locate the boundary of the incoming VT Path Trace Message (within the incoming VT-data-stream) as depicted below.

- 0 - Configures the VT-De-Mapper block to expect the "VT Path Trace Message" boundary to be denoted by a "Line Feed" character.
- 1 - Configures the VT-De-Mapper block to except the "VT Path Trace Message" boundary to be denoted by the presence of a "1" in the "MSB" (Most Significant bit) of the first byte (within the incoming VT Path Trace Message). In this case, all of the remaining bytes (within the incoming VT Path Trace Message) will each have a "0" within their MSBs.

BIT [1:0] - VT Path Trace Message Length[1:0]:

These READ/WRITE bit-fields permit the user to specify the length of the "Receive VT Path Trace Message that the "VT-De-Mapper" block will accept and load into the "Actual" Receive VT Path Trace Message Buffer. The relationship between the contents of these bit-fields and the corresponding "Receive VT Path Trace Message" Length is presented below.

VT PATH TRACE MESSAGE LENGTH[1:0]	RESULTING VT PATH TRACE MESSAGE LENGTH (BYTES)
00	1
01	16
1X	64

TABLE 258: CHANNEL CONTROL - VT-DE-MAPPER AUTO AIS CONTROL REGISTER 1 (VTDAAISCR1 = 0XND72)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Auto Transmit AIS-V upon AIS-V Defect	Auto Transmit AIS-V upon UNEQ-V Defect	Reserved	Auto Transmit AIS-V upon LOP-V Defect	Auto Transmit AIS-V upon PLM-V Defect	Reserved
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved:

BIT 5 - Auto Transmit AIS-V upon AIS-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the AIS-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the AIS-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the AIS-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 4 - Auto Transmit AIS-V upon UNEQ-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the UNEQ-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the UNEQ-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the UNEQ-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 3 - Reserved:

BIT 2 - Auto Transmit AIS-V upon LOP-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the LOP-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the LOP-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the LOP-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 1 - Auto Transmit AIS-V upon PLM-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the PLM-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the PLM-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the PLM-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 0 - Reserved:

TABLE 259: CHANNEL CONTROL - VT-DE-MAPPER AUTO AIS CONTROL REGISTER 0 (VTDAAISCR0 = 0XND73)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Auto Transmit AIS-V upon VT Path Trace Message Unstable Defect	Auto Transmit AIS-V upon TIM-V Defect	Auto Transmit AIS-V upon N1 Byte Alarm Defect	Auto Transmit AIS-V upon N2 IAIS Bit Alarm Defect	Auto Transmit AIS-V upon TC LOMF-V Defect	Auto Transmit AIS-V upon TC API-V Message Mismatch Defect	Auto Transmit AIS-V upon TC UNEQ-V Indication Signal Detect	Auto Transmit AIS-V Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Auto Transmit AIS-V upon VT Path Trace Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the VT Path Trace Message Unstable defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the VT Path Trace Message Unstable defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the VT Path Trace Message Unstable defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 6 - Auto Transmit AIS-V upon TIM-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the TIM-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TIM-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TIM-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 5 - Auto Transmit AIS-V upon N1 Byte Alarm Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it detects an all "0" value on the received N1 Byte and declares the N1 Byte Alarm defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the N1 Byte Alarm defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the N1 Byte Alarm defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 4 - Auto Transmit AIS-V upon N2 IAIS Alarm Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the N2 Incoming AIS Alarm defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the N2 Incoming AIS Alarm defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the N2 Incoming AIS Alarm defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 3 - Auto Transmit AIS-V upon TC LOMF-V Alarm Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the TC LOMF-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC LOMF-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC LOMF-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 2 - Auto Transmit AIS-V upon TC API-V Message Mismatch Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the TC API-V Message Mismatch defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC API-V Message Mismatch defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC API-V Message Mismatch defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 1 - Auto Transmit AIS-V upon TC UNEQ-V Indication Signal Condition:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit E1 LIU Block), anytime (and for the duration that) it declares the TC UNEQ-V Indication Signal condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC UNEQ-V Indication Signal condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TC UNEQ-V Indication Signal condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

BIT 0 - Auto Transmit AIS-V Enable:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the down-stream traffic) whenever (and for the duration that) it declares either the AIS-V, LOP-V, TIM-V, UNEQ-V, PLM-V or "VT Path Trace Message Unstable" defect conditions.

- 0 - Configures the VT-De-Mapper block to NOT automatically transmit the AIS-V indicator (via the "downstream traffic) upon declaration of any of the "above-mentioned" defect conditions.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream traffic) upon declaration of any of the "above-mentioned" defect conditions.

NOTE: *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator upon detection of a given alarm/defect condition.*

TABLE 260: CHANNEL CONTROL - VT-MAPPER TRANSMIT J2 BYTE VALUE REGISTER (VTMJ2VR = 0XND76)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit J2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit J2 Byte Value[7:0]:

These READ/WRITE bit-fields permit the user to have software control over the value of the J2 byte, within the outbound VT data-stream.

If the user configures the VT-Mapper block to use this register as the source of the J2 byte, then it will automatically write the contents of this register into the J2 byte location, within each "outbound" VT multi-frame.

This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Transmit VT-Path Trace Message Source[1:0]) within the "Channel Control - VT Mapper Block - Ingress Direction - VT Path Trace Message Control" Register.

TABLE 261: CHANNEL CONTROL - VT-MAPPER TRANSMIT N2 BYTE VALUE REGISTER (VTMN2VR = 0XND77)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit N2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit N2 Byte Value[7:0]:

These READ/WRITE bit-fields permit the user to have software control over the value of the N2 byte, within the outbound VT data-stream.

The VT-Mapper block will (unconditionally) use this register as the source of the N2 byte, then it will automatically write the contents of this register into the N2 byte location, within each "outbound" VT multi-frame.

TABLE 262: CHANNEL CONTROL - VT-MAPPER TRANSMIT PATH TRACE MESSAGE CONTROL REGISTER (VTMPTMCR = 0XND79)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit TC Enable[1:0]		Transmit IAIS	Reserved	Transmit VT Path Trace Message Length[1:0]		Transmit VT Path Trace Message Source[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Transmit TC Enable[1:0]:

These READ/WRITE bit-fields are used to enable the Tandem Connection feature in the VT Mapper. The VT Path Trace Message Length [1:0] on Bit-3 and Bit-2 must be set to the value "0x00" or "0x01" depending on the desired 1-Byte or 16-Bytes message length.

The relationship between the contents of these bit-fields and the corresponding Transmit Tandem Connection Messaging Type is presented below.

TRANSMIT TC ENABLE[1:0]	TRANSMIT TANDEM CONNECTION OPERATION
00	Tandem Connection feature is disabled. The N2 byte transmitted is the value written on N2 byte software register 0xND77.
01	Tandem Connection Enabled for 16-Bytes Messaging Operation. The N2 Byte Messaging memory buffer segment is shared with the J2 64-Byte memory buffer. The written value is transmitted along with the multiframe alignment pattern, and TC ODI and TC RDI. 16-Bytes message length must be selected using the appropriate values written on VT Path Trace Message Length[1:0] Bit-3 and Bit-2.
10	Reserved.
11	Tandem Connection Enabled for 1-Byte Messaging Operation. The N2 byte transmitted is the value written on N2 byte software register 0xND77. The written value is transmitted along with the multiframe alignment pattern, and TC ODI and TC RDI. 1-Byte message length must be selected using the appropriate values written on VT Path Trace Message Length[1:0] Bit-3 and Bit-2.

BIT 5 - Transmit IAIS Bit:

This READ/WRITE bit-field contain the value that will be written on the Incoming AIS bit on Bit-4 of the transmitted N2 byte.

- 0 - The bit value "0" will be transmitted on Bit-4 of the transmitted N2 byte.
- 1 - The bit value "1" will be transmitted on Bit-4 of the transmitted N2 byte.

BIT 4 - Reserved:

BIT [3:2] - Transmit VT Path Trace Message Length[1:0]:

These READ/WRITE bit-fields permit the user to specify the length of the VT Path Trace Message that the VT-Mapper block will repeatedly transmit to the remote VT PTE. The relationship between the contents of these bit-fields and the corresponding VT Path Trace Message Length is presented below.

TRANSMIT VT PATH TRACE MESSAGE LENGTH[1:0]	RESULTING VT PATH TRACE MESSAGE BYTE LENGTH
00	1 Byte
01	16 Bytes
1X	64 Bytes

BIT [1:0] - Transmit VT Path Trace Message Source[1:0]:

These READ/WRITE bit-fields permit the user to specify the source of the "outbound" VT Path Trace Message that will transported via the J2 byte channel (within the outbound VT-data-stream) as depicted below.

TRANSMIT VT PATH TRACE MESSAGE SOURCE[1:0]	RESULTING SOURCE OF THE VT PATH TRACE MESSAGE
00	**Fixed Value:** The VT-Mapper block will automatically set the J2 byte, within the each outbound VT-multi-frame to the value "0x01".
01	**The Transmit VT Path Trace Message Buffer:** The VT-Mapper Block will read out the contents within the "Transmit VT-Path Trace Message" Buffer, and will transmit this message to the remote VT PTE.
10	**From the "Transmit J2 Byte Value[7:0]" Register:** In this setting, the VT-Mapper block will read out the contents of the "Transmit J2 Byte Value Register, and will insert this value into the J2 byte-position within each outbound VT-multi-frame.
11	**DO NOT USE**

TABLE 263: CHANNEL CONTROL - VT-MAPPER TRANSMIT N2 CONTROL REGISTER (VTMN2CR = 0XND7B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Transmit TC UNEQ-V with TC BIP-2 Enable	Transmit TC UNEQ-V Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved:

BIT 1 - Transmit TC UNEQ-V with BIP-2 Enable:

These READ/WRITE bit-fields are used to enable the transmission of the Tandem Connection Unequipped Indication Signal and the 2-bit Bit Interleave Parity feature in the VT Mapper.

- 0 - Disables the transmission of TC UNEQ-V.
- 1 - Enables the transmission of TC UNEQ-V with the generation of TC BIP-2.

BIT 0 - Transmit TC UNEQ-V Enable:

These READ/WRITE bit-fields are used to enable the transmission of the Tandem Connection Unequipped Indication Signal feature in the VT Mapper.

- 0 - Disables the transmission of TC UNEQ-V.
- 1 - Enables the transmission of TC UNEQ-V without the generation of TC BIP-2.

TABLE 264: CHANNEL CONTROL - VT-MAPPER TRANSMIT TANDEM CONNECTION RDI-V CONTROL REGISTER 1 (VTMTCRDICR1 = 0XND7E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					Transmit TC RDI-V upon AIS-V Defect	Transmit TC RDI-V upon LOP-V Defect	Transmit TC RDI-V upon UNEQ-V Detect
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved:

BIT 2 - Transmit TC RDI-V upon AIS-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

BIT 1 - Transmit TC RDI-V upon LOP-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

BIT 0 - Transmit TC RDI-V upon UNEQ-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.

TABLE 265: CHANNEL CONTROL - VT-MAPPER TRANSMIT TANDEM CONNECTION RDI-V CONTROL REGISTER 0 (VTMTCRDICR0 = 0XND7F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit TC RDI-V upon PLM-V Defect	Transmit TC RDI-V upon TIM-V Defect	Transmit TC RDI-V upon VT Path Trace Message Unstable Defect	Transmit TC RDI-V upon TC LOMF-V Defect	Transmit TC RDI-V upon TC UNEQ-V Detect	Transmit TC RDI-V upon IAIS Defect	Transmit TC RDI-V upon TC API-V Message Mismatch Defect	Transmit TC RDI-V upon TC API-V Message Unstable Defect
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Transmit TC RDI-V upon PLM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

BIT 6 - Transmit TC RDI-V upon TIM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

BIT 5 - Transmit TC RDI-V upon VT Path Trace Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.

BIT 4 - Transmit TC RDI-V upon TC LOMF-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.

BIT 3 - Transmit TC RDI-V upon TC UNEQ-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.

BIT 2 - Transmit TC RDI-V upon Incoming AIS-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS defect condition.

BIT 1 - Transmit TC RDI-V upon TC API-V Message Mismatch:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.

BIT 0 - Transmit TC RDI-V upon TC API-V Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection RDI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection RDI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.

TABLE 266: CHANNEL CONTROL - VT-MAPPER TRANSMIT TANDEM CONNECTION ODI-V CONTROL REGISTER 1 (VTMTCODICR1 = 0XND82)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					Transmit TC ODI-V upon AIS-V Defect	Transmit TC ODI-V upon LOP-V Defect	Transmit TC ODI-V upon UNEQ-V Detect
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Reserved:

BIT 2 - Transmit TC ODI-V upon AIS-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

BIT 1 - Transmit TC ODI-V upon LOP-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

BIT 0 - Transmit TC ODI-V upon UNEQ-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V Indication Signal condition.

TABLE 267: CHANNEL CONTROL - VT-MAPPER TRANSMIT TANDEM CONNECTION ODI-V CONTROL REGISTER 0 (VTMTCODICR0 = 0XND83)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit TC ODI-V upon PLM-V Defect	Transmit TC ODI-V upon TIM-V Defect	Transmit TC ODI-V upon VT Path Trace Message Unstable Defect	Transmit TC ODI-V upon TC LOMF-V Defect	Transmit TC ODI-V upon TC UNEQ-V Detect	Transmit TC ODI-V upon IAIS Defect	Transmit TC ODI-V upon TC API-V Message Mismatch Defect	Transmit TC ODI-V upon TC API-V Message Unstable Defect
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Transmit TC ODI-V upon PLM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

BIT 6 - Transmit TC ODI-V upon TIM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

BIT 5 - Transmit TC ODI-V upon VT Path Trace Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the VT Path Trace Message Unstable defect condition.

BIT 4 - Transmit TC ODI-V upon TC LOMF-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC LOMF-V defect condition.

BIT 3 - Transmit TC ODI-V upon TC UNEQ-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC UNEQ-V defect condition.

BIT 2 - Transmit TC ODI-V upon Incoming AIS-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block detects the Incoming AIS defect condition.

BIT 1 - Transmit TC ODI-V upon TC API-V Message Mismatch:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Mismatch defect condition.

BIT 0 - Transmit TC ODI-V upon TC API-V Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the Tandem Connection ODI Code on the VC2 N2 byte towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the Tandem Connection ODI Code (via the N2 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TC API-V Message Unstable defect condition.

TABLE 268: CHANNEL CONTROL - VT-MAPPER TRANSMIT RDI-V CONTROL REGISTER 3 (VTMRDICR3 = 0XND84)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				PLM-V RDI Code[2:0]			Transmit RDI-V upon PLM-V
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

BIT [7:4] - Reserved:

BIT [3:1] - PLM-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the PLM-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon PLM-V) within this register to "1".*

BIT 0 - Transmit RDI-V upon PLM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

TABLE 269: CHANNEL CONTROL - VT-MAPPER TRANSMIT RDI-V CONTROL REGISTER 2 (VTMRDICR2 = 0XND85)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-V RDI Code[2:0]			Transmit RDI-V upon TIM-V	UNEQ-V RDI Code[2:0]			Transmit RDI-V upon UNEQ-V
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	0	0

BIT [7:5] - TIM-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the TIM-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 4 (Transmit RDI-V upon TIM-V) within this register to "1".*

BIT 4 - Transmit RDI-V upon TIM-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 7 through 5 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

BIT [3:1] - UNEQ-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the UNEQ-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon UNEQ-V) within this register to "1".*

BIT 0 - Transmit RDI-V upon UNEQ-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition

TABLE 270: CHANNEL CONTROL - VT-MAPPER TRANSMIT RDI-V CONTROL REGISTER 1 (VTMRDICR1 = 0XND86)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-V RDI Code[2:0]			Transmit RDI-V upon LOP-V	AIS-V RDI Code[2:0]			Transmit RDI-V upon AIS-V
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT [7:5] - LOP-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the LOP-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 4 (Transmit RDI-V upon LOP-V) within this register to "1".*

BIT 4 - Transmit RDI-V upon LOP-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 7 through 5 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

BIT [3:1] - AIS-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the AIS-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon AIS-V) within this register to "1".*

BIT 0 - Transmit RDI-V upon AIS-V:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition

TABLE 271: CHANNEL CONTROL - VT-MAPPER TRANSMIT RDI-V CONTROL REGISTER 0 (VTMRDICR0 = 0XND87)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFI-V upon E1 RAI Enable	Reserved	Reserved	Transmit RDI-V Value[2:0]			RDI-V Type	RDI-V Insert Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT 7 - RFI-V upon E1 RAI Enable:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RFI-V indicator (within the outbound VT-data-stream) whenever (and for the duration) that the corresponding Ingress Direction Receive E1 Framer block declares the RAI defect condition.

- 0 - Does not configure the VT-Mapper block to automatically transmit the RFI-V indicator whenever (and for the duration) that the corresponding Ingress Direction Receive E1 Framer block declares the RAI defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RFI-V indicator whenever (and for the duration) that the corresponding Ingress Direction Receive E1 Framer block declares the RAI defect condition.

BIT 6 - Reserved

BIT 5 - Reserved:

BIT [4:2] - Transmit RDI-V Value[2:0]:

These three READ/WRITE bit-fields permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) regardless of any defects that the corresponding VT-De-Mapper block is (or is NOT) currently declaring.

NOTE: *The user MUST set bit 0 (RDI-V Insert Type) within this register to "1" in order to configure the VT-Mapper block to use these bit-fields as the "source" of the RDI-V value.*

BIT 1 - RDI-V Type:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to either support the "SRDI-V" (Single-Bit - RDI-V) or "ERDI-V" (Extended - RDI-V) form of signaling. If the user opts to use only "Single-Bit" RDI-V, then the RDI-V indicator will only be transported via Bit 0 (RDI-V) within the V5 byte in a VT-data-stream. Conversely, if the user opts to use the "Extended" RDI-V, then the RDI-V indicator will be transported via both Bit 0 (RDI-V) within the V5 byte, and Bits 3, 2 and 1 within the Z7/K4 byte.

- 0 - Configures the VT Mapper block to use the SRDI-V form of signaling.
- 1 - Configures the VT-Mapper block to use the ERDI-V form of signaling.

NOTE: *This configuration setting only applies to the VT-Mapper block. If the user wishes to configure the VT-De-Mappe block to support either the "SRDI-V" or the "ERDI-V" form of signaling, then he/she must set Bit 0 (RDI-V Type) within the "Channel Control - VT-De-Mapper Block - Egress Direction - E1 Drop Control Register - Byte 2.*

BIT 0 - RDI-V Insert Type:

This READ/WRITE bit-field permits the user to select the source of the RDI-V code word that the VT-Mapper block will transmit within the outbound VT-data-stream, as depicted below. In this case, the user has two options.

- To configure the VT-Mapper block to transmit the appropriate RDI-V code (based upon defects that the corresponding VT-De-Mapper block declares). In this case, the VT-Mapper block will transmit the RDI-V codes, as configured in the "Channel Control - VT Mapper Block - Ingress Direction - Transmit RDI-V Control Register - Bytes 3 - 1" registers.
- To configure the VT-Mapper block to use the value written into the "Transmit RDI-V Value[2:0]" bit-fields within this register.

▶ 0 - Configures the VT-Mapper block to transmit the appropriate RDI-V code (based upon defects that the corresponding VT-De-Mapper block declares).

▶ 1 - Configures the VT-Mapper block to use the value written into the "Transmit RDI-V Value[2:0]" bit-fields within this register.

TABLE 272: RECEIVE J2 TRACE IDENTIFIER MESSAGE MEMORY BUFFER (VTDJ2MEM00 = 0XNE00 - VTDJ2MEM3F = 0XNE3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J2 Trace Identifier Message Byte[0:63]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Receive J2 Trace Identifier Message - 16 Byte Message Buffer:

Address Location: 0xNE00 - 0xNE0F

Receive J2 Trace Identifier Message - 64 Byte Message Buffer:

Address Location: 0xNE00 - 0xNE3F

NOTE: *J2 Trace Identifier 64-Byte Messaging is not permitted when N2 Access Point Indentifier 16-Byte Messaging is enabled.*

TABLE 273: RECEIVE N2 ACCESS POINT IDENTIFIER MESSAGE MEMORY BUFFER (VTDN2MEM20 = 0XNE20 - VTDN2MEM2F = 0XNE2F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N2 Access Point Identifier Message Byte[0:15]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Receive N2 Access Point Identifier Message - 16 Byte Message Buffer:

Address Location: 0xNE20 - 0xNE2F

NOTE: *J2 Trace Identifier 64-Byte Messaging is not permitted when N2 Access Point Indentifier 16-Byte Messaging is enabled.*

TABLE 274: TRANSMIT J2 TRACE IDENTIFIER MESSAGE MEMORY BUFFER (VTMJ2MEM00 = 0XNF00 - VTMJ2MEM3F = 0XNF3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J2 Trace Identifier Message Byte[0:63]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Transmit J2 Trace Identifier Message - 16 Byte Message Buffer:

Address Location: 0xNF00 - 0xNF0F

Transmit J2 Trace Identifier Message - 64 Byte Message Buffer:

Address Location: 0xNF00 - 0xNF3F

NOTE: *J2 Trace Identifier 64-Byte Messaging is not permitted when N2 Access Point Indentifier 16-Byte Messaging is enabled.*

TABLE 275: TRANSMIT N2 ACESS POINT IDENTIFIER MESSAGE MEMORY BUFFER (VTMN2MEM20 = 0XNF20 - VTMN2MEM2F = 0XNF2F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N2 Access Point Identifier Message Byte[0:15]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Transmit N2 Access Point Identifier Message - 16 Byte Message Buffer:

Address Location: 0xNF20 - 0xNF2F

NOTE: *J2 Trace Identifier 64-Byte Messaging is not permitted when N2 Access Point Indentifier 16-Byte Messaging is enabled.*

7.0 MICROPROCESSOR INTERFACE TIMING

7.1 MICROPROCESSOR INTERFACE TIMING - INTEL ASYNCHRONOUS MODE

In Intel Asynchronous mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, ALE, $\overline{WR}$, $\overline{RD}$ and $\overline{RDY}$. A READ cycle starts with assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus. Inside XRT86SH221 address is latched on the falling edge of the ALE input. Address may change on the ADDR inputs after the falling edge of the ALE.

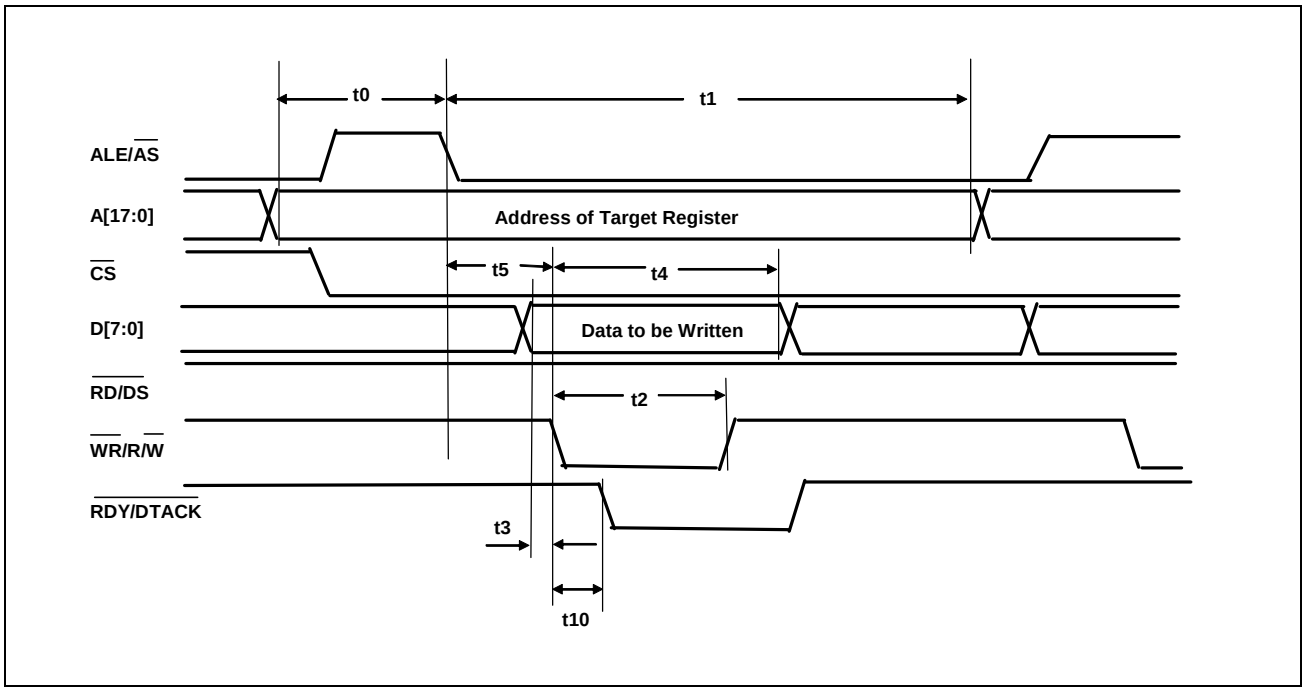
Multiplexed Address & Data bus is supported in this mode using ALE input. It is possible to pull-up the ALE input if multiplexed address and data mode is not used. In this case the address should be stable through entire read or write instruction cycle.

Following falling edge of ALE, $\overline{RD}$ is asserted for the READ operation. $\overline{RD}$ must remain asserted until $\overline{RDY}$ is asserted by the XRT86SH221 device, which indicates DATA from the addressed location is available on the data bus. $\overline{RD}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{RDY}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that following falling edge of ALE $\overline{WR}$ is asserted. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WR}$ is asserted. $\overline{WR}$ should remain asserted until $\overline{RDY}$ is asserted by the XRT86SH221 device. Following $\overline{RDY}$ assertion $\overline{WR}$ and $\overline{CS}$ may be de-asserted.

FIGURE 55. INTEL-ASYNCHRONOUS MODE TIMING - WRITE OPERATION

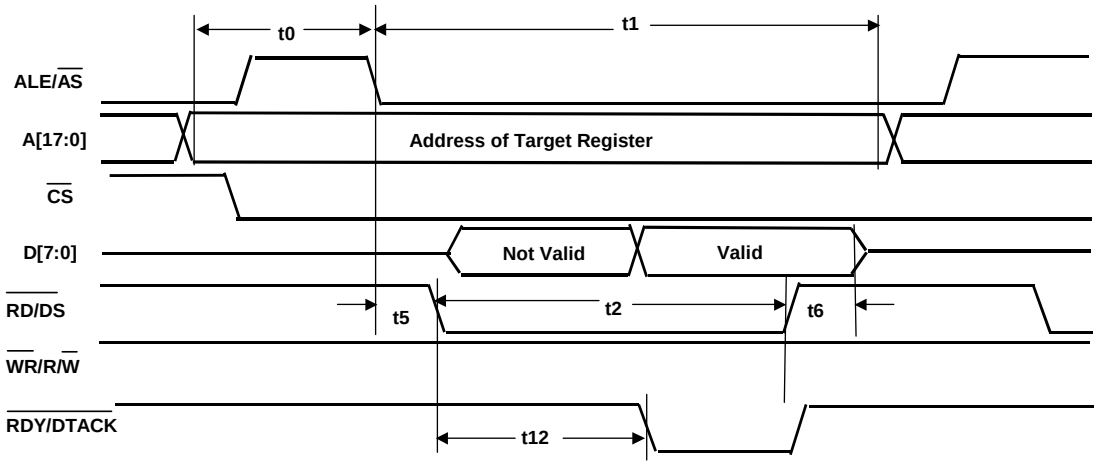


Note: The values for t0 through t10, within this figure can be found in **Table 276**.

Table 276 Intel Asynchronous Mode Timing - Write Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
TimingSymbol	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t0	Address setup time to ALE "Low"	5	-	-	ns
t1	Address hold time from ALE "Low"	5	-	-	ns
t2	$\overline{WR}$ strobe pulse width	150	-	-	ns
t3	Data setup time to $\overline{WR}$ "Low"	25	-	-	ns
t4	Data hold time from $\overline{WR}$ "Low"	200	-	-	ns
t5	ALE "Low" set-up time to $\overline{WR}$ "Low"	50	-	-	ns
t10	$\overline{WR}$ "Low" to $\overline{RDY}$ "Low" delay time	-	-	125	ns

FIGURE 56. INTEL-ASYNCHRONOUS MODE TIMING - READ OPERATION



Note: The values for t0 through t10, in this figure can be found in **Table 277**.

Table 277 Intel Asynchronous Mode Timing - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
TimingSymbol	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t0	Address setup time to ALE "Low"	5	-	-	ns
t1	Address hold time from ALE "Low"	5	-	-	ns
t2	$\overline{RD}$ strobe pulse width	200	-	-	ns
t5	ALE "Low" set-up time to $\overline{RD}$ "Low"	50	-	-	ns
t6	Data Invalid delay from $\overline{RD}$ “High”	-	-	9	ns

Table 277 Intel Asynchronous Mode Timing - Read Operation

t12	$\overline{RD}$ "Low" to $\overline{RDY}$ "Low" delay time	-	-	125	ns

7.2 MICROPROCESSOR INTERFACE TIMING - MOTOROLA ASYNCHRONOUS (68K) MODE

In Motorola Asynchronous mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{DS}$ and $\overline{DTACK}$. A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

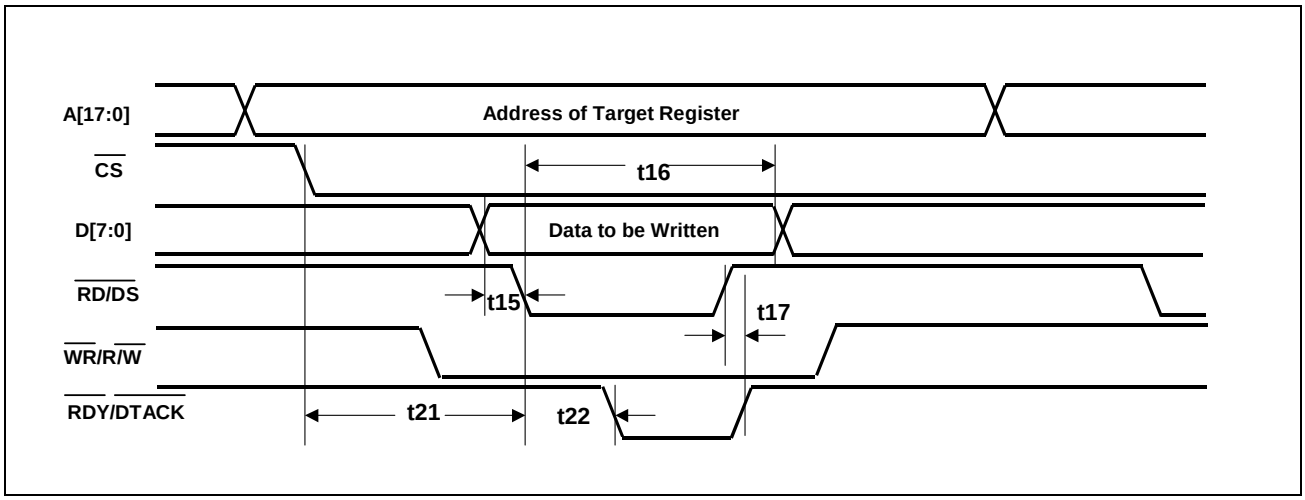
In this mode the address should be stable through entire read or write instruction cycle.

Following falling edge of $\overline{CS}$, $\overline{DS}$ is asserted for the READ operation. $\overline{DS}$ must remain asserted until $\overline{DTACK}$ is asserted by the XRT86SH221 device, which indicates DATA from the addressed location is available on the data bus. $\overline{DS}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{DTACK}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{DS}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{DS}$ is asserted. $\overline{DS}$ should remain asserted until $\overline{DTACK}$ is asserted by the XRT86SH221 device. Following assertion of $\overline{DTACK}$ $\overline{DS}$ and $\overline{CS}$ may be de-asserted.

FIGURE 57. MOTOROLA-ASYNCHRONOUS MODE TIMING - WRITE OPERATION



Note: The values for t15 through t22 can be found in **Table 278**.

Table 278 Motorola (68K) Asynchronous Mode Timing Information - Write Operation

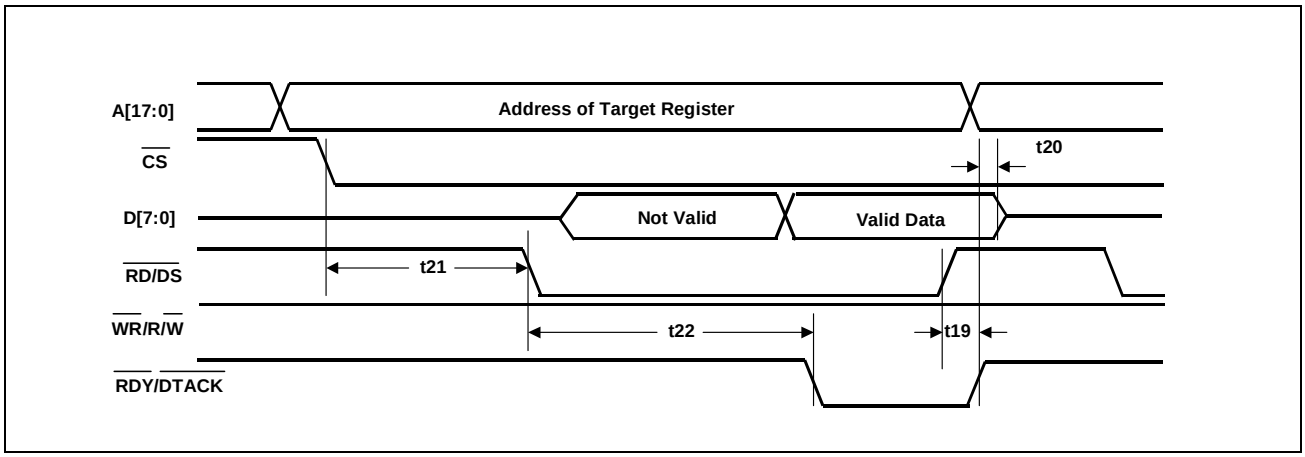
Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t15	Data setup time to $\overline{DS}$ "Low"	25	-	-	ns
t16	Data hold time to $\overline{DS}$ "Low"	150	-	-	ns
t17	$\overline{DS}$ "High" to $\overline{DTACK}$ "High"	-	-	9	ns
t21	$\overline{CS}$ "Low" to $\overline{DS}$ set-up time	50	-	-	ns

Table 278 Motorola (68K) Asynchronous Mode Timing Information - Write Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t22	$\overline{DS}$ "Low" to $\overline{DTACK}$ "Low" delay time	130	-	-	ns

7.2.1 Motorola-Asynchronous Mode Timing - Read Operation

FIGURE 58. MOTOROLA-ASYNCHRONOUS MODE TIMING - READ OPERATION



Note: The values for t13 through t24 can be found in **Table 278**.

Table 279 Motorola (68K) Asynchronous Mode Timing - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t19	$\overline{DS}$ "High" to $\overline{DTACK}$ "High"	-	-	8	ns
t20	$\overline{DTACK}$ "High" to Data invalid	-	-	8	ns
t21	$\overline{CS}$ "Low" to $\overline{DS}$ set-up time	50	-	-	ns
t22	$\overline{DS}$ "Low" to $\overline{DTACK}$ "Low" delay time	120	-	-	ns

7.3 PowerPC 403 Synchronous Mode:

In PowerPC mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{WE}$, $\overline{DBEN}$, $\overline{RDY}$ and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 66 MHz.

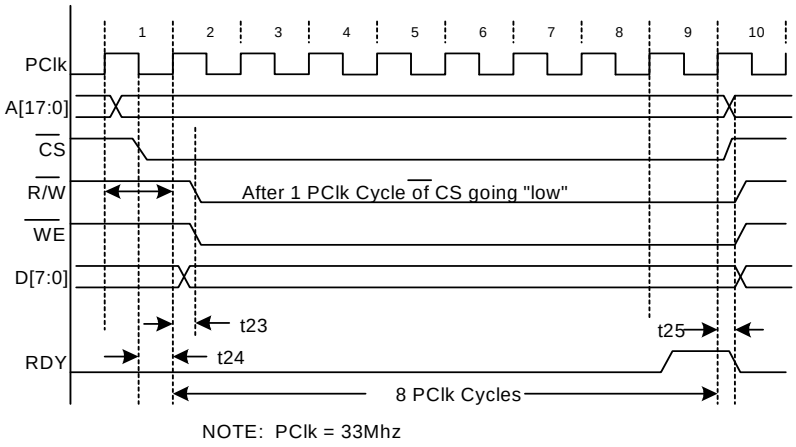
A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

Following falling edge of $\overline{CS}$, $\overline{DBEN}$ is asserted for the READ operation. $\overline{DBEN}$ must remain asserted until RDY is asserted by the XRT86SH221 device, which indicates DATA from the addressed location is available on the data bus. $\overline{DBEN}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor. $\overline{WE}$ should be high during the entire read cycle.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of RDY is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{WE}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WE}$ is asserted. $\overline{WE}$ should remain asserted until RDY is asserted by the XRT86SH221 device. Following RDY assertion $\overline{WE}$ and $\overline{CS}$ may be de-asserted. $\overline{DBEN}$ should be high during the entire write cycle.

FIGURE 59. POWERPC 403 MODE TIMING - WRITE OPERATION

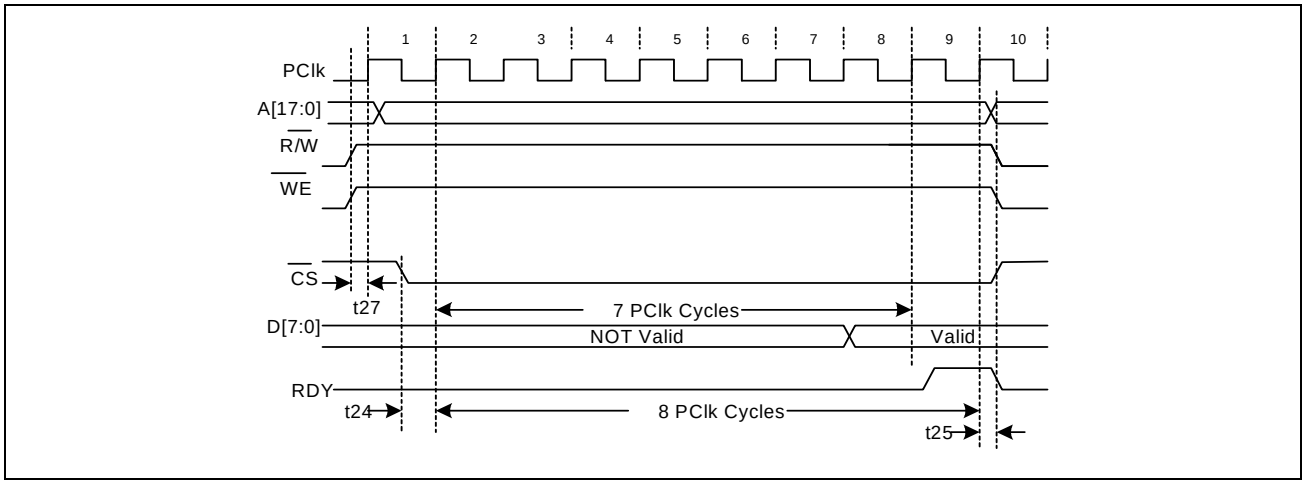


Note: The value for t25 through t38 can be found in **Table 280**.

Table 280 Power PC403 Mode Timing - Write Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t23	R/$\overline{W}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "Low" delay	4	-	-	ns

FIGURE 60. POWERPC 403 MODE TIMING - READ OPERATION



Note: The value for t25 through t38 can be found in **Table 281**.

Table 281 Power PC403 Mode Timing - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY “Low” delay	4	-	-	ns
t27	R/$\overline{W}$ “High” to rising edge of PCLK set-up time	5	-	-	ns

7.4 MICROPROCESSOR INTERFACE TIMING - MCP860 SYNCHRONOUS MODE

In MPC86x mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{WE}$, $\overline{DBEN}$, $\overline{TA}$ and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 66 MHz.

A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

Following falling edge of $\overline{CS}$, $\overline{DBEN}$ is asserted for the READ operation. $\overline{DBEN}$ must remain asserted until $\overline{TA}$ is asserted by the XRT86SH221 device, which indicates DATA from the addressed location is available on the data bus. $\overline{DBEN}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor. $\overline{WE}$ should be high during the entire read cycle.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{TA}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{WE}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WE}$ is asserted. $\overline{WE}$ should remain asserted until $\overline{TA}$ is asserted by the XRT86SH221 device. Following assertion of $\overline{TA}$ $\overline{WE}$ and $\overline{CS}$ may be de-asserted. $\overline{DBEN}$ should be high during the entire write cycle.

FIGURE 61. MPC86X MODE TIMING - WRITE OPERATION

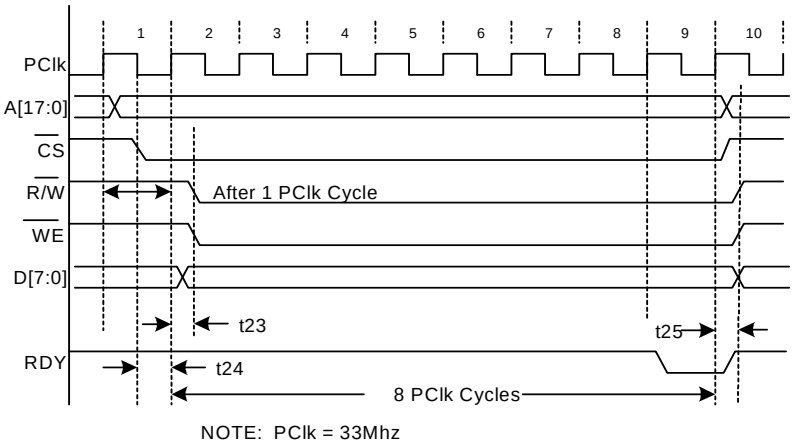


Table 282 MPC86X Mode Timing - Write Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t23	R/$\overline{W}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	4	-	-	ns
t25	Rising edge of PCLK to RDY “High”delay	4	-	-	ns

FIGURE 62. MPC86X MODE TIMING - READ OPERATION

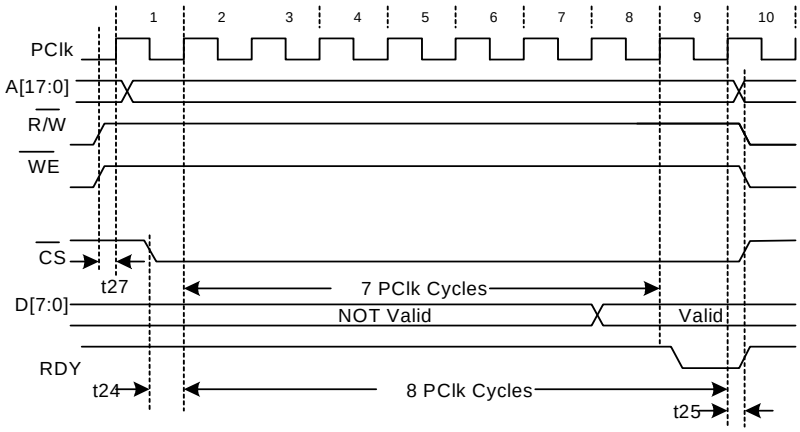


Table 283 MPC86X Timing Information - Read Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "High" delay	4	-	-	ns
t27	R/$\overline{W}$ "High" to rising edge of PCLK set-up time	5	-	-	ns

8.0 INTERFACE TIMING SPECIFICATIONS

8.1 STM-0/STM-1 TELECOM BUS INTERFACE TIMING INFORMATION

This Section presents the timing requirements of the STM-0/STM-1 Telecom Bus Interface, for the following conditions/modes.

- Whenever the STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-0 Mode.
- Whenever the STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-1 Slot Master Mode
- Whenever the STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-1 Slot Slave Mode

This section presents the timing requirements for the STM-0/STM-1 Telecom Bus Interface. In particular this section indicates the following.

a) Identifies which edge of TxA_CLK in which the TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP, TxA_ALARM and TxA_DP output pins are updated on.

b) The clock to output delays (from the rising edge of TxA_CLK to the instant that the TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP, TxA_ALARM and TxA_DP output pins are updated.

c) Identifies which edge of RxD_CLK that the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input pins are sampled on.

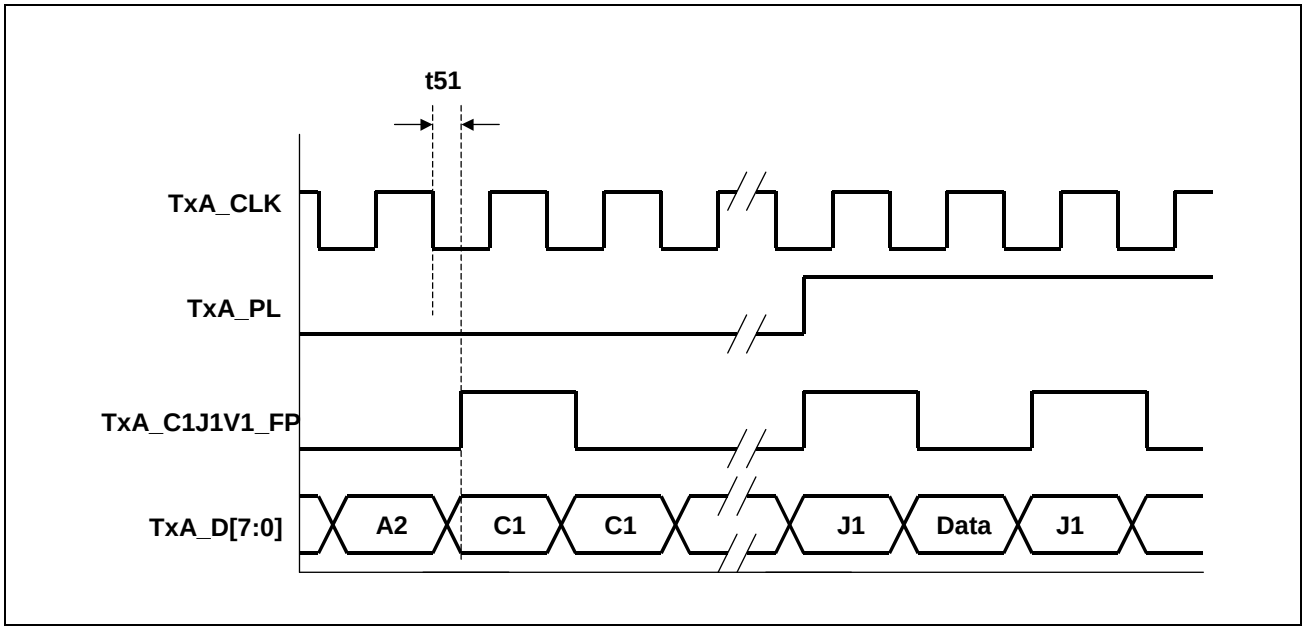
d) The set-up time requirements (from an update in the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input signals to the rising edge of RxD_CLK).

e) The hold-time requirements (from the rising edge of RxD_CLK to a change in the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input signals)

8.2 The Transmit STM-0/STM-1 Telecom Bus Interface Timing - STM-0 Applications

Whenever the Transmit STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-0 Mode, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (6.48MHz clock signal).

FIGURE 63. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STM-0/ STM-1 TELECOM BUS INTERFACE (FOR STM-0 APPLICATIONS)



Note: The value for t51 can be found in **Table 284**.

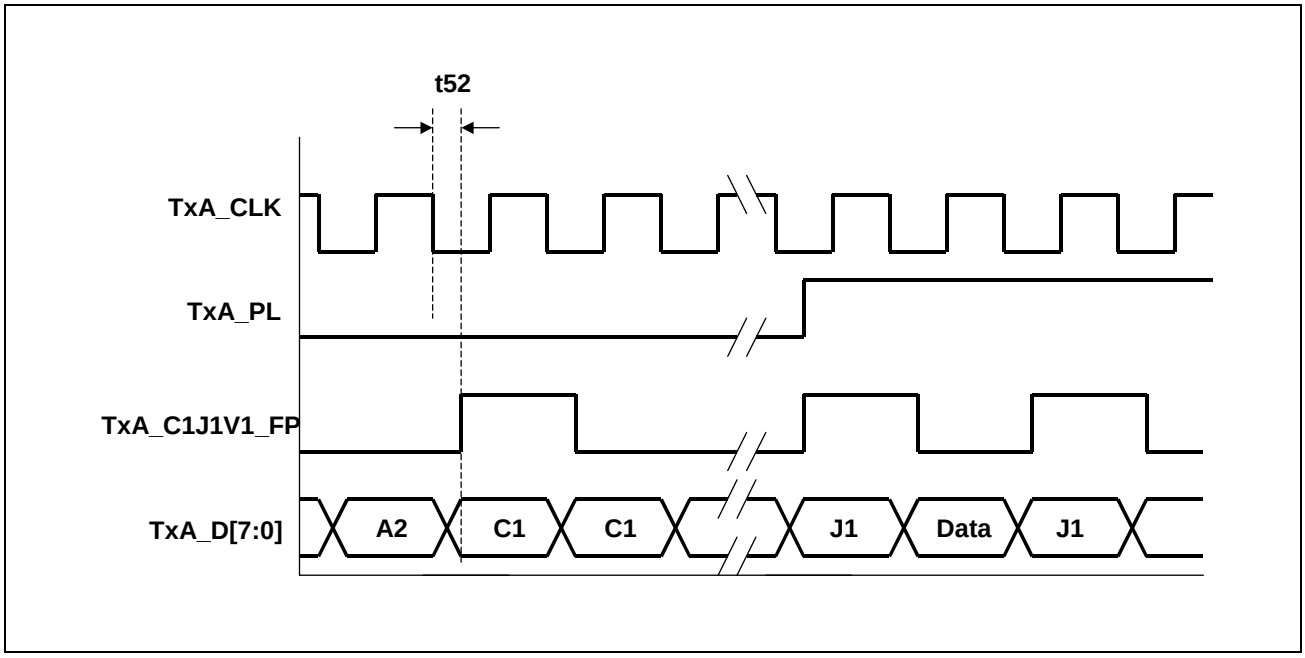
Table 284 Timing Information for the Transmit STM-0 Telecom Bus Interface - STM-0 Applications

Symbol	Description	Min.	Typ.	Max.
t51	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	2.0ns		3.1ns

8.3 The Transmit STM-0/STM-1 Telecom Bus Interface Timing - STM-1 Slot Master Applications

Whenever the Transmit STM-0/STM-1 Telecom Bus Interface has been configured to operate in both the STM-1 and the Slot Master Mode, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (19.44MHz clock signal).

FIGURE 64. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STM-0/ STM-1 TELECOM BUS INTERFACE (FOR STM-1 APPLICATIONS)



If the XRT86SH221 is configured to operate as the Slot Master, then it will pulse the TxSBFP_IN_OUT output pin "High" coincident to the instant that the chip outputs the very first byte of a given STM-1 frame. The XRT86SH221 will update the TxSBFP_IN_OUT output pin upon the falling edge of TxA_CLK.

FIGURE 65. AN ILLUSTRATION OF THE TIMING RELATIONSHIPS BETWEEN THE TXSBFP_IN_OUT OUTPUT PIN, AND THE TXA_CLK OUTPUT PIN, WITHIN THE TRANSMIT STM-1 TELECOM BUS INTERFACE (SLOT MASTER MODE APPLICATION)

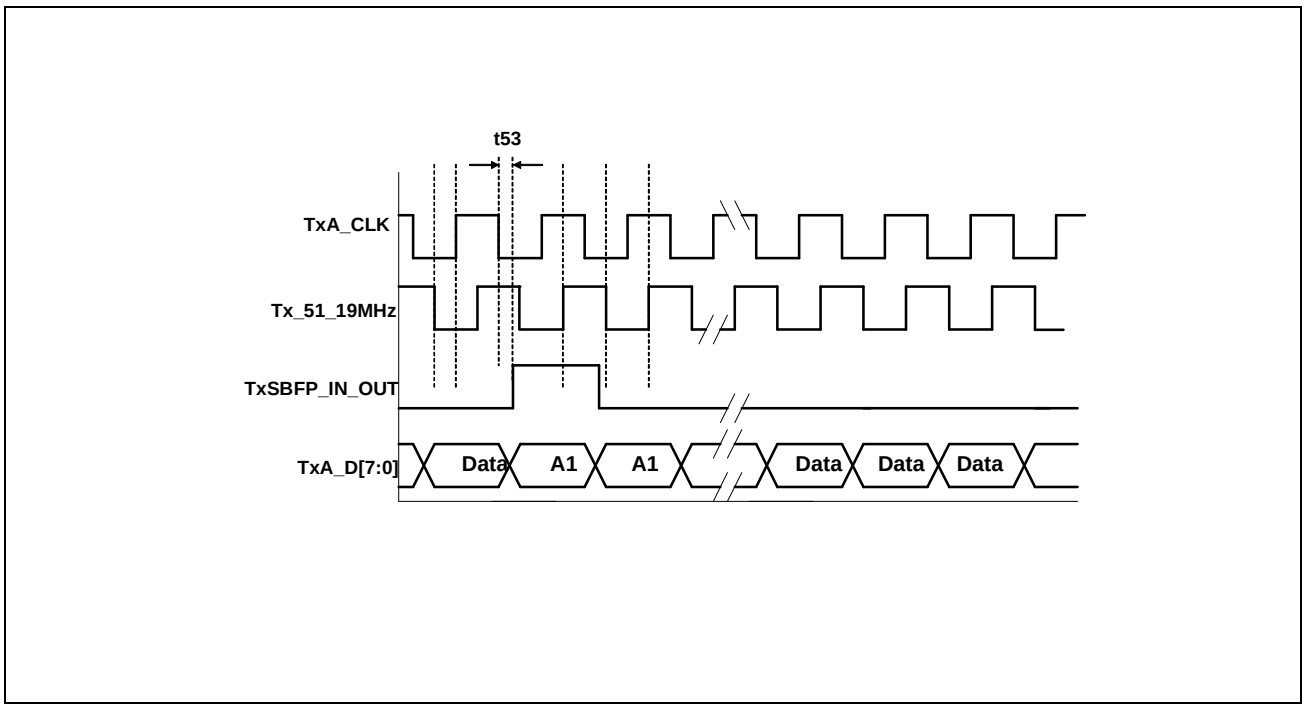


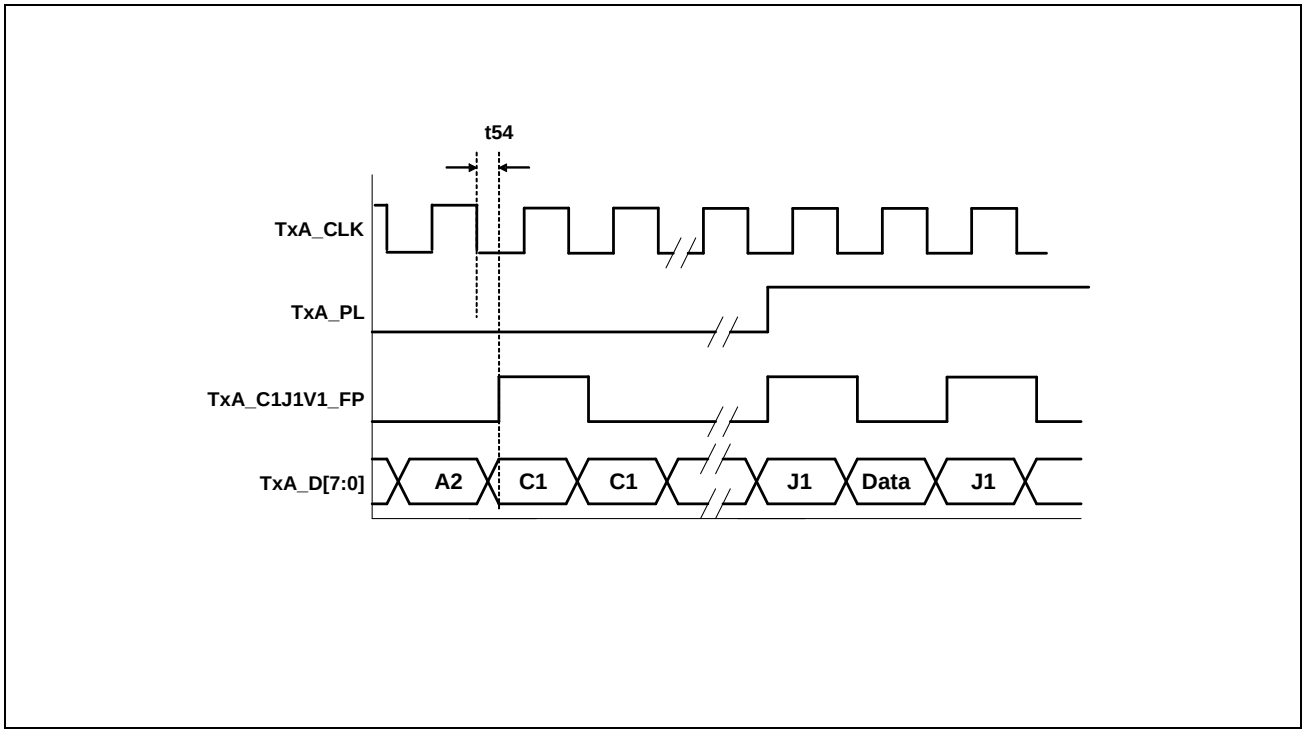
Table 285 Timing Information for the Transmit STM-0/STM-1 Telecom Bus Interface - STM-1 Slot Master Applications

Symbol	Description	Min.	Typ.	Max.
t52	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	2.0ns		4.0ns
t53	Falling edge of TxA_CLK to update in the TxSBFP_IN_OUT signal	0.1		0.3

8.4 The Transmit STM-0/STM-1 Telecom Bus Interface Timing - STM-1 Slot Slave Applications

Whenever the Transmit STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-1, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (19.44MHz clock signal).

FIGURE 66. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STM-0/ STM-1 TELECOM BUS INTERFACE (FOR STM-1 APPLICATIONS)



If the XRT86SH221 is configured to operate as the Slot Slave, then it will sample the TxSBFP_IN_OUT signal via an internal clock. The timing relationship between the TxSBFP_IN_OUT signal and the other Transmit STM-0/STM-1 Telecom Bus Interface signals is presented below in Figure 67.

FIGURE 67. AN ILLUSTRATION OF THE TIMING RELATIONSHIPS BETWEEN THE TXSBFP INPUT PIN AND THE TXA_CLK OUTPUT PIN WITHIN THE TRANSMIT STM-0/STM-1 TELECOM BUS INTERFACE (STM-1 SLOT SLAVE APPLICATIONS)

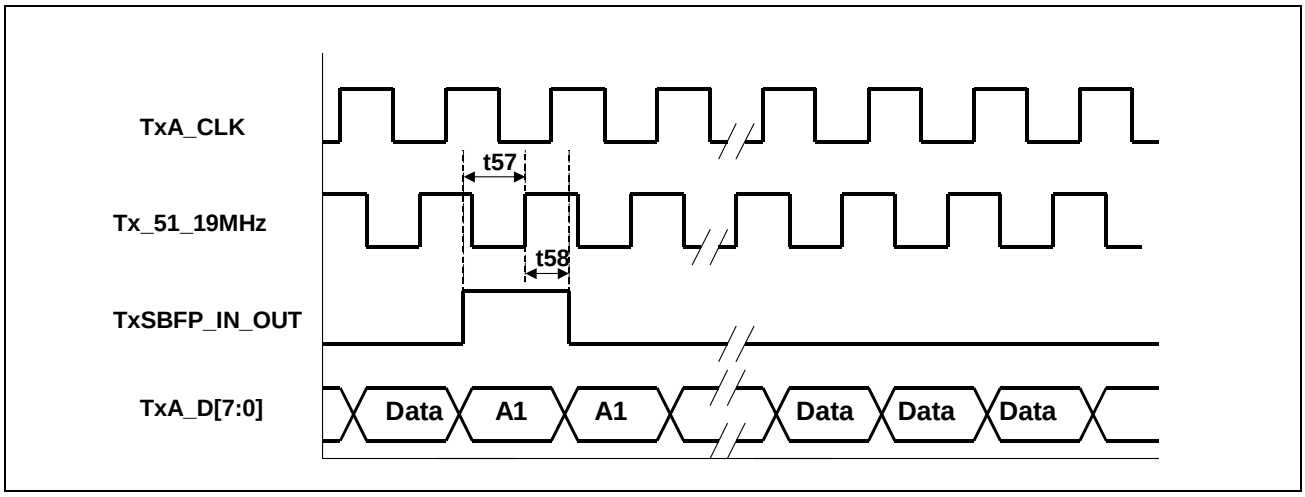


Table 286 Timing Information for the Transmit STM-0/STM-1 Telecom Bus Interface - STM-1 Slot Slave Applications

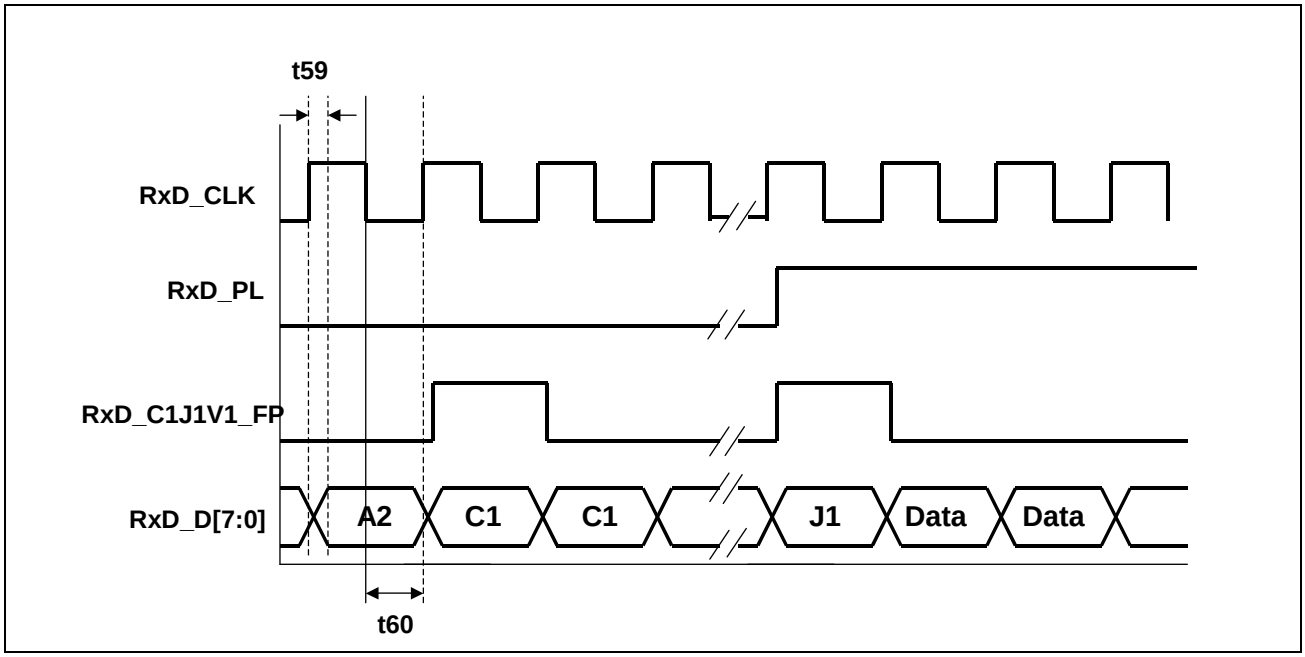
Symbol	Description	Min.	Typ.	Max.
t54	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	1.1ns		2.5ns
t57	TxSBFP Set-up time to rising edge of Tx51_19MHz	6ns		
t58	Rising edge of Tx51_19MHz to TxSBFP_IN_OUT Hold Time	1ns		

Note: In Slave mode, TxSBFP_IN_OUT is input to XRT86SH221. Inputs are applied using input clock Tx_51_19MHz and are sampled on rising edge of Tx_51_19MHz internally. The t57 parameter is referenced to the rising edge of Tx_51_19MHz, which provides the minimum setup and hold time required for TxSBFP_IN_OUT. TxA_CLK should be used to sampe the output signals not the input signals.

8.5 The Receive STM-0/STM-1 Telecom Bus Interface Timing - STM-0 Applications

Whenever the Receive STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-0 Mode, then all of the signals (which are accepted via this Bus Interface) are sampled upon the rising edge of RxD_CLK (6.48MHz clock signal).

FIGURE 68. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STM-0/ STM-1 TELECOM BUS INTERFACE



Note: The value for t59 and t60 can be found in **Table 287**. *The data and control signals are applied on the falling edge of RxD_CLK. The XRT86SH221 samples the data and control signals on the rising edge of RxD_CLK.*

Table 287 Timing Information for the Receive STM-0/STM-1 Telecom Bus Interface - STM-0 Applications

Symbol	Description	Min.	Typ.	Max.
t59	RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP to rising edge of RxD_CLK set-up time requirements	6 ns		

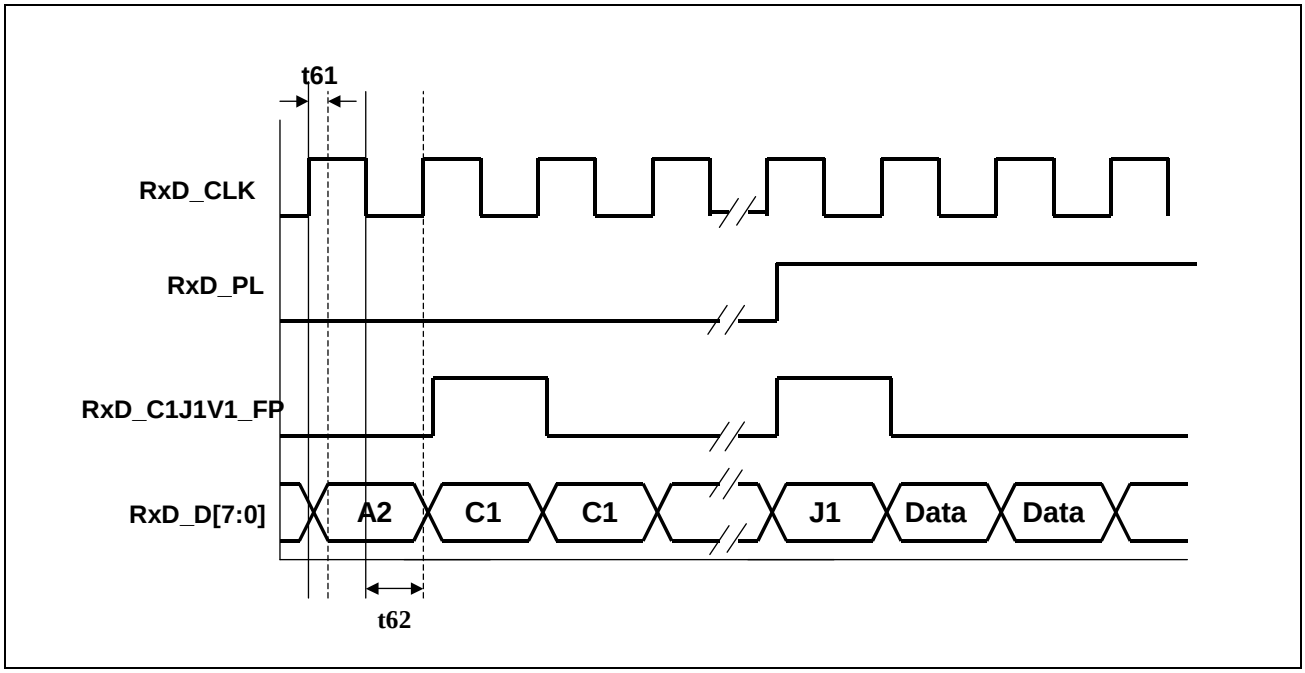
Table 287 Timing Information for the Receive STM-0/STM-1 Telecom Bus Interface - STM-0 Applications

Symbol	Description	Min.	Typ.	Max.
t60	rising edge of RxD_CLK to RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP hold time requirements	2 ns		

8.6 The Receive STM-0/STM-1 Telecom Bus Interface Timing - STM-1 Applications

Whenever the Receive STM-0/STM-1 Telecom Bus Interface has been configured to operate in the STM-1 Mode, then all of the signals (which are accepted via this Bus Interface) are sampled upon the rising edge of RxD_CLK (19.44MHz clock signal).

FIGURE 69. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STM-0/ STM-1 TELECOM BUS INTERFACE



Note: The value for t61 and t62 can be found in **Table 288**.

Table 288 Timing Information for the Receive STM-0/STM-1 Telecom Bus Interface - STM-1 Applications

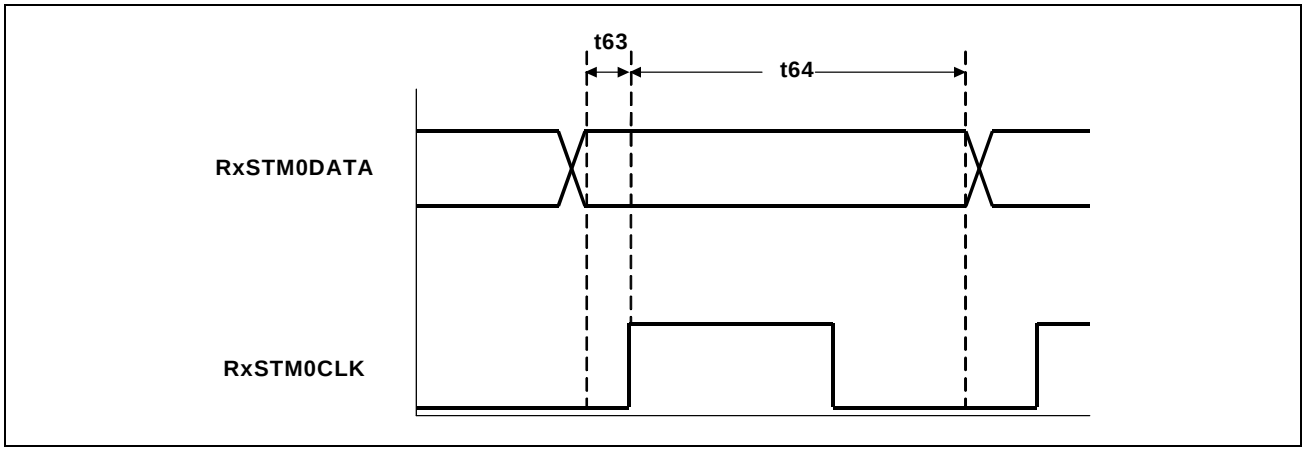
Symbol	Description	Min.	Typ.	Max.
t61	RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP to rising edge of RxD_CLK set-up time requirements	6 ns		
t62	Rising edge of RxD_CLK to RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP hold time requirements	2 ns		

8.7 STM-0 LIU INTERFACE TIMING INFORMATION

In addition to the Telecom Bus, the XRT86SH221 can be configured for High-Speed STM-0/STM-1 LIU Interface Ports.

8.7.1 Receive STM-0/STM-1 LIU Interface Timing

FIGURE 70. AN ILLUSTRATION OF THE WAVEFORMS OF THE RECEIVE STM-0/STM-1 SIGNALS THAT ARE INPUT TO THE RECEIVE STM-0/STM-1 LIU INTERFACE BLOCK - SHARED PORT



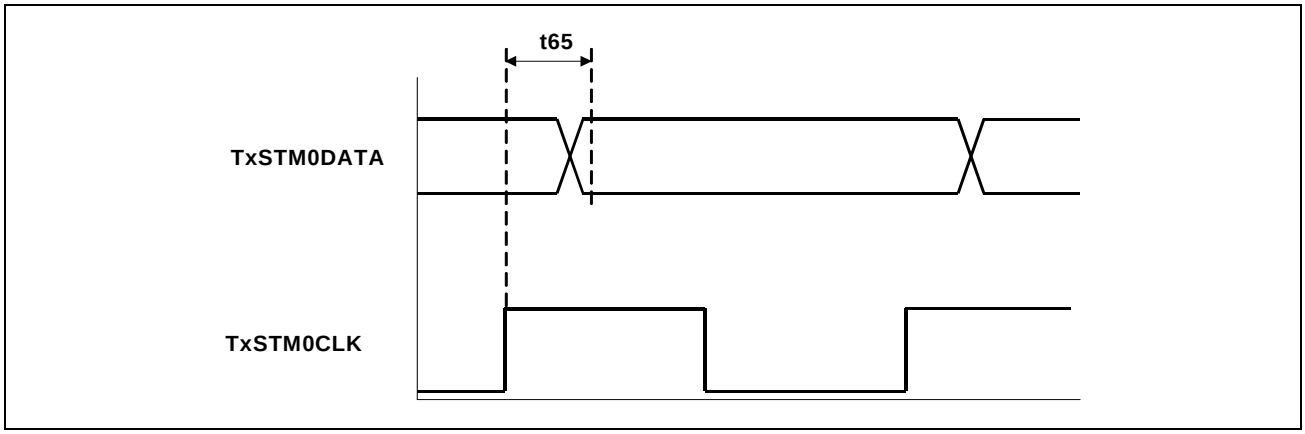
Note: The values for t63 and t64 are presented in **Table 289**.

Table 289 Timing Information for the Receive STM-0/STM-1 LIU Interface when the Receive STM-0/STM-1 TOH Processor block has been configured to sample the RxSTM0DATA signal upon the rising edge of the RxSTM0CLK signal

Symbol	Description	Min.	Typ.	Max.
t63	RxSTM0DATA to rising edge of RxSTM0CLK set-up time requirements	5ns		
t64	Rising edge of RxSTM0CLK to RxSTM0DATA Hold time requirements	0ns		

8.7.2 Transmit STM-0/STM-1 LIU Interface Timing

FIGURE 71. AN ILLUSTRATION OF THE WAVEFORMS OF THE STM-0/STM-1 SIGNALS THAT ARE OUTPUT FROM THE TRANSMIT STM-0/STM-1 LIU INTERFACE - DEDICATED PORT



Note: The value for t65 is presented in **Table 290** .

Table 290 Timing Information for the Transmit STM-0/STM-1 LIU Interface when the Transmit STM-0/STM-1 TOH Processor block has been configured to update the TxSTM0DATA signal upon the rising edge of the TxSTM0CLK signal

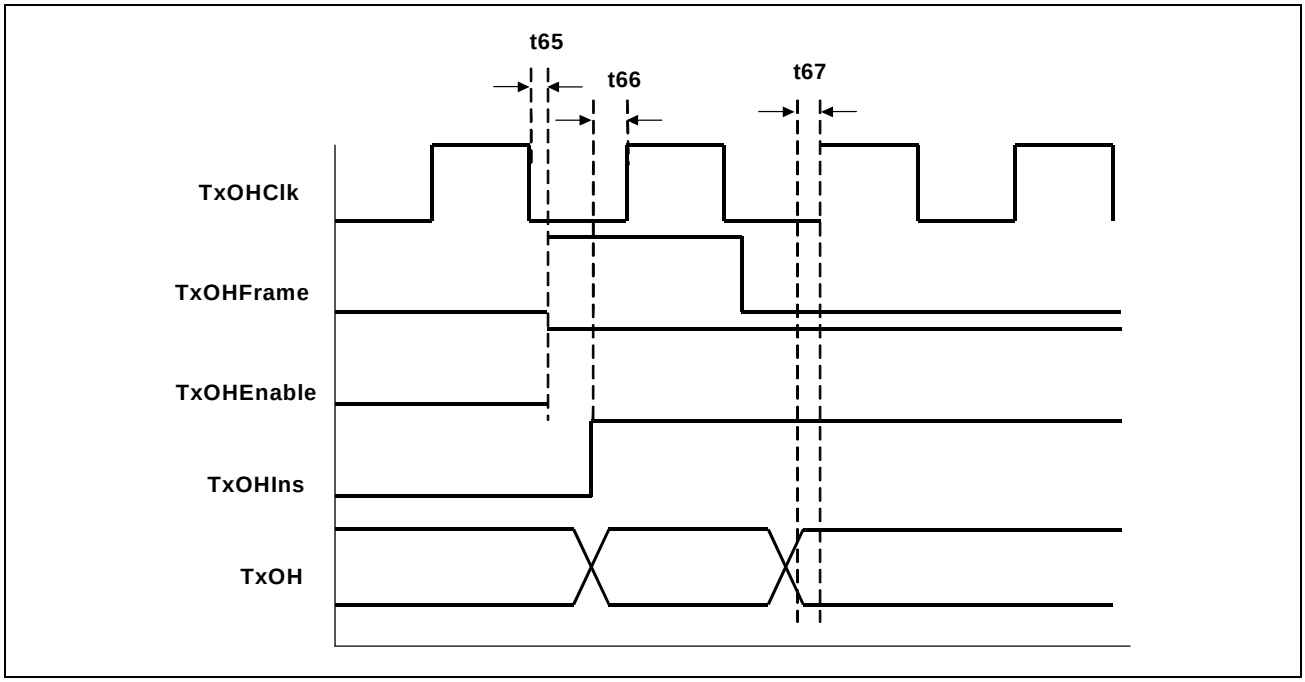
Symbol	Description	Min.	Typ.	Max.
t65	Rising edge of TxSTM0CLK to TxSTM0DATA output delay	2.0ns		5.0ns

8.8 TRANSMIT STM-0/STM-1 TOH and POH DATA INPUT PORT

The Transmit STM-0/STM-1 TOH and POH Data Input Port is used to insert a value for the TOH and POH bytes into the outbound STM-0/STM-1 data-stream.

Note: The TxOHIns and the TxOH input pins are sampled (by the Transmit STM-0/STM-1 TOH and POH Overhead Input Port) upon the rising edge of TxOHClk. All of the remaining signals (e.g., TxOHFrame and TxOHEnable) are updated upon the falling edge of TxOHClk.

FIGURE 72. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT STM-0/STM-1 TOH AND POH OVERHEAD DATA INPUT PORT



Note: The values for t65, t66 and t67 can be found in **Table 291**.

Table 291 Timing Information for the Transmit STM-0/STM-1 TOH and POH Overhead Data Input Port

Symbol	Description	Min.	Typ.	Max.
t65	Falling edge of TxOHClk to rising edge of TxOHFrame, TxOHEnable and TxPOHInd output delay	-3.0ns		-2.0ns
t66	TxOHIns to rising edge of TxOHClk set-up time	6.0ns		
t67	TxOH Data to rising edge of TxOHClk set-up time	6.0ns		
F1	TxOHClk Frequency	3.08MHz		

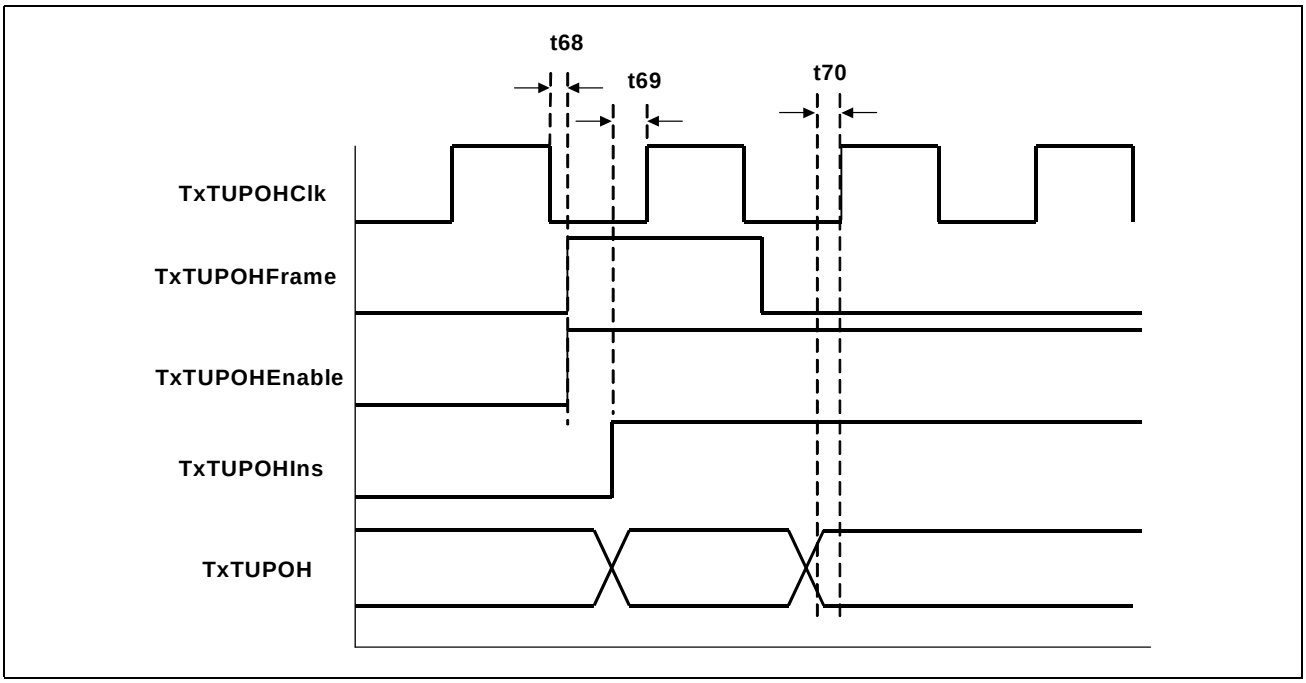
Note: The XRT86SH221 uses faster SYSCLK (49MHz) and enable at STM-0 byte rate (6.48MHz) to generate all the outputs including TxOHClk, TxOHEnable and TxOHFrame. This can make t65 have negative min and max times.The rising of TxOHClk should be used to sample TxOHEnable and TxOHFrame which provides enough setup and hold times.

8.9 TRANSMIT VC-4 POH DATA INPUT PORT

The Transmit VC-4 POH Data Input Port is used to insert a value for the VC-4 POH bytes into either the outbound VC-4 data-stream (which is output via the Transmit STM-1 Telecom Bus.

Note: The TxTUPOHIns and the TxTUPOH input pins are sampled (by the Transmit VC-4 POH Data Input Port) upon the rising edge of TxTUPOHClk. All of the remaining signals (e.g., TxTUPOHFrame and TxTUPOHEnable) are updated upon the falling edge of TxTUPOHClk.

FIGURE 73. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT VC-4 POH DATA INPUT PORT



Note: The values for t68, t69 and t70 can be found in **Table 292**.

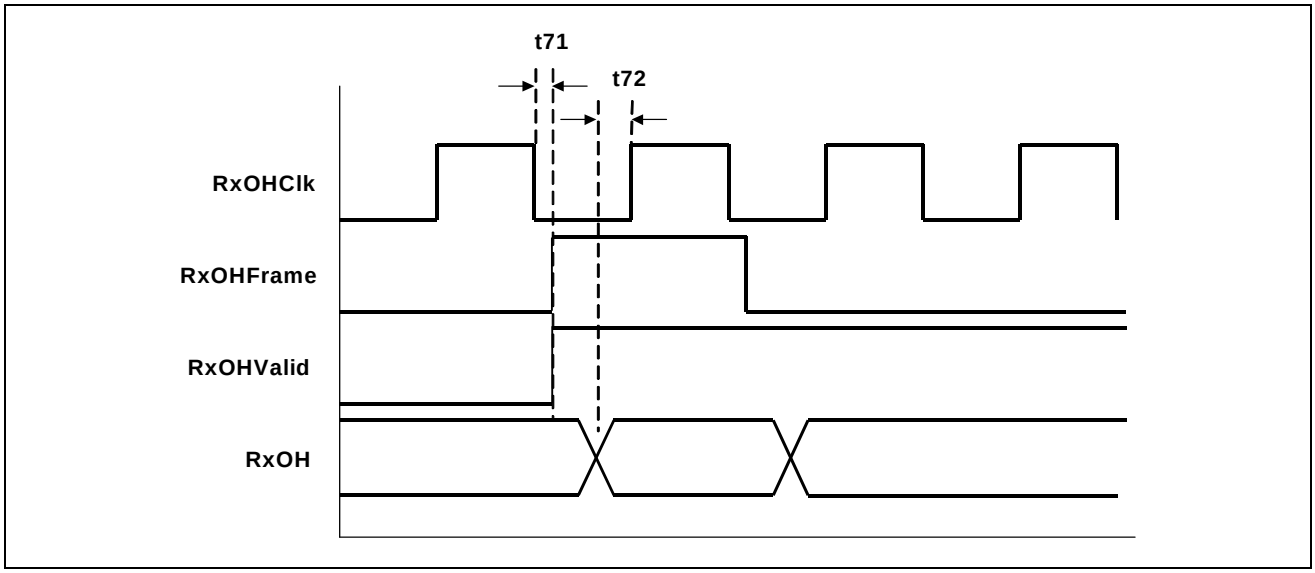
Table 292 Timing Information for the Transmit VC-4 POH Data Input Port

Symbol	Description	Min.	Typ.	Max.
t68	Falling edge of TxTUPOHClk to rising edge of TxTUPOHFrame and TxTUPOHValid output delay	-0.5ns		0.5ns
t69	TxTUPOHIns to rising edge of TxTUPOHClk set-up time	6ns		
t70	TxTUPOH Data to rising edge of TxTUPOHClk set-up time	6ns		

8.10 Receive STM-0/STM-1 TOH and POH Data Output Port

The Receive STM-0/STM-1 TOH and POH Data Output port is used to extract out the values of the TOH and POH bytes within the incoming STM-0/STM-1 data-stream. All of the Receive TOH and POH Data Output port signals are updated upon the falling edge of RxOHClk.

FIGURE 74. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE STM-0/STM-1 TOH AND POH DATA OUTPUT PORT



Note: The values for t71 and t72 can be found in **Table 293**.

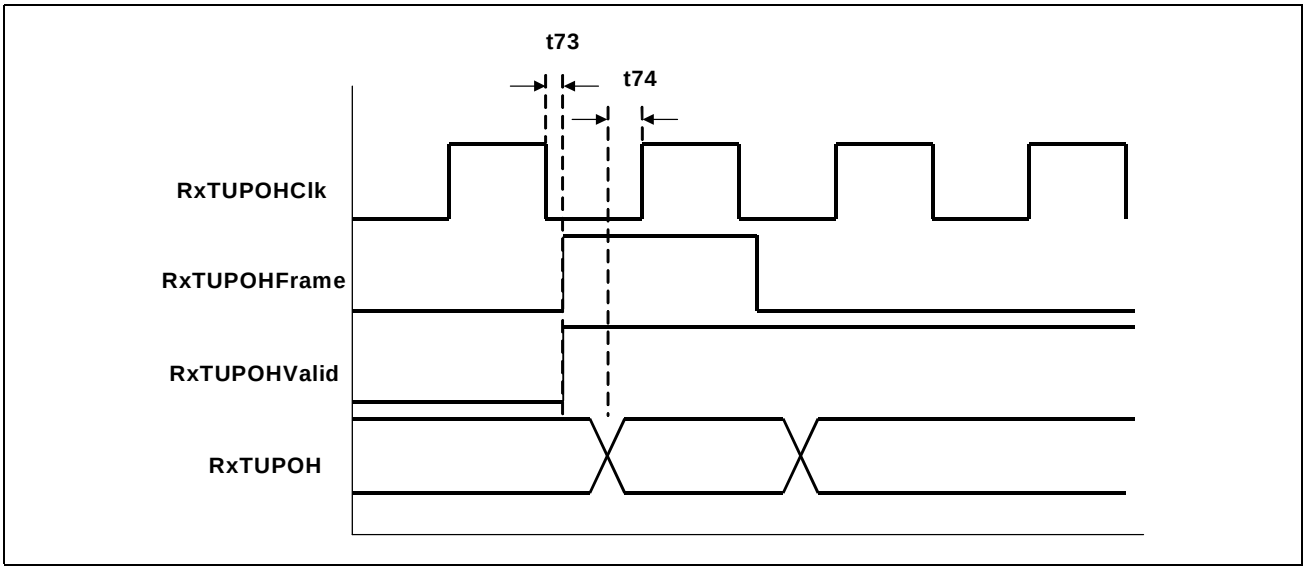
Table 293 Timing Information for the Receive STM-0/STM-1 TOH and POH Data Output Port

Symbol	Description	Min.	Typ.	Max.
t71	Falling edge of RxOHClk to rising edge of RxOHFrame, RxOHValid, and RxPOHInd	-0.2ns		0.2ns
t72	Falling edge of RxOHClk to RxOH output delay	-0.2ns		0.2ns

8.11 RECEIVE VC-4 POH DATA OUTPUT PORT

The Receive VC-4 POH Overhead Output port is used to extract out the values of the VC-4 POH bytes within the incoming STM-1 data-stream. All of the Receive VC-4 POH Overhead Output port signals are updated upon the falling edge of RxTUPOHClk. The timing wave-form and information for the Receive VC-4 POH Data Output Port is presented below.

FIGURE 75. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE VC-4 POH DATA OUTPUT PORT



Note: The values for t73 and t74 can be found in **Table 294**.

Table 294 Timing Information for the Receive VC-4 POH Data Output Port

Symbol	Description	Min.	Typ.	Max.
t73	Falling edge of RxTUPOHClk to rising edge of RxTUPOHFrame and RxTUPOHValid	-0.2ns		0.2ns
t74	Falling edge of RxTUPOHClk to RxTUPOH output delay	-0.2ns		0.2ns

8.12 INGRESS DIRECTION - ADD/DROP PORT TIMING

8.12.1 Ingress Direction - Add Port Timing

FIGURE 76. ILLUSTRATION OF THE INGRESS-DIRECTION ADD PORT SIGNALS

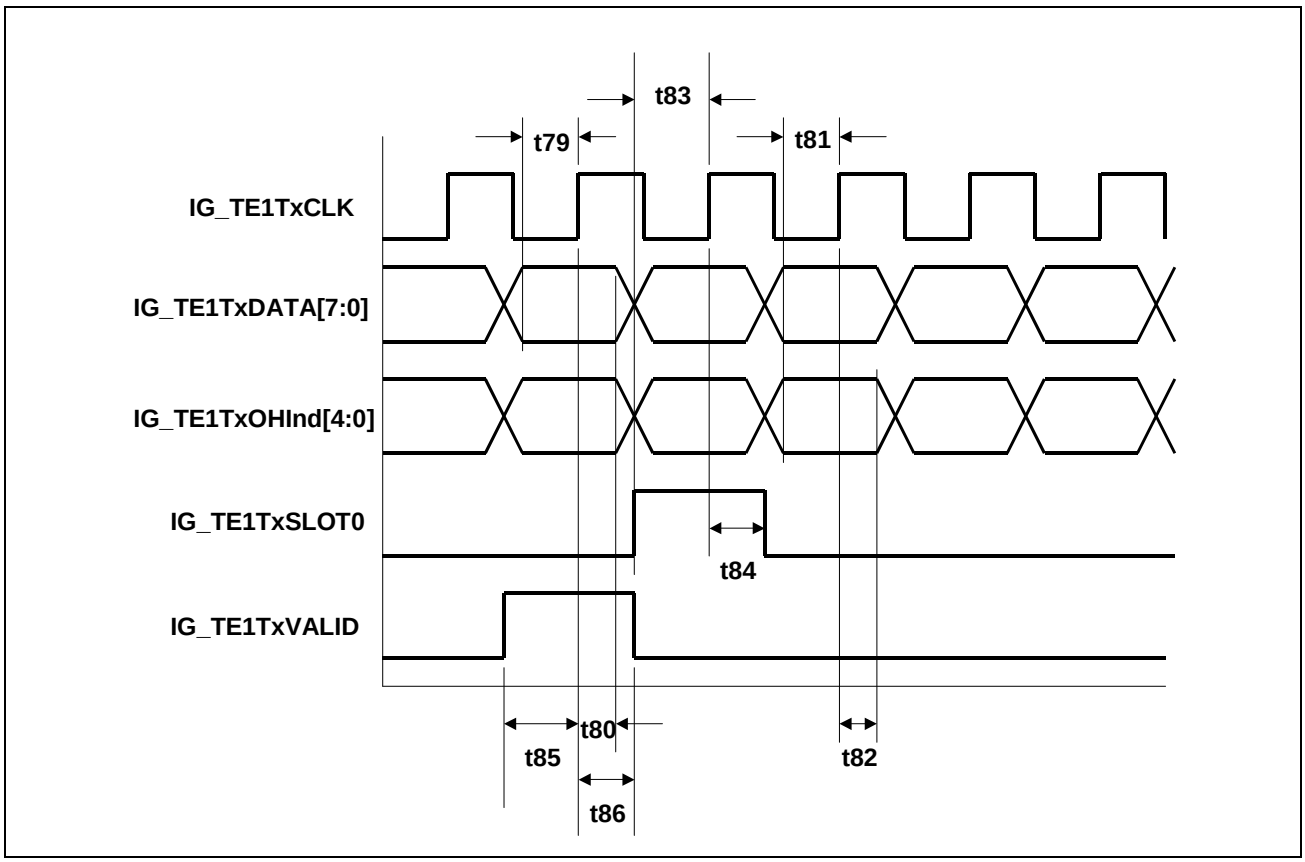


Table 295 Timing Information for the Ingress-Direction Add Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t79	IG_TE1TxDATA[7:0] to rising edge of IG_TE1TxCLK set-up time	4.5			ns
t80	Rising edge of IG_TE1TxCLK to IG_TE1TxDATA[7:0] hold time	3.0			ns
t81	IG_TE1TxOHInd[4:0] to rising edge of IG_TE1TxCLK set up time	4.5			ns
t82	Rising edge of IG_TE1TxCLK to IG_TE1TxOHInd[4:0] hold time	3.0			ns
t83	IG_TE1TxSLOT0 to rising edge of IG_TE1TxCLK set-up time	5.0			ns
t84	Rising edge of IG_TE1TxCLK to IG_TE1TxSLOT0 hold time	3.0			ns
t85	IG_TE1TxVALID to rising edge of IG_TE1TxCLK set-up time	5.0			ns
t86	Rising Edge of IG_TE1TxCLK to IG_TE1TxVALID hold time	3.0			ns

8.12.2 Ingress Direction - Drop Port Timing

FIGURE 77. ILLUSTRATION OF THE INGRESS-DIRECTION DROP PORT SIGNALS

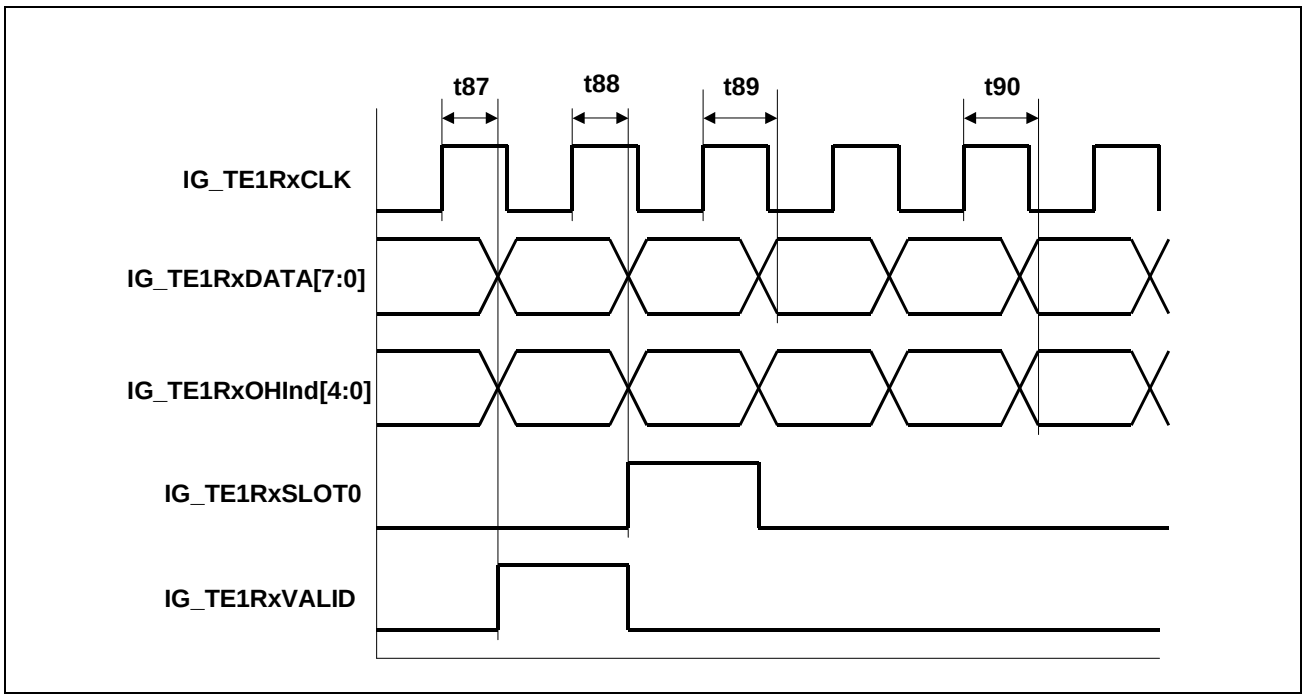


Table 296 Timing Information for the Ingress-Direction Drop Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t87	Falling Edge of IG_TE1RxCLK to IG_TE1RxVALID output delay	-0.2		3.0	ns
t88	Rising edge of IG_TE1RxCLK to IG_TE1RxDATA[7:0] hold time	6.0			ns
t89	IG_TE1RxOHInd[4:0] to rising edge of IG_TE1rxCLK set up time	4.5			ns
t90	Rising edge of IG_TE1RxCLK to IG_TE1RxOHInd[4:0] hold time	6.0			ns

8.13 EGRESS DIRECTION - ADD/DROP PORT TIMING

8.13.1 Egress Direction - Add Port Timing

FIGURE 78. ILLUSTRATION OF THE EGRESS-DIRECTION ADD PORT SIGNALS

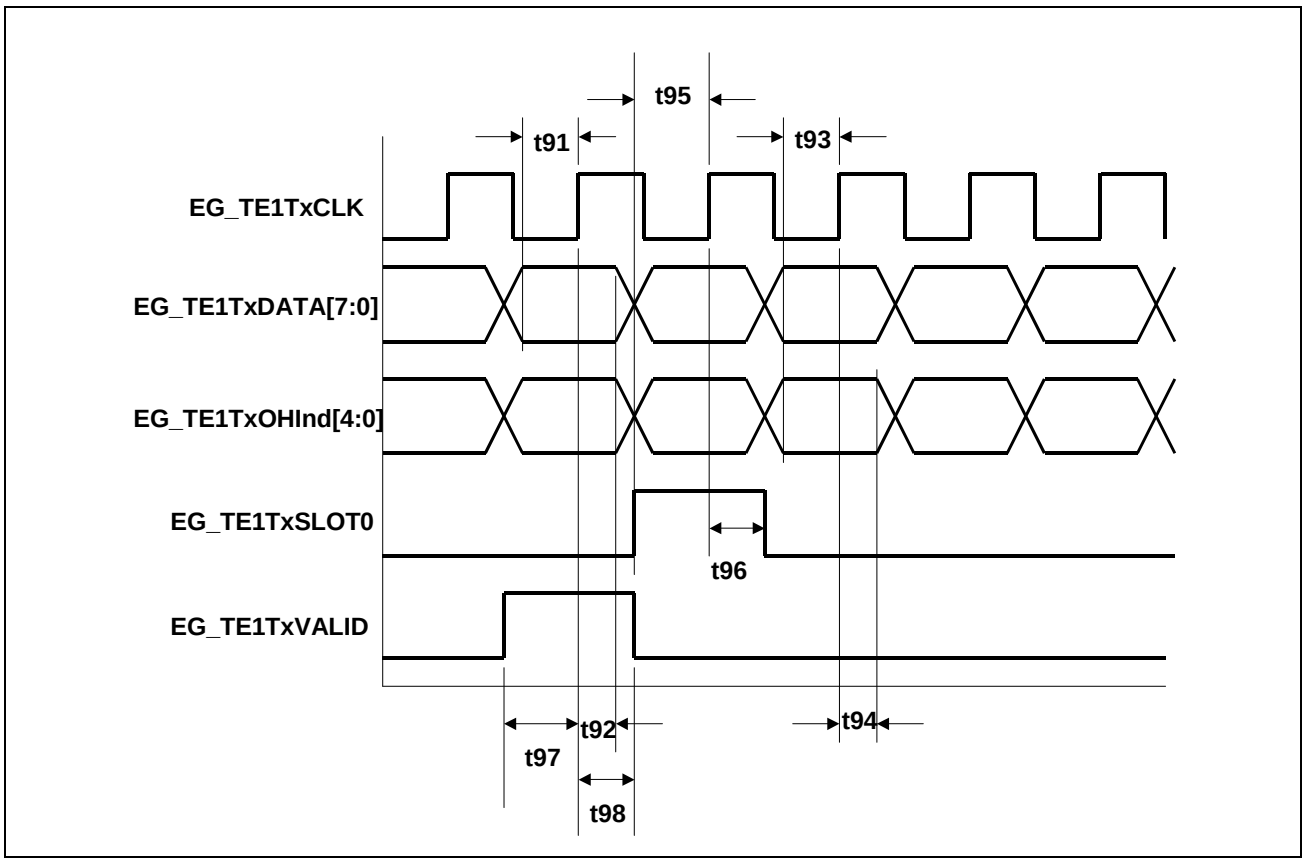


Table 297 Timing Information for the Egress-Direction Add Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t91	EG_TE1TxDATA[7:0] to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t92	Rising edge of EG_TE1TxCLK to EG_TE1TxDATA[7:0] hold time	2.0			ns
t93	EG_TE1TxOHInd[4:0] to rising edge of EG_TE1TxCLK set up time	7.0			ns
t94	Rising edge of EG_TE1TxCLK to EG_TE1TxOHInd[4:0] hold time	2.0			ns
t95	EG_TE1TxSLOT0 to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t96	Rising edge of EG_TE1TxCLK to EG_TE1TxSLOT0 hold time	2.0			ns
t97	EG_TE1TxVALID to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t98	Rising Edge of EG_TE1TxCLK to EG_TE1TxVALID hold time	2.0			ns

8.13.2 Egress Direction - Drop Port Timing

FIGURE 79. ILLUSTRATION OF THE EGRESS-DIRECTION DROP PORT SIGNALS

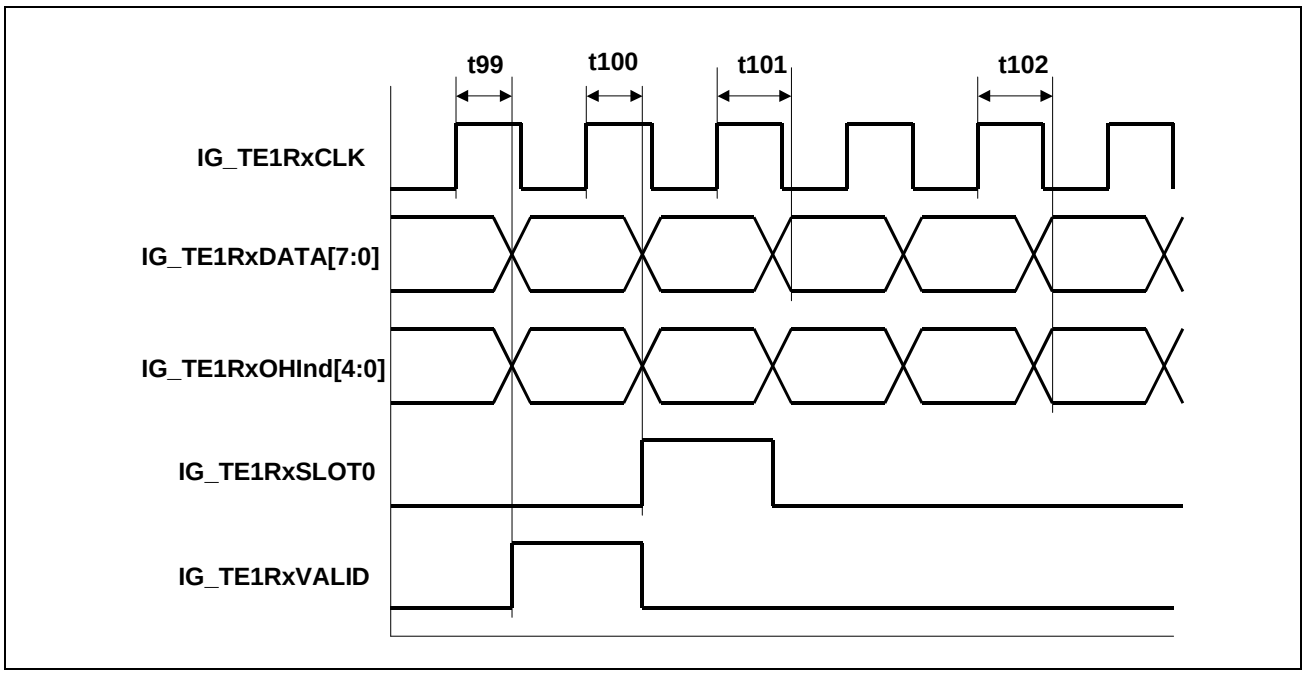


Table 298 Timing Information for the Egress-Direction Drop Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t99	Falling Edge of EG_TE1RxCLK to EG_TE1RxVALID output delay	-0.2		3.0	ns
t100	Rising edge of EG_TE1RxCLK to EG_TE1RxDATA[7:0] hold time	6.0			ns
t101	EG_TE1RxOHInd[4:0] to rising edge of EG_TE1RxCLK set up time	4.5			ns
t102	Rising edge of EG_TE1RxCLK to EG_TE1RxOHInd[4:0] hold time	6.0			ns

9.0 ELECTRICAL CHARACTERISTICS

Table 299 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	3.465	v	Note 1
V_{DD18}	Supply Voltage	-0.5	1.890	v	Note 1
S_{TEMP}	Storage Temperature	-65	+150	℃	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	+85	℃	Linear air flo w (TBD) ft/min
ThetaJA	Thermal Resistance		TBD	℃/W	
ThetaJC	Thermal Resistance		TBD	℃/W	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-8
ESD	ESD Rating - HBM		2000	v	Note 2

Notes:

1. *Exposure to or operating near the Min or Max values for extended periods may cause permanent failure and impair reliabilty of the device.*
2. *ESD testing method is per JESD22-A114.*

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25℃, unless otherwise specified					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Voltage (3.3V)	VDD33	3.13	3.3	3.46	V
Power Supply Voltage (1.8V)	VDD18	1.71	1.8	1.89	V
Current Consumption (3.3V)			659		mA)
Current Consumption (1.8V)			309		mA
Power Consumption (3.3V)			2.175		W
Power Consumption (1.8V)			556		mW
Total Power Consumption			2.73		W
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage IOH=-2.0mA	V_{OH}	2.4	-		V
Output Low Voltage IOL=2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_L	-	-	±10	µA
Input Capacitance	C_I	-	5.0		pF
Output Load Capacitance	C_L	-	-	25	pF

NOTE: *Input leakage current excludes pins that are internally pulled "Low" or "High"*

TABLE 300: E1 RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25°C, unless otherwise specified					
Receiver loss of signal:					
Number of consecutive zeros before LOS is set	-	32	-	bit	Cable attenuation @1024KHz ITU-G.775, ETS1 300 233
Input signal level at LOS	13	16	-	dB	
RLOS Clear	12.5	-	-	% ones	
Receiver Sensitivity Cable + Flat Loss	6+6	-	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Interference Margin	-18	-14	-	dB	With 6dB cable loss
Input Impedance	15		-	KΩ	
Jitter Tolerance: 1 Hz 10KHz---100KHz	 37 0.3	 - -	 - -	 UIpp UIpp	 ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	-	20	36 0.5	KHz dB	ITU G.736
Jitter Attenuator Corner Frequency(-3dB curve) JABW=0 JSBW=1	 - -	 10 1.5	 - -	 Hz Hz	ITU G.736
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	 12 18 14	 - - -	 - - -	 dB dB dB	 ITU G.703

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25°C, unless otherwise specified					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude					
75Ω	2.13	2.37	2.60	V	1:2 Transformer
120Ω	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	15	-	-	dB	ETSI 300 166
102kHz - 2048kHz	9	-	-	dB	
2048kHz - 3072kHz	8	-	-	dB	

10.0 BACKGROUND AND PROTOCOLS

This section intends to provide a background coverage of the theory of communication protocols involved in Voyager-Lite development. Only brief descriptions of their formats, control flows, and application-specific features are presented here.

10.1 SYNCHRONOUS DIGTIAL HIERARCHY (SDH) STANDARD

This section intends to provide a background coverage of the theory of communication protocols involved in SDH standard. Only brief descriptions of their rates, formats, control flows, and application-specific features are presented here.

Synchronous digital hierarchy (SDH): The SDH is a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks.

Synchronous transport module (STM): An STM is the information structure used to support section layer connections in the SDH. It consists of information payload and Section Overhead (SOH) information fields organized in a block frame structure which repeats every 125 µs. The information is suitably conditioned for serial transmission on the selected media at a rate which is synchronized to the network. A basic STM is defined at 155 520 kbit/s. This is termed STM-1. Higher capacity STMs are formed at rates equivalent to N times this basic rate. STM capacities for N=4, N=16, N=64 and N=256 are defined; higher values are under consideration.

The STM-0 comprises a single Administrative Unit of level 3. The STM-N, N = 1, comprises a single Administrative Unit Group of level N (AUG-N) together with the SOH.

Virtual container-n (VC-n): A Virtual Container is the information structure used to support path layer connections in the SDH. It consists of information payload and Path Overhead (POH) information fields organized in a block frame structure which repeats every 125 or 500 us. Alignment information to identify VC-n frame start is provided by the server network layer.

Two types of Virtual Containers have been identified.

- Lower order Virtual Container-n: VC-n (n=1, 2, 3). This element comprises a single Container-n (n=1, 2, 3) plus the lower order Virtual Container POH appropriate to that level.
- Higher order Virtual Container-n: VC-n (n=3, 4). This element comprises either a single Container-n (n=3, 4) or an assembly of Tributary Unit Groups (TUG-2s or TUG-3s), together with Virtual Container POH appropriate to that level.

Administrative unit-n (AU-n): An Administrative Unit is the information structure which provides adaptation between the higher order path layer and the multiplex section layer. It consists of an information payload (the higher order Virtual Container) and an Administrative Unit pointer which indicates the offset of the payload frame start relative to the multiplex section frame start.

Two Administrative Units are defined. The AU-4 consists of a VC-4 plus an Administrative Unit pointer which indicates the phase alignment of the VC-4 with respect to the STM-N frame. The AU-3 consists of a VC-3 plus an Administrative Unit pointer which indicates the phase alignment of the VC-3 with respect to the STM-N frame. In each case the Administrative Unit pointer location is fixed with respect to the STM-N frame.

One or more Administrative Units occupying fixed, defined positions in an STM payload are termed

an Administrative Unit Group (AUG). An AUG-1 consists of a homogeneous assembly of AU-3s or an AU-4.

Tributary unit-n (TU-n): A Tributary Unit is an information structure which provides adaptation between the lower order path layer and the higher order path layer. It consists of an information payload (the lower order Virtual Container) and a Tributary Unit pointer which indicates the offset of the payload frame start relative to the higher order Virtual Container frame start.

The TU-n (n=1, 2, 3) consists of a VC-n together with a Tributary Unit pointer. One or more Tributary Units, occupying fixed, defined positions in a higher order VC-n payload is termed a Tributary Unit Group (TUG). TUGs are defined in such a way that mixed capacity payloads made up of different size Tributary Units can be

constructed to increase flexibility of the transport network. A TUG-2 consists of a homogeneous assembly of identical TU-1s or a TU-2. A TUG-3 consists of a homogeneous assembly of TUG-2s or a TU-3.

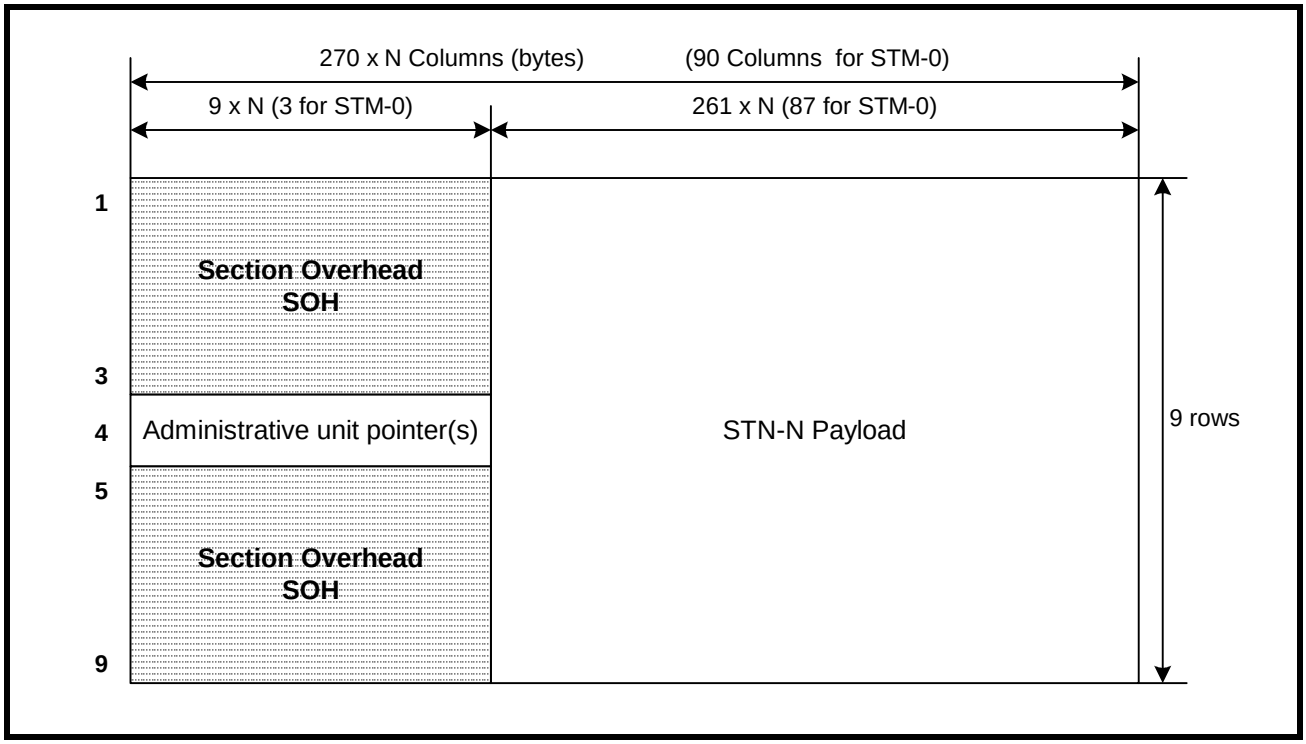
Container-n (n=1-4): A container is the information structure which forms the network synchronous information payload for a Virtual Container. For each of the defined Virtual Containers there is a corresponding container. Adaptation functions have been defined for many common network rates into a limited number of standard containers.

10.2 BASIC FRAME STRUCTURE

STM-N frame structure is shown in Figure 80. The three main areas of the STM-N frame are indicated:

- SOH;
- Administrative Unit pointer(s);
- Information payload.

FIGURE 80. STM-N FRAME STRUCTURE



Section overhead

Rows 1-3 and 5-9 of columns 1 to 9 x N of the STM-N in **Figure 80** are dedicated to the SOH.

Administrative Unit pointers

Row 4 of columns 1 to 9 × N in **Figure 80** is available for Administrative Unit pointers.

Administrative Units in the STM-N

The STM-N payload supports one AUG-N where the:

A. AUG-256 may consist of:

1. four AUG-64;
2. one AU-4-256c.

B. AUG-64 may consist of:

1. four AUG-16;
2. one AU-4-64c.

C. AUG-16 may consist of:

1. four AUG-4;
2. one AU-4-16c.

D. AUG-4 may consist of:

1. four AUG-1;
2. one AU-4-4c.

E. AUG-1 may consist of:

1. one AU-4;
2. three AU-3s.

The VC-n associated with each AU-n does not have a fixed phase with respect to the STM-N frame. The location of the first byte of the VC-n is indicated by the AU-n pointer. The AU-n pointer is in a fixed location in the STM-N frame.

The AU-4 may be used to carry, via the VC-4, a number of TU-ns (n=1, 2, 3) forming a two-stage multiplex. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-4. The TU-n pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

The AU-3 may be used to carry, via the VC-3, a number of TU-ns (n=1, 2) forming a two-stage multiplex. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-3. The TU-n pointer is in a fixed location in the VC-3 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

11.0 REFERENCE DOCUMENTATION

- Telcordia, Transport Systems Generic Requirements (TSGR): Common Requirements GR-499-CORE Issue 2, December 1998
- ITU-T Recommendation G.707 Network Node Interface for the Synchronous Digital Hierarchy (SDH) (03/96)
- ITU-T Recommendation G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks (01/94)
- ITU/CCITT Recommendation O.151 Error Performance Measuring Equipment Operating at the Primary Rate and Above (10/92)
- ANSI T1.107, "Digital Hierarchy - Formats Specifications", 1988.
- ANSI 1.107a, Addendum to ANSI T1.107, 1988", 1990.
- ANSI T1.403 - 1999, Network-to-Customer Installation - DS1 Metallic Interface
- ANSI T1.408-1990, Integrated Services Digital Network (ISDN) Primary Rate - Customer Installation Metallic Interfaces Layer 1 Specification
- ETS 300 011, ISDN primary rte user-network interface layer 1 specification and test principles, April 1992
- ETS 300 233, ISDN; Access digital section for ISDN primary rate, May 1994
- Intel i750, i860, i960 Processors and Related Products Data Book, 1994
- Intel 8-bit Embedded Controllers Data Book
- Motorola MC68302, Integrated Multi-Protocol Processor User's Manual

11.1 TERMINOLOGY

11.1.1 NOMENCLATURE

"Transmit" refers to the flow of data from the user interface to the physical line interface.

"Receive" refers to the flow of data from the physical line interface to the user interface.

"Ingress" refers to the flow of data from the E1 LIU's to the SDH interface.

"Egress" refers to the flow of data from the SDH interface to the E1 LIU's.

11.1.2 SIGNAL NAME PREFIXES AND SUFFIXES

The following lists the convention used in this design for naming distinguished signals.

Tx	Signals pertaining to the DS1 transmit framer
Rx	Signals pertaining to the DS1 receive framer
Li	Signals pertaining to LIU interface module
p	Signals pertaining to microprocessor interface

11.1.3 ABBREVIATIONS

AIS	Alarm Indication Signal
AMI	Alternate Mask Inversion
AU	Administrative Unit
AUG	Administrative Unit Group
BIP	Bit Interleaved Parity
BPV	Bipolar Violation
CRC	Cyclic Redundancy Check

DSn	Digital Signal n (any of DS1, DS1A, DS1C or DS2)
DL	Data Link
FA	Frame Alignment
FAS	Frame Alignment Signal
FCS	Frame Check Sequence
FIFO	First In First Out
FPS	Framing Pattern Sequence
HDLC	High level Data Link Control protocol
ITU	The International Telecommunications Union
LAPD	Link Access Protocol D
LCV	Line Code Violation
LIU	Line Interface Unit
LOF	Loss Of Frame synchronization
LOP	Loss Of Pointer
LOS	Loss Of Signal
LTE	Line Terminating Equipment
MSOH	Multiplex Section Overhead
NRZ	Non Return to Zero
OH	OverHead
OOF	Out Of Frame synchronization
OC	Optical Carrier
PLM	Payload Label Mismatch
POH	Path Overhead
PM	Performance Monitor
PMDL	Path Maintenance Data Link
PMON	Performance Monitor
PTE	Path Terminating Equipment
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
REI	Remote Error Indication
RFI	Remote Failure Indication
RSOH	Regenerator Section Overhead
SDH	Synchronous Digital Hierarchy
Rx	Receive
SF	Super Frame
SDH	Synchronous Digtial Hierarchy
SPE	Synchronous Payload Envelop

STM	Synchronous Transport Module
TU	Tributary Unit
TUG	Tributary Unit Group
Tx	Transmit
T1DM	T1 Data Multiplexer
mp(uP)	Microprocessor
VC	Virtual Container
VT	Virtual Tributary

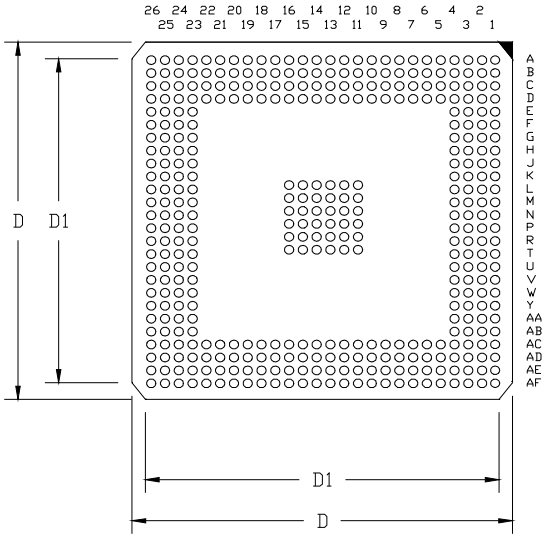
ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT86SH221IB	388 PBGA	-40℃ to +85℃

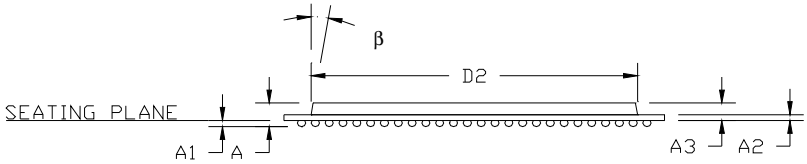
PACKAGE DIMENSIONS 388 PBGA

E

388 Ball Plastic Ball Grid Array
(27 mm x 27 mm, PBGA)
Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.067	0.106	1.70	2.70
A1	0.016	0.028	0.40	0.70
A2	0.008	0.028	0.20	0.70
A3	0.039	0.051	1.00	1.30
D	1.055	1.071	26.80	27.20
D1	0.984 BSC		25.00 BSC	
D2	0.937	0.953	23.80	24.20
b	0.024	0.035	0.60	0.90
e	0.039 BSC		1.00 BSC	
β	10°	20°	10°	20°

REVISIONS

REV. #	DATE	DESCRIPTION
P1.0.0	September 2006	First Release of the XRT86SH221 Preliminary Data Sheet.
P1.0.1	September 2006	Added the Application and Physical Interface section.
P1.0.2	November 2006	Added Power Consumption Numbers, Register Descriptions, and general edits.
P1.0.3	December 2006	Updated Register Information.
P1.0.4	March 2007	Updated Register Information, Pin descriptions, and Timing Diagrams.
P1.0.5	May 2007	General edits, updated electrical specifications, and clarified register descriptions.

Datasheet May 2007.

All effort hs been made to provide correct information in this data sheet, iIf discrepencies are found or more information is required please contact Exar Application Engineering at <NTApplications@exar.com>