DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1830

FILTER-CONTAINING VIDEO CHROMA, SYNCHRONIZING SIGNAL PROCESSING LSI COMPATIBLE WITH NTSC/PAL SYSTEM

DESCRIPTION

The μPC1830 is a filter-containing video chroma, synchronizing signal processing LSI compatible with the NTSC/PAL system. A decoder which converts composite video or separate Y/C video signals into a brightness signal and a color difference signal and outputs the result, and a matrix which comprises independent brightness signal/color difference signal input pins are integrated on one chip.

Decoder output can be used to drive an A/D converter; it is appropriate for picture-in-picture screen signal processing and multimedia boards.

FEATURES

- Contains a trap filter, band-pass filter, delay line, and color difference output low-pass filter.
  Peripheral parts can be drastically reduced.
- Low power consumption
  Appropriate for use with digital boards because of 5-V single power supply operation.
- DC control for user adjustment pins
  Centralized control can be performed by a microcontroller.
- One chip compatible with both NTSC and PAL systems
  Boards common to NTSC and PAL systems can be easily constructed.
- S pin input
  Supports composite and separate Y/C video signal inputs.
- Demodulation ratio/demodulation angle change (matrix)
  Demodulation ratio/demodulation angle can be selected in response to the NTSC or PAL system.
- Contains color difference tint control
  Fine adjustment of the demodulation axis can be made for both the NTSC and PAL systems.

ORDERING INFORMATION

Part Number	Package
μPC1830GT	42-pin plastic shrink SOP (375 mil)

The information in this document is subject to change without notice.

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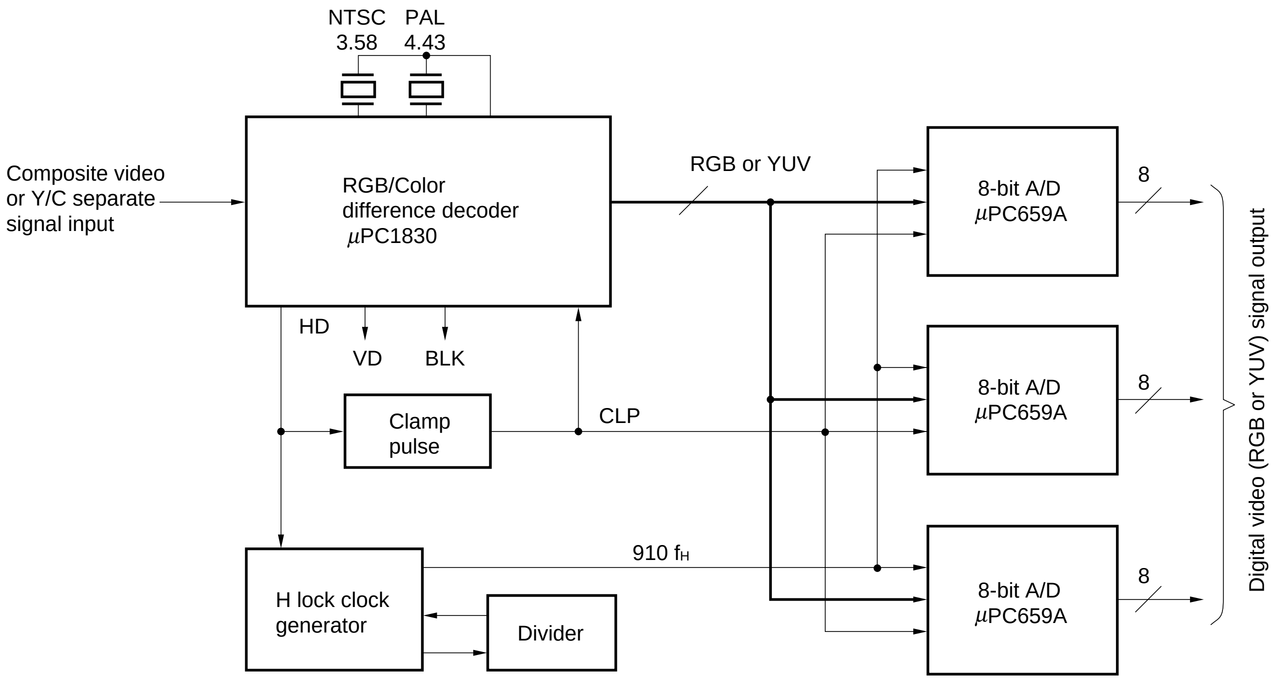
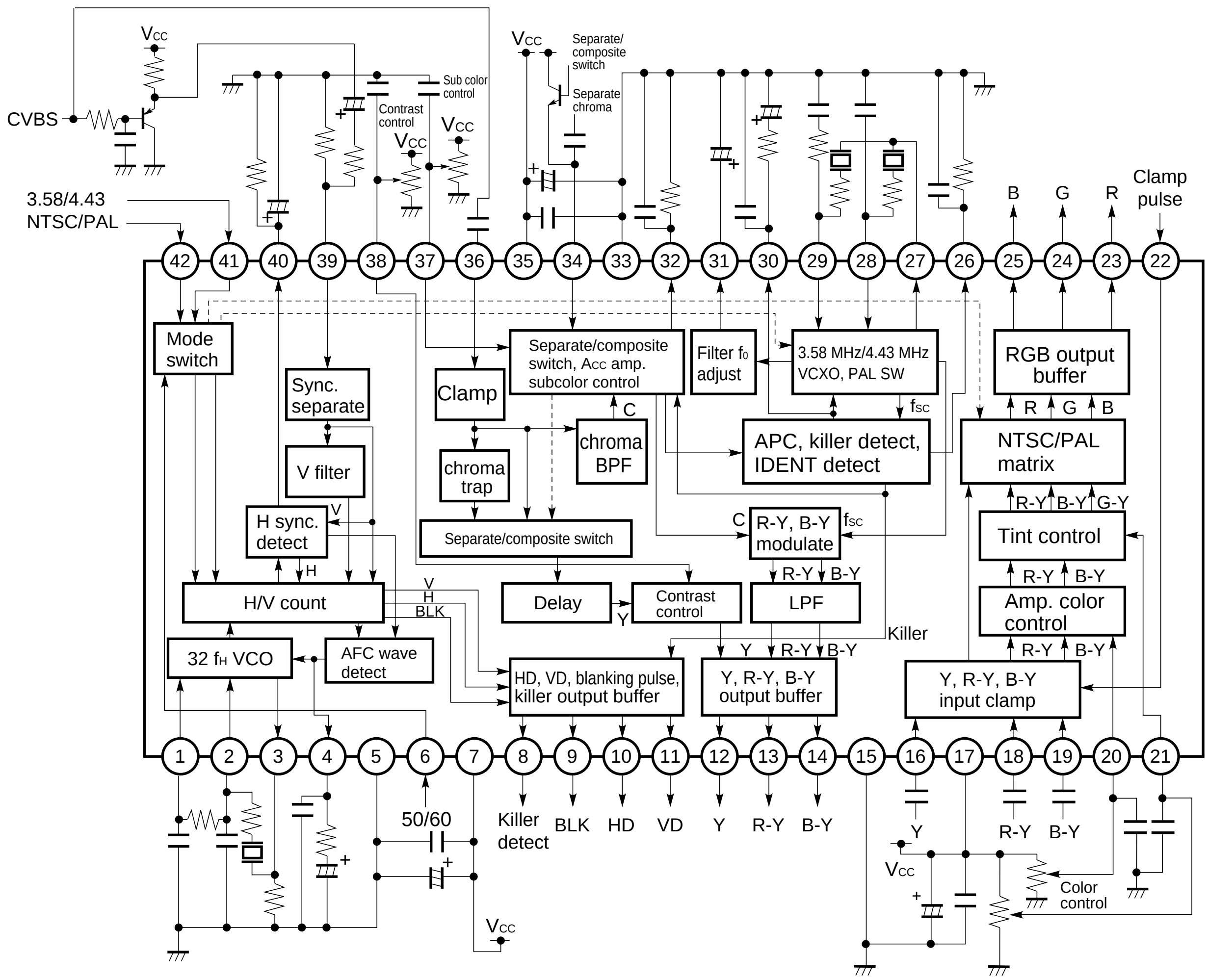
1. SYSTEM BLOCK DIAGRAM

VIDEO CAPTURE SYSTEM BLOCK DIAGRAM

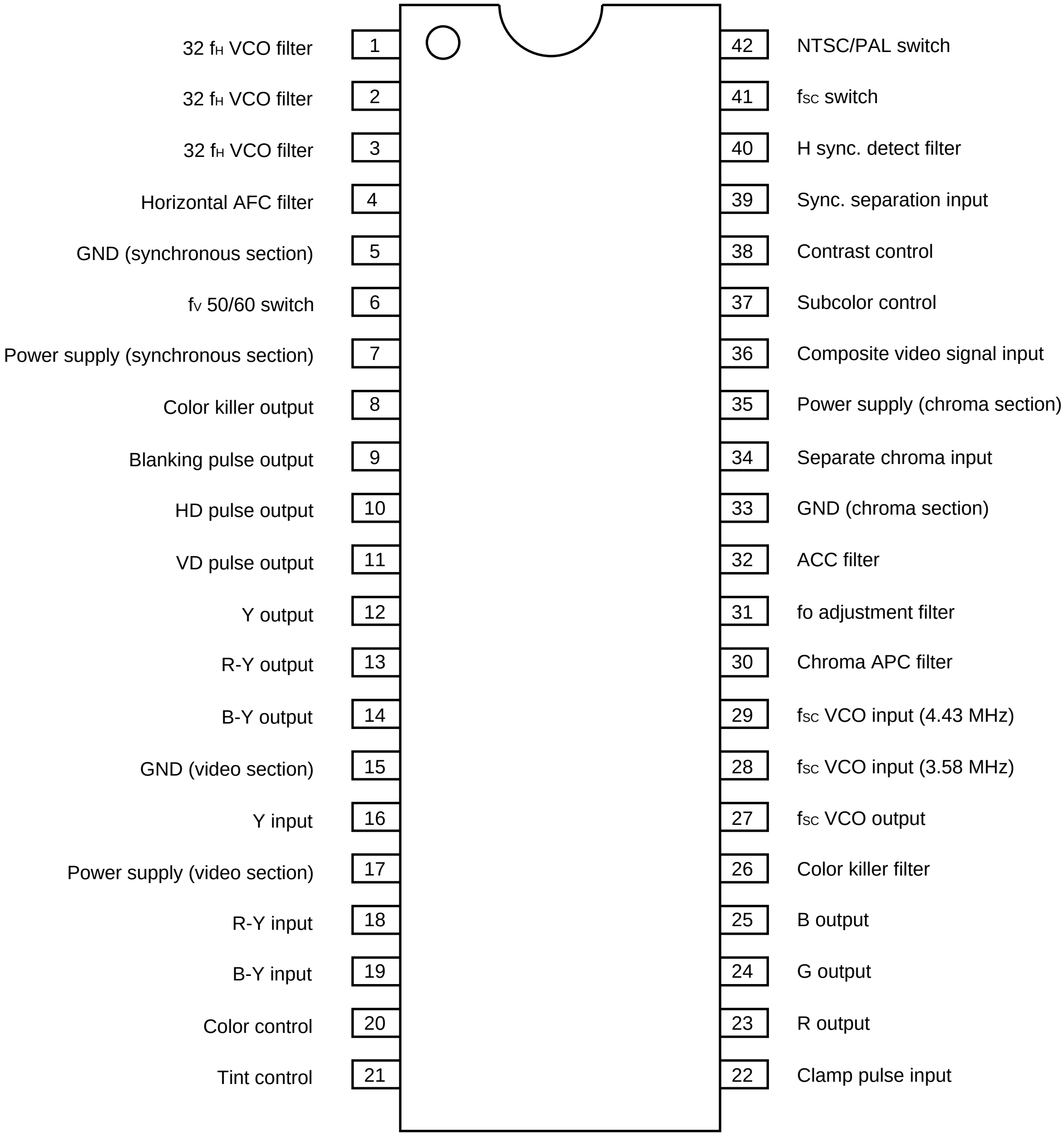


2. BLOCK DIAGRAM

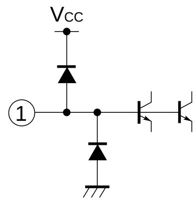
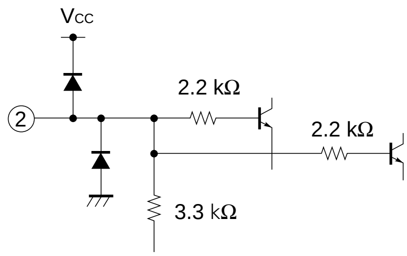
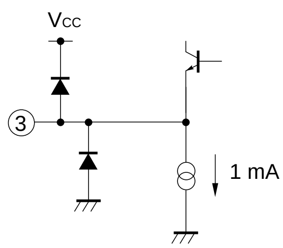
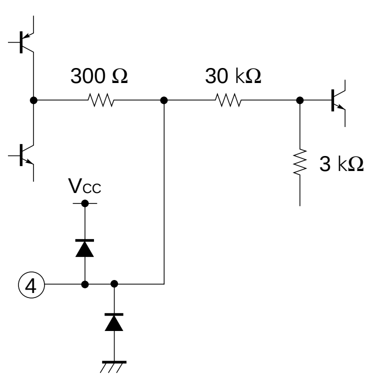


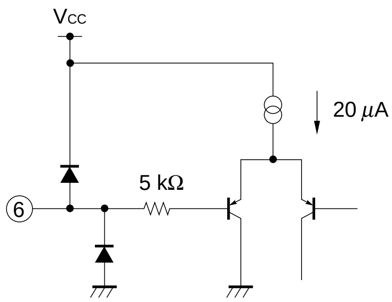
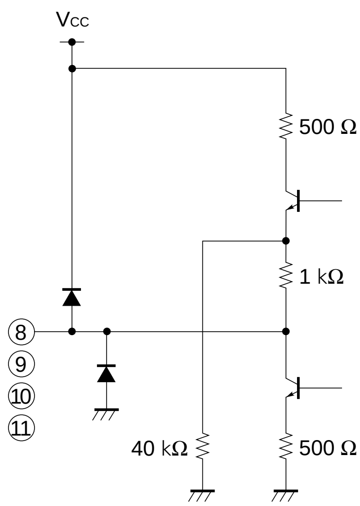
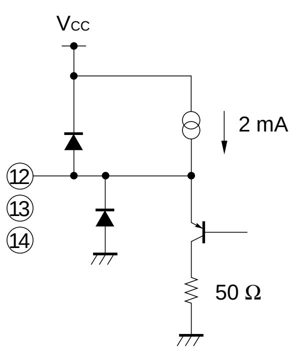
3. PIN CONFIGURATION (Top View)

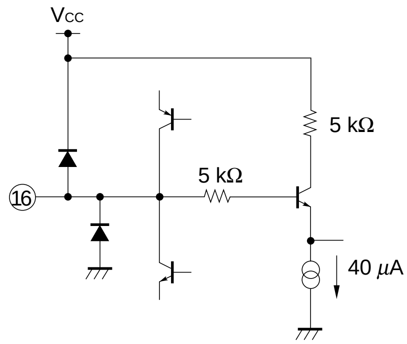
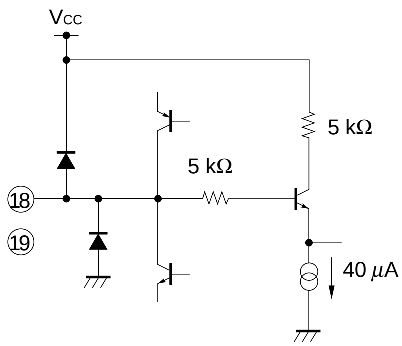
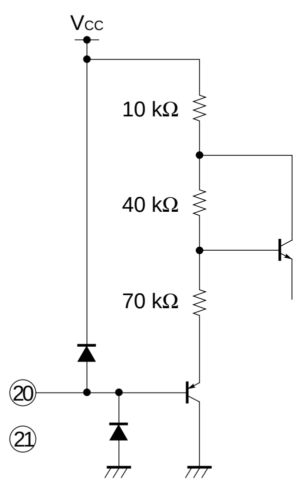
42-pin plastic shrink SOP (375 mil)
μPC1830GT

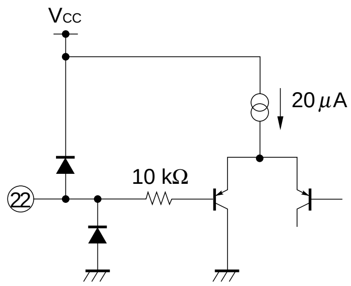
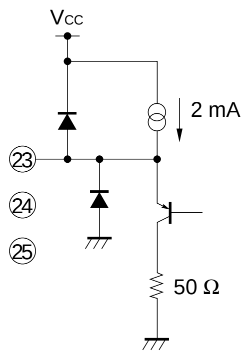
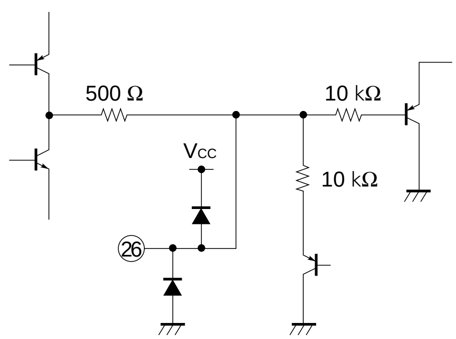
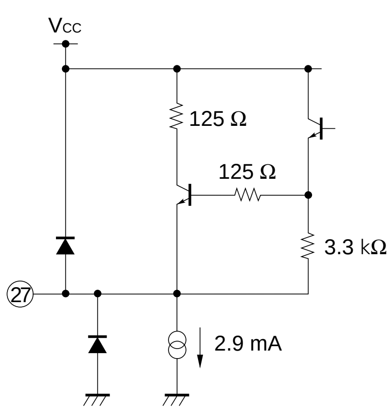


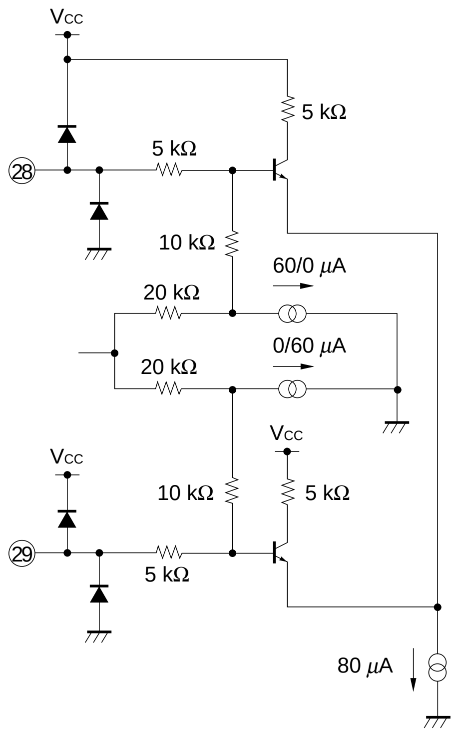
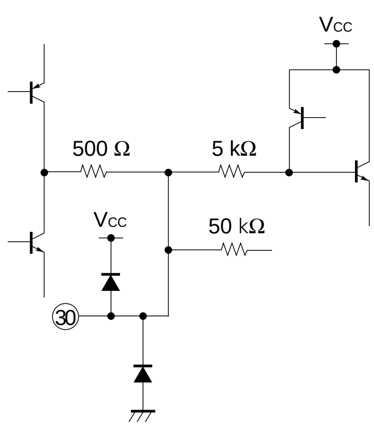
4. PIN EQUIVALENT CIRCUIT DIAGRAMS

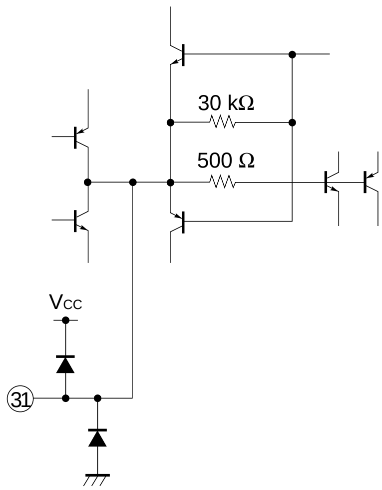
Pin No.	Pin name	Equivalent circuit	Function descriptions
1 2 3	32 f_H VCO filter	  	Pins for connecting a 32 f_H oscillation filter. For resonator, use 500 kHz ceramic resonator in both NTSC and PAL modes. Bias of pin 1 is supplied from pin 2 via an external resistor between pins 1 and 2.
4	Horizontal AFC filter		Pin for connecting filter of horizontal AFC detector.
5	GND (synchronous section)		Synchronous section ground.

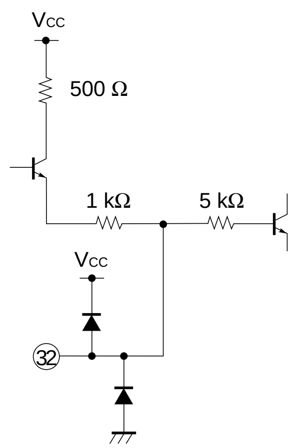
Pin No.	Pin name	Equivalent circuit	Function descriptions
6	fv 50/60 switch		Vertical frequency (fv) switch pin. When the pin voltage is 2.2 V or less, the vertical frequency changes to 50 Hz; when 2.8 V or more, to 60 Hz.
7	Power supply (synchronous section)		Synchronous section power supply.
8	Color killer output		Color killer output pin.
9	Blanking pulse output		Horizontal blanking pulse output pin.
10	HD pulse output		HD pulse output pin
11	VD pulse output		VD pulse output pin.
12	Y output		Y signal is output. DC level is approx. 2.0 V.
13	R-Y output		Decoder R-Y and B-Y color difference signal output pins. DC level is approx. 2.5 V.
14	B-Y output		
15	GND (video section)		Video section ground.

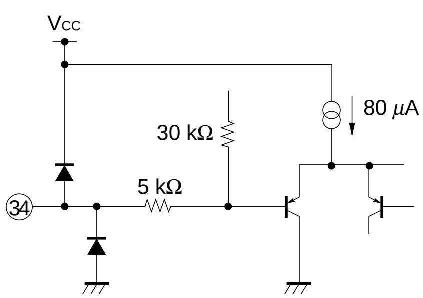
Pin No.	Pin name	Equivalent circuit	Function descriptions
16	Y input		Matrix Y signal input pin. This pin also serves as a clamp pin. Input the signal with C coupling. DC level is approx. 2.0 V.
17	Power supply (video section)		Video section power supply.
18	R-Y input		Matrix R-Y and B-Y color difference signal input pins. These pins also serve as clamp pins. Input the signals with C coupling. DC level is approx. 2.5 V. Output in PAL mode is “pseud PAL”.
19	B-Y input		
20	Color control		Pin for color adjustment of matrix circuit.
21	Tint control		Pin for tint adjustment of matrix circuit.

Pin No.	Pin name	Equivalent circuit	Function descriptions
22	Clamp pulse input		Matrix clamp pulse input pin. Clamp operation is performed at 2.8 V or more.
★ 23	R output		Matrix R, G, and B output pins. DC level is approx. 2.0 V. Sync. signal component, added to Y-input (16 pin), appears in R, G, and B output pins.
★ 24	G output		
★ 25	B output		
26	Color killer filter		Filter connection pin of color killer sync detector.
27	fSC VCO output		fSC VCO oscillator output pin. Connect this pin to pin 28 via a 3.58 MHz oscillation filter and to pin 29 via a 4.43 MHz oscillation filter.

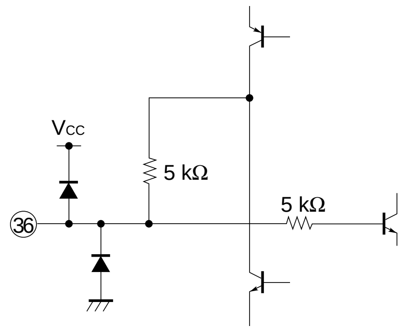
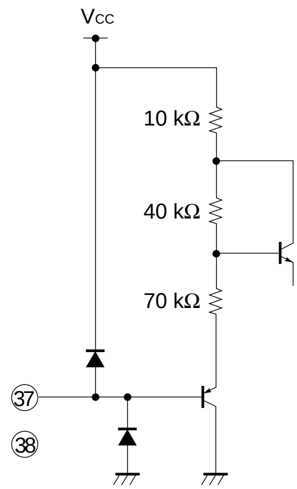
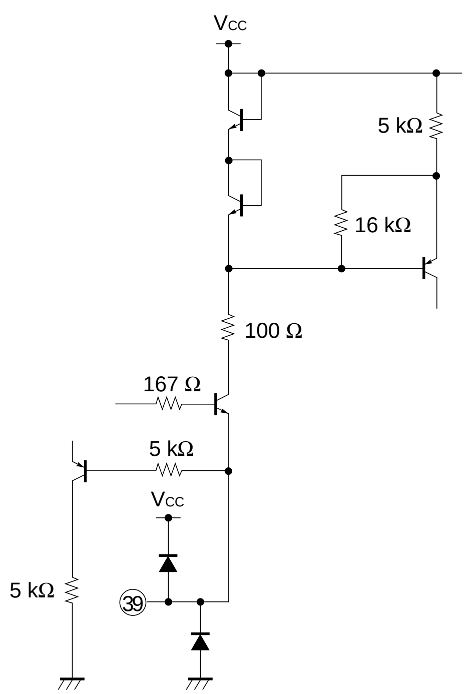
Pin No.	Pin name	Equivalent circuit	Function descriptions
28	f_{SC} VCO input (3.58 MHz)		f_{SC} VCO input pins. Connect a 3.58 MHz oscillation filter between pins 27 and 28 and a 4.43 MHz oscillation filter between pins 27 and 29. Switch of pin 28 input and pin 29 input is suppressed in response to pin 41 (f_{SC} switch) voltage.
29	f_{SC} VCO input (4.43 MHz)		
30	Chroma APC filter		Pin for connecting filter of chroma APC detector.

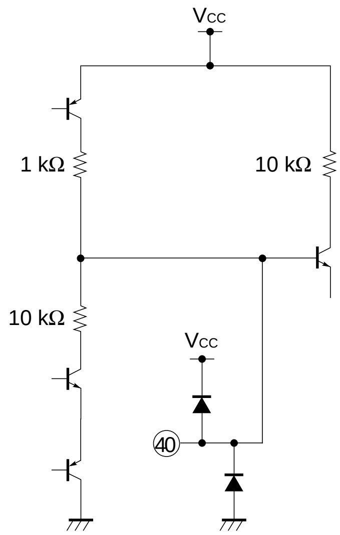
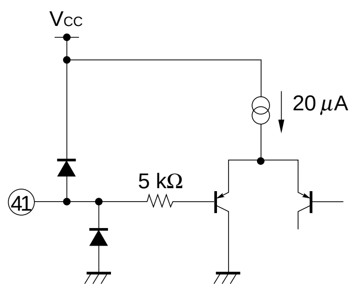
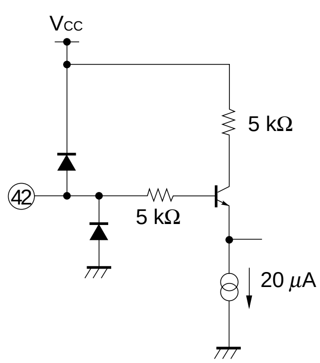
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Equivalent circuit</th><th>Function descriptions</th></tr>
<tr><td>31</td><td>fo adjustment filter</td><td>


</td><td>Pin for connecting filter of fo automatic adjustment loop.</td></tr>
<tr><td>32</td><td>ACC filter</td><td>


</td><td>Pin for connecting filter of ACC detector.</td></tr>
<tr><td>33</td><td>GND (chroma section)</td><td></td><td>Chroma section ground.</td></tr>
<tr><td>34</td><td>Separate chroma input</td><td>


</td><td>Separate chroma signal input pin. This pin also serves as a separate and composite switch input pin. If the pin voltage is set to 3.7 V or more, composite input mode is entered.</td></tr>
<tr><td>35</td><td>Power supply (chroma section)</td><td></td><td>Chroma section power supply.</td></tr>
</table>

Pin No.	Pin name	Equivalent circuit	Function descriptions
36	Composite video signal input		Composite video signal or separate Y signal input pin. This pin also serves as a clamp pin. Input the signal with C coupling. DC level is approx. 2.3 V.
37	Subcolor control		Decoder color and contrast adjustment pins.
38	Contrast control		
39	Sync. separation input		Input pin of sync. separation circuit.

Pin No.	Pin name	Equivalent circuit	Function descriptions
40	H sync. detect filter		Pin for connecting filter of H sync. detector.
41	fsc switch		Pin for controlling fsc VCO input (pins 28, 29) switch. When the pin voltage is 2.8 V or more, the mode changes to the 3.58 MHz mode; when 2.2 V or less, to the 4.43 MHz mode.
42	NTSC/PAL switch		Pin for controlling switch of NTSC and PAL modes of decoder and matrix. One of the following three combinations of decoder and matrix modes can be selected depending on the value of the pin 42 voltage V42: 1. When V42 = 0 V decoder = PAL matrix = PAL 2. When V42 = 2.5 V decoder = NTSC matrix = NTSC 3. When V42 = 5 V decoder = NTSC matrix = PAL

5. BLOCK OPERATION

5.1 Video Signal Processing Section

(1) Input signal

After coupling by a capacitor (0.22 μF), a 1 V_{p-p} composite video signal is input to the composite video signal input pin (pin 36).

(2) Clamp circuit

The clamp circuit controls the pedestal voltage level to be constant to make it a reference voltage for the post-stage signal processing.

(3) Chroma trap circuit

Eliminates the chroma signal (NTSC system: approximately 3.58 MHz, PAL system: approximately 4.43 MHz) from a composite video signal and extracts a brightness signal.

(4) Separate/composite switching circuit

Operates as shown in Table 5-1 according to the voltage of the separate chroma input pin (pin 34).

Table 5-1. Operation when Switching Separate/Composite Signals

Separate chroma input pin (pin 34) voltage	Mode	Brightness signal processing	ACC amp input
Less than 3.7 V	Y/C separate input	Without chroma trap	Input from separate chroma
3.7 V or higher	Composite video input	With chroma trap	Input from chroma BPF

(5) Delay circuit

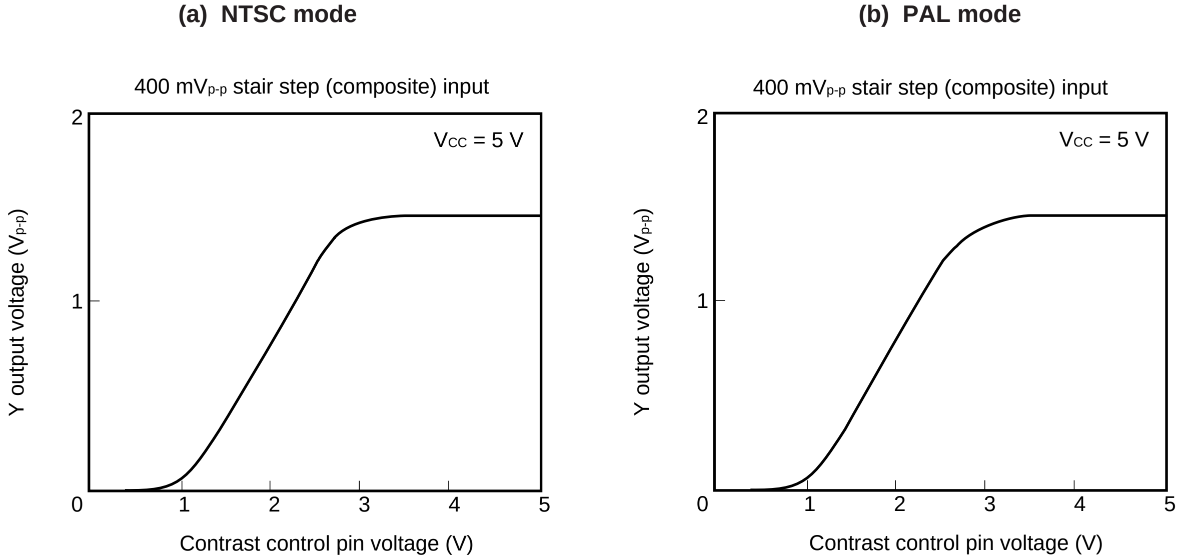
Compensates for the delay between the brightness signal and chroma signal by delaying the brightness signal.

(6) Contrast adjustment circuit

Adjusts the amplitude of the brightness signal output from the Y output pin (pin 12) according to the voltage of the contrast control pin (pin 38).

The control characteristic is shown in Figure 5-1.

Figure 5-1. Contrast Control Characteristic



5.2 Chroma Signal Processing Section

(1) Input signal

- **Composite video signal input**
  After coupling by a capacitor (0.22 μF), a 1 V_{p-p} composite video signal is input to the composite video signal input pin (pin 36).

- **Separate chroma signal input**
  After coupling by a capacitor (1000 pF), a chroma signal whose burst signal amplitude is 150 mV_{p-p} is input to the separate chroma input pin (pin 34).

(2) Chroma BPF circuit

Separates the chroma signal from a composite video signal.

(3) Separate/composite switching circuit

When the potential of the separate chroma input pin (pin 34) is 3.7 V or higher (in composite mode), switches the ACC amp input from the chroma input pin to the chroma BPF circuit output. Processing of the brightness signal at this time is switched so that it passes through the chroma trap circuit.
Operation when switching separate/composite signals is shown in Table 5-1.

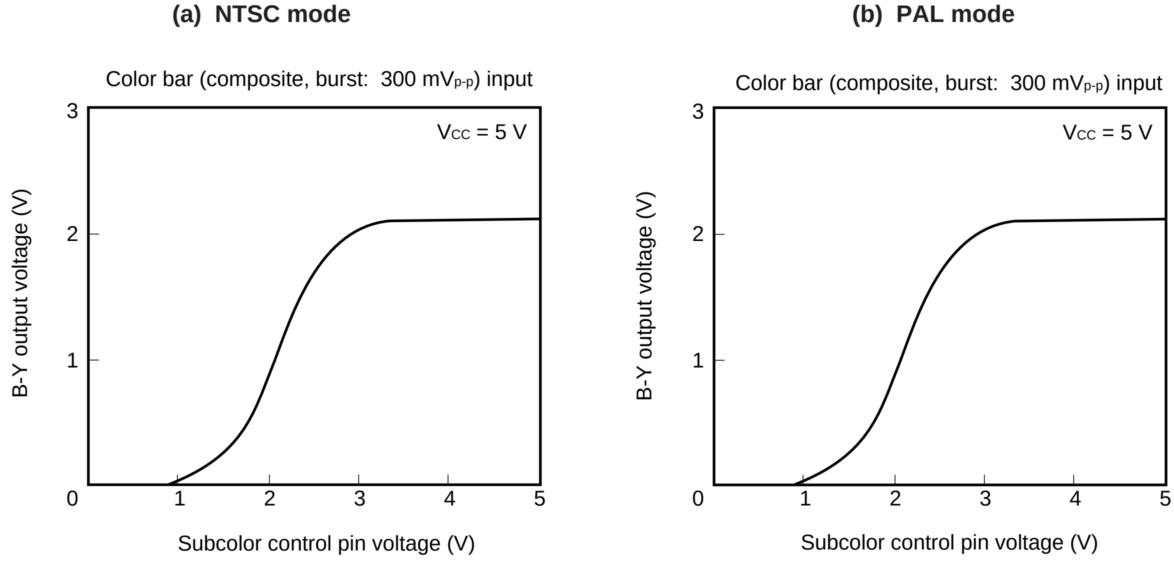
(4) ACC (Auto Color Control) amplification circuit

Extracts the burst signal, detects its level and smoothes the voltage of the ACC filter pin (pin 32) by an external capacitor.
This smoothed voltage controls color gain to keep the amplitude of the burst signal constant.

(5) Subcolor control circuit

According to the voltage of the subcolor control pin (pin 37), controls the amplitude of the chroma signal output from the ACC amplification circuit after separating the burst signal from it, and adjusts the amplitude of the color difference signal output from the R-Y output pin (pin 13) and B-Y output pin (pin 14). This controls color density on the screen. The control characteristic is shown in Figure 5-2.

Figure 5-2. Subcolor Control Characteristic



(6) Chroma APC (Auto Phase Control) circuit

Detects the phase difference between the burst signal extracted from the chroma signal and the signal from f_{SC}VCXO and smoothes the chroma APC filter pin (pin 30) using a capacitor. This smoothed voltage is used to control the f_{SC}VCXO oscillation frequency.

(7) Killer detection circuit

Detects the amplitude of the burst signal and executes a mute on the subcolor control circuit when there is no burst signal, preventing it from outputting a chroma signal to avoid color noise. In this case, the output of the color killer output pin (pin 8) is driven high.

The color killer sensitivity is determined by the time constant of a resistor and capacitor connected to the color killer filter pin (pin 26).

(8) IDENT detection circuit

Performs IDENT detection. With IDENT detection, if an NTSC signal (PAL signal in NTSC mode) is input in PAL mode, the color killer turns on and no chroma signal is output.

(9) 3.58 MHz/4.43 MHz VCXO, PAL SW circuit

Switches the f_{SC}VCO input pin between pin 28 (for 3.58 MHz) and pin 29 (for 4.43 MHz) by controlling the voltage of the f_{SC} switching pin (pin 41) (2.8 V or higher: 3.58 MHz mode, 2.2 V or below: 4.43 MHz mode) to perform f_{SC} oscillation at 3.58 MHz or 4.43 MHz. VCXO is controlled by the voltage of the chroma APC filter pin (pin 30) smoothed by the chroma APC circuit and its phase is synchronized with the input burst signal.

The PAL SW circuit inverts the phase of a signal on the R-Y demodulation axis every 1H by IDENT detection.

(10) R-Y, B-Y demodulation circuit

Performs demodulation using the chroma signal output from the ACC circuit, an R-Y demodulation axis signal and a B-Y demodulation axis signal output from f_{SC}VCXO, and multiplies R-Y by 1.4 and B-Y by 2.03.

5.3 Matrix Section

(1) Input signal

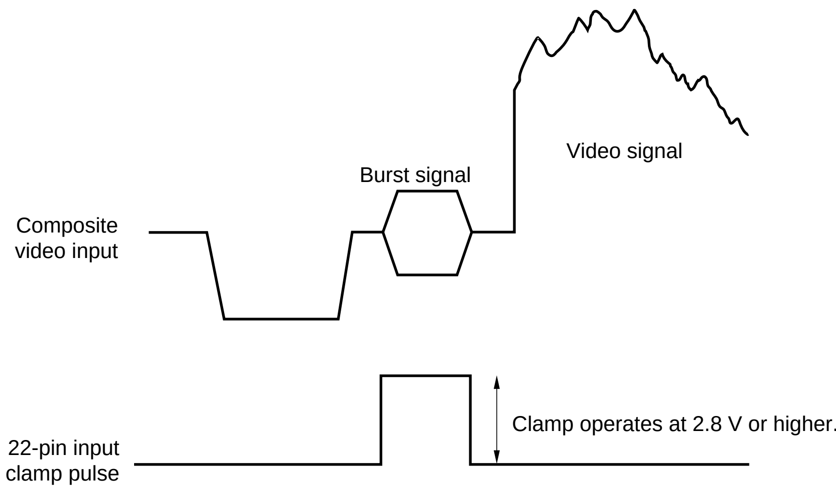
- **Brightness input signal**
  After coupling by a capacitor (0.22 μF), a brightness signal which has 1 V_{p-p} of video part is input to the Y input pin (pin 16).

- **Color difference input signal**
  After coupling by a capacitor (0.22 μF), 1 V_{p-p} R-Y and B-Y signals are input to the R-Y and B-Y input pins (pins 18 and 19).

(2) Y, R-Y and B-Y input clamp circuit

Clamps Y, R-Y and B-Y signals when the voltage of the clamp pulse input pin (pin 22) is 2.8 V or higher.
Input a clamp pulse to the clamp pulse input pin (pin 22) in synchronization with the burst section of an input signal as shown in Figure 5-3.
In the application circuit example, adjust the position of the clamp pulse by DELAY (μPD4538B external variable resistor: 10 kΩ) and the clamp pulse width by PD (μPD4538B external variable resistor: 10 kΩ).

Figure 5-3. 22-Pin Input Clamp Pulse Waveform



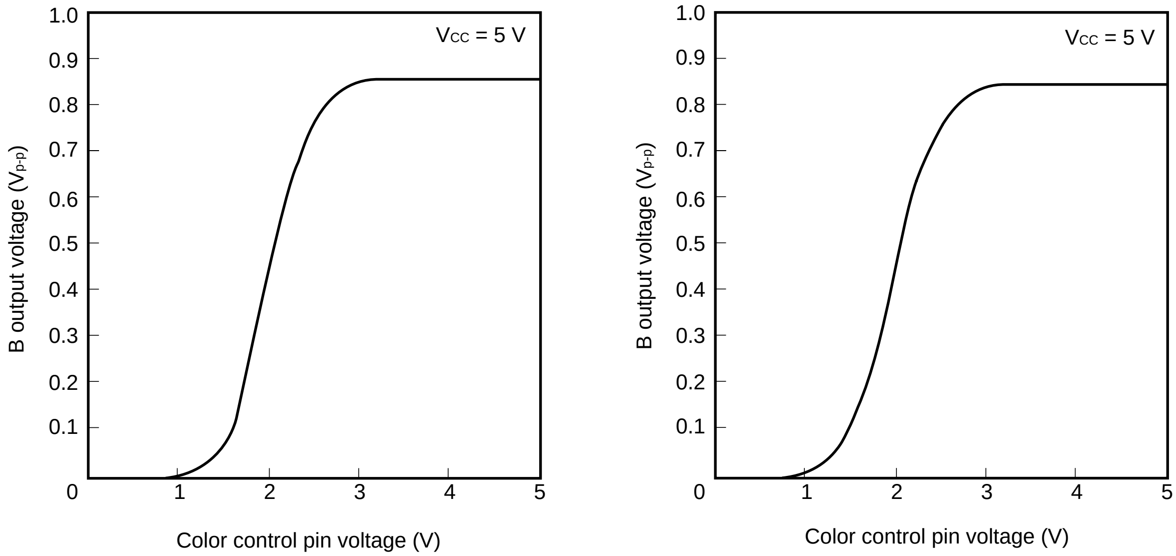
(3) Amplification color control circuit

Adjusts the amplitude of a color difference signal input to the R-Y input pin (pin 18) and B-Y input pin (pin 19) according to the voltage of the color control pin (pin 20). This controls the color density on the screen.
When using a matrix, adjust the color density mainly using this color control and fix the voltage of the subcolor control pin (pin 37) at 2 V (TYP.).
The control characteristic is shown in Figure 5-4.

Figure 5-4. Color Control Characteristic

(a) NTSC mode | **(b) PAL mode**

400 mV$_{p-p}$ stair step B-Y input
Tint control pin voltage: 2 V



(4) Tint control circuit

Controls the phase of a color difference signal whose amplitude is adjusted by the color control circuit, in a range of ±45° according to the voltage of the tint control pin (pin 21), and adjusts tint on the screen.

Table 5-2 shows the demodulation angle and demodulation ratio in each mode and Figure 5-5 shows the control characteristic.

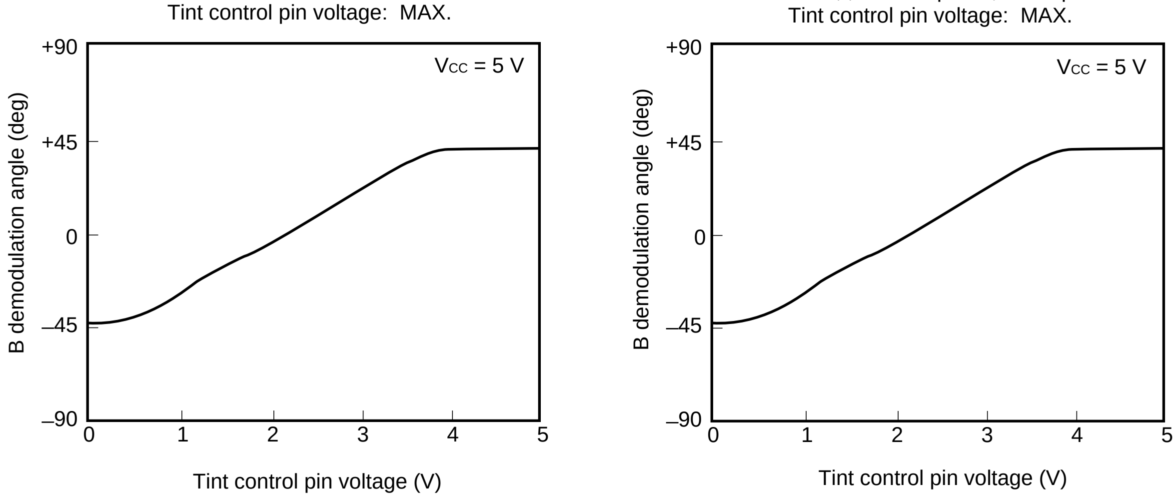
Table 5-2. Demodulation Angle and Demodulation Ratio when Tint Control Pin (Pin 21) Voltage = 2 V (TYP.)

Mode	Demodulation angle (∠R-Y)	Demodulation ratio (R-Y/B-Y)
NTSC	105° (TYP.)	0.75 (TYP.)
PAL	90° (TYP.)	0.61 (TYP.)

Figure 5-5. Tint Control Characteristic

(a) NTSC mode | **(b) PAL mode**

400 mV$_{p-p}$ stair step R-Y, B-Y input
Tint control pin voltage: MAX.



(5) G-Y demodulation circuit

Demodulates G-Y using (R-Y)', (B-Y)' which is color difference signal after tint adjustment and the following expression.

G-Y demodulation expression: (G-Y) = –0.51 × (R-Y)' – 0.19 × (B-Y)'

(6) RGB matrix circuit

Adds a brightness signal: Y to each of (R-Y)', (B-Y)' and G-Y to create R, G, and B signals.

5.4 Synchronizing Signal Processing Section

(1) Input signal

A composite video signal or brightness signal is input to the synchronizing separate input pin (pin 39) at 1 V_{P-P}.

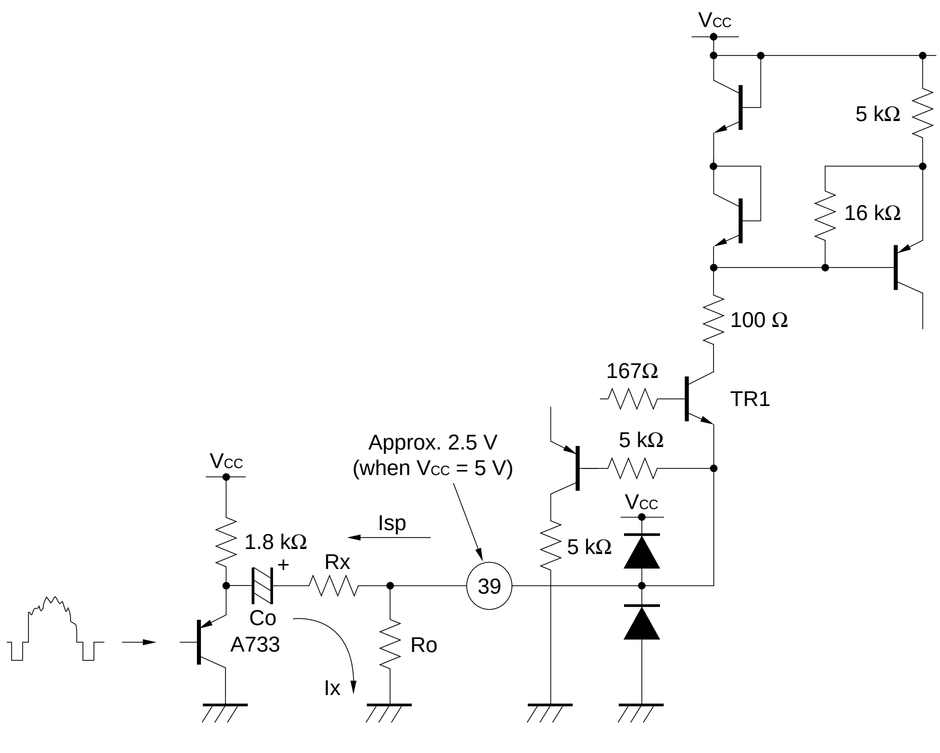
(2) Sync. separation circuit

Separates the sync. signal from a composite video signal. The slice level can be changed using an external resistor: R_X (see **Figure 5-6,** TYP. = 220 Ω).

The operation of the μPC1830 sync. separation circuit is explained below.

Figure 5-6 is an equivalent circuit diagram of the μPC1830 sync. separation circuit.

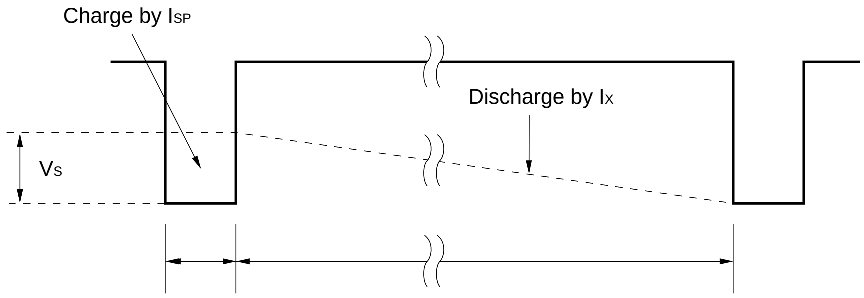
Figure 5-6. μPC1830 Sync. Separate Input Section Equivalent Circuit



In Figure 5-6, the slice level of sync. separation is determined as follows:

When a negative sync. video signal is input, charge current I_{SP} flows from the μPC1830 to C_O so that the synchronization peak (minimum potential) becomes approximately 2.5 V. The voltage of the sync. separate input pin (pin 39) becomes 2.5 V or higher during a period other than the synchronization peak (minimum potential), thus cutting off transistor TR1 (reducing the collector current of TR1). Consequently, a charge in C_O is discharged via R_O and R_X by current I_X during this cut-off period. Figure 5-7 illustrates this situation.

Figure 5-7. Sync. Separation Waveform



V_S in Figure 5-7 represents the slice voltage and can be expressed in the following expression if it is assumed that C_O is sufficiently large, and both I_X and I_{SP} are linear.

$V_S = 2.5 \times (R_X/R_O) \times (T2/T1)$ [V]

The μPC1830 amplifies the part lower than this slice voltage (V_S) to perform sync. separation.

To determine sync. separation sensitivity, change R_X to set V_S. Decreasing V_S is advantageous for separation of the horizontal sync. part, but disadvantageous for separation of the vertical sync. part. On the contrary, increasing V_S may cause a sync. failure (jitter) due to noise (spikes) of the horizontal sync. part. Therefore, it is necessary to optimize the constant in accordance with a signal input. As capacitance C_O, select a sufficiently large value compared with the charge/discharge current. However, an excessive value may deteriorate the excessive response characteristic, failing to catch up with drastic APL variations of the input signal.

The larger R_X, the larger the slice level becomes. However, with large R_X if the sync. signal level drops (weak electric field signal, etc.) a video signal may be confused with a sync. signal and sliced, making synchronization unstable (abnormal).

Caution Since the measuring circuit uses capacitor coupling for input for ease of measurement, it is susceptible to APL variations. Therefore, when configuring the actual circuit, use a Sync Tip clamp circuit in the stage prior to inputting to the emitter follower to stabilize the synchronization peak potential and this will make the circuit more resistant to APL variations.

(3) Vertical filter circuit

Separates the vertical sync. signal from the sync. signal separated by the sync. separation circuit.

(4) Horizontal sync. detection circuit

Detects the presence of a horizontal sync. signal and changes the AFC time constant.

(5) AFC detection circuit

Performs phase detection on an input sync. signal and f_H and outputs the phase difference in voltage.
Stops phase detection for 9H of the vertical blanking period.

(6) $32f_H$ VCO

Controls VCO according to the voltage output by the AFC detection circuit and generates $32f_H$ oscillation clocks.

(7) Horizontal/vertical counter circuit

- **Horizontal counter circuit**
  Divides a $32f_H$ signal to generate horizontal timing signals such as HD and BLK signals.

- **525/625 counter circuit**
  Performs counting at $4f_H$ and generates a vertical timing signal.
  Generates VD in 0.75H delay from the falling edge of a vertical sync. signal in an odd field and in 0.75H delay from the falling edge of a vertical sync. signal in an even field.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25 °C unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	7.0	V
Video input signal voltage	V_{IY}	V_{CC}	V
Chroma input signal voltage	V_{IC}	V_{CC}	V
Synchronous separation input signal voltage	V_{IS}	V_{CC}	V
Control signal voltage	V_{Icnt}	V_{CC}	V
★ Permissible package power dissipation	P_D	500 (on board, T_A = +75 °C)	mW
Operating ambient temperature	T_A	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this values when using the product.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}		4.5	5.0	5.5	V
Composite video input voltage	V_{YC}		—	1.0	—	V_{p-p}
Separate chroma input signal voltage	V_C		—	150	—	mV_{p-p}
Synchronous separation input signal voltage	V_S		—	1.0	—	V_{p-p}
Control signal voltage	V_{cont}		0	—	V_{CC}	V
Color difference input voltage	V_{R-Y} V_{B-Y}			1.0		V_{P-P}

ELECTRICAL SPECIFICATIONS (T_A = +25 ±3 °C, V_{CC} = +5 V unless otherwise specified)

VIDEO SIGNAL PROCESSING SECTION

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
Power supply current	I_{CC}	With no input signal	–	–	–	–	50	70	90	mA
Video voltage gain	$A_{V(comp)}$	Contrast = max.	Stair step ① (400 mV_{p-p})	Both	3.58/ 4.43	–	10.0	12.0	14.0	dB
Contrast variable range	e_{VC}	Max./min. contrast ratio	Stair step ① (400 mV_{p-p})	Both	3.58/ 4.43	–	30	–	–	dB
Video output DC voltage fluctuation when contrast is variable	ΔE_{OYC}	Output DC fluctuation, Contrast = max./min.	Sync. signal (300 mV_{p-p}) only	Both	3.58/ 4.43	–	–	0	±400	mV
Video frequency characteristics	f_{V1}	200 kHz/1.8 MHz gain difference, Contrast = max.	Sine wave ① (400 mV_{p-p})	Composite	4.43	–	–4	–2	0	dB
	f_{V2}				3.58	–	–5	–3	0	dB
	f_{V3}	200 kHz/5.5 MHz gain difference, Contrast = max.		Separate	4.43	–	0	+2	+4	dB
	f_{V4}				3.58	–	–1	+1	+3	dB
Video input DC voltage	E_{YI}	DC voltage of pin 36	Sync. signal (300 mV_{p-p}) only	Both	3.58/ 4.43	–	2.1	2.5	3.0	V
Video output DC voltage	E_{YO}	Scan period voltage of pin 12 Contrast = max.				–	1.7	2.0	2.4	V
Video output DC power supply voltage fluctuation	ΔE_{YOV}	E_{YO} change when V_{CC} changes from 4.5 to 5.5 V Contrast = max.	Sync. signal (300 m V_{p-p}) only	Both	3.58/ 4.43	–	–	0	±100	mV
Video output gain power supply voltage fluctuation	ΔA_{VV}	Video voltage gain change when V_{CC} changes from 4.5 to 5.5 V, Contrast = max.	Stair step ① (400 mV_{p-p})	–	–	–	–0.5	0.0	+0.5	dB
Trap attenuation amount	Δd_t	Gain difference of 200 kHz/3.58 MHz and 200 kHz/4.43 MHz Contrast = max.	Sine wave ① (400 mV_{p-p})	Composite	3.58/ 4.43	–	–20	–	–	dB

Remark For the input signal, see **Measuring Input Signal**.

CHROMA SECTION

(1/3)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
A_{CC} amplitude characteristics	A_{CC1}	B-Y output level fluctuation. With reference to burst 300 mV_{p-p}.	Color bar ② Burst 600 mV_{p-p}	Composite	4.43	–	–2.0	0.0	+2.0	dB
	A_{CC2}		Color bar ② Burst 30 mV_{p-p}	Composite	4.43	–	–7.0	–3.0	+1.0	dB
	A_{CC3}		Color bar ② Burst 600 mV_{p-p}	Composite	3.58	–	–2.0	0.0	+2.0	dB
	A_{CC4}		Color bar ② Burst 30 mV_{p-p}	Composite	3.58	–	–7.0	–3.0	+1.0	dB
	A_{CC5}	B-Y output level fluctuation. With reference to burst 300 mV_{p-p}.	Color bar ② Burst 300 mV_{p-p}	Separate	4.43	–	–2.0	0.0	+2.0	dB
	A_{CC6}		Color bar ② Burst 15 mV_{p-p}	Separate	4.43	–	–7.0	–3.0	+1.0	dB
	A_{CC7}		Color bar ② Burst 300 mV_{p-p}	Separate	3.58	–	–2.0	0.0	+2.0	dB
	A_{CC8}		Color bar ② Burst 15 mV_{p-p}	Separate	3.58	–	–7.0	–3.0	+1.0	dB
Color killer setting point	e_{KPC}	Level at which killer output goes high with burst signal 300 mV_{p-p} set to 0 dB.	Color bar ①	Composite	4.43	PAL	–48	–40	–32	dB
					3.58	NTSC	–48	–40	–32	dB
	e_{KPS}	Level at which killer output goes high with burst signal 150 mV_{p-p} set to 0 dB.	Color bar ①	Separate	4.43	PAL	–48	–40	–32	dB
					3.58	NTSC	–48	–40	–32	dB
Color killer color remainder	e_{OK}	B-Y output remaining level when killer output is high.	Color bar ①	–	–	–	0	–	50	mV_{p-p}
Color killer output, high	E_{CKH}	Color killer output level when color killer is ON, I_{OH} = –200 μA.	–	–	–	–	3.9	4.05		V
Color killer output, low	E_{CKL}	Color killer output level when color killer is OFF, I_{OL} = +200 μA.	–	–	–	–		0.5	0.6	V
Subcolor control variable range	e_{CC}	B-Y output level ratio of max./min. subcolor.	Color bar ①	Composite	4.43	–	30	45	–	dB
Subcolor control color remainder	e_{OC}	B-Y output remaining subcolor difference level, Color = min.	Color bar ①	Composite	4.43	–	0	–	50	mV_{p-p}
APC pull-in range	f_{SP}	APC pull-in frequency range when burst chroma frequency changes. (f_{sc} = reference)	Color bar ①	Composite	4.43	PAL	±400	±600	–	Hz
					3.58	NTSC	±400	±600	–	Hz
				Separate	4.43	PAL	±400	±600	–	Hz
					3.58	NTSC	±400	±600	–	Hz
VCO control sensitivity	β_S	Calculate from oscillation freq. when APC filter pin voltage is 2.3/2.7 V.	–	–	4.43	–	1.0	1.2	1.4	Hz/mV
					3.58	–	1.0	1.2	1.4	Hz/mV

Remark For the input signal, see **Measuring Input Signal**.

(2/3)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
VCO free-running frequency	f_S	VCO oscillator freq.	Sync. signal (300 mV_{p-p}) only	–	4.43	–	±400	–	–	Hz
					3.58	–	±400	–	–	Hz
PAL mode demodulation ratio	$\left(\frac{R-Y}{B-Y}\right)_{DP}$	R-Y/B-Y output ratio	Rainbow color bar (300 mV_{p-p})	Composite	4.43	PAL	0.9	1.0	1.1	Times
NTSC mode demodulation ratio	$\left(\frac{R-Y}{B-Y}\right)_{DN}$				3.58	NTSC	0.9	1.0	1.1	Times
PAL mode demodulation angle	$\angle R\text{-}Y_{DP}$	R-Y demodulation angle	Rainbow color bar (300 mV_{p-p})	Composite	4.43	PAL	85	90	95	deg
NTSC mode demodulation angle	$\angle R\text{-}Y_{DN}$				3.58	NTSC	85	90	95	deg
Maximum color difference output	e_{BYM}	Subcolor = max.	Rainbow color bar (300 mV_{p-p})	Composite	4.43	–	1.3	1.6	1.9	V_{p-p}
Color difference output remaining carrier level	e_{CAR}	R-Y, B-Y output remaining carrier level	–	–	3.58	NTSC	0	–	100	mV_{p-p}
Color difference output remaining harmonic level	e_{HAR}	Output remaining harmonic level, R-Y, B-Y = 1 V_{p-p}	Color bar ①	–	3.58	NTSC	0	–	100	mV_{p-p}
Color difference output frequency characteristics	f_{CP}	Δf = 50/500 kHz R-Y, B-Y output level ratio	Since wave ② (400 mV_{p-p})	Composite	4.43	PAL	–5	–3	0	dB
					3.58	NTSC				
	f_{CS}	Δf = 50 kHz/1 MHz R-Y, B-Y output level ratio		Separate	4.43	PAL	–5	–3	0	dB
					3.58	NTSC				
Blanking stage difference	e_{BLK}	Subcolor = max. R-Y/B-Y output blank period/scan period DC voltage difference	Burst (300 mV_{p-p}) only	–	4.43	PAL	–	0	20	mV
Line fluctuation	ΔE_{ORY}	Subcolor = max. Scan period DC voltage difference at every horizontal scanning period of R-Y output	Burst (300 mV_{p-p}) only	–	4.43	PAL	–	0	20	mV
Color difference output pin voltage	E_{ORY}	R-Y output DC voltage, With no signal	–	–	4.43	PAL	2.2	2.5	3.0	V
	E_{OBY}	B-Y output DC voltage, With no signal								
Color difference output pin voltage fluctuation with power supply fluctuation	ΔE_{ORYV}	E_{ORY} change when V_{CC} changes from 4.5 to 5.5 V	–	–	4.43	PAL		0	±100	mV
	ΔE_{OBYV}	E_{OBY} change when V_{CC} changes from 4.5 to 5.5 V						0	±100	mV

Remark For the input signal, see **Measuring Input Signal**.

(3/3)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
Separate chroma input pin voltage	E_{IC}	DC voltage of pin 34	–	Separate	–	–	1.2	1.5	1.8	V
Separate chroma input resistance	R_{IC}	Calculate from input when EIC → EIC + 2 V	–	Separate	–	–	26	35	44	kΩ
Separate/composite change threshold voltage	E_{ICTH}	Voltage of pin 34 at which separate/ composite mode is changed	–	–	3.58	NTSC	3.1	3.4	3.7	V

Remark For the input signal, see **Measuring Input Signal**.

SYNCHRONOUS SECTION

(1/2)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
Sync. separation input DC voltage	E_{IS}	Sync. separation input DC voltage at no signal	–	–	–	–	2.25	2.55	2.85	V
H sync. pull-in range	f_{HP}	Frequencies at which horizontal AFC can be pulled, H sync width = 4.8 μs	Sync. signal (300 mV_{p-p}) only	–	–	–	±400	–	–	Hz
Horizontal VCO control sensitivity	β_H	Calculated from HD output frequency change when horizontal AFC filter pin voltage changes from 2.9 to 3.4 V, With no signal	–	–	–	–	1.2	1.5	1.9	Hz/mV
Horizontal VCO free-running freq.	f_H	Difference for 15.680 kHz of HD output frequency, With no signal	–	–	–	–	–200	0	+200	Hz
Horizontal VCO free-running freq. fluctuation with power supply voltage fluctuation	Δf_{HV}	Change of f_H when V_{CC} changes from 4.5 to 5.5 V	–	–	–	–		0	±50	Hz
HD pulse output, high	E_{HDH}	I_{OH} = –200 μA	Sync. signal (300 mV_{p-p}) only	–	–	–	3.9	4.05	–	V
HD pulse output, low	E_{HDL}	I_{OL} = +200 μA	Sync. signal (300 mV_{p-p}) only	–	–	–	–	0.5	0.6	V
HD pulse output width	t_{WHD}	When HD pulse rising, falling is 2.5 V	Sync. signal (300 mV_{p-p}) only	–	–	–	3.9	4.4	4.9	μs
Blanking pulse output, high	E_{BLH}	I_{OH} = –200 μA	Sync. signal (300 mV_{p-p}) only	–	–	–	3.9	4.05	–	V
Blanking pulse output, low	E_{BLL}	I_{OL} = +200 μA	Sync. signal (300 mV_{p-p}) only	–	–	–	–	0.5	0.6	V
Blanking pulse output, width	t_{WBL}	When blanking pulse rising, falling is 2.5 V	Sync. signal (300 mV_{p-p}) only	–	–	–	9.9	10.4	10.9	μs
Vertical free-running frequency (in 50-Hz mode)	f_{V1}	H sync. detect filter pin voltage = 0 V	Sync. separate input of 3.5 V	–	–	–	–	f_H/368	–	Hz
	f_{V2}	H sync. detect filter pin voltage = 5 V		–	–	–	–	f_H/352	–	Hz
	f_{V3}	H sync. detect filter pin voltage = 0 V	Sync. separate input of –1 mA	–	–	–	–	f_H/272	–	Hz
	f_{V4}	H sync. detect filter pin voltage = 5 V		–	–	–	–	f_H/288	–	Hz

Remark For the input signal, see **Measuring Input Signal**.

(2/2)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
Vertical free-running frequency (in 60-Hz mode)	f_{V5}	H sync. detect filter pin voltage = 0 V	Sync. separate input of 3.5 V	–	–	–	–	f_H/296	–	Hz
	f_{V6}	H sync. detect filter pin voltage = 5 V		–	–	–	–	f_H/288	–	Hz
	f_{V7}	H sync. detect filter pin voltage = 0 V	Sync. separate input of –1 mA	–	–	–	–	f_H/232	–	Hz
	f_{V8}	H sync. detect filter pin voltage = 5 V		–	–	–	–	f_H/240	–	Hz
VD pulse output, high	E_{VDH}	I_{OH} = –200 μA	Sync. signal of 300 mV_{p-p}	–	–	–	3.9	4.05	–	V
VD pulse output, low	E_{VDL}	I_{OL} = +200 μA		–	–	–	–	0.5	0.6	V
Even field VD pulse output width	t_{WVDE}		Sync. signal of 300 mV_{p-p}	–	–	–	–	5.5	–	H
Odd field VD pulse output width	t_{WVDO}			–	–	–	–	6.0	–	H

Remark For the input signal, see **Measuring Input Signal**.

MODE CONTROL SECTION

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
NTSC/PAL mode switch threshold voltage	E_{PN1}	Voltage of pin 42 at which both decoder and matrix changes to NTSC or PAL mode simultaneously.	–	–	–	–	1.37	1.67	1.97	V
	E_{PN2}	Voltage of pin 42 at which only matrix changes to NTSC or PAL mode and decoder remains in NTSC mode.	–	–	–	–	3.03	3.33	3.63	V
NTSC/PAL mode switch input pin current	I_{IPN}	Input current of pin 42.	–	–	–	–	–0.5	+0.2	+2.0	μA
Subcarrier frequency switch threshold voltage	E_{SC}	Voltage of pin 41 at which f_{SC} 3.58/4.43 mode is changed.	–	–	–	–	2.2	2.5	2.8	V
Subcarrier frequency switch input pin current	I_{ISC}	Input current of pin 41.	–	–	–	–	–2.0	–0.2	+0.5	μA
Vertical frequency switch threshold voltage	E_{FV}	Voltage of pin 6 at which f_V 50/60 mode is changed.	–	–	–	–	2.2	2.5	2.8	V
Vertical frequency switch input pin current	I_{IFV}	Input current of pin 6.	–	–	–	–	–2.0	–0.2	+0.5	μA

NTSC/PAL MODE SETTING

SW setting of pin 42	Voltage of pin 42	Decoder mode	Matrix mode
Mode 1	Lower than E_{PN1}	PAL	PAL
Mode 2	Between E_{PN1} and E_{PN2}	NTSC	NTSC
Mode 3	Higher than E_{PN2}	NTSC	PAL

VERTICAL FREQUENCY (f_V) SWITCHING

Voltage of pin 6	Vertical frequency fv
Lower than E_{FV}	50 Hz
Higher than E_{FV}	60 Hz

SUBCARRIER FREQUENCY (f_{SC}) SWITCHING

Voltage of pin 41	Subcarrier frequency f_{SC}
Lower than E_{SC}	4.43 MHz
Higher than E_{SC}	3.58 MHz

MATRIX SECTION

(1/2)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
Original color output Y voltage gain	A_Y	B output voltage gain.	Y:stair step ② (1 V_{p-p})	–	–	–	–2.0	0.0	+2.0	dB
Y voltage gain RGB output mutual difference	ΔA_{YRGB}	Mutual difference of R, G, and B output voltage gains.	Y:stair step ② (1 V_{p-p})	–	–	–	–1.0	0.0	+1.0	dB
Y voltage gain fluctuation with power supply voltage fluctuation	ΔA_{YV}	Difference between B output voltage gain and A_Y under the same conditions as A_Y except that V_{CC} = 4.5 V, 5.5 V.	Y:stair step ② (1 V_{p-p})	–	–	–	–0.5	0.0	+0.5	dB
Y frequency characteristics	f_Y	200 kHz/6 MHz B output gain difference.	Sine wave ④ (1 V_{p-p})	–	–	–	0	–3	–5	dB
B output color difference voltage gain	A_B	B output voltage gain. Tint control voltage 2.0 V, Color = max.	B-Y: stair step ① (400 mV_{p-p})	–	–	–	4.0	6.0	8.0	dB
Color control variable range	e_{CM}	Difference between B output gain and A_B. Tint control voltage 2.0 V, Color = min.	B-Y: stair step ① (400 mV_{p-p})	–	–	–	35	45	–	dB
Color control color remainder	e_{OCM}	B output remaining color difference level. Tint control voltage 2.0 V, Color = min.	B-Y: stair step ① (400 mV_{p-p})	–	–	–	0	5	50	mV_{p-p}
Color difference voltage gain fluctuation with power supply voltage fluctuation	ΔA_{BV}	Difference between each B output voltage gain and A_B under the same condition as A_B except that V_{CC} is changed from 4.5 to 5.5 V	B-Y: stair step ① (400 mV_{p-p})	–	–	–	–0.5	0.0	+0.5	dB
Color difference freq. characteristics	f_B	B output gain difference when freq. changes from 200 kHz to 6 MHz. Tint control voltage 2.0 V, Color = max.	B-Y: sine wave ③ (400 mV_{p-p})	–	–	–	0	–3	–5	dB
Tint control variable range	$e_{TMAX.}$	See **Note**. Color = max.	Stair step ① (400 mV_{p-p})	–	–	PAL/ NTSC	+35	–	–	deg
	$e_{TMIN.}$						–	–	–35	deg

Note B demodulation angle ϕ_B is obtained from B output signal voltages using the following expressions:

$$\text{B demodulation angle } \phi_B = \tan^{-1}\frac{B_1}{B_2}$$

Where, B_1: B output signal voltage when signal is input only to R-Y
B_2: B output signal voltage when signal is input only to B-Y,

e_{TMAX}. and e_{TMIN}. are obtained from the ϕ_B values using the following expressions:

$e_{TMAX.} = \phi_{B(4)} - \phi_{B(2)}$, $e_{TMIN.} = \phi_{B(2)} - \phi_{B(10)}$

Where, $\phi_{B(0)}$, $\phi_{B(2)}$, $\phi_{B(4)}$: ϕ_B values when tint control voltage is 0, 2, 4 V, respectively.

Remark For the input signal, see **Measuring Input Signal**.

(2/2)

Parameter	Symbol	Conditions	Input signal	Composite /Separate	f_{SC} (MHz)	PAL or NTSC	MIN.	TYP.	MAX.	Unit
PAL mode demodulation ratio	$\left(\frac{R-Y}{B-Y}\right)_P$	Tint control = 2 V, Color = max. See **Note1**.	Stair step ① (400 mV_{p-p})	–	–	PAL	0.50	0.56	0.62	Times
	$\left(\frac{G-Y}{B-Y}\right)_P$						0.31	0.35	0.39	Times
PAL mode demodulation angle	$\angle R\text{-}Y_{MP}$						85	90	95	deg
	$\angle G\text{-}Y_{MP}$						228	237	246	deg
NTSC mode demodulation ratio	$\left(\frac{R-Y}{B-Y}\right)_{MN}$					NTSC	0.69	0.75	0.83	Times
	$\left(\frac{G-Y}{B-Y}\right)_{MN}$						0.22	0.25	0.28	Times
NTSC mode demodulation angle	$\angle R\text{-}Y_{MN}$						100	105	110	deg
	$\angle G\text{-}Y_{MN}$						238	247	256	deg
Clamp pulse input threshold voltage	E_{CLP}	**Note 2**	–	–	–	–	2.1	2.5	2.9	V
R-Y input pin voltage	E_{RYI}		–	–	–	–	2.1	2.5	2.9	V
B-Y input pin voltage	E_{BYI}		–	–	–	–	2.1	2.5	2.9	V
R output pin voltage	E_{RO}		–	–	–	–	1.6	2.0	2.4	V
G output pin voltage	E_{GO}		–	–	–	–	1.6	2.0	2.4	V
B output pin voltage	E_{BO}		–	–	–	–	1.6	2.0	2.4	V
DC difference voltage between R, G, B outputs	$\Delta E_{X\text{-}Y}$	Maximum value of difference voltages between E_{RO}, E_{GO}, and E_{BO}	–	–	–	–			300	mV
RGB output DC fluctuation in color control mode	ΔE_{RGBC}	Maximum value of E_{RO}, E_{GO}, E_{BO} fluctuation Color control = max./min. Tint control = 2.0 V	–	–	–	–	–	0	±300	mV
RGB output DC fluctuation in tint control mode	ΔE_{RGBT}	Maximum value of E_{RO}, E_{GO}, E_{BO} fluctuation Tint control = max./typ./min. Color control = max.	–	–	–	–	–	0	±300	mV
Y input DC fluctuation in color control mode	ΔE_{YIC}	Color control = max./min. Tint control = 2.0 V	–	–	–	–	–	0	±300	mV
Y input DC fluctuation in tint control mode	ΔE_{YIT}	Tint control = max./typ./min. Color control = max.	–	–	–	–	–	0	±300	mV
Y input pin voltage	E_{YI}		–	–	–	–	1.6	2.0	2.4	V

Notes 1. From R, G and B output voltages R1, G1 and B1 when signal is input only to R-Y and R, G, and B output voltages R2, G2 and B2 when signal is input only to B-Y, R, G, B demodulation ratio and demodulation angles are obtained by the following expressions:

$$\left(\frac{R-Y}{B-Y}\right) = \sqrt{\frac{R_1^2 + R_2^2}{B_1^2 + B_2^2}}\ ,\quad \left(\frac{G-Y}{B-Y}\right) = \sqrt{\frac{G_1^2 + G_2^2}{B_1^2 + B_2^2}}$$

$$\angle R - Y = -\tan^{-1}\frac{R_2}{R_1} - \tan^{-1}\frac{B_1}{B_2} + 90°$$

$$\angle G - Y = -\tan^{-1}\frac{G_1 - \sqrt{3}G_2}{\sqrt{3}G_1 + G_2} - \tan^{-1}\frac{B_1}{B_2} + 240°$$

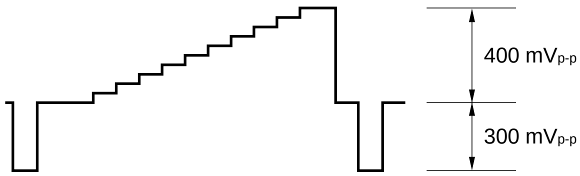
2. Clamp pulse input voltage which gets 80 μA or more at Y input pin voltage = V_{CC}.

Remark For the input signal, see **Measuring Input Signal**.

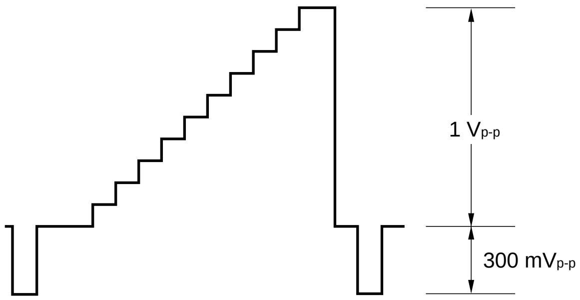
Measuring Input Signal

- **Stair step**

① 400 mV$_{p-p}$



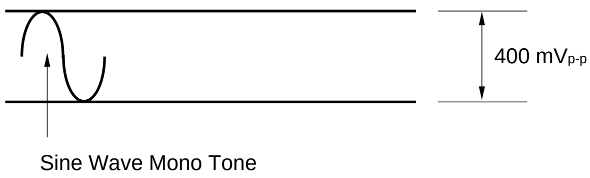
② 1 V$_{p-p}$



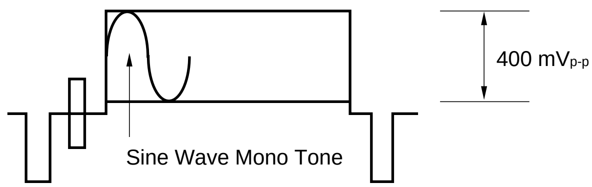
- **Sync. signal (300 mV$_{p-p}$) only**

- **Sine wave**

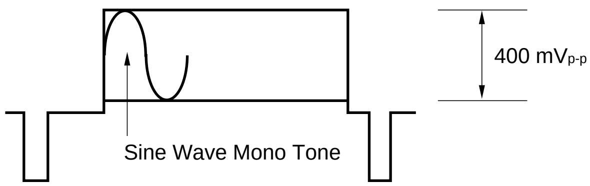
① 400 mV$_{p-p}$



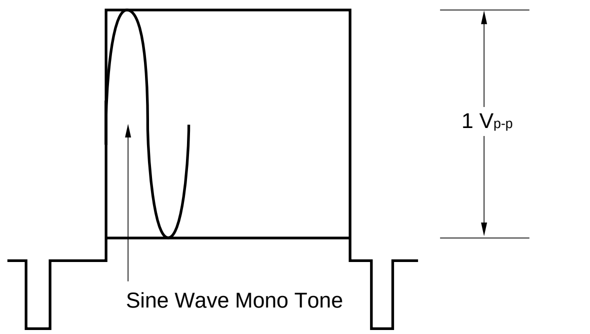
② 400 mV$_{p-p}$



③ 400 mV$_{p-p}$

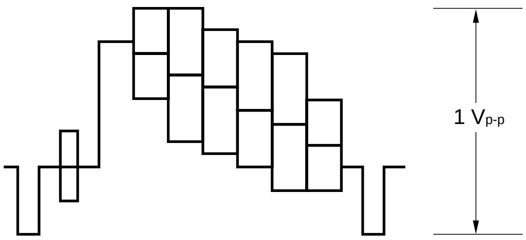


④ 1 V$_{p-p}$

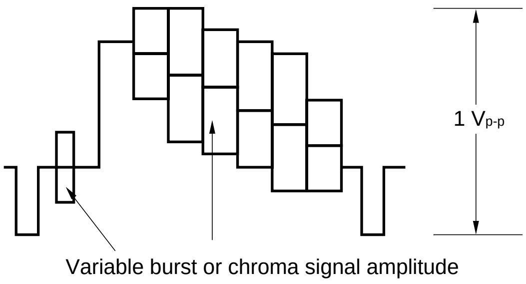


- **Color bar**

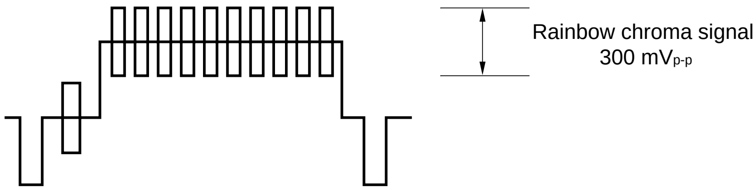
①



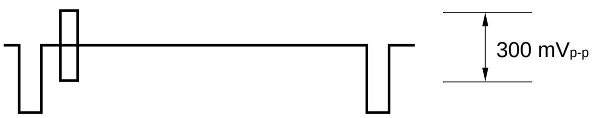
② **Variable burst or chroma signal amplitude**



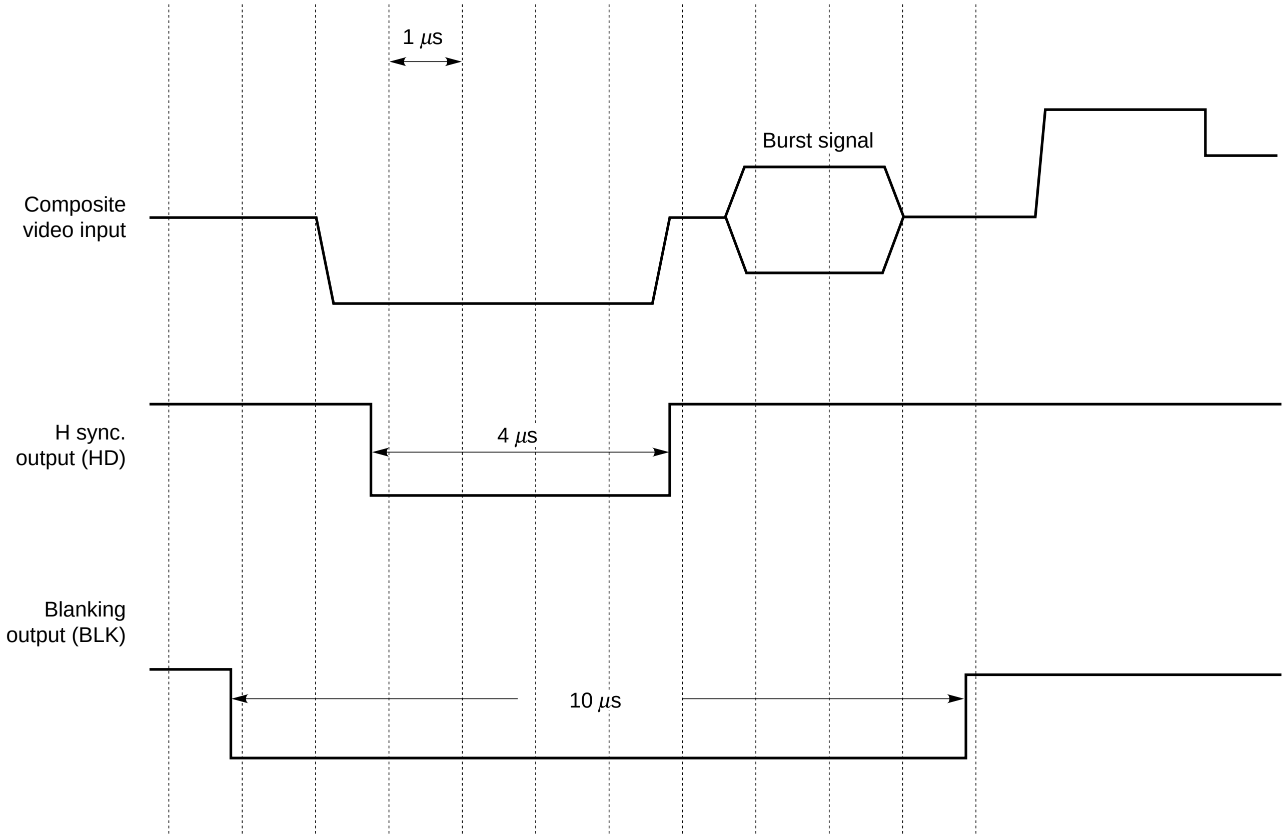
- **Rainbow color bar (300 mV$_{p-p}$)**



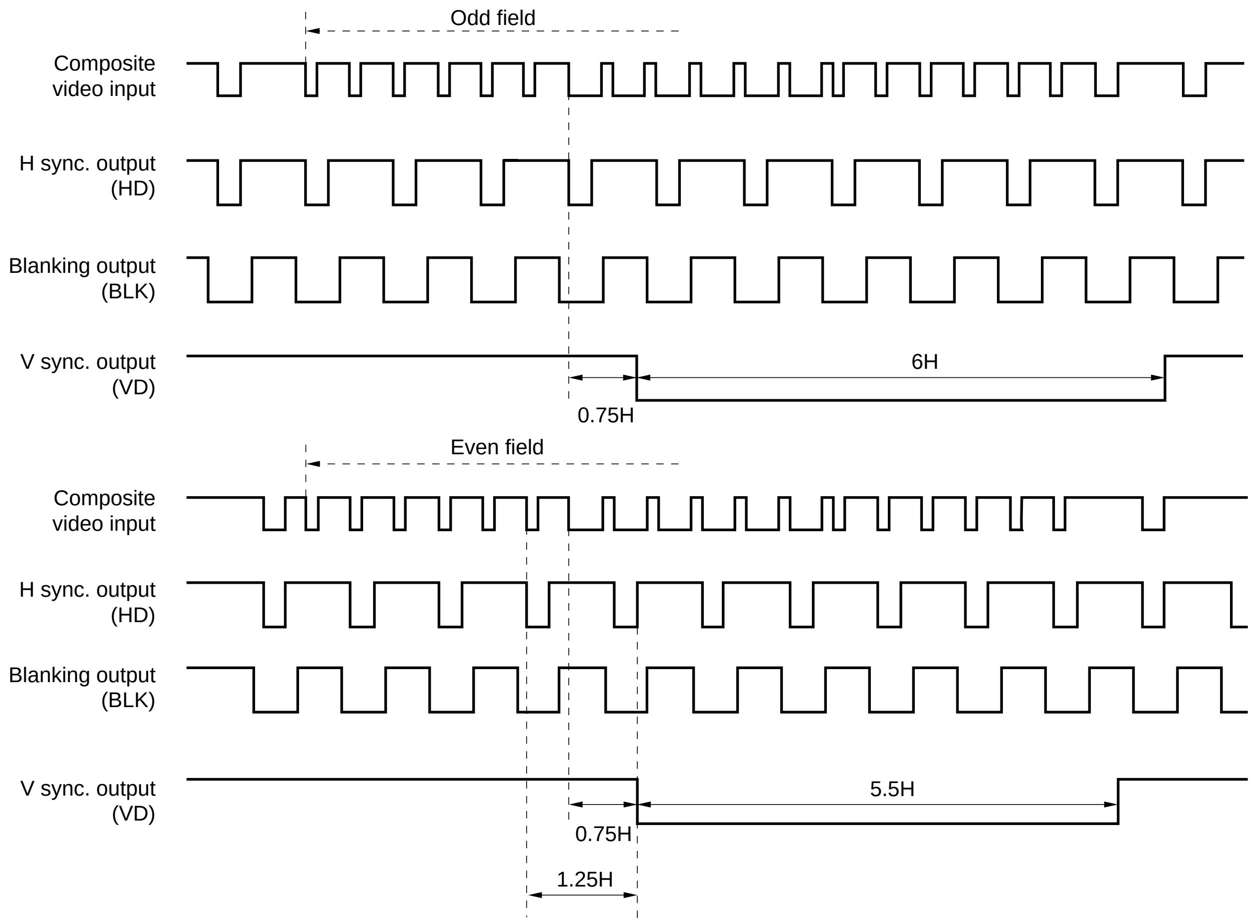
- **Burst (300 mV$_{p-p}$) only**



Timing chart (horizontal period)



Timing chart (vertical period/standard signal input)

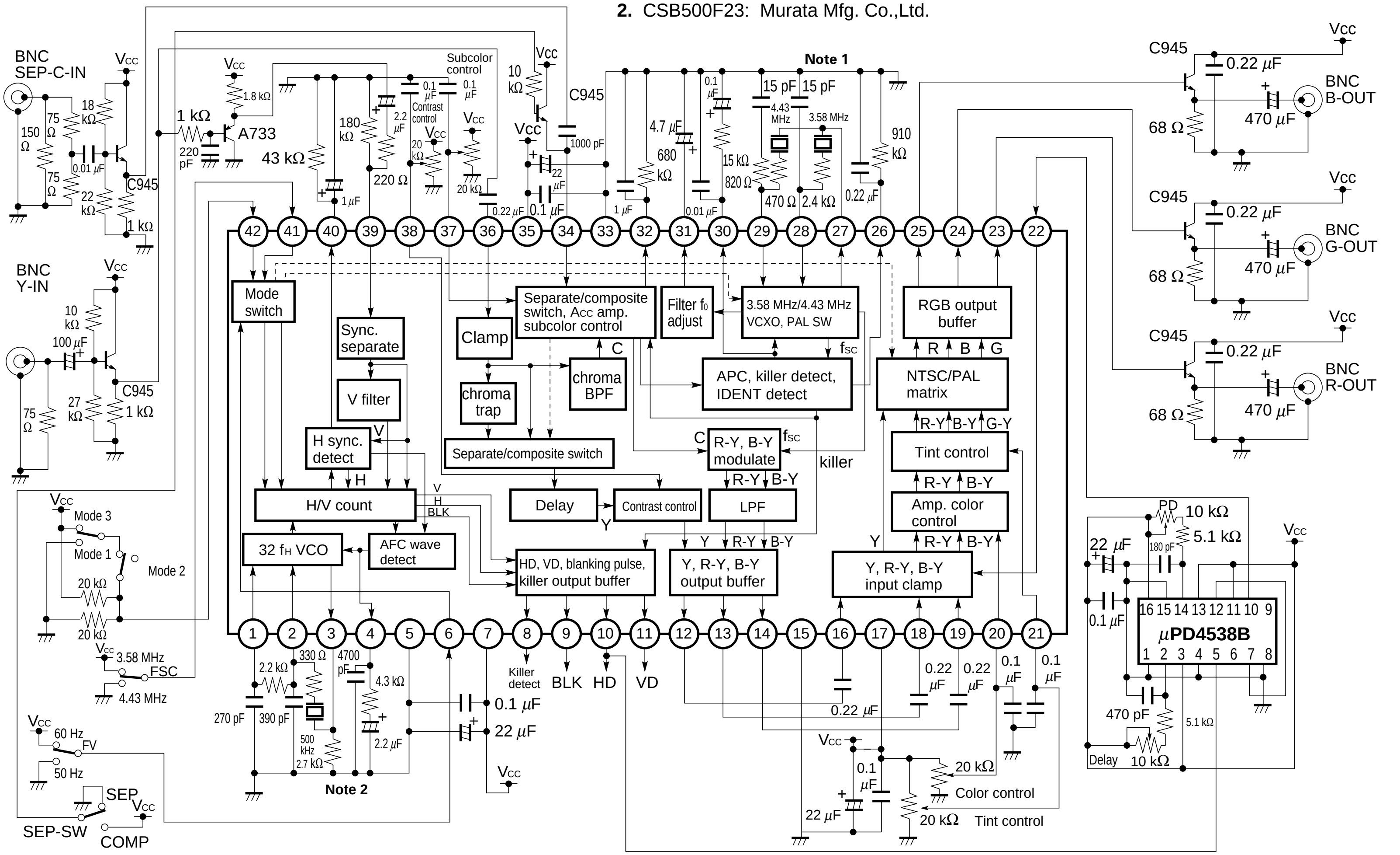


Remark H represents horizontal scanning period.

7. APPLICATION CIRCUIT EXAMPLE

Example 1

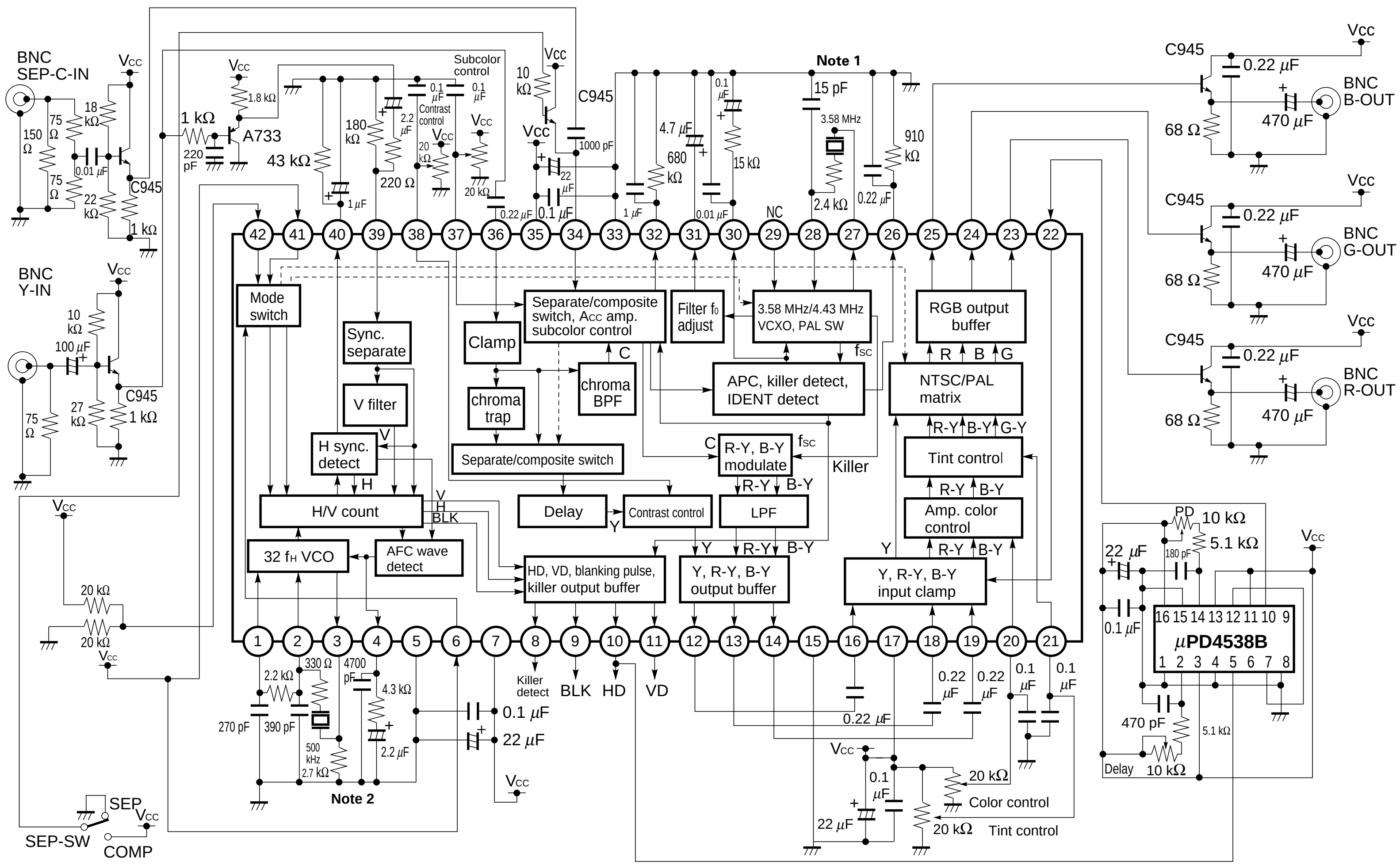
Notes 1. Crystal resonator for load of 16 pF.
4.433 619 MHz (PAL) : DAISHINKU CORP. (Type: HC-49/U)
3.579 545 MHz (NTSC) : Toyo Communication Equipment Co., Ltd. (Type: TQC203A-8R)
2. CSB500F23: Murata Mfg. Co.,Ltd.



Example 2 (for NTSC limited use)

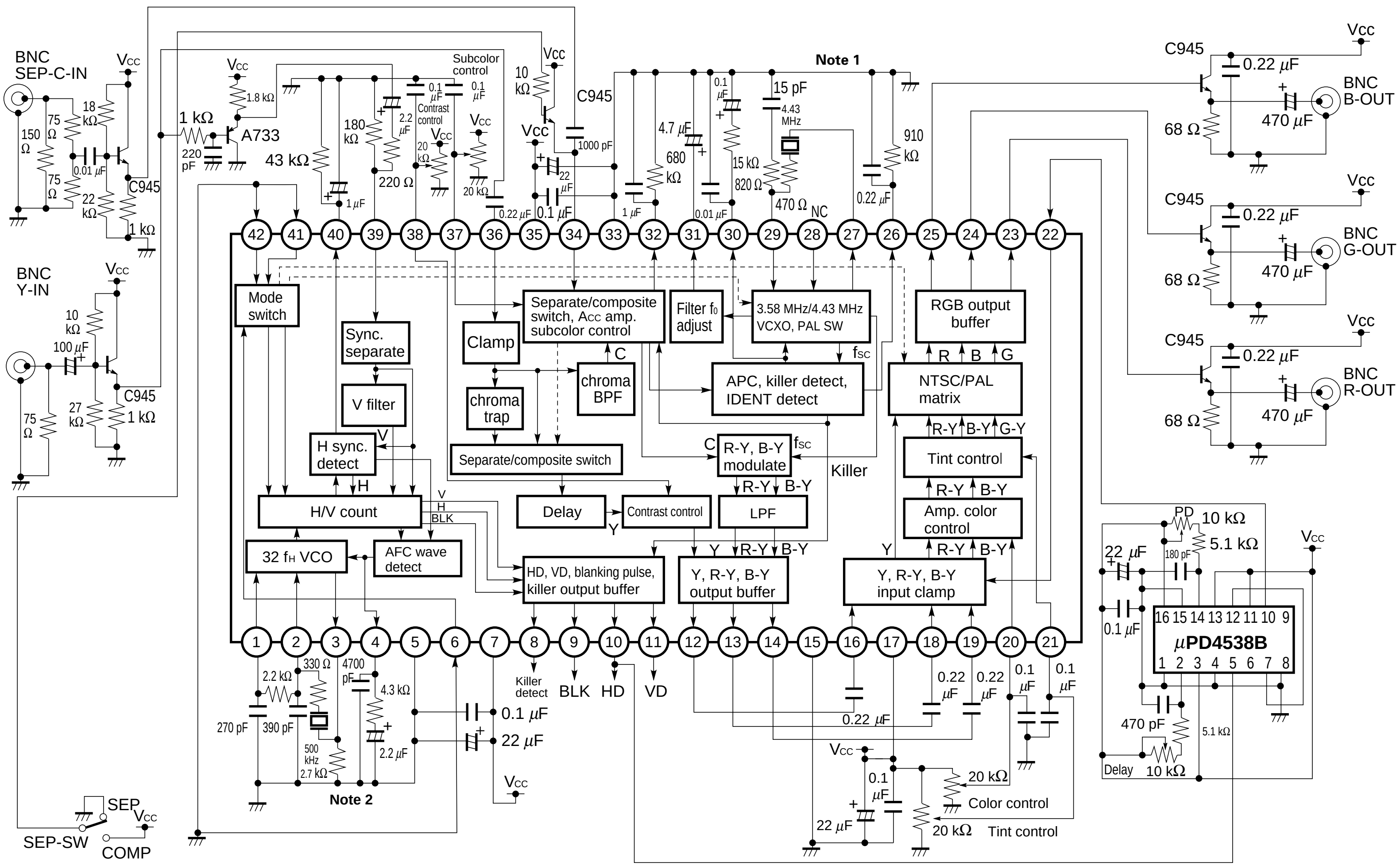
Notes 1. Crystal resonator for load of 16 pF.
3.579 545 MHz (NTSC) : Toyo Communication Equipment Co., Ltd. (Type: TQC203A-8R)

2. CSB500F23: Murata Mfg. Co.,Ltd.



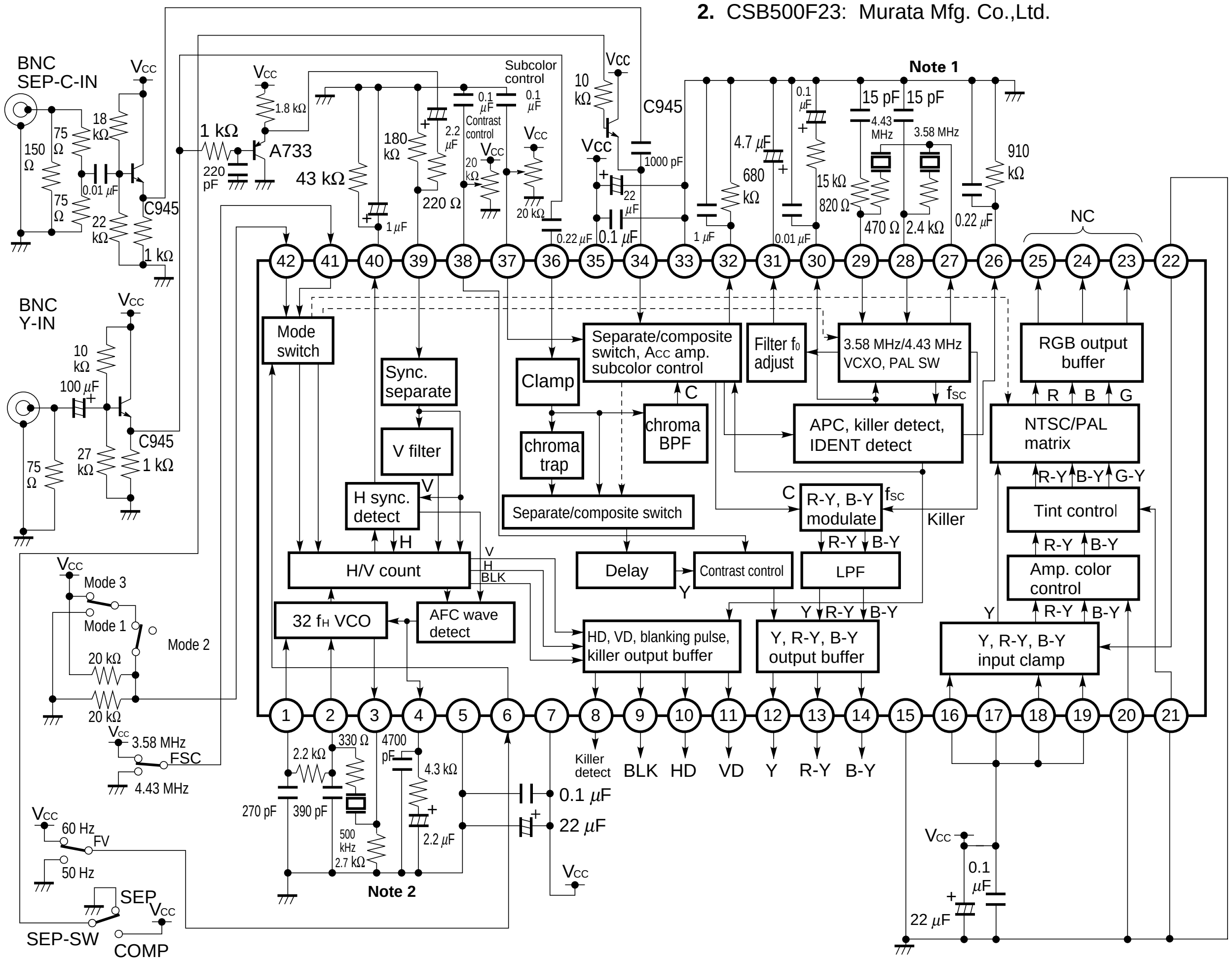
Notes 1. Crystal resonator for load of 16 pF.
4.433 619 MHz (PAL) : DAISHINKU CORP. (Type: HC-49/U)

2. CSB500F23: Murata Mfg. Co.,Ltd.



Example 4 (When RGB matrix section not used)

Notes 1. Crystal resonator for load of 16 pF.
4.433 619 MHz (PAL) : DAISHINKU CORP. (Type: HC-49/U)
3.579 545 MHz (NTSC) : Toyo Communication Equipment Co., Ltd. (Type: TQC203A-8R)
2. CSB500F23: Murata Mfg. Co.,Ltd.



8. OPERATING PRECAUTIONS

8.1 μPC1830 External Components

(1) Resistors

Use E24 series resistors (approximately 5% precision) of 1/4 W or higher.

(2) Capacitors

- **Ceramic capacitors of 1000 pF or below**
  Capacitors used for the time constant circuit. Basically use E12 series (10% precision) ones with the center value = 0 in nominal temperature characteristic.

- **Ceramic capacitors of 1000 pF or higher**
  Equivalent to capacitors for non-critical time constant circuits and for clamp, and bypass capacitors between power supply and GND. Use E12 series (10% precision) ones. Use a type whose capacitance is not extremely affected by temperature variations (ie. with an excellent temperature characteristic).

- **Electrolytic capacitors**
  Use E6 series (20% precision) ones. Use ones whose capacitance is not extremely affected by temperature variations (ie. with an excellent temperature characteristic).

(3) Crystal resonators

Use crystal resonators of 16 pF load type as shown below.

- For PAL : 4.433 619 MHz (model name: HC-49/U, manufactured by Kinseki, Ltd.)
- For NTSC : 3.579 545 MHz (model name: TQC203A-8R (HC-49/U-10 type), manufactured by Toyo Communication Equipment Co., Ltd.)

Note that use of crystal resonators other than the above may deteriorate electrical characteristics.

(4) Ceramic resonators

Use ceramic resonators as shown below.

- CSB500 F23 (manufactured by Murata Mfg. Co., Ltd.)

Note that use of ceramic resonators other than the above may deteriorate mainly electrical characteristics of the sync. section.

8.2 μPC1830 Pattern Wiring

(1) GND line

Solid grounding should be applied to three GNDs: synchronous section GND (pin 5), video section GND (pin 15) and chroma section GND (pin 33). They should not be connected to other digital GNDs except the one point of origin. Use thick connection (thick through hole) for each GND pin of the IC.

When an emitter follower circuit, amplifier, etc. is connected to the color difference output stage or RGB output stage, separate the solid ground of the output stage from that of the IC output stage.

(2) Power supply line

The three analog power supplies, synchronous section power supply (pin 7), video section power supply (pin 17) and chroma section power supply (pin 35) should be independent of each other and unified at the supply source. Ensure that there is no unnecessary routing.

Separate the digital section power supply from the analog section power supply and connect them only at one point.

(3) Signal line

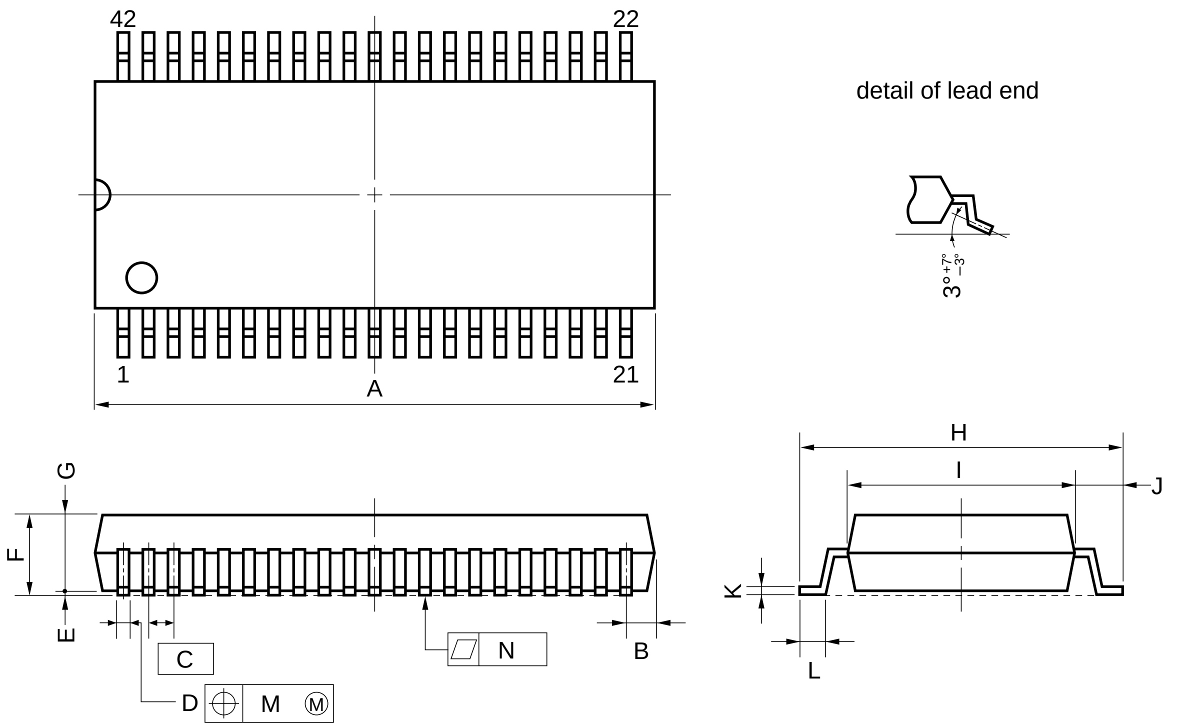
In order to avoid signal cross talk, ensure that the color difference signal line (pins 12, 13, and 14) and RGB signal line (pins 23, 24, and 25) are not placed close to or in parallel with the digital signal line or HD (pin 10), VD (pin 11) and BLK (pin 9) lines, or cross those lines.

(4) Placement of peripheral components of each pin

Place components which are connected with pins 1, 2, 5, 7, 15, 16, 17, 18, 19, 23, 24, 25, 28, 29, 33, 34, and 35 close to the IC. When the placed components are connected to the power supply line or other lines, route low-impedance lines and make sure that the thickest possible lines are used for connection with the IC pins.

9. PACKAGE DRAWING

42 PIN PLASTIC SHRINK SOP (375 mil)



S42GT-80-375B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.16 MAX.	0.715 MAX.
B	1.13 MAX.	0.044 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.5±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.15±0.2	$0.281^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.10	0.004
N	0.10	0.004

10. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface Mount Device

μPC1830GT: 42-pin plastic shrink SOP (375 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
Vapor phase soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

[MEMO]

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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