VNQ500PEP-E

QUAD CHANNEL HIGH SIDE DRIVER

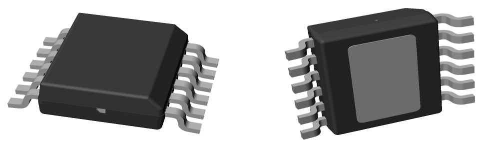
TARGET SPECIFICATION

Table 1. General Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ500PEP-E	500 mΩ	0.4 A	36V

- CMOS COMPATIBLE I/O's
- CHIP ENABLE
- JUNCTION OVERTEMPERATURE PROTECTION AND DIAGNOSTIC
- CURRENT LIMITATION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



PowerSSO-12

DESCRIPTION

The VNQ500PEP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active current limitation combined with latched thermal shutdown, protect the device against overload.

In case of overtemperature of one channel the relative I/O pin is pulled down.

Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-12	VNQ500PEP-E	VNQ500PEPTR-E

This is preliminary information on a new product foreseen to be developed. Details are subject to change without notice.

Figure 2. Block Diagram

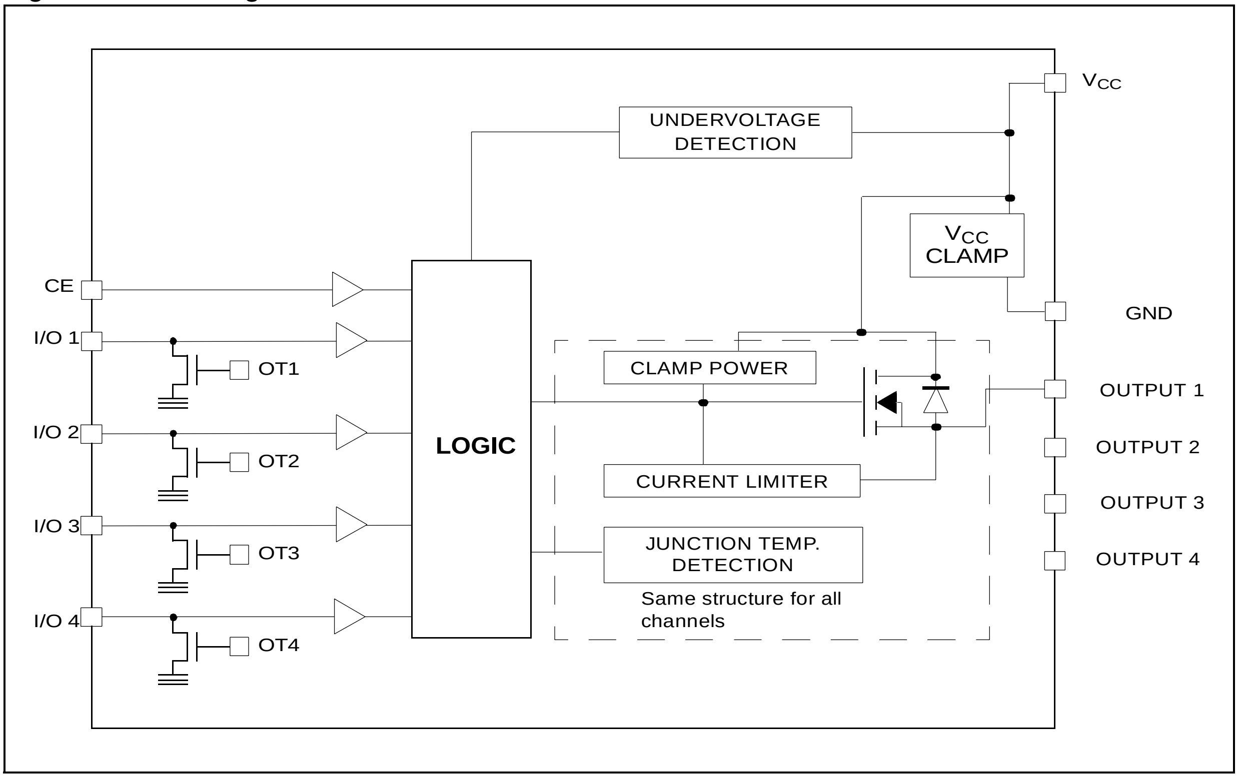


Table 3. Pin Definitions And Functions

Pin No	Symbol	Function
TAB	V_{CC}	Positive power supply voltage
7,12	V_{CC}	Positive power supply voltage
1	GND	Logic ground
2	CE	Chip Enable
3	I/O 1	Input/Output of channel 1
4	I/O 2	Input/Output of channel 2
5	I/O 3	Input/Output of channel 3
6	I/O 4	Input/Output of channel 4
8	OUTPUT 4	High-Side output of channel 4
9	OUTPUT 3	High-Side output of channel 3
10	OUTPUT 2	High-Side output of channel 2
11	OUTPUT 1	High-Side output of channel 1

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$- I_{GND}$	DC Ground pin reverse current	- 250	mA
I_{OUT}	DC Output current	Internally Limited	A
$- I_{OUT}$	Reverse DC output current	-1	A
I_{IN}	DC Input current	+/- 10	mA
V_{ESD}	Electrostatic discharge (R=1.5KΩ; C=100pF) - I/On - OUTn & Vcc	4000 5000	V V
T_j	Junction operating temperature	Internally Limited	°C
T_{stg}	Storage temperature	- 55 to 150	°C

Figure 3. Configuration Diagram (Top View)

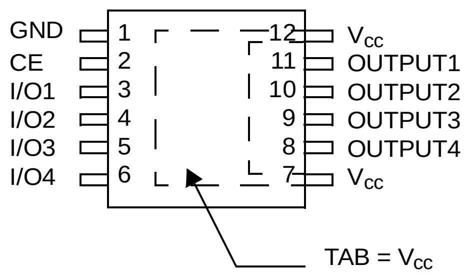


Figure 4. Current and Voltage Conventions

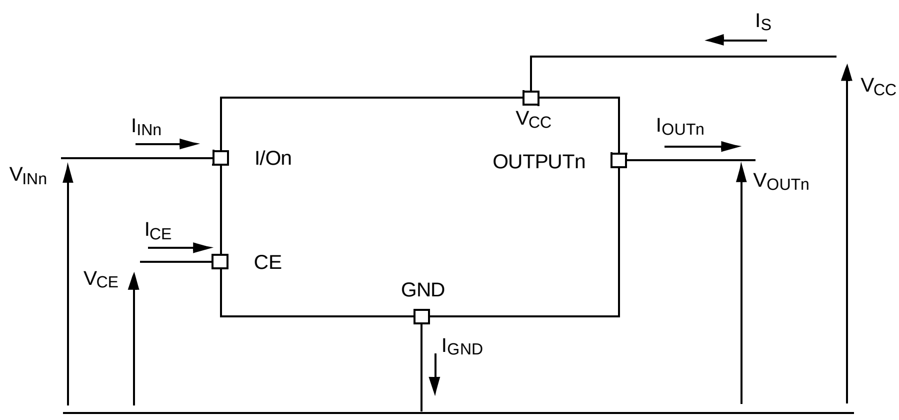


Table 5. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	Max	4.6	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	60 (*)	°C/W

Note: (*) When mounted on FR4 printed circuit board with 0.5 cm^2 of copper area (at least 35µ thick) connected to all TAB pins.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

Table 6. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} (**)	Operating supply voltage		5.5	13	36	V
V_{USD} (**)	Undervoltage shut-down		3	4	5.5	V
V_{OV} (**)	Overvoltage shutdown		36			V
R_{ON}	On state resistance	I_{OUTn}=0.25A; T_j=25°C I_{OUTn}=0.25A			500 1000	mΩ mΩ
I_S	Supply current	V_{CE}=$V_{I/On}$=0V; V_{CC}=13V; T_{case}=25°C On state (all channels ON); V_{CC}=13V			20 8	µA mA
I_{LGND} (**)	Output current at turn-off	V_{CC}=V_{CE}=$V_{I/On}$=V_{GND}=13V V_{OUTn}=0V			1	mA
$I_{L(off)}$ (**)	Off state output current	$V_{I/On}$=V_{OUTn}=0V	0		5	µA
I_{Loff2} (**)	Off state output current	$V_{I/On}$=0V, V_{OUTn}=0V, V_{CC}=13V; T_{case}=25°C			1	µA

Note: (**) Per channel

Table 7. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on time	R_L=52Ω from 80% V_{OUT} (1)		50		µs
t_{off}	Turn-off time	R_L=52Ω to 10% V_{OUT} (1)		75		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L=52Ω from V_{OUT}=1.3V to V_{OUT}=10.4V (1)		0.3		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L=52Ω from V_{OUT}=11.7V to V_{OUT}=1.3V (1)		0.3		V/µs

Note: (1) see figure 5 :switching time waveforms

Table 8. Input & CE Pin

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{INL}	I/O low level				1.25	V
I_{INL}	Low level I/O current	V_{IN}=1.25V	1			µA
V_{INH}	I/O high level		3.25			V
I_{INH}	High level I/O current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	I/O hysteresis voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

ELECTRICAL CHARACTERISTICS (continued)

Table 9. Protections

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OL}	I/O low level default detection	I_{IN}=1mA, latched thermal shutdown			0.5	V
T_{TSD}	Junction shut-down temperature		150	175	200	°C
I_{lim}	DC Short circuit current	V_{CC}=13V; R_{LOAD}=10mΩ	0.4		0.9	A
V_{demag}	Turn-off output clamp voltage	I_{OUT}=0.25 A; L=50mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
t_{reset}	Thermal latch reset time	Tj < T_{TSD} (see figure 3 in waveforms)			10	µs

Figure 5. Switching Time Waveforms: Turn-on & Turn-off

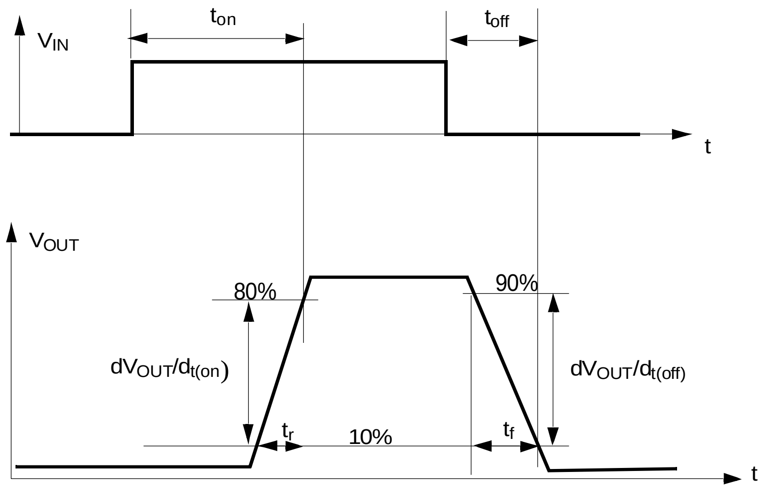
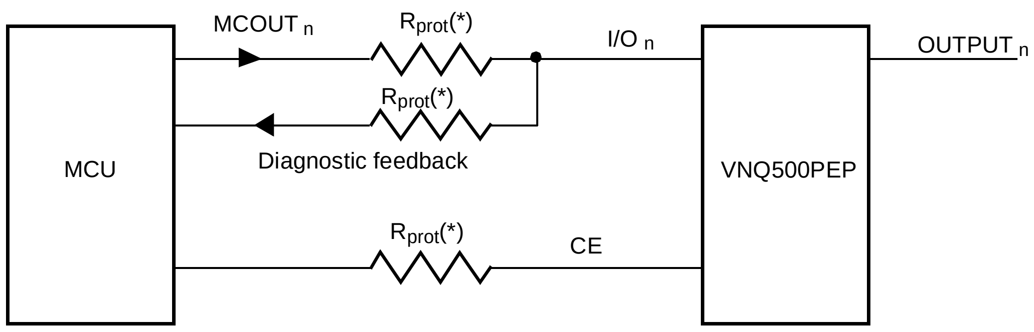


Figure 6. Driving Circuit



(*) see pag. 8

Figure 7. Truth Table

CONDITIONS	MCOUTn	CE	I/On	OUTPUTn
Normal operation	L H	H H	L H	L H
Current limitation	L H	H H	L H	L H
Overtemperature	L H	H H	L L (latched)	L L
Undervoltage	L H	H H	L H	L L
Stand-by	X	L	X	L

Table 10. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 8. Waveforms

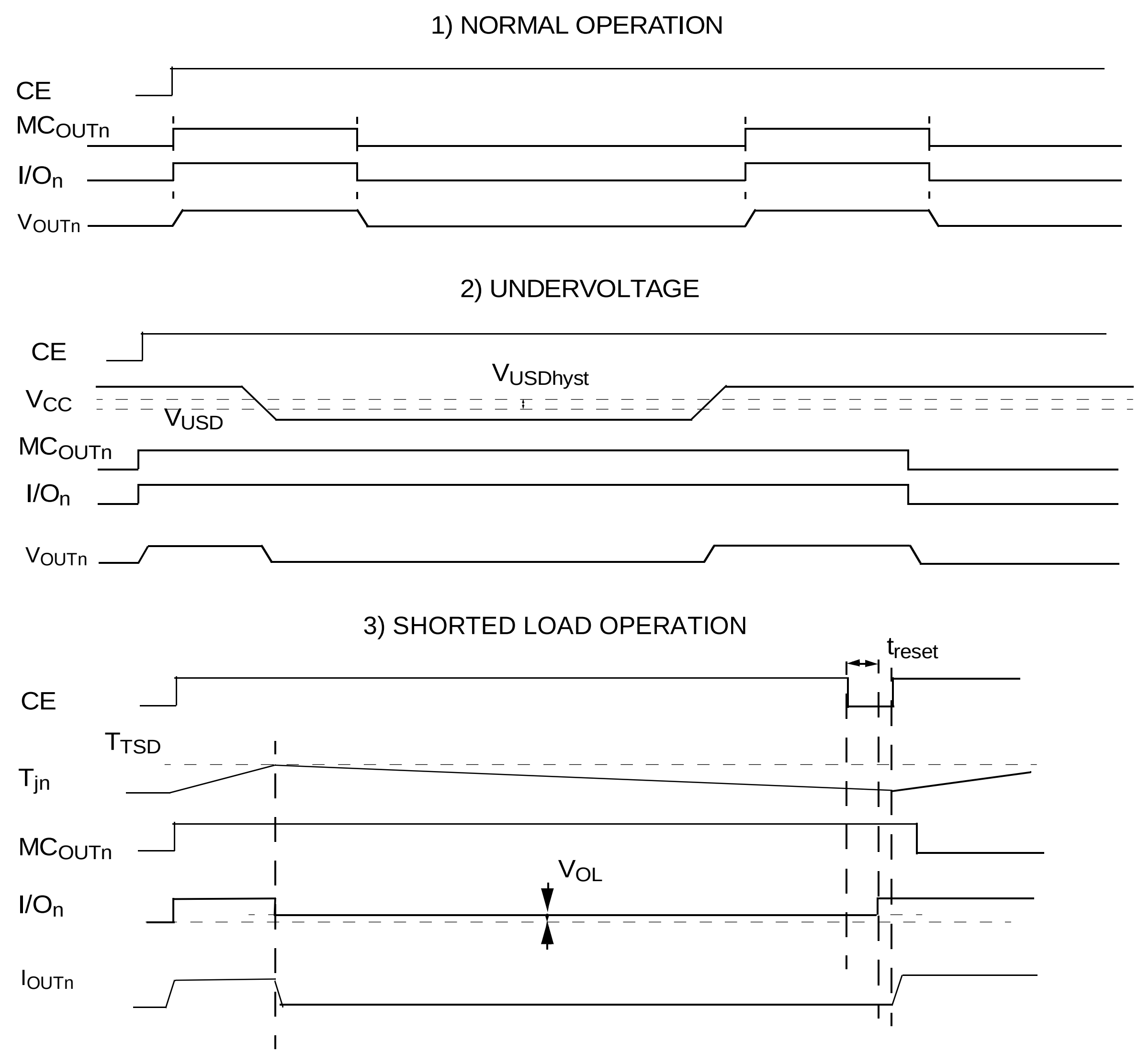
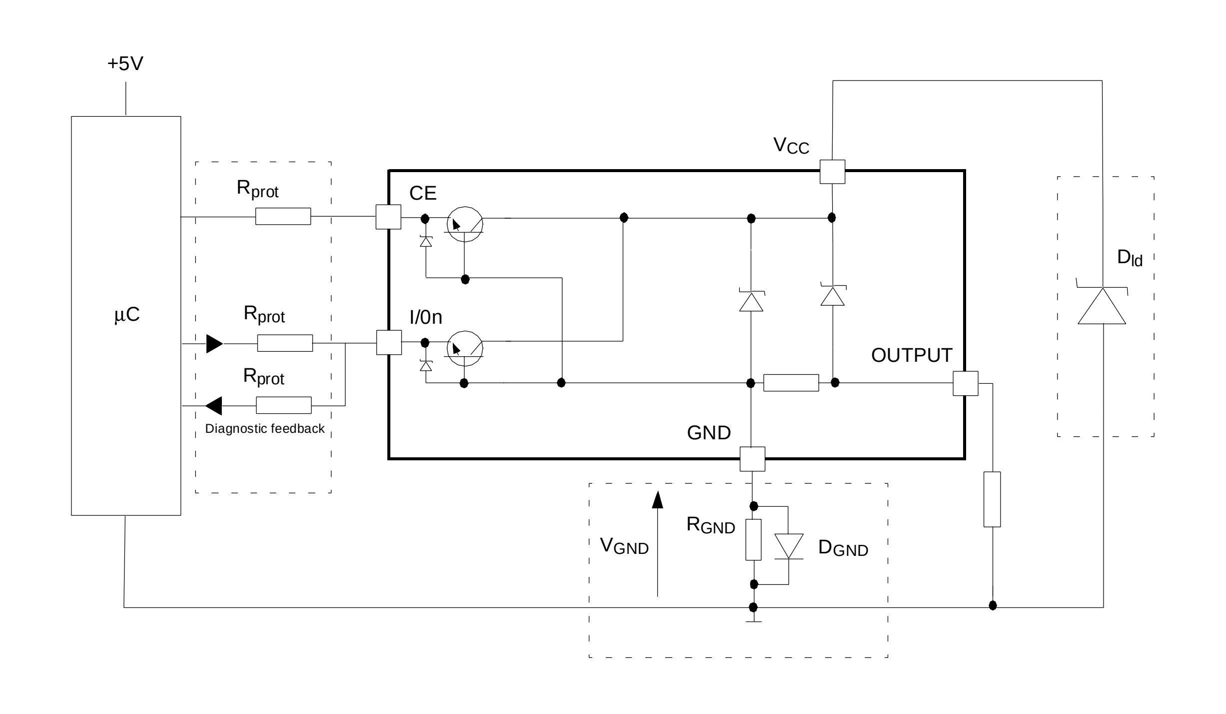


Figure 9. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

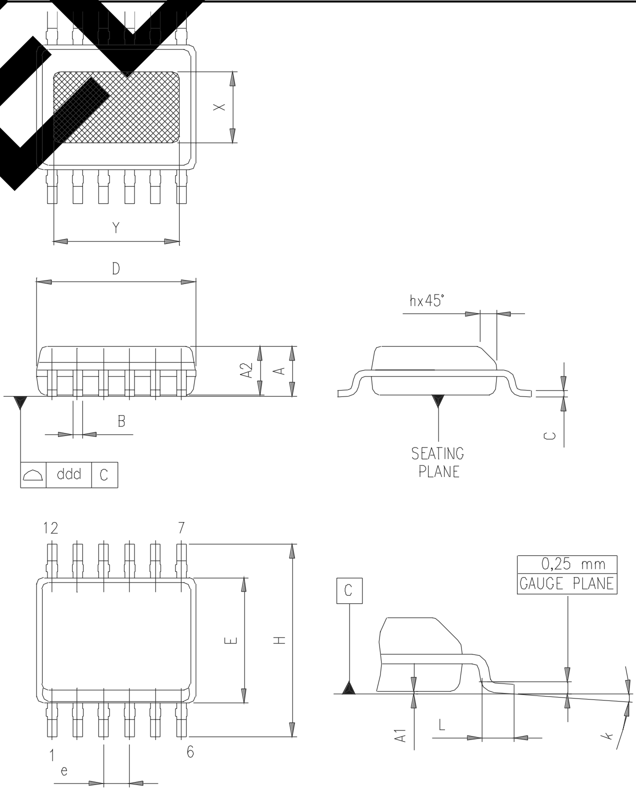
Recommended R_{prot} value is 10kΩ.

PACKAGE MECHANICAL

Table 11. PowerSSO-12™ Mechanical Data

Symbol	millimeters		
	Min	Typ	
DIM.	mm.		
	MIN.	TYP	MAX.
A	1.250		[illegible]
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0º		8º
X	1.900		2.500
Y	[illegible]		4.200
ddd			0.100

Figure 10. PowerSSO-12™ Package Dimensions



REVISION HISTORY

Table 12. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	First Issue.