A. HE82006 Introduction

HE82006 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. It is a power speech controller. The 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 208K ROM Size can be used in the storage of speech (64 seconds at 3Kbytes per second). In order to simplify IC function, this IC have not exit follow list circuit, Slow Clock, Timer2 and Watch-dog Timer. Please pay attention.

The instruction set of HE82006 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B. HE82006 Features

- Operation Voltage： 2.4V – 5.5V
- System Clock： DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM： 208K Bytes(16K PROM+192K DROM(start from 10000h))
- Internal RAM： 128 Bytes（without Bit7 of Address, only Address[6:0]）
- Clock System： Fast Clock: 32.768K ~ 8MHz
- Operation Mode： FAST、SLEEP Mode.
- 8 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin.
- One 7-bit current-type DAC output.
- With PWM device. (VDD with PWM pin).
- Two external interrupts and one internal timer interrupt.
- One 16-bit timer. (Clock Source reference by Fast Clock)
- nstruction set： 32 instructions, 4 addressing mode. 7-bit DATA POINTER for RAM and 16-bit TABLE POINTER for ROM.

C. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
—	—	—	16KB	192KB	16-bit	◎	128B	—	7-bit	8	—	—	T1

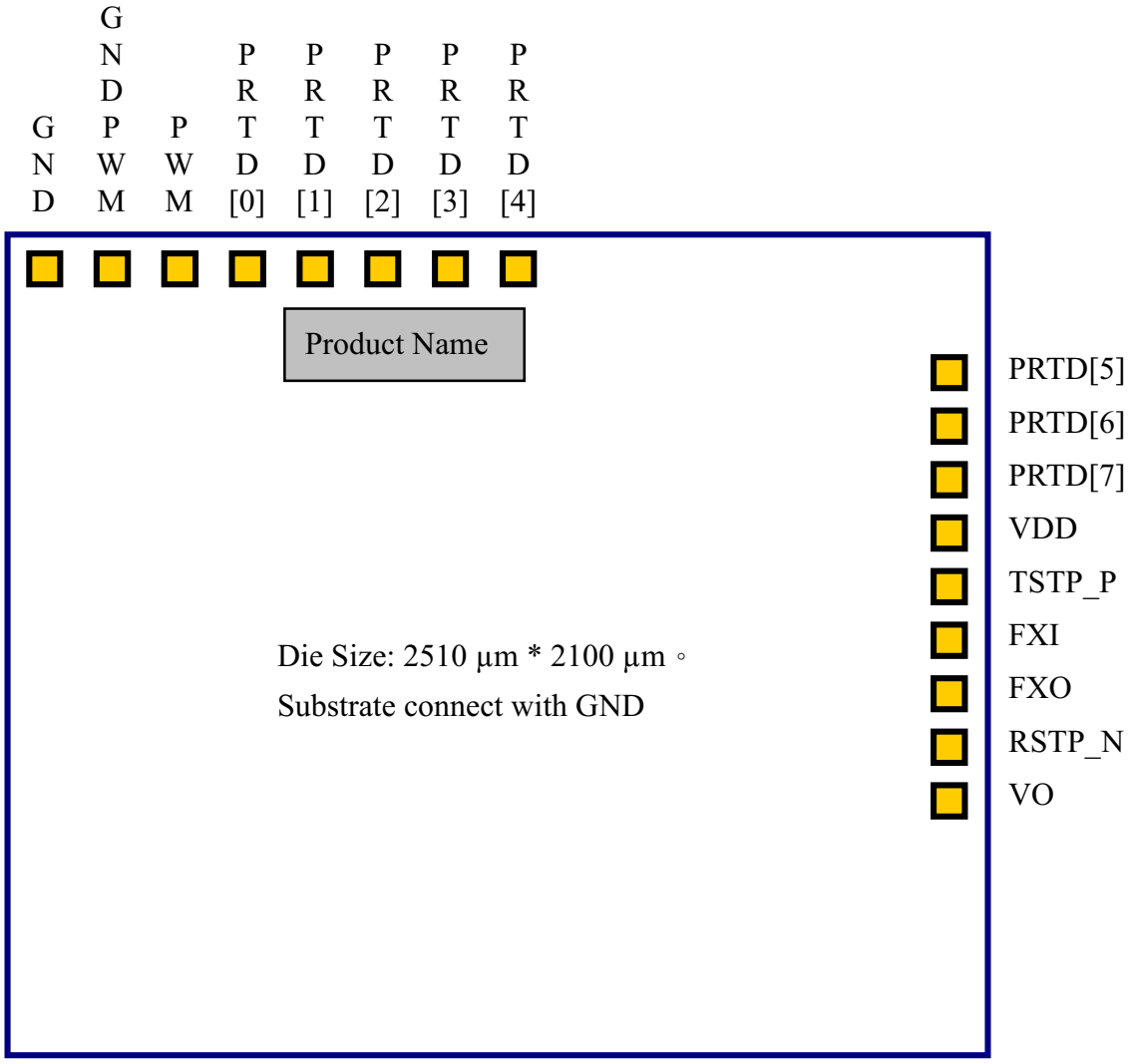
VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
◎	—	—	◎	—	—	—	—	—	—	—	—	—	—

D. 腳位說明

Pin #	Pin name	I/O	Function	Description
4 3	**FXI,** **FXO**	B, O	外部快速振盪時脈(External Fast Clock)接腳。用以連接 Crystal 或接 R,C 振盪，來產生 32.768K ~ 8MHz 之系統主頻。	Mask Option 之設定： MO_FXTAL=0：R,C 振盪 for Fast Clock 1：Crystal 振盪 for Fast Clock 可在程式中使用 OP1 及 OP2 之設定來切換不同之操作模式 (Normal 及 Sleep)。

Pin #	Pin name	I/O	Function	Description
2	**RSTP_N**	I	系統重置訊號。	提供此輸入腳位一低電位，將使系統產生重置。
5	**TSTP_P**	I	Test Pin, 高電位動作。輸入一高電位將使 IC 進入測試模式。	請將 TSTP_P 這個 PIN 連接到一個測試點(Test Point)，讓這個測試點浮接（Floating)。讓 KB 能在 PCB 上做測試的工作。
7..14	**PRTD[7:0]**	B	Port D 雙向 I/O 接腳，共有 8 個腳位。其中 PRTD[7:2]亦做為 Wake-up 腳；PRTD[7:6]則可用做中斷輸入。	用 Mask Option MO_DPP[7:0]設定其輸出型態： MO_DPP 為'1'時，為 Push-pull output； 為'0'時，為 Open-drain output。 當做輸入腳時，需先輸出'1'！才能讀入正確輸入值。
15	**PWM**	O	PWM 輸出，可直接驅動 Speaker 或 Buzzer。做為聲音輸出之用。	設定 VOC 暫存器的 Bit2: PWM =1；turn on PWM。
1	**VO**	O	D/A 聲音輸出。	設定 VOC 暫存器的 Bit1: DA=1；turn on VO。
6	**VDD**	P	Positive Power Input	
17	**GND**	P	Power Ground Input	
16	**GND_PWM**	P	PWM Dedicated GND	

E. Pin Diagram



F . Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate
1	VO	X= 1171.70	Y= -129.35
2	RSTP_N	X= 1171.70	Y= -13.45
3	FXO	X= 1171.70	Y= 102.45
4	FXI	X= 1171.70	Y= 218.35
5	TSTP_P	X= 1171.70	Y= 334.25
6	VDD	X= 1171.70	Y= 450.15
7	PRTD[7]	X= 1171.70	Y= 566.05
8	PRTD[6]	X= 1171.70	Y= 681.95
9	PRTD[5]	X= 1171.70	Y= 797.85
10	PRTD[4]	X= -349.45	Y= 965.45
11	PRTD[3]	X= -465.35	Y= 965.45
12	PRTD[2]	X= -581.25	Y= 965.45
13	PRTD[1]	X= -697.15	Y= 965.45
14	PRTD[0]	X= -813.05	Y= 965.45
15	PWM	X= -937.35	Y= 965.45
16	GND_PWM	X= -1061.35	Y= 965.45
17	GND	X= -1177.25	Y= 965.45

G. DC/AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

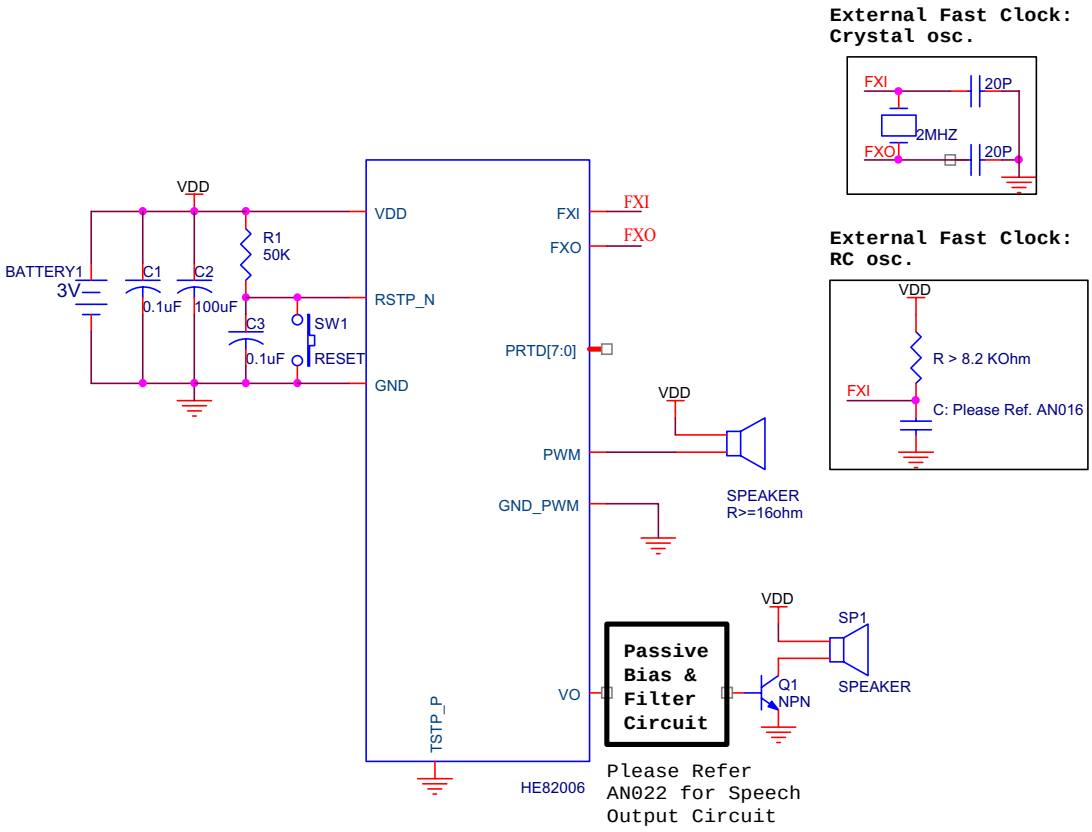
Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Test Condition: TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oLPWM}	PWM Output Sink Current	PWM*2	V_{DD}=3V; V_{oL}=1V	40	60		mA
I_{oVO}	DAC Output Current	VO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current. (I_{oHPWM}、I_{oLPWM} * N; N=0,1,2,3,4,5)

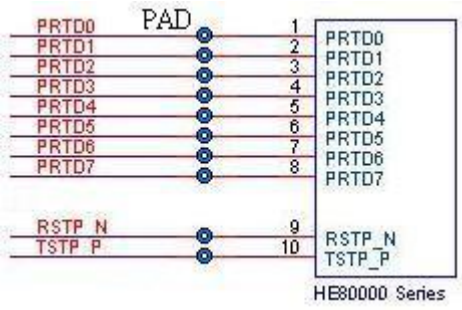
H. Application Circuit



I. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.

2. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



J. Updated Record

Version	Date	Section	Original Content	New Content
V1.4	Nov 20, 2001	B, G	2.2V (VDD operation voltage)	2.4V
		I, J		New Section